#147 October 2002

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THE MAGAZINE FOR COMPUTER APPLICATIONS

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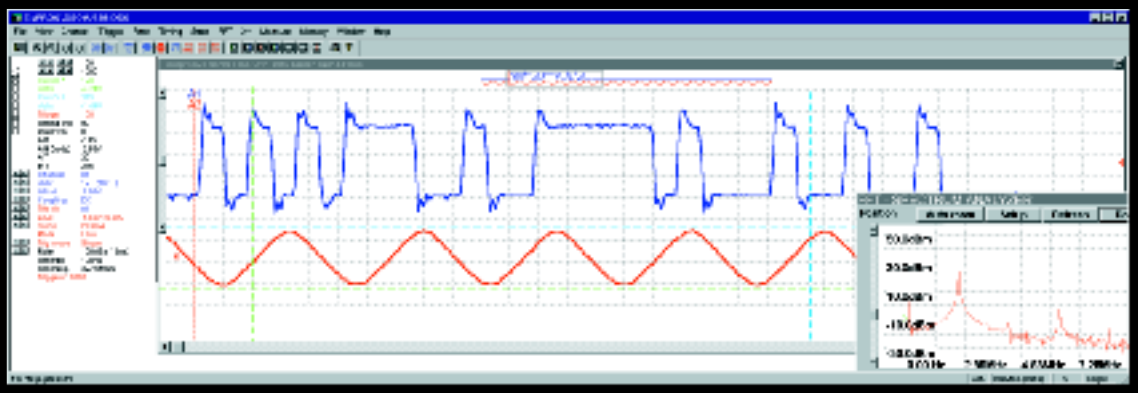
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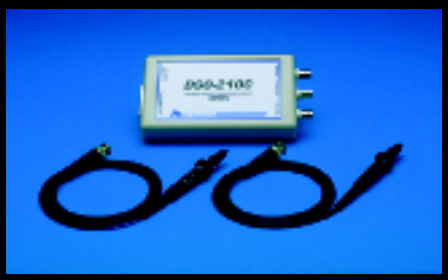
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Digital Oscilloscopes

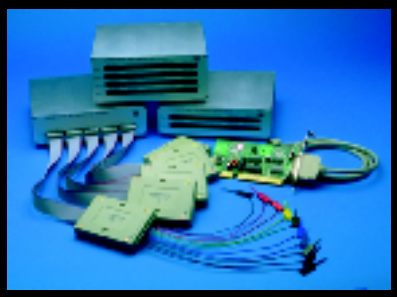


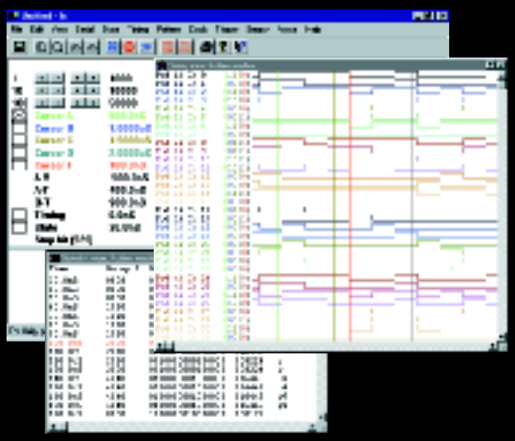
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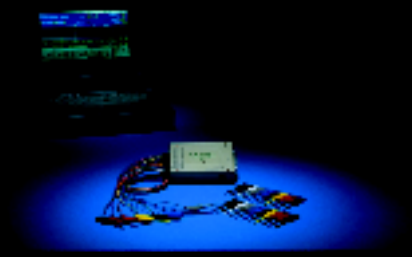


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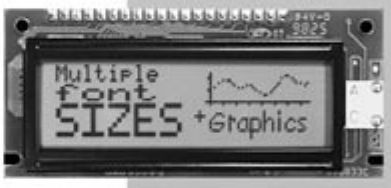
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TASK MANAGER

Be a Contender

The pages of *Circuit Cellar* brim with practical yet intriguing information. Our goal is to enlighten and entertain you with every issue. In keeping with our goal, we have a number of features throughout the magazine that inform, teach, and hopefully inspire you. Most of our articles serve as tutorials, giving you step-by-step instructions on how to build with a new part or sophisticated technology. And, you can always count on columnist Tom Cantrell for updates on the industry. In every issue, you'll also find thought-provoking quiz questions (page 11), announcements about products fresh to the shelves (page 8), and a guide to find the ads of your favorite manufacturers (page 94). But, one of our best staples is our challenging design contests.

Circuit Cellar contests have become one of our most successful ventures. Each one draws out top engineers who specialize in everything from chip design to embedded systems, and from neuroscience to rocket science. The varied backgrounds of the contestants always ensure a plethora of unique entries.

If you haven't already participated in one of our contests, don't miss your next opportunity. Start building your project for the Mad Dash for Flash Cash Design Contest 2002, sponsored by Microchip Technology, today! You have until December 16 to enter, so that still gives you a couple of months to work on your project. The Microchip PIC family of microcontrollers has become universally popular; in fact, we continually receive scores of articles about projects that feature various PIC parts. With a well-liked PIC at the center of your design, you'll have no trouble creating a masterpiece of ingenuity.

Those of you who want an edge in the competition should incorporate one of the following features: TC1047 temperature sensor; MCP6022 op-amp; MCP3002 analog-to-digital converter; MCP42100 digital potentiometer; MCP1541 VREF; at least one communication port; or a CCP to control an event. Entries that showcase any of these features will be given bonus consideration by the judges; for more information, read the official contest rules on our web site (www.circuitcellar.com/flash2002).

Consummate designers get all of the facts first. Before you begin working with these features, I recommend reading columnist Jeff Bachiochi's article, starting on page 62. Jeff's thorough introduction to Microchip components will ready you for the task. After reading his article, you'll be armed with the knowledge needed to design a competitive project.

Aside from the prestige winners earn from succeeding in a *Circuit Cellar* contest, they also receive prizes. A total of nine entries will be awarded prizes: Grand, First, Second, Third, and five Honorable Mention prizes. The lucky winner of the Grand Prize stands to receive the Microchip MPLAB ICE2000 processor module and free registration to the Microchip Annual Summer Technical Exchange Review (MASTERs). Additionally, don't forget that we'll recognize all of the winners in the magazine as well as on our web site.

jennifer.huber@circuitcellar.com

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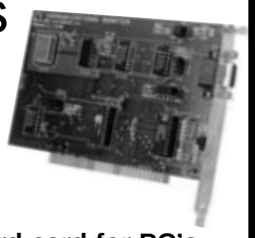
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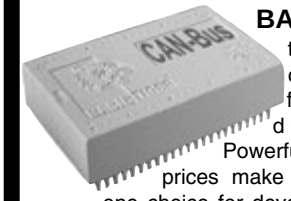
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C Contest Related Articles



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NEW PRODUCT NEWS

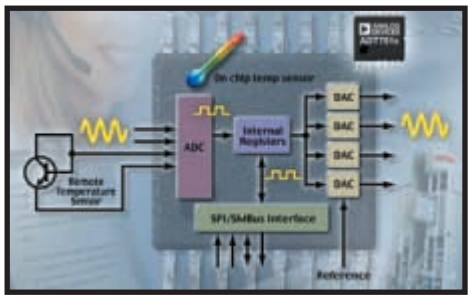
Edited by John Gorsky

MULTICHANNEL THERMAL MONITORING

The **ADT7*xxx*** family of temperature-to-digital converters offers a combination of multichannel ADCs and DACs in addition to its core ambient and remote temperature measurement functions. Used in conjunction with the thermal monitoring channels, this additional functionality allows compensation, control, and monitoring of circuits and subsystems, including power amplifiers, oscillators, power devices, power supplies, and fans. Combining these multiple functions into a low-cost, one-chip solution allows designers to have more flexibility in optimizing their system's performance.

These new products are all compatible with SPI/I²C and feature a 10-bit digital ambient and remote temperature sensor. The ADT7411 adds an eight-channel ADC. The ADT7316/17/18 adds a quad voltage output 12-/10-/8-bit DAC. And, the ADT7516/17/18 adds a four-channel ADC and a quad-voltage output 12-, 10-, or 8-bit DAC. All are fully operational with 2.7- to 5.5-V power supplies and over a temperature range from –55 to 125°C.

This family of multichannel temperature sensors is designed for applications such as PCs, communication systems, industrial instrumentation, and portable equipment.



In 1000-piece quantities, the ADT7411 is priced at **$2.29** per unit; the ADT7316/17/18 are priced at **$4.95**, **$2.95**, and **$1.75** per unit, respectively; and the ADT7516/17/18 are priced at **$5.65**, **$3.65,** and **$2.65** per unit, respectively.

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TOUCH SCREEN CONTROLLER

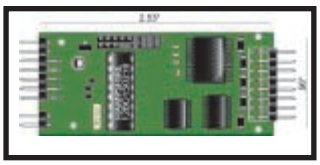
The **TSHARC Octopus** board is a touch screen controller that can concurrently and inexpensively support all communication standards and analog-resistive touch screen overlays.

The versatile Octopus has jumper-selectable communications capabilities for RS-232, PS/2, and USB, as well as four-, five-, and eight-wire analog resistive screen technologies. It is available in 10- or 12-bit configurations, delivering up to 4096 × 4096 resolution.

Available optionally to OEMs as a TSHARC-10 or 12 chip, the Octopus controller can be integrated on motherboards. Through the use of Hampshire's proprietary dynamic point flow rate decoding, the controller quickly and accurately decodes screen touch points in touch-only, drawing, and writing applications.

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The board costs **$45** and the chip costs **$7** in quantity purchases.



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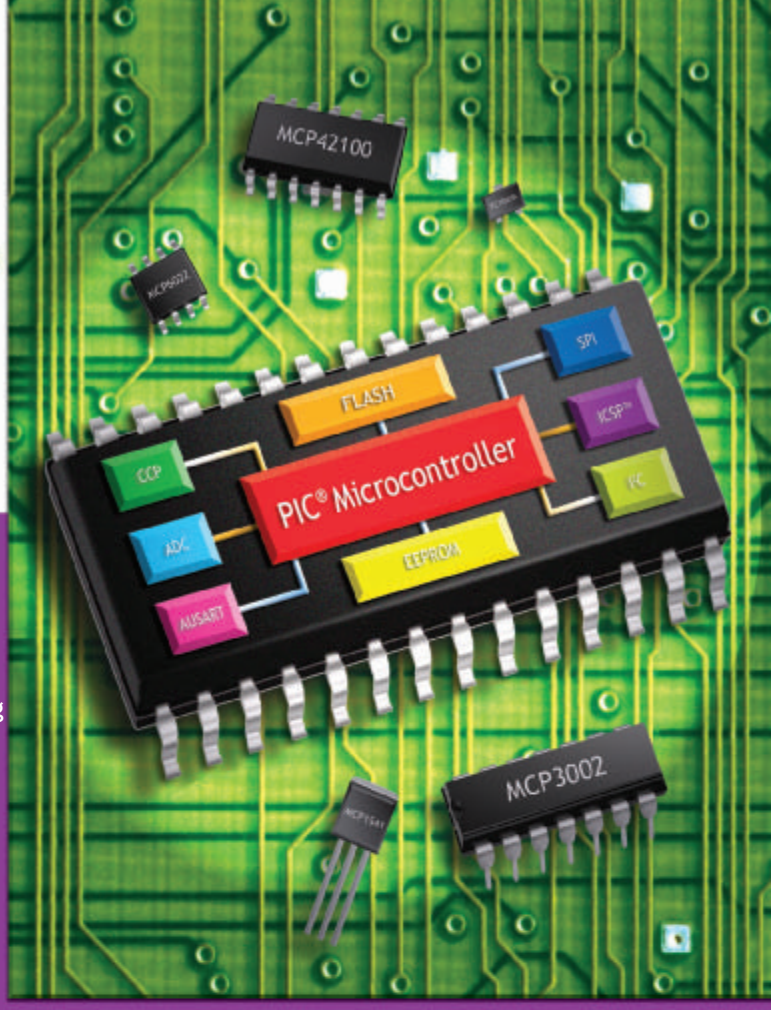
The PCA954*x* switches are designed for I²C buses or SMBuses where multiple devices have the same address or different voltage levels. These switches allow voltage-level shifting between devices operating at 5, 3.3, 2.5, or 1.8 V at serial clock frequencies of up to 400 kHz. They provide multiplexing and interrupt controlling to eliminate the need for glue logic and general-purpose I/Os. Four devices with two, four, or eight-channel configurations are currently in production. In addition, the switches are equipped with a hardware reset pin that returns the device to the default state of no channels selected, thereby circumventing the usual step of cycling power to restore the bus from a lock-up situation, which is a significant concern in critical server applications.



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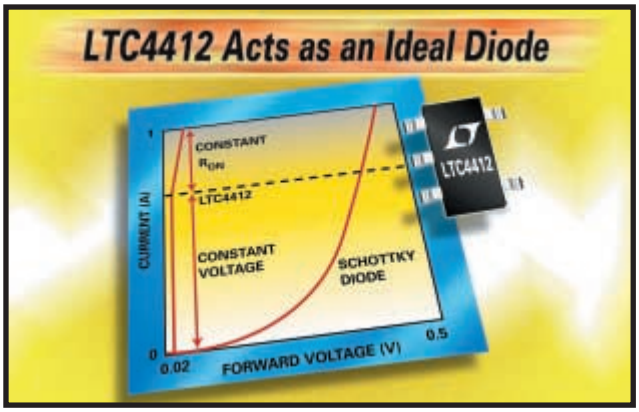
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Contributed by Naveen PN

Problem 2—The following DC measurements are made on a differential amplifier. Vi1 and Vi2 are the input voltages. V_{out} is the output voltage.
Vi1 = 0 V, Vi2 = 0V, V_{out} = –0.1 V
Vi1 = 0.02 V, Vi2 = 0 V, V_{out} = 0.4 V
Assuming the common mode rejection ratio (CMRR) is infinity, find the differential-mode gain and the offset voltage referred to the input.

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Problem 3—You have two bars of iron. One is magnetized along its length, the other is not. Without using any other instrument (e.g., thread, filings, other magnets, etc.), find out which is which.

Contributed by Naveen PN

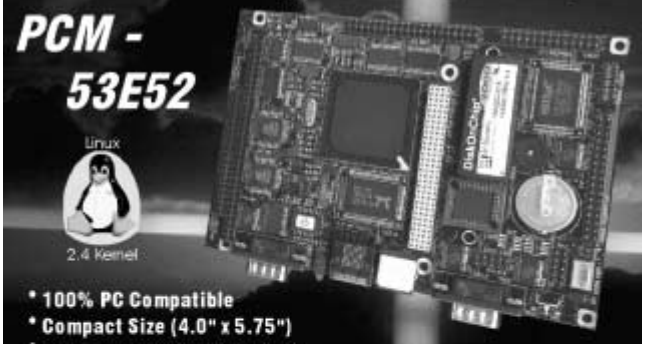
Problem 4—A helium-filled balloon is tied to the floor of a car that makes a sharp right turn. Does the balloon move while the turn is made? If so, which way? The windows are closed so there is no connection with the outside air.

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FEATURE ARTICLE

Martin Courtney

2-D or Not 2-D?

If you're at that point where 2-D surface images just aren't doing the job anymore, then it's time for you to move on to more sophisticated 3-D surfaces. In this article, Martin walks us step-by-step through a project to create 3-D surfaces that can be oriented in real time.

One thing I've learned: It's graphics that gets people's attention. People may not appreciate what it took to create your data acquisition masterpiece, but they'll appreciate its visual side.

So, why restrict users to viewing flat, 2-D color maps? Complement your creation with 3-D surfaces that can be oriented in real time (see Photo 1). Here's a step-by-step guide.

THE BIG PICTURE

Maybe your data represents the surface features of a biological sample, or maybe your data isn't really a surface at all. Perhaps it's multiple vibration spectra from a jet engine and you just want to present that data as if it were a surface. In any case, the problems involved in displaying the information are the same. You need to scale the data, map it from three physical dimensions to the two dimensions of the computer display, and then render the surface.

There are a number of fine texts devoted to this subject. The standard approach uses four-by-four matrices to rotate an object about an arbitrary axis and to scale it to make it appear closer or further away. This approach also allows either perspective or projective drawing, and it permits an object to be located anywhere around the viewer.

For engineering data, however, that's overkill. You can get by nicely doing no more than just rotating the surface about two axes.

BUILDING THE FOUNDATION

A few preliminaries are in order before tackling scaling, mapping, and rendering. For starters, it helps to understand the kind of data to which this method is suited. The only restriction is that it be a single-valued function of two independent variables—the usual case in data acquisition.

In symbols, $z = f(x,y)$, where for every x and y there is a unique z value. For example, a basketball would not qualify. You could drive a stake vertically through it and you would hit two points, one on the upper side, and the other on the lower side. But that same basketball cut in half would qualify.

Now think of your data in the same terms. Each physical sample point is a function of two independent variables. Define the underlying

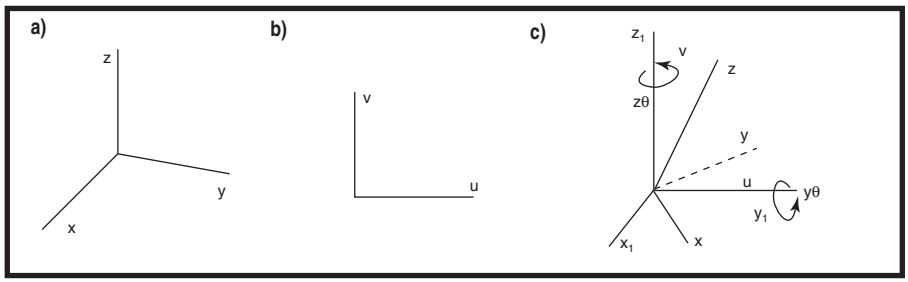


Figure 1a—*A three-dimensional orthogonal coordinate system is used to define a surface. Note that the coordinate system is right-handed.* ***b***—*The two-dimensional coordinate system of the computer display is a right-handed coordinate system like its three-dimensional counterpart.* **c**—*These coordinate systems have a common origin: the x_1-y_1-z_1 system is the fixed reference system; the x-y-z system is the body system, which is free to tilt and rotate; the u-v system is the fixed system attached to the display. As you can see, the body system is tilted about the y_1-axis of the reference system and twisted around the reference system's z_1-axis.*

orthogonal coordinate system to be right-handed with axes x, y, and z as shown in Figure 1a.

Think of the computer display as a screen with orthogonal axes denoted u and v (see Figure 1b). One data type that will be handy is the three-dimensional analog of a point structure (see Listing 1). The triplet structure makes it easy to handle samples that are not uniformly spaced.

Finally, if you would like the surface you'll draw to be rendered in color, you'll want to create an array with the same dimensions as your data. Quantize your data to as many levels as the number of colors in your palette. Loop through the data looking at four adjacent points at the same time. Find the largest value and store it in the array. Later, you'll use this array as a look-up table to select the color to paint the polygon defined by the projection of each group of four adjacent points. If you'll be painting with a 255-color palette, for example, the relevant code looks like Listing 1.

NORMALIZE THE DATA

Suppose your sample measures 2000 units along the x-axis and one unit along the y-axis. Eventually, when you render the surface, you'll need to fit the largest dimension inside a window. Assuming you have more than a few samples, if you keep the 2000:1 ratio, the data along the shorter axis will be so compressed that it will be impossible to decipher. Therefore, you'll want to scale the data to have the same range along each axis. There is also code in Listing 1 that accomplishes that.

Listing 1—*Study this source code carefully. It illustrates some of the most important concepts involved in rendering three-dimensional data on the two-dimensional surface of a computer display.*

```
//************************************************************************
// The triplet structure is used to define a point in 3-D space.
//************************************************************************
typedef struct TRIPLET {
  double x;
  double y;
  double z;
};
//************************************************************************
// Find the largest z value of the four vertices in a quadrilateral piece
// of the surface, and quantize it to 255 colors.
//************************************************************************
double  m = 254.0 / pDoc->m_fSpanZ;
double  b = 0 - m * pDoc->m_fMinZ;
for (i=0; i<pDoc->m_nNumRows-1; i++) {
  for (j=0; j<pDoc->m_nNumCols-1; j++) {
    float zLocalMax = pDoc->m_pXYZ[i][j].z;
    if (zLocalMax < pDoc->m_pXYZ[i+1][j].z)
      zLocalMax = pDoc->m_pXYZ[i+1][j].z;
    if (zLocalMax < pDoc->m_pXYZ[i+1][j+1].z)
      zLocalMax = pDoc->m_pXYZ[i+1][j+1].z;
    if (zLocalMax < pDoc->m_pXYZ[i][j+1].z)
      zLocalMax = pDoc->m_pXYZ[i][j+1].z;
    m_pnColorIndex[i][j] =
     (int) (m * (zLocalMax + pDoc->m_fMidZ) + b);
  }
}
//************************************************************************
// Normalize x and y so the range of data is the same along all axes.
//************************************************************************
double dSpanZ  = dMaxZ - dMinZ;
if (dSpanZ != 0.0) {
  dScaleX = dSpanZ / dSpanX;
  dScaleY = dSpanZ / dSpanY;
  for (i=0; i<m_nNumRows; i++) {
    for (j=0; j<m_nNumCols; j++) {
      m_pXYZ[i][j].x *= dScaleX;
      m_pXYZ[i][j].y *= dScaleY;
    }
  }
}
else {
  dScaleX = 1.0;
  dScaleY = dSpanX / dSpanY;
  for (i=0; i<m_nNumRows; i++) {
    for (j=0; j<m_nNumCols; j++) {
      m_pXYZ[i][j].y *= dScaleY;
```

(Continued)

SCALE TO THE WINDOW

To maximize the display size of the surface while confining it to a view, you need to do two things. First, move the center of the data to the center of the view. Second, you have to calculate a scaling factor. The scaling factor tells you how many pixels it takes to move one unit of data. You'll use it after you transform your data from three dimensions to two dimensions.

It's not difficult to determine the scaling factor. Because you normalized your data it fits inside a cube. A line segment that runs from corner to corner of the cube (a diagonal) is the greatest distance between any two points you will encounter. The diagonal will have to fit inside the view no matter how the surface, and therefore the bounding cube, may be rotated. This means that with the bounding cube centered in the view, all of the data will need to be scaled so that the diagonal is no greater than either the height or width of the view, whichever of these two is smaller. All it takes is a little Pythagoras (see Listing 1).

MAP FROM 3-D TO 2-D

So, how do you represent physical data on a flat display? The answer is by judiciously choosing your coordinate systems, and then calculating the projection of one system onto the other.

Three coordinate systems are shown in Figure 1c. The first is the x_1-y_1-z_1 system. Its orientation is fixed in space, and it is the reference system. The second, the u-v system, is also fixed in space; it represents the flat computer display. Note that the u-axis coincides with the y_1-axis, and the v-axis coincides with the z_1-axis. The origins of the two systems are coincident, as well.

The final system is the x-y-z system, which is not fixed in space, but

attached to the surface that represents your data. This is the body coordinate system. Notice that the origin of this system coincides with the origin of the other two. This is important. Even though the body system can rotate, the location of its origin is fixed.

How you allow the surface to rotate is also of importance. You'll find that you get nice results by just twisting the surface around the z_1-axis and tilting it around the y_1-axis of the reference system (see Figure 1c).

Now, in order to determine how a surface that's been twisted and tilted projects onto the u-v plane of the display, you have only to consider how the axes of the body coordinate system project. That's because every point that makes up the surface can be represented as a linear combination of the x-y-z axes of the body system (i.e., a point is located by moving so much along the x-axis, plus so much along the y-axis, plus so much along the z-axis).

To see how this works in practice, choose a data point with coordinates A, B, and C in a body coordinate system that initially coincides with the reference coordinate system. Twist the body coordinate system by zθ and observe how the components along each axis project onto the reference coordinate system. Then, tilt the body coordinate system by yθ and see how the components project.

Look first at the vector along x with length A. After twisting by zθ, where the angle is measured from the x_1-axis, its projection onto the reference system is A sin(zθ) along the y_1-axis. Its projection has no component along the z_1-axis of the reference system. Notice, however, that there is a component out of the plane of the display (i.e., along the x_1-axis of the reference system) with length A cos(zθ).

Now, tilt by yθ (this angle is measured from the z_1-axis) and see how the components you just calculated project. The projection that lies along the y_1-axis, A sin(zθ), is unaffected by a rotation about y_1. It's like spinning a pipe about its long axis.

For the component along the x_1-axis, A cos(zθ), it's a different story. This is like swinging a pipe by one end. After tilting, this component has no projec-

Listing 1—*Continued*

```
    }
  }
}
*************************************************************************
Calculate the scaling factor so that the surface always fits inside
the window.
*************************************************************************
GetClientRect(&m_rcClient);              //Get window size
m_nHCenter  = m_rcClient.Width() / 2;
m_nVCenter  = m_rcClient.Height() / 2;

int nMinDmn = (m_rcClient.Width() < m_rcClient.Height()) ?
                m_rcClient.Width() : m_rcClient.Height();
//Calculate the distance from corner to corner of bounding cube
double dDiagonal;
dDiagonal = sqrt(SQR(pDoc->m_fSpanX) +
                 SQR(pDoc->m_fSpanY) +
                 SQR(pDoc->m_fSpanZ)));
m_dPixelsPerUnit = nMinDmn / dDiagonal; //Calculate scale factor
*************************************************************************
The simple expressions transform from 3-D to 2-D.
*************************************************************************
inline POINT xyz2uv(float x, float y, float z) {
  POINT pt;
  pt.x  =
    (long) (m_dPixelsPerUnit *
     ((+x * m_dSinThetaZ) + (+y * m_dCosThetaZ))); //Along u-axis
  pt.y  =
    (long) (m_dPixelsPerUnit *
     (-(((-x * m_dCosThetaZ + +y * m_dSinThetaZ) * m_dSinThetaY)
         + (+z * m_dCosThetaY))));               //Along v-axis
  return pt;
}
*************************************************************************
The code to render the surface is minimal.
*************************************************************************
if (m_zTheta < 90) {  // Inc X, Dec Y
  for (i=0; i<pDoc->m_nNumRows-1; i++) {
    for (j=pDoc->m_nNumCols-1; j>0; j--) {
      apt[0]  = m_pUV[i][j];
      apt[1]  = m_pUV[i+1][j];
      apt[2]  = m_pUV[i+1][j-1];
      apt[3]  = m_pUV[i][j-1];
      m_pdcData->SelectObject(&m_abr[m_pnColorIndex[i][j-1]]);
      m_pdcData->SelectObject(&m_apen[m_pnColorIndex[i][j-1]]);
      m_pdcData->Polygon(apt, 4);
    }
  }
  pDC->BitBlt(0, 0, rect.Width(), rect.Height(),
              m_pdcData, 0, 0, SRCCOPY);
}
*************************************************************************
The code to render a slice is just as simple.
*************************************************************************
if (m_zTheta < 90) {                 //Increase x, decrease y.
  for (i=0; i<pDoc->m_nNumRows; i++) {
    for (j=pDoc->m_nNumCols-1; j>=0; j--) {
      aptSlice[j+1] = m_pUV[i][j];
    }
    aptSlice[0] =                    //Attach the vertical sides.
      xyz2uv(pDoc->m_pXYZ[i][0].x, pDoc->m_pXYZ[i][0].y, fMinZ);
    aptSlice[0].x += nRectWidthDiv2;
    aptSlice[0].y += nRectHeightDiv2;
    aptSlice[pDoc->m_nNumCols+1] =
      xyz2uv(pDoc->m_pXYZ[i][pDoc->m_nNumCols-1].x,
             pDoc->m_pXYZ[i][pDoc->m_nNumCols-1].y, fMinZ);
    aptSlice[pDoc->m_nNumCols+1].x += nRectWidthDiv2;
    aptSlice[pDoc->m_nNumCols+1].y += nRectHeightDiv2;
    m_pdcData->Polygon(aptSlice, pDoc->m_nNumCols+2);
  }
  pDC->BitBlt(0, 0, rect.Width(), rect.Height(),
              m_pdcData, 0, 0, SRCCOPY);
}
```

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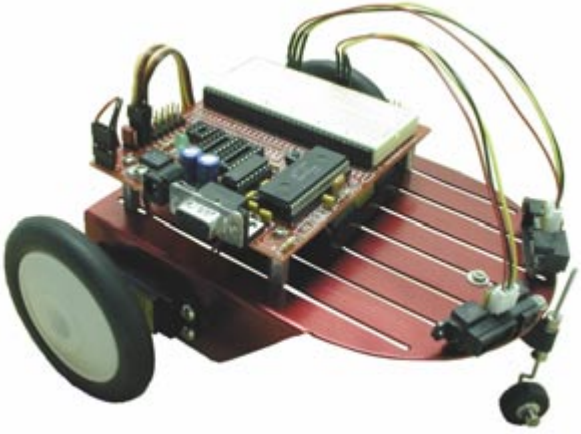
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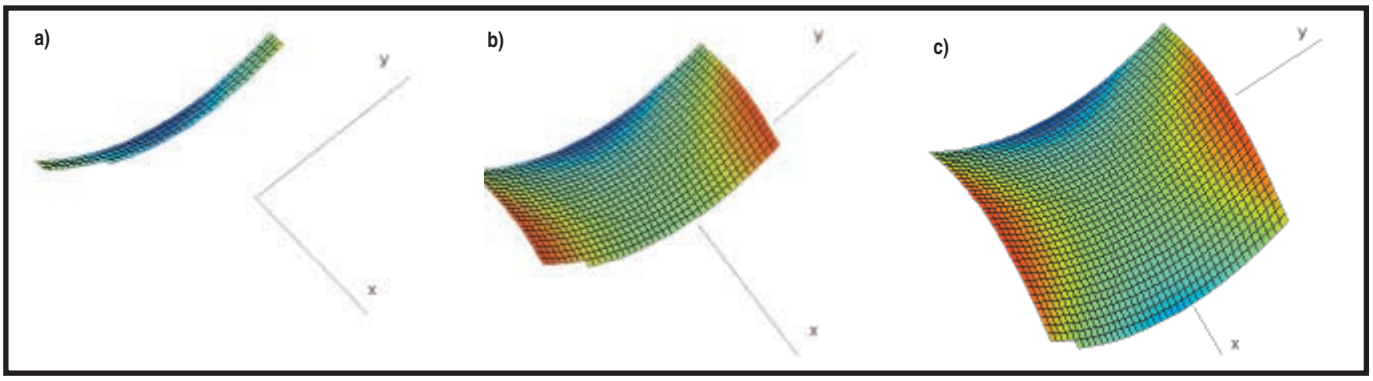


Figure 2a—*The surface is rendered one quadrilateral at a time, starting with the most distant row. When one complete row is drawn, the next closest row to the viewer is rendered. Here, only the first few rows of the surface have been drawn.* **b—***The same surface as rendering continues. Note that drawing proceeds in the direction begun earlier, from the back to the front.* **c—***Here, the surface is almost completed. Rendering in this way, drawing every quadrilateral from furthest to closest, and possibly drawing over already rendered quadrilaterals in the process, is called the Painter's Algorithm.*

tion along the y_1-axis; it does have a projection along the positive z_1-axis given by (A cos(zθ)) cos(yθ + 90). The reason for the addition of 90 is that the angle is measured from the positive z_1-axis. A trigonometric identity allows the preceding to be simplified to (A cos(zθ)) (–sin(yθ)). There is also a projection along the x_1-axis, but you don't care about it because it points directly out of the plane of the display and isn't visible.

One down, two to go. The same procedure applies to the other vectors.

The vector along the y-axis with length *B*, when twisted by zθ, has a projection along the y_1-axis of B cos(zθ). It has no projection along the z_1-axis, but does have one along the positive x_1-axis given by (B cos(zθ + 90)). This can be simplified to B sin(zθ).

Once again, tilt by yθ and find the projection of these components. The one along the y_1-axis, B cos(zθ), is unaffected. The one along the x_1-axis, B sin(zθ), has a projection along the positive z_1-axis of (B sin(zθ)) sin(yθ). Like before, you don't have to care about the projection along x_1 because it's out of the plane of the display.

Calculating projections for the final axis of the body system, the z-axis, is a snap. Twist the vector that has length C along the z-axis by zθ and it will remain orthogonal to both the x_1- and y_1-axes. Therefore, there's no projection along those two, only a component along z_1 with a length of C.

Tilt by yθ and you have a projection on the z_1-axis of C cos(yθ). There's no projection on the y_1-axis. The projection on the x_1-axis doesn't show up because it's out of the plane of the display.

Remembering that the u and v components of the display system are coincident with the y_1 and z_1 components of the reference system, respectively, you now have the necessary transforms

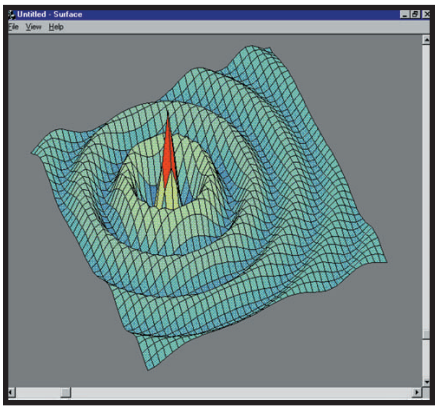


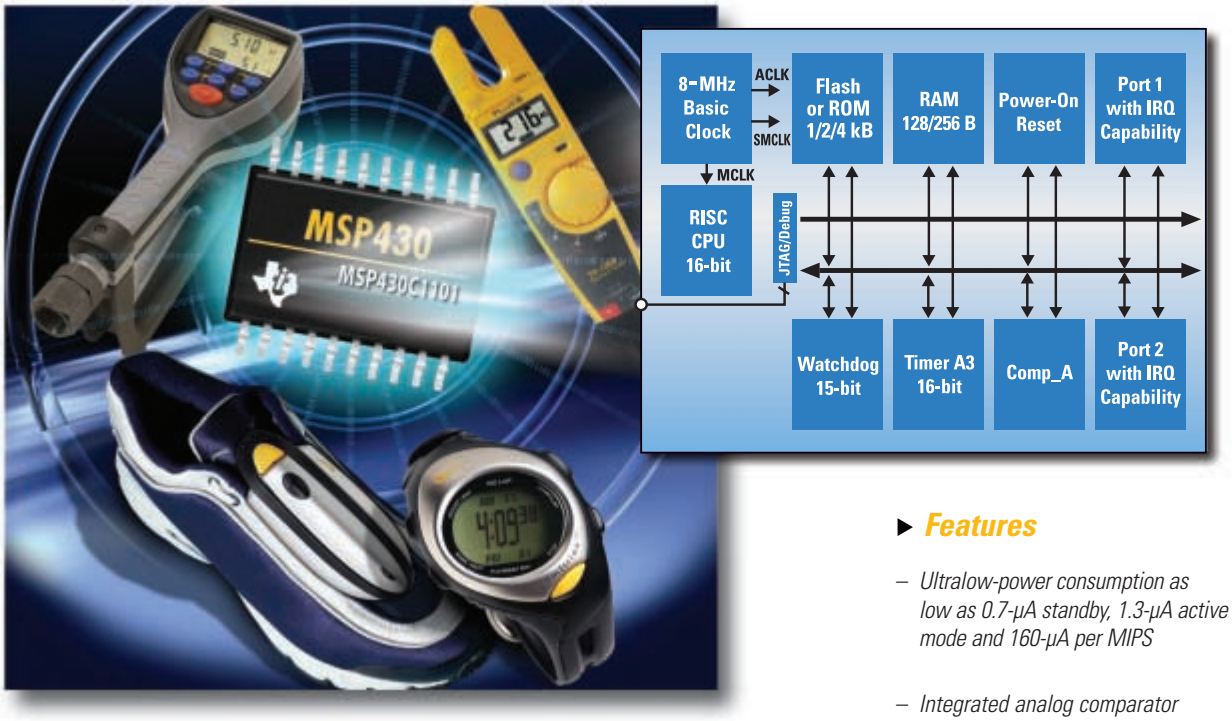
Photo 1—*This mathematically synthesized three-dimensional surface illustrates the results of projecting data onto the two-dimensional surface of a computer display. The accompanying source code provides everything necessary to build a surface from acquired data, as well as to rotate, tilt, and display it in a window.*



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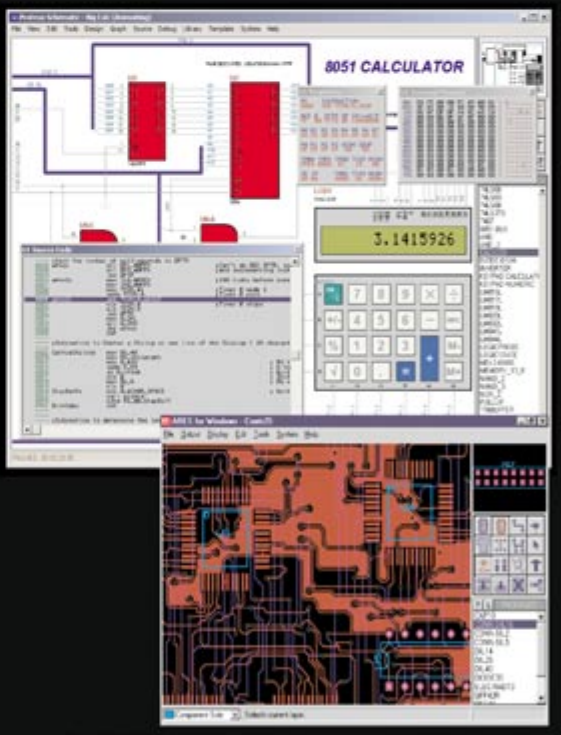
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to map 3-D data to the two dimensions of the display. The only problem is that the graphics device interface for systems such as Windows is oriented with the positive vertical axis pointing down. But that's easy to account for. Just multiply each v component by –1. All of this can be reduced to just two statements, as shown in Listing 1.

The code I've described is in-lined because you'll call it for every data point. As promised, the pixels-per-unit scaling factor is applied here. It's important to apply it before casting the result from floating point to integer.

RENDERING

All of the pieces of the puzzle are now in place for rendering the surface. You just need to connect the dots.

That's because you can create the surface as a collection of filled polygons laid edge to edge. Four adjacent points that have been projected onto the display define each polygon.

The polygons are drawn in strips. The strip furthest from view is drawn first, and the strip closest is drawn last. This way, hidden portions of the surface are painted over by closer portions that obscure the view of what's behind them. This is like painting a picture of the Alps by first painting the more distant mountains, and then partially covering them with a mountain range that is closer.

That sounds easy, but there's a catch. Which side is the back, and which is the front? The question arises because if you twist the surface 180° from where you started, what was the back is now the front and vice versa. If you twist the surface 90°, what was one side becomes the back and the other side becomes the front. The solution is to look at the surface as it's twisted through each of four 90° increments.

Referring to Figure 1c, when the body coordinate system is not rotated, the x-axis points out of the display and the y-axis points along its positive horizontal axis. When the body coordinate system is twisted by 90°, the x-axis points along the positive horizontal axis of the display while the y-axis points inward. Between these two limits, you'll draw from further away to closer if you draw in the direction of increasing x values and decreasing y values. This is illustrated in Figure 2. I put all of these ideas into the code that you see in Listing 1.

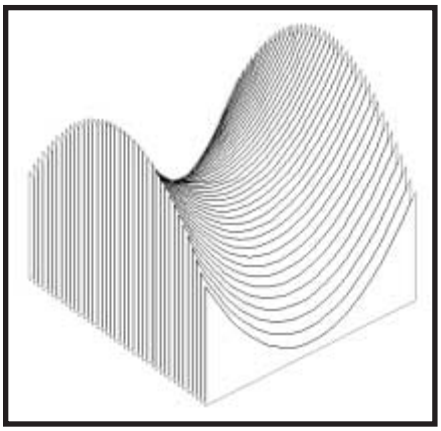


Figure 3—*Data can be represented in a different way. Instead of mapping out a surface, vertical slices can be drawn through the data, as if it were a solid object.*

Here's how to proceed in the remaining cases. When the surface is twisted between 90° and 180°, you draw in the direction of decreasing x and decreasing y values. From 180° to 270°, you draw along decreasing x and increasing y. Finally, when the twist is between 270° and 360°, the drawing is done along increasing x and increasing y.

In terms of speed, you'll find that the worst bottleneck is the polygon function. More sophisticated methods reduce the number of polygons to draw by checking if a surface is hidden. If it is, it doesn't need to be rendered.

An alternative approach is to reduce the number of polygons required by visualizing the surface in a different way. This works in the following way.

VARIATIONS ON A THEME

A surface is not the only useful representation of your data. It also can be helpful to view it as a series of cross sections, which is akin to slicing your data as though it were a Thanksgiving turkey, and then placing the slices upright, side by side.

You already have everything you need to do this; no new calculations are required. It's just a matter of taking the projections you found and connecting them a little differently.

Suppose you want to slice your data by cutting it into sections parallel to the y-axis. In this case, choose a fixed value for x and iterate through all of the y values. Draw line segments from the projection of one triplet to the next. At each end of this polyline, draw a vertical line that extends down to the projection of the minimum z value of your data. By connecting the two vertical lines with one final line, you'll have one slice of data (see Figure 3).

Repeat this for each value of x, and you'll reconstruct the data as a series of slices. In practice, rather than drawing lines, you'll use the polygon function so that you generate a closed, filled slice. This will paint over any part of a previously drawn slice that's obscured by the current one.

Just as with drawing a surface, you'll want to draw the slices from back to front. As before, what constitutes the back and front depends on how the data is oriented. Again, you need to consider four cases.

In the first case, when the data is twisted between 0° and 90°, draw your slices along increasing values of x (see Listing 1).

For the other three intervals, the slices are drawn as follows: from 90° to 180° along decreasing x; from 180° to 270° along increasing x; and from 270° to 360° degrees along decreasing x.

ONE CALL AWAY

The accompanying sample app demonstrates how the ideas presented here come together by displaying a surface that you can orient in space. Because the required calculations are minimal, you can rotate the surface in real time (even for large data sets).

With very little effort you can turn this code into a useful component of your project. When you do, viewing your data as a three-dimensional surface is just a function call away.

Martin Courtney earned a BS and MS in Applied Mathematics, and is pursuing a graduate degree in engineering. Currently, Martin is a senior software engineer at Information Systems Laboratory in California. You may reach him at mcourtn1@san.rr.com.

PROJECT FILES

To download the code, go to ftp.circuitcellar.com/pub/Circuit_Cellar/ 2002/147/.

Design Logic CONTEST 2001 WINNER

FEATURE ARTICLE

Richard Hosking

High-Frequency Job

Frequency Counter and VFO Controller

If you're looking for a way to stabilize a free-running local oscillator and obtain a frequency readout in one fell swoop, then Richard has the solution for you. How about a board that's comprised of an AT90S1200, a gate/prescaler circuit, and a loop filter/VCO control circuit?

Most receivers and transmitters nowadays use synthesized local oscillators that are locked to a crystal standard; however, there are still older and homebrew rigs with free-running local oscillators that are prone to drift. Many of these rigs don't have a frequency readout, which is virtually mandatory in today's crowded bands.

This article describes a board that you can use to stabilize a free-running local oscillator and provide a frequency readout in one package. As you can see in Photo 1, the board is quite compact; it can be mounted on the back of its LCD if required.

FUNCTIONAL DESCRIPTION

The board consists of a front-end gate/prescaler circuit, a microcontroller, and a loop filter/VCO control circuit using a passive integrator and voltage follower (see Figure 1).

The front-end samples the VFO signal, squares it, and gates and prescales it under the control of the microcontroller. The microcontroller counts the frequency of the VFO, decodes the data, and then displays it on an LCD module. The controller itself has only an 8-bit counter, which contains the most significant 8 bits of the count data at the end of each count period (100 ms).

The prescaler U2 (74HC4020) contains the other 14 bits of data. To access this, the prescaler is toggled via U1:C (pin 9) until the prescaler output changes state. The controller keeps track of how many pulses are required, and from this calculates the contents of the prescaler. Thus, the overall resolution is 22 bits. This means that frequencies up to about 40 MHz can be counted to a resolution of 10 Hz, which should be adequate for most applications. The controller converts the binary data to BCD and ASCII to drive the LCD (see Figure 2).

PLL CIRCUIT

The controller compares the frequency from one count to the next. If the loop is locked, the controller corrects any drift in the VFO by outputting a positive or negative pulse to an integrator/filter circuit.

A voltage follower buffers the integrator so that there is no significant voltage sag across the filter capacitor between counts. The voltage follower output is connected to a varactor diode that must be placed across the VFO tank circuit. The varactor should produce a frequency swing of about 5 kHz for a controlled voltage swing between 0.5 and 4.5 V. If the VFO is likely to drift more than this, then it should probably be redesigned or repaired.

If the error between counts is more than 50 Hz, it's assumed that the VFO is being tuned and the loop is unlocked. In this case, the circuit sets the VCO

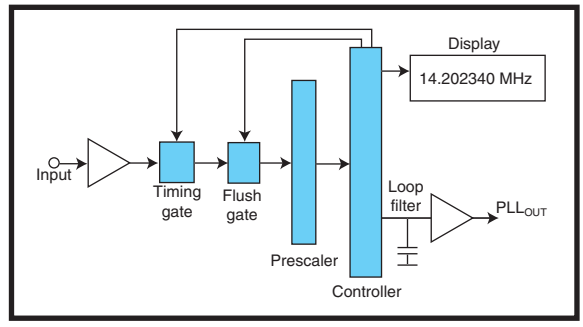


Figure 1—*The controller does most of the work, performing the main count and controlling the various peripheral devices.*

control to mid-range and waits until there are three counts without change before locking the loop again. There is no need to lock the loop manually; the PLL system is invisible to the user. This sequence is shown in Figure 3.

Pin	Definition
1	GND
2	VCC (5 V)
3	Contrast
4	RS (register select 1 = data 0 = command)
5	R/W (0 = write to display, 1 = read from display)
6	OE (enable—data clocked on negative transition)
7-14	D0–D7 (data)

Table 1—*This 4- to 8-bit parallel interface seems to have become the industry de facto standard for small LCD modules.*

PLL ANALYSIS

As far as the PLL is concerned, the controller is merely an intelligent phase detector. Assuming that the VFO can be shifted 5 kHz by the PLL with a swing of 0.5 to 4.5 V, the VCO gain (K_v) is 5000/4, or 1250 Hz/V. The frequency count takes about 120 ms with a pulse duration to the sample and hold circuit of 2 ms per 10-Hz error. Thus, phase detector gain (K_p) is:

$$\frac{4\left(\frac{2}{120}\right)}{10}\text{V/Hz}$$

or 7.5 mV/Hz. Using the PLL analysis program from KD9JQ with the loop values as shown (RC at 82 kΩ and 33 µF, damping 2.2 kΩ), then the 3-dB loop bandwidth is 9.8 Hz, and the lock time is 34 ms. The 10-Hz reference (i.e., the correction pulse) isn't attenuated significantly; it's audible on the VFO output, but this was not a problem in practice.

If the 2.2-kΩ damping resistor (R3) is omitted, the attenuation of correction pulses is improved. In such a case, the resistor is replaced by a short circuit. In theory, this would result in an unstable loop, but because the loop doesn't have to capture lock, it doesn't appear to be a problem in practice.

OFFSETS

Most rigs use an IF, and many also have a mixing scheme to allow use on several bands. With SSB rigs, there are usually different BFO frequencies for USB and LSB. Thus, the readout from the VFO requires a method of setting offsets to give the actual operating frequency. In this case, the board has four I/O lines available to select offset frequencies. Therefore, there are 16 possible offsets that you can set to 10-Hz resolution with a positive or negative offset. Note that it's only necessary to ground the I/O pin because there are on-board pull-ups on these inputs (see Figure 4).

After the data is entered, it's stored in the controller's nonvolatile EEPROM memory. To enter the offset data, you have to connect two pushbutton switches between bits 0 and 1 of port B and the ground.

If ENTER (bit 0) is grounded during normal counter operation, then the controller enters the offset setup code routine. You are then prompted to enter "POS" or "NEG" for offset. The SCROLL (bit 1) key is used to select the appropriate option. When Enter is pressed again, the program moves to

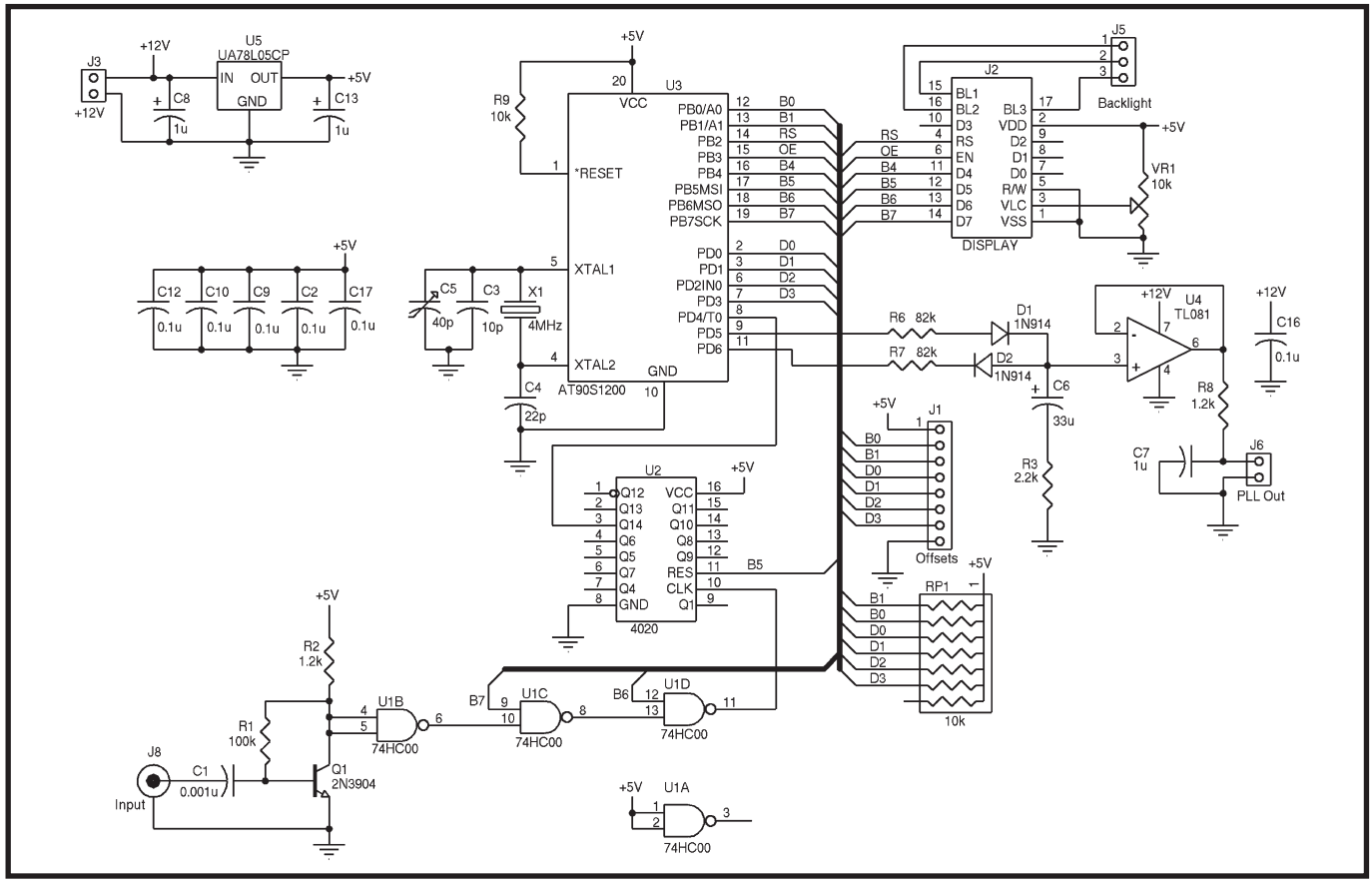


Figure 2—*The use of a microcontroller simplifies the circuit dramatically. There are only five ICs for a complete counter and phase-locked loop.*

the offset frequency. The flashing cursor indicates which digit is being entered. The Scroll key advances the digit from zero to nine and then rolls over to zero again if the Scroll button is pressed repeatedly. When Enter is pressed, the next digit is selected. Note that the final digit is always zero to indicate the frequency in hertz.

After the final digit is entered, the program returns to normal counting. The offset data is stored in the EEPROM at an address selected by the four offset select lines. You should set these lines appropriately before entering the setup program. When the counter is in operation, it accesses the EEPROM at the address selected by the offset select lines and adds/subtracts the offset from the VFO frequency accordingly.

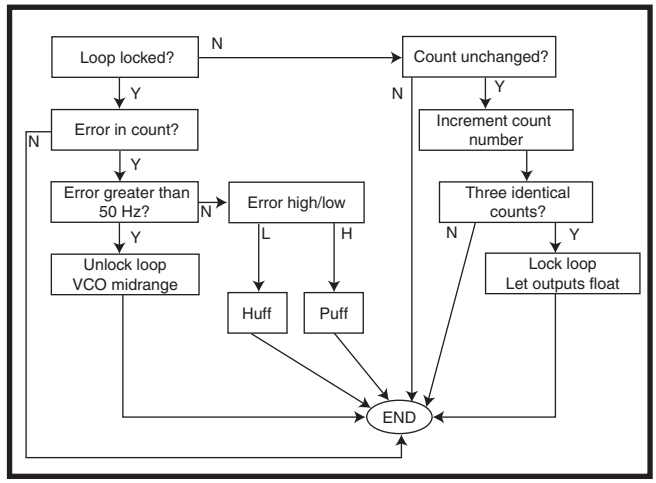


Figure 3—*The controller acts as an intelligent phase detector.*

DISPLAY

The board was designed to interface with 2 × 16 displays with a 4-bit parallel interface. This interface appears to be a de facto industry standard for small displays such as the Hitachi HD44780. In this mode, the display requires a 10-wire interface. Take a look at Table 1 for a list of the connections. In the 4-bit mode, only D4 through D7 are used. There are also two wires for the backlight if required.

At start-up, the display requires a fairly involved sequence to initialize it reliably, unless you can guarantee the rise time of the power supply. Unfortunately, it's not possible to poll the display before it's initialized. Some displays (e.g., Sharp) should mount directly via 0.1" spacing connectors (e.g., IDC style). Alternatively, a cable can be made using an IDC socket/plug or by wiring the connections individually. If you're going to use the backlight, it will require about 2.3 V at 70 to 100 mA.

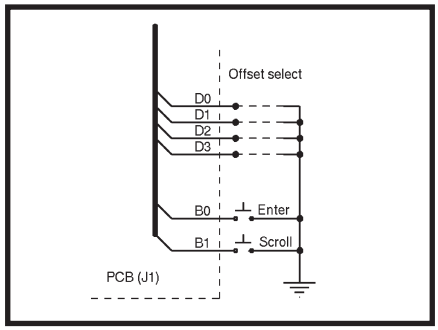


Figure 4—*Up to 16 offsets can be programmed using two push-button switches and selected via a 4-bit port.*

CONTROLLER

The controller is an AT90S1200. It has a 512-byte program memory, EEPROM, and serial flash memory programming, which means that it can be placed in the circuit where it is to be used and programmed there if desired.

The program memory appears to be small, but because of the rich instruction set, compact code can be written. In fact, this program used nearly all of the memory (510 of 512 bytes)! Take a look at Listing 1 for the count sequence I wrote as pseudo-code.

VFO CONNECTIONS

Connections to the VFO/rig will depend on the rig circuit. A typical scheme is shown in Figure 5. Beware of high voltages in valve rigs! If voltages are more than 50 V, then use high-voltage blocking capacitors at the input to the counter (C4) and for C1 in Figure 5.

If the board is to be built into an existing rig, then it's necessary to make connections to the VFO tank, VFO output, and an 8- to 12-V supply. Consult the rig circuit diagram to determine the appropriate connections. The components D1, R1, and C1 should be added across the VFO tank circuit. Use the smallest value of C1 possible that's consistent with obtaining a sufficient tuning range (5 kHz). You will have to experiment in order to determine this. For example, I used this circuit to stabilize a 5- to 6-MHz VFO. In this case, the varactor I used was a BB405B VHF diode with C1 at 2 pF. Bear in mind that a varactor is a low-Q device, which may add to VFO noise or even cause the VFO to stop oscillating.

If the varactor loads the VFO too much, the tuning range could be reduced to 3 kHz without too much of a problem. The VFO will probably have a buffer circuit. A sample should be taken at the output of the buffer via C4 for the input of the counter. For this article, I've shown an emitter follower buffer, but remember that each rig will have a different configuration. The counter input presents an impedance of about 1000 Ω, so the take-off point should have reasonably low impedance. The counter requires about 100-mV_{PP} for satisfactory operation.

CONSTRUCTION

The counter is built on a double-sided, plated-through, masked, and overlaid PCB. You may download the board overlay from the *Circuit Cellar* ftp site.

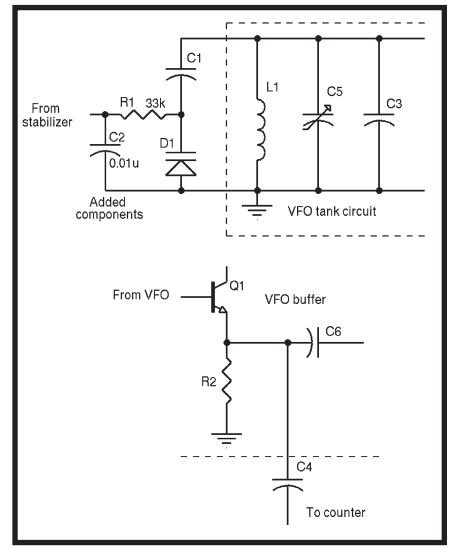


Figure 5—*These are connections to the VFO and VFO buffer. Suggested components are shown for a typical rig setup. Some experimentation may be required, depending on your particular rig.*

Make sure you mount the polarized components carefully (diodes/ICs/tantalums). Build the regulator section first, and check that the supply is 5 V before proceeding further. Although it's not mandatory, it's probably a good idea to use a socket for the controller. Be careful with static-sensitive devices (ICs/controller) by keeping them in conductive foam before mounting, and do not handle ungrounded objects. If you're going to solder the display in place, it's a good idea to wire the display via a temporary harness to check the operation of the counter before permanently wiring the display. Note that the underside of the board will be inaccessible for troubleshooting after the display is mounted. The board is simple, so it should not present any great difficulty to a designer of intermediate experience.

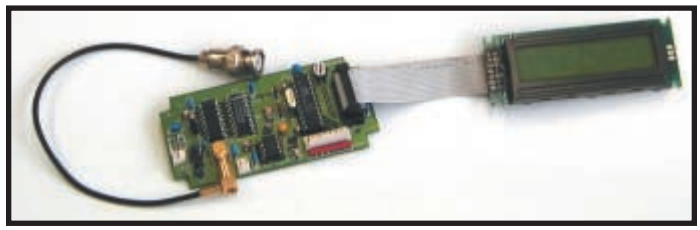


Photo 1—*This is the completed module. As you can see, the board is compact enough to be mounted on the back of the LCD.*

TROUBLESHOOTING

In every project I've built, there has been at least one error in the construction. Before powering up the board, you should check your construction again. You may download a parts list for this project from the *Circuit Cellar* ftp site.

Check the polarity of each component, and go over the board with a magnifying glass to inspect for bad joints and shorts. Look for shorts to ground from 5 V. Make sure that there is continuity between 5 V and the relevant pins on each IC. If the board does not work at first, adopt a systematic approach to troubleshooting.

Assuming the regulator works correctly, check the front-end circuit by applying a ~200-mV_{PP} signal, and then look at the output of the square (U1 pin 6). A square wave at the input frequency should be present. Check pins 4 and 5 of the controller where a 4-MHz clock signal should be present. Also, verify the continuity of the connections between the board and LCD module. There should be a series of pulses at a repetition rate of about 10 Hz on the control lines to the prescaler and LCD data lines. Adjust VR1 to give best display contrast. If you're still in trouble, check every connection on the board for continuity. Assuming the counter is working correctly, set the clock to exactly 4 MHz. Apply a signal of a known accuracy to the counter and adjust C5 until the correct reading is obtained.

UPDATE

A number of these modules have been successfully built. Current drain is modest at about 10 mA, which makes them suitable for use in portable rigs. In theory, the upper-frequency limit is about 40 MHz, even though the 2N3904 front-end buffer starts to run out of steam at this frequency. Replacing this transistor with a more capable one should improve top-end sensitivity.

As I mentioned before, the PLL damping resistor (R3) can be omitted without problems. This improves the attenuation of the 10-Hz correction pulses. The circuit does not have to respond to a step (i.e., to capture lock), so stability does not appear to be a practical problem. If there was a problem with stability, or a failure to lock, R3 could be replaced with a low-value resistor that is, say, 10 to 100 Ω.

The AT90S2313 is pin-compatible with the AT90S1200, and it has a more capable timer and added code space. For those of you who wish to develop the circuit further (i.e., for better frequency resolution), this controller can be used. Just remember that some code rewriting (e.g., register definitions) will be necessary.

Richard Hosking is a primary care physician in Australia. His technical interests include radio, DSP, and healthcare informatics. You may reach him at richardh@iinet.net.au.

Listing 1—*The pseudo-code describes the count sequence.*

```
Reset prescaler
Open gate/start count
Wait 100ms
End count
Toggle prescaler until the output changes state (keep track of
     number of toggles)
Calculate 22-bit binary count
Convert count to BCD
Add/subtract offset from EEPROM
Write to display
PLL routine
Repeat sequence
```

PROJECT FILES

To download the PCB layouts and parts list, go to ftp. circuitcellar.com/pub/Circuit_Cellar/2002/147/.

RESOURCES

Atmel Corp., "8-bit AVR Microcontroller with 1K Byte of In-System Programmable Flash—AT90S1200," 0838H, March 2002.

E. Skelton, "Frequency display and VFO stabilizer," *Elektor,* February 1998.

SOURCES

AT90S1200 Microcontroller
Atmel Corp.
(408) 441-0311
www.atmel.com

Hitachi HD44780
Hitachi, Ltd.
(800) 448-2244
www.hitachi.com



ROBOTICS CORNER

Jens Altenburg

SOPHOCLES

A Solar-Powered MSP430 Robot

Worried about the side effects of that presumably noxious gas that's lingering in your basement? Rather than trying to waft samples into an empty jar for your local health department to assay, try following Jens' lead by building your own gas-detecting robot.

Design contests are an excellent way to open the mind to special ideas. Without any pressure from customers, bosses, or other hindrances of the daily grind, you can work on a variety of splendid projects. The result of such a project is SOPHOCLES, which stands for SOlar Powered Hidden Observing VehiCLE(S).

SOPHOCLES is a robot with a detector that looks for poisonous gases or dusty air (see Photo 1). When gases are detected, its motors bring it to that location and a built-in camera takes pictures of the dangerous areas. The robot's radio then gives you information about the detected materials. You can control the robot and how the solar cells spend power for missions that require low-power intermittent operation over the course of many weeks.

THE BASICS

Since the first microcontroller was produced, robots have been controlled by a piece of silicon. In this article, I'll describe how I applied the Texas Instruments MSP430 (see Figure 1). In addition, you'll learn about my robot's special features, which include an air quality sensor, solar cell, and CMOS camera sensor that's used for picture transmission via a wireless radio.

This is not merely a fun project for freaky engineers or enthusiasts. SOPHOCLES can perform real tasks such as observing potentially dangerous areas and checking air quality. In addition, you can use its wireless radio to connect several robots to each other or to a central PC.

The robot has two main operation modes, Autonomous and Command. Autonomous mode is powered by the implemented artificial intelligence of each robot. The robot works independently, checks air quality, and gives you a signal if any difference has occurred. In Command mode, you can operate the robot by sending commands such as left, right, go ahead, go back, and so on. Of course, you can also take pictures with the built-in camera. Short picture sequences can be saved as an animated slide show (e.g., for documentation).

This is a complex electronics project that can be realized even if you have a low budget; therefore, this robot can be used for either academic training or fun.

THE DETAILS

The MSP430 microcontroller controls SOPHOCLES. Why did I need an MSP430? There are lots of other micros, some of which have more power than the MSP430, but the word "power" shows you the right way. SOPHOCLES is the first robot (with the exception of space robots like Sojourner and Lunakhod) that I know of that's

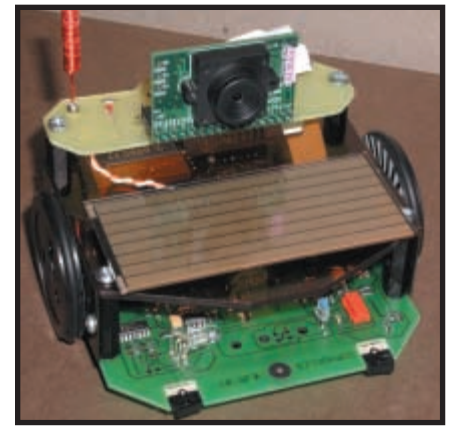


Photo 1—*Take a look at the complete SOPHOCLES. The case for the optical gas sensors, consisting of the multicolor LED and the TSL250 in front of the robot, has been removed to give you a better view. The CMOS camera is placed on top of the robot, and the radio modem is hidden behind the camera so only the antenna is visible. A flexible cable connects the camera with the MSP430 microcontroller.*

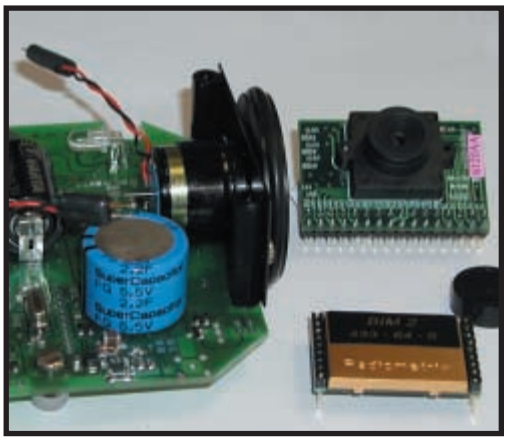


Photo 2 (*left*)—*On the PCB, the iron plates fix the DC motors. The second motor shaft later carries an optical shutter for counting revolutions. The cylindrical component is the gold cap for the power.*

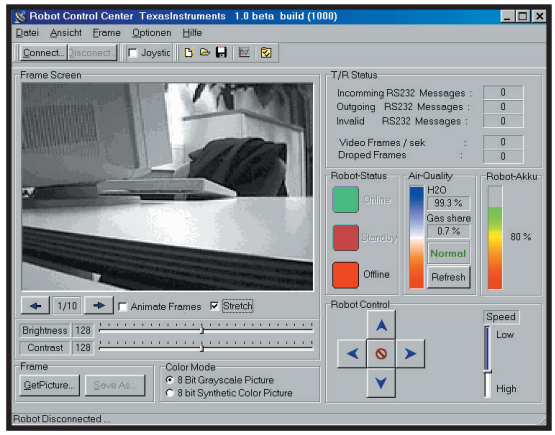


Photo 3 (*right*)—*The Robot Control Center serves as an interface to control the robot. Its main feature is to display the transmitted pictures and measurement values of the sensors. With enough power (maximum charged gold cap), the robot can be controlled by a remote.*

powered by a single lithium battery and a solar cell for long missions.

How is this possible? The magic mantra is, "Save power, save power, save power." In this case, the most important feature of the MSP430 is its low power consumption. It needs less than 1 mA in Operating mode and even less in Sleep mode because the main function of the robot is sleeping (my main function, too). From time to time the robot wakes up, checks the sensor, takes pictures of its surroundings, and then falls back to sleep. Nice job, not only for robots, I think.

The power for the active time comes from the solar cell. High-efficiency cells provide electric energy for a minimum of approximately two minutes of active time per hour. Good lighting conditions (e.g., direct sunlight or a light beam from a lamp) activate the robot permanently. The robot needs only about 25 mA for actions such as driving its wheel, communicating via radio, or takes pictures with its built in camera. Isn't that impossible? No! Let's have a look at the inner workings of SOPHOCLES.

POWER SUPPLY

The robot has two power sources. One source is a 3-V lithium battery with a 600-mAh capacity. The battery supplies the CPU in Sleep mode, during which all other loads are turned off. The other source of power comes from a solar cell. The solar cell charges a special 2.2-F capacitor. A step-up converter changes the unregulated input voltage into 5-V main power. The LTC3401 changes the voltage with an efficiency of about 96% (see Figure 2). If the input voltage increases to about 3.5 V (at the capacitor), the robot will wake up, changing into Standby mode. Now the robot can work.

The approximate lifetime with a full-charged capacitor depends on its tasks. With maximum activity, the charging is used after one or two minutes and then the robot goes into Sleep mode. Under poor conditions (e.g., low light for a long time), the robot has an Emergency mode, during which the robot charges the capacitor from its lithium cell. Therefore, the robot has a chance to leave the bad area or contact the PC.

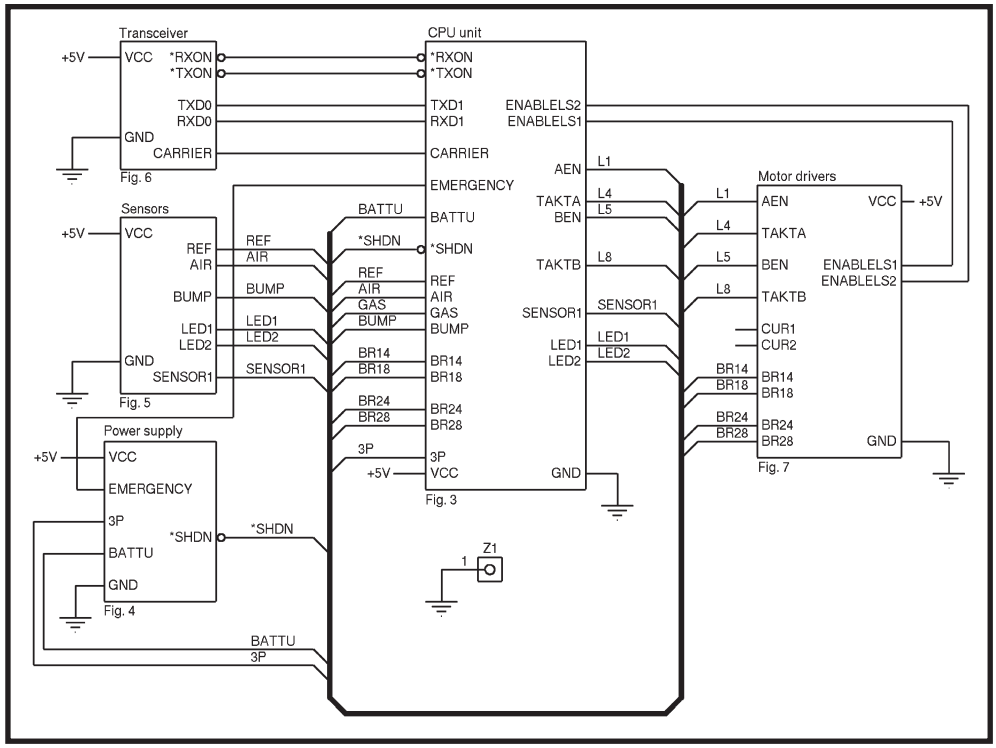


Figure 1—*The electronics of SOPHOCLES consists of several blocks, including the transceiver, sensors, power supply, motor drivers, and MSP430 CPU. Some block functions (i.e., the motor driver or radio modems) are represented by software modules. Such combined hardware and software modules can be used in numerous other projects with minor modification.*

WIRELESS RADIO

If the robot finds a suspicious measurement, it communicates the information via an alarm system like a PC. Wireless radio works with a 433-MHz low-power device (see Figure 3). Because of the restricted power conditions, an intermittent working regime is implemented. After every 50 ms in Active mode, the robot checks the carrier signal from the radio. When a signal is not found, the radio will be switched to Standby mode.

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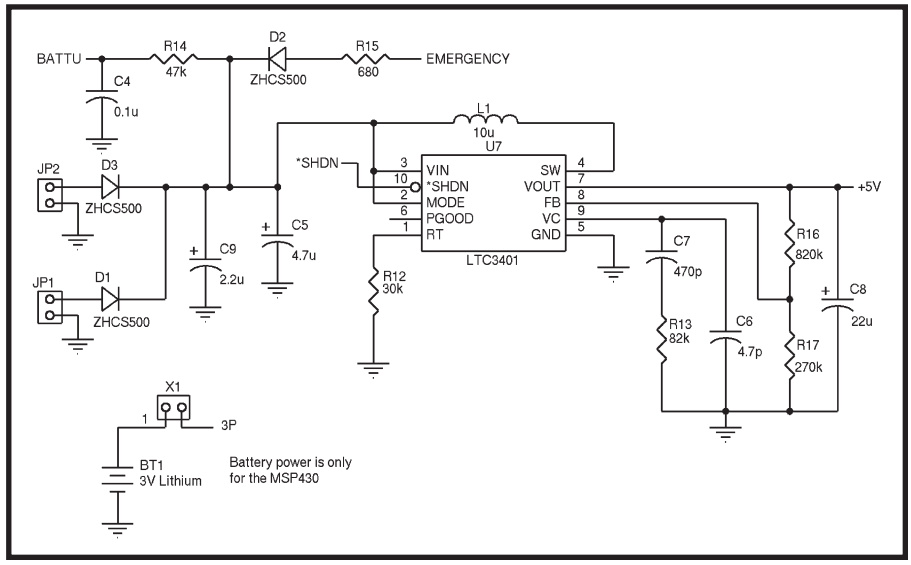


Figure 2—*Because of the changing light conditions, a step-up voltage converter is needed for generating stabilized V_{CC} voltage. The LTC3401 is a high-efficiency converter that starts up from an input voltage as low as 1 V. The selection of L1, C8, and C11 is important to ensure that the LTC3401 works correctly. Linear Technology recommends X5R capacitors and inductors by Sumida (www.sumida.com).*

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The robot is also controlled via radio. As soon as power is available, the robot accepts direct commands from an operator. Theoretically, the highest data transmission rate is 64,000 bps.

DC MOTORS

Servos for RC models are often used for driving the wheels in small robot designs. Usually, these servos have enough power for driving their own current needs of approximately 10 mA for electronics and about 80 mA for the built-in motor itself. As a result, two of these servos need 150 to 200 mA during motion. That was much too much for my needs, so I chose another motor.

The Black Forrest region of Germany is well known for the cuckoo clocks produced there; however, high-precision gear motors are produced there too. Take a look at Photo 2 and then refer to the FTB Feintechnik Bertsch GmbH web site to see what I mean (www.ftb-bertsch.de).

The secret of the miniature motor's low profile is in its flat rotor (not iron), which is composed of three flat, oval-shaped windings that rotate in the axial-magnetized stator air gap. The rotor doesn't suffer from cogging or iron losses, but benefits from its low inertia. This results in a low starting voltage, high efficiency, excellent acceleration capability, smooth low-speed motion, simple linear speed control, and high short-time overload capacity. In short, it's the ideal power supply for SOPHOCLES (see Figure 4).

I also replaced the integrated commercial H-Bridge drivers, like L293 and others, with a simple CMOS circuit. The 74ABT126 drives about 60 mA. I used two parallel stages in the circuit, and 120 mA is more than enough for the DC motors.

In addition, two optoelectronic components serve as a revolution counter. A shutter interrupts the light beam twice per revolution, so an exact measurement of the moving distances is possible.

CAMERA

One of the most interesting features of my robot is its built-in CMOS camera. The main problem with transmitting video signals is the broad channel width for quality videos. Streaming

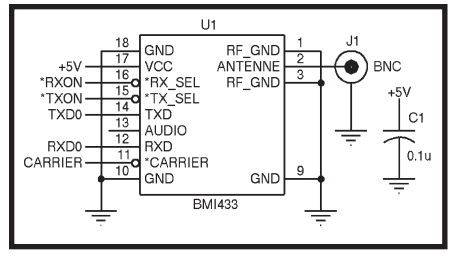


Figure 3—*The Radiometrix BiM 433 module serves as a radio transceiver. Depending on the series, data rates up to 160 kbps are possible. The transceiver works as a low-power device with 10 mW in the 433-MHz frequency range.*

video wasn't necessary for this project; still pictures are sufficient. The solution to the problem of obtaining pictures was a direct connection between the CMOS sensor and MSP430 (see Figure 5). The MCU controls the camera, gathers the pixel data, and saves a picture before transmission starts.

How does the MSP430 do this? The pictures have a resolution of 176 × 144 pixels. To save one picture, the controller needs about 26 KB of memory. But only 2 KB of RAM is available, right? Well, you can reprogram the MSP430's internal ROM (48 KB of flash memory). About 100,000 writing cycles are typically allowed, and that was enough for my application.

The camera offers two working modes, Master (default) and Slave. In Master mode, the internal logic of the camera chip sends the pixels as an endless datastream to the parallel port Y[0..7] (black and white camera). The typical pixel clock time is about 112 ns long. This time is too short to capture the data bytes from the Y port into the MSP430 memory.

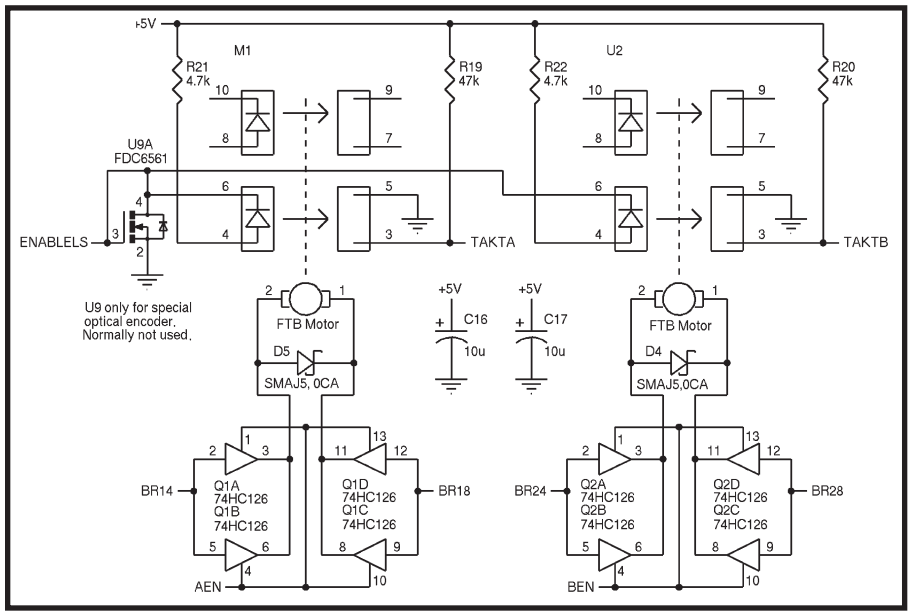


Figure 4—*The DC motors are controlled by an H-Bridge. Because of the low power consumption of the DC motors, a 74ABT126 works as a power stage. Two stages are connected in parallel, so the maximum output current is about 100 mA. That's enough for the motors. The photo interrupter serves for revolution detection and distance measurement. The MSP430 counts every light ray interrupt for motor revolution measurement.*

One solution is the SX28 micro (camera in Master mode), which Rowe, Rosenberg, and Nourbakhsh describe in their paper, "A Simple Low-Cost Color Vision System." [1] In Slave mode, the chip gets an external clock and timing signals from the MSP430. With these signals the MSP430 controls the camera chip. Now there is enough time to store the picture in flash ROM (see Figure 6).

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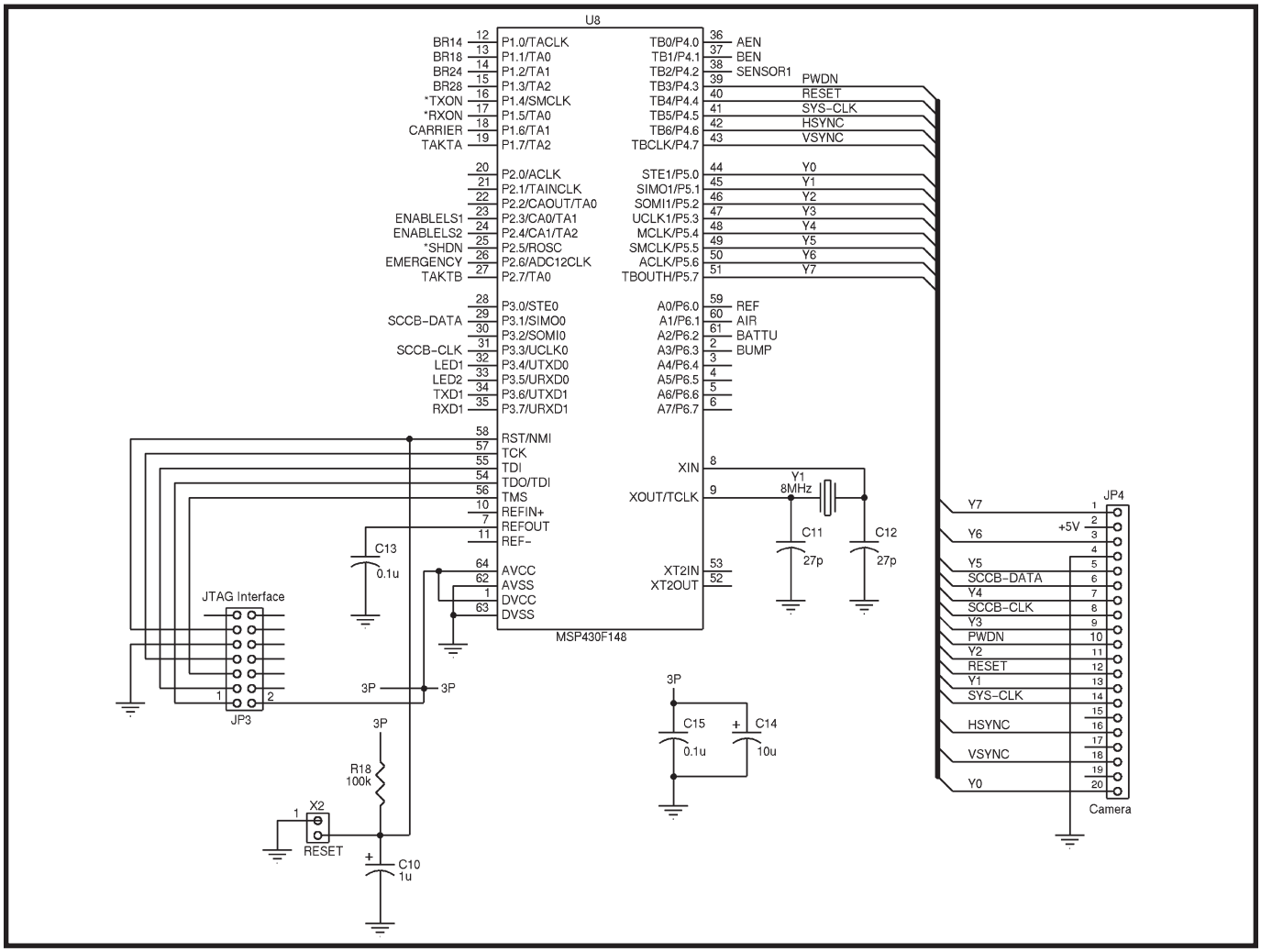


Figure 5—*The heart of SOPHOCLES is the MSP430148 microcontroller. An 8-MHz crystal clocks the MSP430 device. The JTAG interface, which is used for programming and debugging, is available via a JP3 connector. JP4 connects the CMOS camera to the CPU.*

GAS DETECTOR

There are several gas sensors available, and most of them use a heated crystal for detection. The crystal's electrical resistance depends on the gas concentration. It's easy to measure concentration of poisonous gases like CO_2, NO, and CO, but the crystals must be heated. The heating time lasts about two minutes with a heating current of 150 mA, which is too much.

I had to design a new sensor, so I looked for an optical detector (see Figure 7). The light absorption depends on the different gases in the air, and the changing of the proportions changes the optical density.

I used the MSP430's high-precision A/D converter in combination with a multicolor LED. Two identical optical channels were built in. One of these stays in contact with the air, and the other is in airtight packaging. The difference between the channels is the value for detection of bad or poison gases.

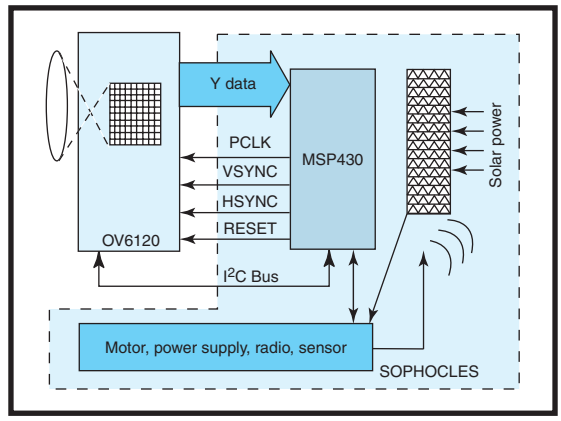


Figure 6—*The relationships among the MSP430, CMOS camera, and peripheral devices are demonstrated here. The MSP430 controls the camera via an I²C interface. The video data is captured as 8-bit values, and it should be synchronized by several clock signals (i.e., PCLK, VSYNC, etc.).*

CONTROL SOFTWARE

The robot is not only useful for serious applications, it's also fun, which is important too. Therefore, the control software should be easy and understandable for everyone, especially for kids.

The control software runs on a normal PC, and all you need is a small radio box to get the signals from the robot. Various buttons and throttles give you full control of the robot when power is available or sunlight hits the solar cells. In addition, it's easy to make short slide shows from the pictures captured by the robot. Each session can be saved on a disk and played in the Robot Control Center, which is shown in Photo 3. The software and sample missions are available.

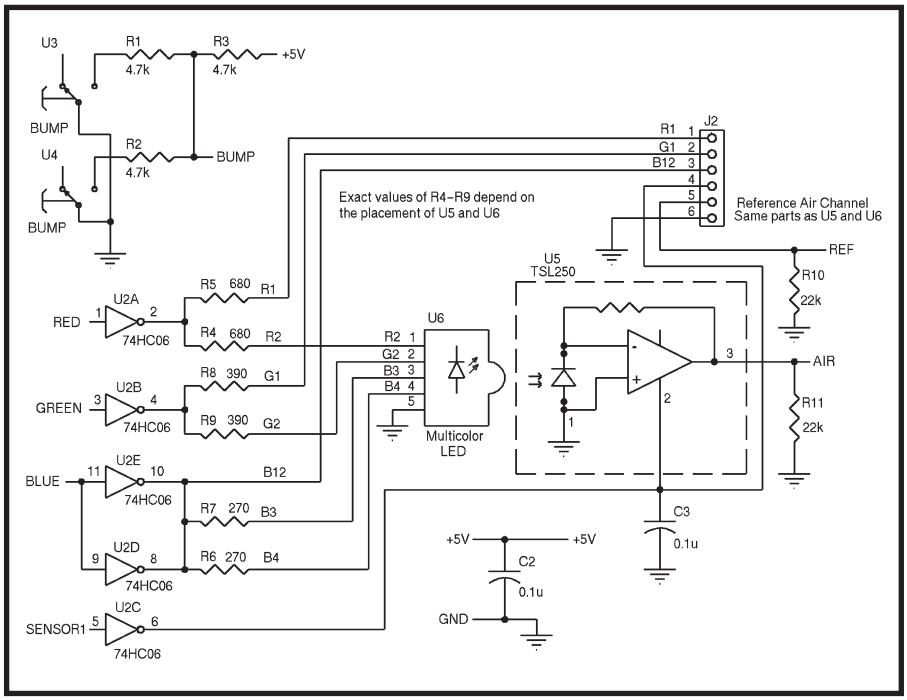


Figure 7—*The sensor unit consists of the gas sensor (multicolor LED and TSL250 photo sensor) and bumpers (microcontroller switches for edge detection). A third sensor for voltage measurement is placed in the power supply unit (R27, C7).*

PRICE AND PERFORMANCE

The fact that SOPHOCLES is both small and powerful illustrates the possibilities of modern technology. By combining a high-performance microcontroller with less power consumption and other electrical components, I came up with a robot that's both interesting and useful.

Building the robot was an expensive endeavor, but it was cheaper than you might expect. You can purchase the camera for about $60 and the motors for $70. Notably, the powerful MSP430 is the least expensive of the main components.

Jens Altenburg is a project leader at Software & Systeme Erfurt GmbH in Germany. He studied information technology at the Technical University of Ilmenau, Germany and qualified as an engineer in 1990. His interests include microcontroller technology, electronics, mechanics, and software. You may reach him at jens.altenburg@t-online.de.

PROJECT FILES

To download the code, go to ftp.circuitcellar.com/pub/Circuit_Cellar/2002/147/.

REFERENCE

[1] A. Rowe, C. Rosenberg, and I. Nourbakhsh "A Simple Low Cost Color Vision System," www-2.cs.cmu.edu/~cmucam/.

RESOURCES

J. Altenburg and U. Altenburg, *Mobile Roboter*, Carl Hanser Verlag, München, 2002.

J. Labrosse, *MicroC/OS-II*, R&D Books, Lawrence, KS, 1999.

R. Man and C. Willrich, "A Minimalist Multitasking Executive," *Circuit Cellar* 101.

SOURCES

LTC3401
Linear Technology Corp.
(408) 432-1900
www.linear-tech.com

BiM 433
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FEATURE ARTICLE

Philip Ching & Bruce Land

Light the Way

An LED-Based Alternative

Actors get paid big bucks to feign abstractions such as happiness. But when it comes to imitating the physical world, Hollywood looks to engineers. Philip and Bruce describe how they faked a flame and illuminated an audience with a real-time LED-based candle.

Do you remember the theme to the *Sorcerer's Apprentice* in Disney's *Fantasia*? One of the more memorable images in *Fantasia* is that of the sorcerer's apprentice as performed by Mickey Mouse. Now, inside any self-respecting sorcerer's study, you'll probably find candles, which provide light for the sorcerer to read his book of spells well into the late hours of the night. However, if you have a background in theater, or at least some common sense, then you know that bringing an open flame onstage probably isn't such a good idea. This is especially true if you're around children, unless you enjoy regular visits from the fire department. Therefore, an open flame is one prop you can most likely do without.

During the fall of 2001, we spoke with this fellow from Cornell University's Neurobiology and Behavior department named Tom. He mentioned he was participating in a play and that he wanted to use a candle for added effect. However, as we mentioned, having an open flame onstage isn't a good idea. But what if we could build a candle for him, one that used an LED that looked convincingly like a real flame? If you were a problem solver, or a person who enjoys fun projects, you'd give it a try, wouldn't you? Besides, an idea as brilliant as this spells dot-com startup, and more importantly, Tom will have a candle for his play!

MAKE IT CONVINCING

If you'd like your own candle too, you're in luck because we're going to tell you how we did it. Building a candle is challenging because it consists of three smaller projects: designing the flame dynamics, adding the breeze sensors, and packaging the candle.

Our primary concern was to make the candle's LED be convincing enough to pass for a real flame. What must be considered so that the candle looks real? Well, the candle must have time-variable light output. Anyone who looks at a candle flame will notice that it's not always periodic, but seems to have a random component.

The candle also must have breeze sensors. A candle flame dances when subjected to light breezes, or blows out when the breeze is too strong. In addition, everything must be in real time. How convincing would a candle look if you blew on it, and the flicker dynamics changed three minutes later? Not convincing at all, that we can tell you! Last but not least, the packaging should be made to look like a real candle.

FLAME DYNAMICS

We wanted to simulate the flame dynamics by using time-variable light output to match the statistics of a real flame without having to worry about dynamics such as turbulence. After several searches on the Internet, we found an article written by Fujiwara and Kiyozawa called the "Spectral Model and Statistical Parameters of

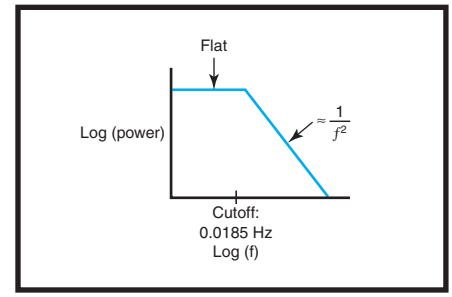


Figure 1—*Take a look at the time-variable light output. The flame dynamic follows this pattern.*

Biostimulation with 1/f Fluctuation Power." [1] Don't be intimidated by the title, which sounds rather technical. Unlike many of the papers out there, the article was actually quite readable.

The authors found that the flame dynamics follow a flat power spectrum at low frequencies and fall off at $1/f^n$ power spectrum with $n = 2.12 \pm 0.7$ at higher frequencies (see Figure 1). The variable n that Fujiwara and Kiyozawa found is not distinguishable from the slope of a one-pole, low-pass filter. A simple low-pass filter has a slope of 2.0. Because real candles seem unpredictable, we tried passing white noise through a digital low-pass filter to produce simulated candlelight.

We generated white noise by using a random number generator that was written in C and adapted from Brian Kernighan and Dennis Ritchie's book *The C Programming Language: ANSI C Version*. [2] The excerpt of code in Listing 1 was taken from the final program. A uniformly distributed number between –0.5 and 0.5 is generated, with an average value of zero.

The following equations were used to calculate the new number to set the intensity of the light. A single-pole low-pass filter was modeled as:

$$z_{t+1} = z_t\alpha + (1 - \alpha)w \qquad [1]$$

Equation 1 was adapted from Samuel Stearns' book *Digital Signal Analysis*. [3] In the equation, z_t is the filter output at time t with an initial value of zero at $t = 0$. And w is the white noise input.

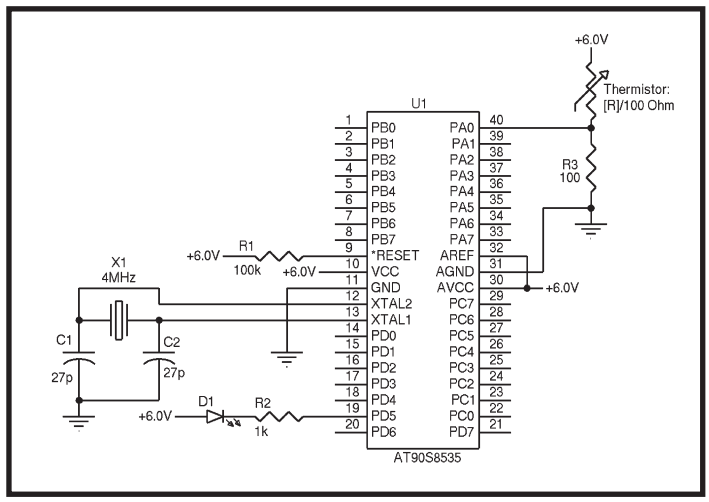


Figure 2—*The final circuit for the candle is based on the Atmel AT90S8535.*

Alpha, α, serves as a weight. A smaller alpha will place more emphasis on the white noise input, implying a higher cutoff frequency of the low-pass filter. Alpha is calculated as follows:

$$e^{\frac{\Delta t}{\tau}} = \alpha \qquad [2]$$

Alpha is a measure of how much the signal would decay if the filter's impulse response were exponential with a time constant of τ. In Equation 2, Δt is equal to 64 ms in our code, which determines how often the new number to set the intensity of the light is calculated.

The complete new number to set the intensity of the light is calculated as follows:

$$\text{New brightness} \equiv (z_{t+1} \times I_{scale}) + I_{offset} + (\text{blow} \times w) \qquad [3]$$

where I_{SCALE} sets the standard deviation of the filtered white noise, and I_{OFFSET} sets the average intensity. The last term depends on a breeze sensor to supply a variable *blow*, which represents the wind speed. We modeled flickering as a result of a breeze as unfiltered white noise that's proportional to *blow*, in addition to the modification to I_{SCALE}, which we'll explain next.

The brightness variable controls the pulse width modulator hardware in the Atmel AT90S8535 microcontroller. When the PWM mode is selected (Timer 1/Counter 1), the output compare register 1A (OCR1A) forms a dual 8-bit, 9-bit, or 10-bit free-running, glitch-free, and phase-correct PWM with outputs on the port D5 pin. [4] The port D5 pin directly drives the flame LED.

Listing 1—*For this excerpt of code,* `next` *is an unsigned long int, and* `finalRandomNum` *is a float.*

```
next = next * 1103515245 + 12345;
randomNum = (unsigned int)(next/65536) % 32768;
finalRandomNum = randomNum;
finalRandomNum = finalRandomNum/32767 - 0.5;
```

BREEZE SENSORS

The detection of breezes in the environment is accomplished by implementing a thermistor (see Figure 2). The principle behind a thermistor is that the resistance changes as a function of temperature. As the thermistor heats up, the resistance decreases; the resistance increases when there's a decrease in temperature. Enough current will heat the thermistor above ambient temperature.

The 0603 surface-mount thermistor we used requires 3 mW to heat it 1°C. We picked a DC current so that the temperature was approximately 50°C. Because it's self-heated, a gentle breeze cools the thermistor so that the resistance increases and the voltage across the 100-Ω resistor decreases. The voltage read by the 8535 ADC value is represented by 8 bits; it's approximately 20 mV per bit. We read a change in voltage of around 50 mV for a breeze caused by blowing on the sensor. The *blow* variable depends linearly on the change in voltage read by the ADC.

PACKAGING

Because the candle was destined for the stage, several people who looked at the prototype suggested that the candle would appear more realistic if the circuitry and wiring were hidden from sight.



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Photo 1—*The LED-based candle burns brightly! If you look closely, you'll notice that it's an LED and not a real flame.*

So, we used a cardboard shipping tube approximately two inches in diameter, and cut it to about 7″ in height. The circuitry and the battery pack were hidden inside, with the battery pack sitting at the bottom to serve double duty as a stabilizing weight. In addition, we applied three coats of white semi-gloss paint so that the exterior looked waxy, which gives the added effect of looking like a real candle. Lastly, the LED was lightly sanded to diffuse the light and covered with frosted tape. We cut the tape into the general shape of a flame.

ADDITIONAL DETAILS

The basic operating principle is simple. At start-up, continuously compare the current ADC value to the last five ADC values. If there are at least three matches with the history table, then the current ADC value becomes the V_{ZERO} value. The V_{ZERO} serves as a base to compare future voltage changes in the system. This scheme compensates for variability in the thermistor and background air motion.

Why did we choose five previous values instead of more (or less)? Four and fewer values did not give a good V_{ZERO}. We wanted the system to have as accurate a V_{ZERO} value as possible, but not stall in the start-up state on the condition when the ADC value bounces between two values. At initial start-up, the thermistor heats up and the ADC changes in one direction only in a still-air environment.

After the V_{ZERO} value has been obtained, we continuously read the ADC value. We found a set of parameters that looked convincing in a breeze between the change in voltage and the parameters: *I_scale*, *alpha*, and *blow*. With increasing breeze strength, *I_scale* and *alpha* decreased while *blow* increased. The combination of parameter changes makes the flame appear to flicker faster and more randomly.

PROGRAM THE ’8535

The coding for the AT90S8535 was completed using the CodeVision AVR C compiler for Atmel. You may download the final version of the code from the *Circuit Cellar* ftp site.

CodeVision offers several versions of its compiler, which include a free downloadable evaluation version as well as a commercial version. The difference between the two is that the free version will not allow you to program the chip when the file size exceeds the preset limit and lacks some libraries. For our candle project, we needed to purchase a license for the commercial version for its size and libraries.

Because we used the built-in CodeWizard automatic program generator, we were able to write all of the code needed for implementing a great many of the functions (e.g., input/output port, timers/counters, and A/D converter initializations) in a matter of minutes. The built-in in-system AVR programmer is compatible with the Kanda Systems STK200+ development board we used, with automatic programming after successful compilation through the parallel port of the PC.



Photo 2—*With this view from above, you can see the LED flame with the thermistor, which is the little black dot on the right.*

After programming the '8535 on the STK200+ board, it was taken off and placed in a 40-pin ZIF socket. Taking the chip off the board is not a difficult task; it requires a crystal, a few capacitors, and a resistor to run, in addition to the correct supply voltage.

PUT IT TOGETHER

Take a look at Figure 2 to see what the circuit looks like when its completed. The breeze sensor is located on the top right. You can see the LED on the bottom left. The rest of the components are added so that the AT90S8535 can run off the development board. The components are fairly easy to obtain at a local electronics store. What isn't shown in Figure 2 is the 6-V battery pack (consisting of four AA batteries), switch, resistor, or an additional LED to indicate that the power is on.

A CLOSER LOOK

Refer to Photo 1 and Photo 2 for snapshots of the final candle. The candle looks real, but in order to do it true justice, you need to see it in person or in the soon-to-be-available online movie featuring it.

FUTURE WORK

According to several people, our candle looks convincingly real. If time permits, we'll measure the output spectrum; however, there's always room for upgrades. One such upgrade would involve sensitivity controls. Depending on whether or not a certain, say, button is pushed, the candle may be more sensitive to breezes in the environment. Another variation would involve changing the uniform white noise to Gaussian white noise. We hope to implement these changes in the near future.

Philip Ching received both a BS and MS in Electrical Engineering from Cornell University in 2001. His interests include computer engineering and digital VLSI. You may reach him at pc59@cornell.edu.

Bruce Land is a senior research associate in Neurobiology and Behavior as well as Electrical and Computer Engineering at Cornell University. He received a BS in physics from Harvey Mudd College in 1968 and a Ph.D. in neurobiology from Cornell University in 1976. Currently, Bruce teaches two neurobiology and behavior courses and one electrical and computer engineering course at the university. When time allows, he does some neural modeling. You may reach him at BRL4@cornell.edu.

PROJECT FILES

To download the code, go to ftp.circuitcellar.com/pub/Circuit_Cellar/2002/147/.

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[1] O. Fujiwara and Y. Kiyozawa, "Spectral Model and Statistical Parameters of Biostimulation with 1/f Fluctuation Power," *Electrical Engineering in Japan*, vol. 121, no. 4, 1997.

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SOURCES

AT90S8535 Microcontroller
Atmel Corp.
(408) 441-0311
www.atmel.com

CodeVision AVR C compiler
Dontronics
www.dontronics.com/cvavr.html

STK200+ development board
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FEATURE ARTICLE

David Prutchi &
Michael Norris

Convert Your PC Sound Card

Make a DC-Coupled Arbitrary Waveform Generator

Many consumer-grade sound cards are insufficient for inducing signals that have low-frequency or DC components. However, with the right software, a PLL circuit, and a little know-how, you can convert your PC sound card into a precision DC-coupled arbitrary waveform generator.

A common practice in evaluating the behavior of signal processing or control circuitry is to make use of an analog function generator to produce the necessary test input signals. The typical cookbook waveforms of the function generator are then used to investigate the behavior of the circuit when stimulated by sine, square, and triangle waves of different amplitude and frequency. In most applications, however, repetitive sine, square, and triangle waves are seldom representative of the signals that the equipment being tested is designed to process. For example, the heart's electrical signal that's acquired and processed by cardiac biomedical equipment is a waveform consisting of a complex mixture of these basic wave shapes intertwined with intermittent baseline segments. The same is true for automotive controls, video, radar, and most other real-world applications.

Enter the arbitrary waveform generator (also known as an arb). This device is a generator capable of directly synthesizing an arbitrarily complex analog signal from digital data. It has memory at its core, which contains the full time-domain digital representation of the desired waveform. In order to generate the analog signal, the discrete point-by-point version of the waveform is played in a sequential manner through the generator's digital-to-analog converter. [1]

Commercial arbs are either standalone units or PC add-in cards that typically include high-speed memory and D/A converters to generate one or more arbitrary wide-band waveforms. The complexity of high-performance memory and D/A circuitry, as well as the proprietary nature of the software used to design and download waveforms, has kept the price of arbs out of the range of most hobbyists. But it doesn't have to be that way, especially if your application has a bandwidth limited to a few kilohertz, because $10 worth of hardware will turn your PC into a low-frequency, precision DC-coupled arb.

ARB IN YOUR PC

By the definition above, the PC sound card is a true audio-range arb; it takes the waveform definition stored in the computer's memory and plays it back as an analog signal in the range of 20 Hz to 20 kHz. The simplest way of generating an audio-range arbitrary wave through the PC sound card is to store it as a .wav file and play it back using Windows' Media Player utility.

Unfortunately, the typical 20-Hz high-pass cutoff frequency and uncalibrated output level of consumer-grade sound cards makes them unsuitable for simulating signals that have low-frequency or DC components. In addition, the output stage of sound cards doesn't usually have the output linearity or passband flatness required for the accurate reproduction of low-frequency signals.

In spite of this, a phase-locked loop (PLL) circuit and some software can turn a sound card into a precision DC-coupled arb. The idea is to use a software FM modulator to turn the arbitrary signal to be generated into an audio tone that's played through the PC sound card. The tone's frequency varies as a function of the desired arbitrary signal. The arbitrary signal (with all of its low-frequency and DC components) is then recovered by hardware FM demodulation of the audio signal.

.WAV FILES

A .wav file is a series of samples preceded by a header that tells the player program important things like the sampling rate and number of bits in the sample. The player program reads the header, sets up the sound card, and then feeds the samples to the card's digital-to-analog converter.

PC multimedia data is often encoded in the Resource Interchange File Format (RIFF). RIFF is based on chunks and sub-chunks. Each chunk has a type, represented by a four-character tag. This chunk type comes first in the file, followed by the size of the chunk, and then the contents of the chunk. The .wav format is a subset of RIFF used for storing digital audio, and it requires two kinds of chunks: format (fmt) and data. The former describes the sample rate, sample width, and so on. The latter contains the actual samples.

The .wav format can also contain any other chunk type allowed by RIFF, including list chunks, which are used to contain optional kinds of data such as the copyright date and the author's name. Chunks can appear in any order.

In its simplest form, the .wav format starts with the RIFF header depicted in Table 1. The .wav specification supports a number of different compression algorithms. The format tag entry in the fmt chunk indicates the type of compression used. A value of one indicates linear pulse code modulation (PCM), which is a straight, or uncompressed encoding of the samples, which is the exact amplitude of each sample.

The fmt chunk describes the sample format (see Table 2), and the data chunk contains the sample data, as you can see in Table 3.

Offset	Length	Contents
0	4 bytes	RIFF
4	4 bytes	<file length – 8>, where *8* is the length of the first two entries (i.e., the second entry is the number of bytes that follow in the file)
8	4 bytes	WAVE

Table 1—*The .wav file format starts with the Resource Interchange File Format (RIFF) header, which identifies the data as that belonging to a sound wave.*

All numeric data fields are in the Intel format of low-high byte (usually referred to as "little endian"). Eight-bit samples are stored as unsigned bytes, ranging from 0 to 255. Sixteen-bit samples are stored as two's-complement signed integers, ranging from –32,768 to 32,767.

If you're a Matlab user, you can avoid the hassle of file formatting by directly playing a datastream from within the Matlab environment using the sound command. Matlab can also write .wav files from data variables, or read the .wav file PCM-encoded signal into data that can be manipulated by Matlab.

Another possibility is to use a professional waveform design package, such as the Pragmatic Instruments WaveWorks Pro, to create the desired signal. You can then use software that's freely available on the Internet that can play data written in plain ASCII straight through the PC's sound card. For example, the David Sherman Engineering SoundArb V.1.02 (saset-up.exe freeware for Windows 9*x*/NT) is a free PC sound card signal generator program that not only lets you select standard waveforms, but also load and play arbitrary waveforms from a text wave table file with full control over frequency, amplitude, and trigger mode. [2]

The output jack of a typical sound card carries an amplified AC-coupled signal (20 Hz to 20 kHz) capable of directly driving 8-Ω speakers with 2 W of power. The actual output level is uncalibrated and will depend on the settings of the volume lever, which you can access by double-clicking the speaker icon in the Windows tray. The only way to set the amplitude to a known voltage is by observing the waveform on an oscilloscope. Because sound cards are meant to output sound, the volume control usually has a limited number of discrete steps (e.g., 16) that follow a two-part logarithmic curve.

Offset	Length	Contents
12	4 bytes	fmt
16	4 bytes	0x00000010, which is the length of the fmt data (16 bytes)
20	2 bytes	0x0001, which is the data encoding format tag: 1 = PCM
22	2 bytes	<channels>, which defines the number of channels: 1 = mono, 2 = stereo
24	4 bytes	<sample rate>, in samples per second (e.g., 44,100)
28	4 bytes	<bytes/second>, sample rate × block align
32	2 bytes	<block align>, channels × bits/sample/8
34	2 bytes	<bits/sample>, 8 or 16

Table 2—*The format (fmt) chunk of a RIFF file describes the sample rate, sample width, and other important parameters about the way in which the wave file data is encoded.*

DATASTREAM CONVERSION

Matlab has a function, `vco.m`, which simulates the operation of a voltage-controlled oscillator (VCO)—essentially, an FM modulator. The code in Listing 1 shows how easy it is to use this function to generate an FM signal by modulating a carrier (of frequency F_C) with an arbitrary signal contained in vector *x* (sampled at a rate F_S of more than twice F_C, and with an amplitude range of ±1).

You can use the following Matlab command to look at the spectrum of the FM signal that's played through the sound card:

```
specgram(y,512,Fs,kaiser(256,5),220)
```

If you aren't a Matlab user, you can write a program to generate the FM signal from the arbitrary waveform by remembering that an FM signal, *s(t)*, is expressed by:

$$s(t) = A_c \cos\left(2\pi f_c t + 2\pi k_f \int_0^t m(\tau)\partial\tau\right)$$

where $m(\tau)$ is the modulating signal (the arbitrary waveform), f_C is the carrier frequency, A_C is the carrier amplitude, and k_f defines the frequency deviation caused by $m(\tau)$. The instan-

taneous frequency of the signal is larger than the carrier frequency when the signal $m(\tau)$ is positive; it's smaller when $m(\tau)$ is negative.

FINALLY, THE DEMODULATOR

The circuit in Figure 1 is used to demodulate the FM signal from the sound card, which is AC-coupled by C17 and amplitude-limited by IC1D. Then, an NE565C PLL IC demodulates the FM signal. The PLL tracks the incoming carrier signal and internally estimates the signal based on the frequency of its internal VCO set by R2, R4, and C2. The error between the actual carrier frequency and the estimate is the data signal when the PLL is locked.

A suitable FM frequency deviation for this circuit is ±40%, which allows the bandwidth of the arbitrary signal to be reproduced to be approximately 18.5% of the carrier frequency. Table 4 shows the signal reproduction characteristics for some of the standard frequencies used in FM tape recorders—an application that uses the same FM modulation/demodulation schemes.

The loop output of the PLL IC is fed into a unity-gain differential amplifier (IC1C). The common-mode rejection of this amplifier is used to eliminate DC and high-frequency carrier components present at the output of the PLL.

A Maxim MAX280 switched-capacitor filter IC is used to remove residual carrier-frequency signal components from the desired waveform. This IC is a fifth-order, all-pole, low-pass filter with no DC error, making it an excellent choice for processing low-frequency signals. The filter IC uses an external resistor (R9) and

Offset	Length	Contents
36	4 bytes	data
40	4 bytes	<length of the data block>
44	Bytes needed for data	<sample data> For multichannel data, samples are interleaved between channels: sample 0 for channel 0 sample 0 for channel 1 sample 1 for channel 0 sample 1 for channel 1 ... where channel 0 is the left channel and channel 1 is the right channel. The sample data must end on an even byte boundary.

Table 3—*The data chunk of a RIFF file contains the actual signal samples.*

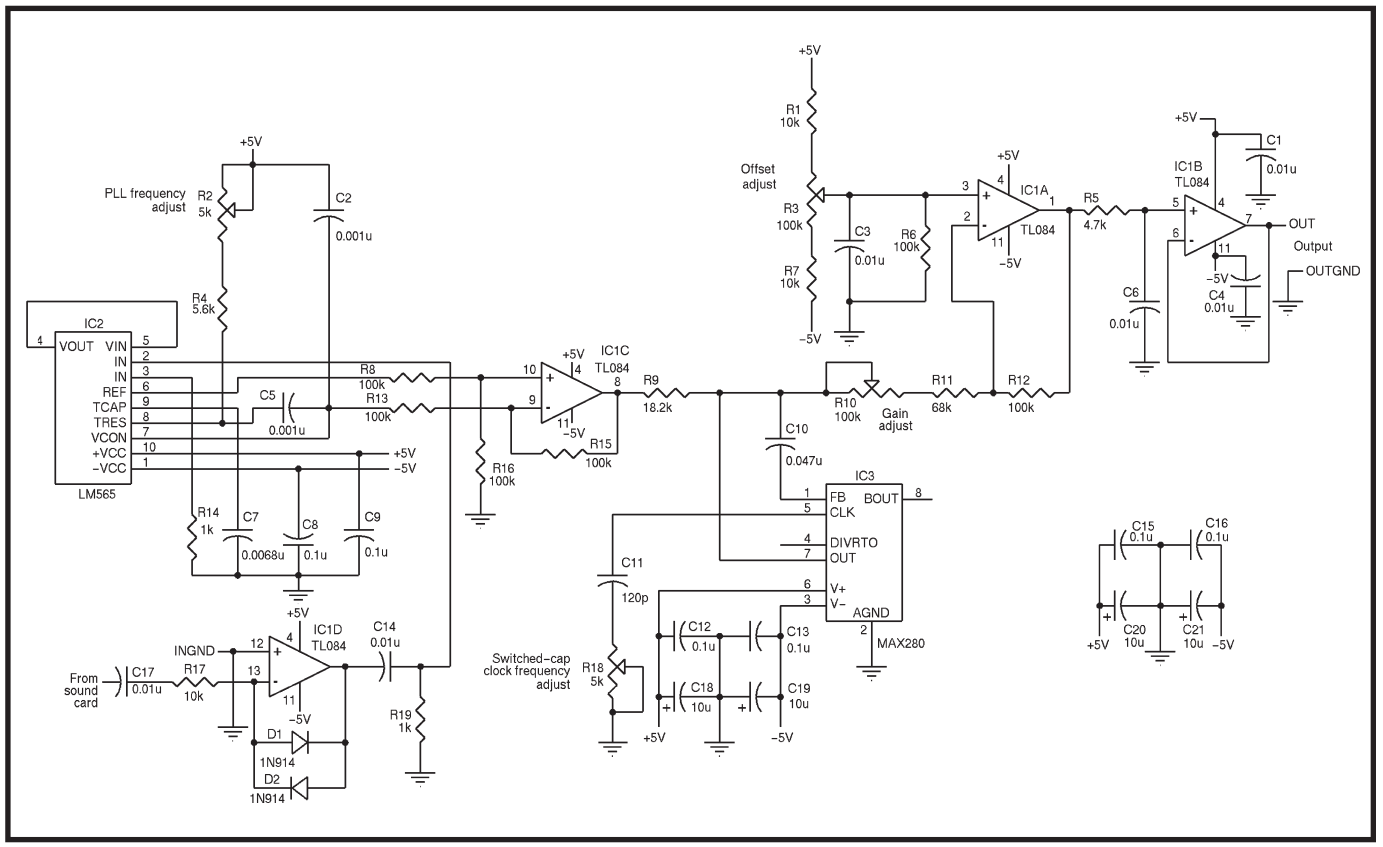
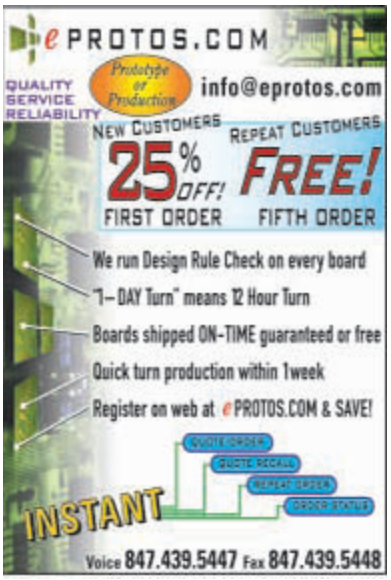


Figure 1—*This PLL-based FM demodulator is used to generate DC-coupled signals from FM modulated signals generated through the PC sound card. IC1D is a limiter for the input signal. IC2 is the PLL. The common-mode rejection of IC1C eliminates DC and high-frequency carrier components present at the output of the PLL. IC3 is a fifth-order, all-pole, low-pass filter with no DC error used to remove residual carrier-frequency signal components from the desired waveform. IC1A adjusts the gain of the circuit and removes any offset introduced by the preceding stages.*


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Listing 1—*The Matlab program uses the* `vco.m` *function to generate an FM signal by modulating a carrier (of frequency F_C) with an arbitrary signal contained in vector* `x` *sampled at a rate F_S.*

```
Fs = 5000;     % Select arbitrary signal sampling frequency in Hz
Fc = 1687;     % Select VCO carrier frequency in Hz
moddev = 40;   % Percent FM frequency deviation
y = vco(x,[1-moddev/100 1+moddev/100]*Fc, Fs);  % VCO simulation
sound(y,Fs)    % Play modulated signal through PC sound card
```

capacitor (C10) to isolate the fourth-order filter implemented within the IC from the DC signal path. The external resistor and capacitor are used as part of the filter's feedback loop, and they also form one pole for the overall filter circuit. The values of these components are chosen such that:

$$f_{cutoff} = \frac{1.62}{2\pi R9 \times C10}$$

where *R9* should be around 20 kΩ.

Now, for the Matlab code in Listing 1, the demodulated signal bandwidth is expected to be:

$$18.5\% \times F_C = 18.5\% \times 1687\,Hz = 312\ Hz$$

which is where the –3-dB cutoff frequency for the low-pass filter should be placed. Selecting the closest standard-value components, R9 = 18.2 kΩ and C10 = 0.047 µF, the –3-dB cutoff will be 301 Hz.

An internal clock that determines the filter's cutoff frequency drives the chip's internal four-pole switched-capacitor filter. For a maximally flat amplitude response, the clock should be 100 times the desired cutoff frequency. The filter has a cutoff frequency ratio of 100:1. The internal oscillator runs at a nominal frequency of 140 kHz that can be modified by connecting an external capacitor (C11) between pin 5 and ground. The clock frequency is given by:

$$f_{CLK} = 140\ kHz\left(\frac{33\ pF}{33\ pF + C11}\right)$$

For the example where the cutoff should be approximately 300 Hz (f_{CLK} = 30 kHz), C11 would be 120 pF. A series resistor (R18) can be added to trim the oscillation frequency. In this case, the new clock frequency is given by:

$$f_{CLK} = \frac{f_{CLK}^{R18=0}}{1-(4 \times R18 \times C11 \times f_{CLK}^{R18=0})}$$

where

$$f_{CLK}^{R18=0}$$

is the oscillator frequency when *R18* is not present (it's obtained through the prior equation).

After filtering, the gain is adjusted through R10, and the offset from the preceding stages is compensated with IC1A by setting R3. Lastly, the RC low-pass filter formed by R5 and C6 removes any switching noise introduced by IC3.

The stability of the PLL circuit depends on the

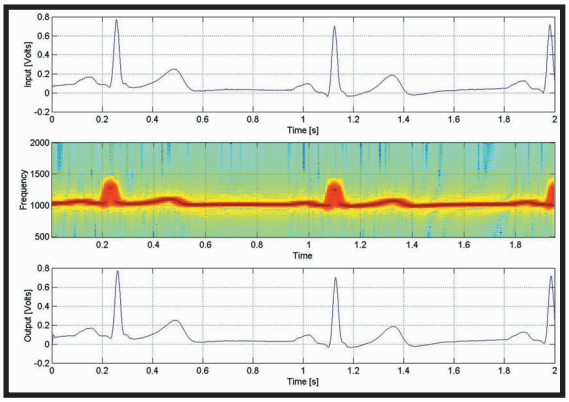


Photo 1—*A real ECG signal that was digitized at a sampling rate of 5 kHz* ***(a)*** *is used to frequency-modulate a 2-kHz carrier using the Matlab* `vco.m` *function* ***(b)****. The output of the PLL-based FM demodulator is shown in* ***(c)****, depicting how the demodulated signal faithfully reproduces the DC offset and low-frequency components of the ECG.*

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1.687	2.362	1.012	DC – 0.312	±1%
3.375	4.725	2.835	DC – 0.625	±1%
6.750	9.450	4.050	DC – 1.250	±1%
13.500	18.900	8.100	DC – 2.500	±1%
27.000	37.800	16.200	DC – 5.000	±1%

Table 4—*Here are the signal characteristics for various standard FM tape recorder frequencies.*

stability of the frequency-setting components. Proper performance requires the use of low-temperature-coefficient components with high tolerance. Resistors should be the precision 1% tolerance type of the RN60D variety. And capacitors should be Mylar, polyester film, or another type that remains stable with age and is not sensitive to temperature variations.

IN CLOSING

Photo 1 demonstrates the performance of the technique. The test signal in Photo 1a is from an electrocardiogram (ECG) that was digitized at a sampling rate of 5 kHz with 12-bit resolution. In Photo 1b, you can see the spectrum of the FM signal. Photo 1c shows how the demodulated signal faithfully reproduces the DC offset and low-frequency components of the ECG.

Because the sound card output is in the audible range, the modulated signal can be transmitted to the demodulator via a voice radio or telephonic link for remote signal generation. To do so, however, the tone frequencies produced by the sound card for a full-scale input must be limited to the band-pass of the communications channel. For a plain telephone line, this range is 400 Hz to 3 kHz, while a commercial FM audio link is specified to cover the 30-Hz to 15-kHz audio bandwidth. Another interesting possibility is to use a small 1:1 audio isolation transformer and a floating power supply to turn the demodulator into an isolated output stage.

Lastly, you should note that the full bandwidth of a single sound card channel could be shared by multiple software modulators occupying separate audio bands to convey various simultaneous low-frequency signals to an array of PLL demodulators. This is exactly what FM telemetry systems do. The U.S. Army's Inter-Range Instrumentation Group (IRIG) of the Range Commanders Council has established a standard, IRIG 106-96, that covers all aspects of frequency modulation (FM) and pulse-code modulation (PCM) telemetry, including transmitters, receivers, and tape recorders. [3] Because of its success as a proven standard and the support from telemetry equipment manufacturers, most commercial data acquisition systems also use the same IRIG standard channels.

The IRIG standard specifies ways of performing frequency division multiplexing (FDM) over a telemetry channel (i.e., how to generate a composite signal consisting of a group of sub-carriers arranged so that their frequencies do not overlap or interfere with each other). Various FM sub-carrier and deviation schemes are available to accommodate different channel needs.

For a consumer-grade sound card, the maximum sampling rate is 44.1 kHz, which imposes an absolute maximum tone frequency limit of around 18 kHz, which ultimately constrains the number of channels that can be simultaneously reproduced with the FM carrier technique. Still, selecting channel bandwidths proportional to their carrier frequencies can accommodate many channels of differing bandwidth.

For example, multiple physiological signals with different bandwidth requirements can be simultaneously generated. A sound card's bandwidth suffices to simultaneously generate a skin conductance signal simulation through an 11-Hz bandwidth channel. A brainwave signal (EEG) can be reproduced through a 45-Hz bandwidth channel, while a 3-lead wideband electrocardiogram (ECG) can be reproduced through three 1-kHz channels.

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Michael Norris is a senior electronics engineer at Impulse Dynamics, where he has developed many cardiac stimulation devices, cardiac contractility sensors, and physiological signal acquisition systems. He can be reached at miken@impulse.co.il.

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MathWorks, Inc.
(248) 596-7920
www.mathworks.com

MAX280
Maxim Integrated Products, Inc.
www.maxim-ic.com

WaveWorks Pro
Pragmatic Instruments, Inc.
(858) 271-6770

FEATURE ARTICLE

Roberto Ferrabone

Choosing Your LCD

Choosing the right LCD and controller can be difficult, especially when their signal names don't match up. But, as Roberto explains, it doesn't have to be a major problem. In this article, he will show you how to pick the appropriate devices for your own applications.

In my part of Italy, there wasn't enough snowfall this year to fill the landscape or skyline. But on one cold morning during the Christmas holiday, a different kind of snow filled my mind.

In many applications, I use graphic displays for building portable and fixed devices. One controller that fits all of the different LCD sizes and interface types, especially the larger ones, is the Seiko SED1330 and its derivatives. The LCD maker usually integrates the controller (e.g., the SED133*x* or another) by soldering it directly onto the LCD board or offers the same LCD without a controller. I prefer the latter version because it seems to be better in terms of electromagnetic compatibility. With the integrated controller, you have to bring the CPU bus through a flat cable to the display. This creates longer bus traces and poorly defined bus timing.

After you've chosen the LCD, the next step is selecting the right controller to generate the interface signals. Here's where the problems begin, because the display that you select often has signal names that differ from those on the controller.

Table 1 shows how the signals match up between the SED133*x* on the left and a typical display (e.g., a Hitachi SP14Q002) on the right.

Now that you're ready to connect your display to the SED133*x* controller, another set of problems is waiting.

The SED133*x* offers a rich set of text modes, giving you the ability to choose between an internal 5 × 7 pixel font and external RAM-based 8 × 8 or 8 × 16 fonts. However, this never matches with the requirements of the customer, who might need the characters to be a bit taller or wider. What if a customer wants to be able to write the contents of the Bible in a single pixel?

At this point, your only choice is to use the graphical mode of the screen, which gives you the ability to build characters and icons in the dimensions that best fit your needs.

GRAPHICAL CHOICE

Choosing the graphic mode was like a spring rain for software people, who immediately began to build an elaborate architecture of data structures, structures of pointers, and so on. After spending some time debugging the initialization routines, I was rewarded with animated icons along with characters of every possible height, width, shadow, and focus. However, I found that if I looked at the screen from certain angles, especially when there was a lot of white on the screen, drawing new items created a strange dot that wandered across the display.

This instigated an exasperating struggle to find a set of initialization parameters that would eliminate the snow. I tried increasing and decreasing the TC/R count to maximize the time that refresh was inactive, but there was always some angle from which the flickering dot would appear.

I consulted the SD133*x* datasheet and tried solutions suggested by the manufacturer. According to the datasheet, display flicker may occur if there is more than one consecutive access that cannot be ignored within a frame. I also learned that the micro could minimize this by either performing these accesses intermittently or continuously checking the status flag (D6) and waiting for it to become

high. All that the factory could suggest was to make updates more and more slowly to avoid the problem.

I slowed all the way down to one access per frame, but this means that if you need to refresh the entire screen, you had better plan to get a cup of coffee (and not an Italian espresso).

The alternative is to actively monitor the busy status of the SED133*x* and make accesses only when it's idle. A driver that implemented this protocol was soon ready for testing, but incredibly, there was still an occasional flicker on the display!

What happened? A simple session with an oscilloscope showed the terrible effects of an interrupt occurring between the status read and the display data write. Essentially, the write cycle would fall well outside the window allowed for interference-free access (see Figure 1).

Digging deeper into one of the numerous datasheets for the chip, I discovered another suggestion that was even more restrictive. You need to wait 5 × 9 Tosc periods before considering the bus free, and you have to complete your access at least 2 × 9 clock periods before the next line starts.

It became clear that it wasn't going to be possible to reconcile the limitations of the controller with the needs of the software, so I decided it was time to build a simplified emulation of the SED1335 in a Xilinx Spartan FPGA that would eliminate its constraints.

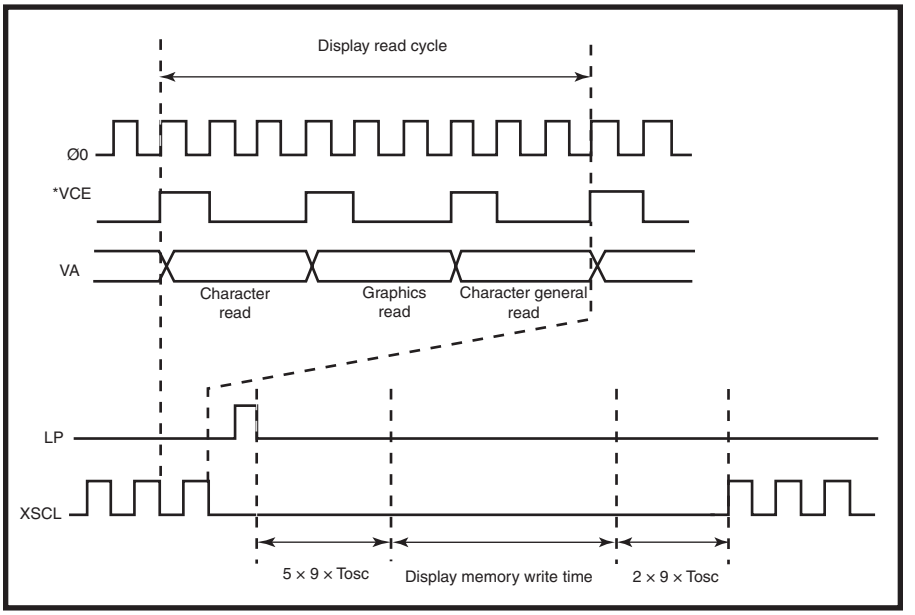


Figure 1—*The SED133x timing keeps the display memory completely busy during the active portion of each delay line. There's only a small window of clock periods ((TC/R – C/R – 7) × 9) for display updates between lines.*

BUILT AT HOME

A look at the SED1335's display refresh timing convinced me that this would not be difficult.

During the active part of the scan, the SED1335 controller generates a continuous series of RAM cycles in the following sequence: character read, graphics read, and character generator read. This doesn't vary, even if you aren't using the character plane and fonts (internal or external); moreover, each read cycle is long compared to modern RAM access times (250 ns) using an 8-MHz controller clock.

The SED1335 applies three clock cycles per memory cycle, using one full clock period as idle time between cycles and two clock periods (250 ns

SED133*x* pin name	SED133*x* function	SP14Q002 pin number	SP14Q002 pin name	SP14Q002 function
XD0–XD3	4-bit X-driver (column drive) data outputs. Connect these outputs to the inputs of the X-driver chips.	1–4	D0–D3	Data display
XSCL	The falling edge of XSCL latches the data on XD0 to XD3 into the input shift registers of the X-drivers. To conserve power, this clock halts between LP and the start of the following display line.	9	CP	Data shift
XECL	The falling edge of XECL triggers the enable chain cascade for the X-drivers. Every sixteenth clock pulse is output to the next X-driver.			
LP	LP latches the signal in the X-driver shift registers into the output data latches. LP is a falling-edge triggered signal, and it pulses once every display line. Connect LP to the Y-driver shift clock on modules.	8	LOAD	Data latch
WF	LCD panel AC drive output. The WF period is selected to be one of two values with the system set command.			
YSCL	The falling edge of YSCL latches the data on YD into the input shift registers of the Y-drivers. YSCL is not used with driver ICs that use LP as the Y-driver shift clock.			
YD	Data pulse output for the Y-drivers. It's active during the last line of each frame and shifted through the Y-drivers one by one (by YSCL) to scan the display's common connections.	6	FRAME	First line marker
YDIS	Power-down output signal. YDIS is high while the display drive outputs are active. YDIS goes low one or two frames after the sleep command is written to the SED1335 series. All Y-driver outputs are forced to an intermediate level (deselecting the display segments) to blank the display. In order to implement power-down operation in the LCD unit, the LCD power drive supplies must also be disabled when the display is disabled by YDIS.	5	Display off	High = on Low = off

Table 1—*When using an external controller, carefully match up the signals between the controller and the selected display (e.g., the Hitachi SP14Q002 shown here).*

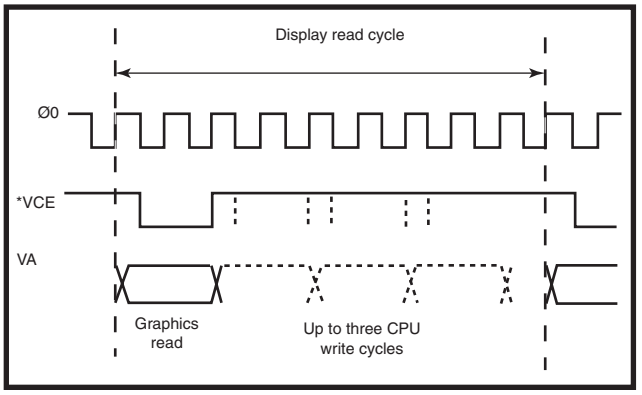


Figure 2—*The FPGA implementation keeps the same basic display cycle timing as the SED133x, but makes only one read access to the display RAM. This leaves time for up to three CPU writes in each cycle.*

at 8 MHz) for the actual memory access time. Three memory cycles fully consume the nine clock cycles allowed for each byte of display refresh.

The emulation controller does only the graphic read cycle, and the timing is also much faster in order to maximize the time available to the microprocessor interface (see Figure 2). The memory cycle is reduced to two clock cycles, with a half clock period of idle time and 1.5 clock periods (187.5 ns at 8 MHz) for the memory access time. This leaves up to six out of nine clocks (67%) of the memory bandwidth, available for interference-free display updates.

Note that the microprocessor cycles shown in Figure 2 aren't real CPU bus cycles; these are internal accesses that are initiated by the microprocessor writing to the controller's command and data registers. The microprocessor can complete those writes at its own pace, and it is only necessary for the controller to buffer the incoming writes and resolve the access as soon as possible. A nine-state counter (0 through 8) controls the refresh state machine. In the active part of the display, the first two states are used to read graphic data to send to the LCD. The controller's microprocessor interface is allowed to start a memory cycle during states 2 through 6. If a cycle were to start in state 7 or 8, it would interfere with the graphics read access of the next refresh cycle. If the microprocessor initiates a write while the refresh controller is in states 7, 8, 0, or 1, the memory cycle must be deferred until state 2. This allows the microprocessor to write to the memory from one to three times for every graphics read cycle, giving high performance without degrading the quality of the display.

MICRO INTERFACE

The FPGA controller emulates the parts of the interface of the SED133*x* controllers that relate to the graphics mode of operation. Figure 3 shows a diagram of the FPGA implementation. You may download the schematic from the *Circuit Cellar* ftp site.

Although the SED controllers support both Intel-style and Motorola-style buses, I chose to emulate only the Intel mode of operation. The interface signals are an 8-bit data bus, read and write signals, one bit of address (selects between command and data registers), and a chip select signal.

The Intel interface operates such that when a Write command arrives (the chip select is low, and then the write signal become active), a latch holds the state of the address bit A0.

On the rising edge of two internal signals (ISDATA or ISCOMMAND), two other signals are generated: NEWDATA and NEWCOMMAND. The latter of the two activates the command just stored in the command register (ACOMMAND bus). This value is compared against specific commands that the FPGA recognizes; it also resets the counter that keeps track of the next set of parameter data when there are multiple bytes. NEWDATA stores a parameter byte in the appropriate register and advances the counter.

With regard to electrical timing, the proposed FPGA emulation is certainly more attractive than the original SED133*x* (see Table 2 and Listing 1). The SED133*x* requires a data setup time of 120 ns, which is much more than the 10 to 20 ns required by the FPGA implementation (depending on the FPGA speed grade you select). Although the hold time requirement of 10.799 ns is a bit longer than the SED controller's specification of 5 ns, it shouldn't cause any problems with most microprocessors.

If your application is more time-sensitive, the use of a global clock buffer (BUFG) is the correct way to address this problem. Another way to further improve the timing performance of the system is to use an 8-bit data-transparent latch (ILD8) controlled by the inverted NWR signal. Use the output of this as input to the data and command registers.

Because display refresh timing is not particularly critical, another benefit of the FPGA implementation is the ability to eliminate an external clock altogether. The internal FPGA

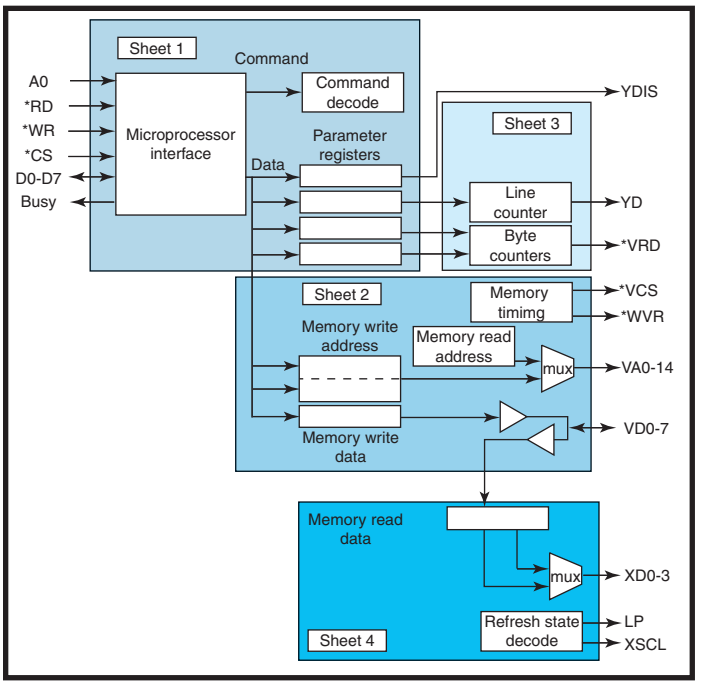
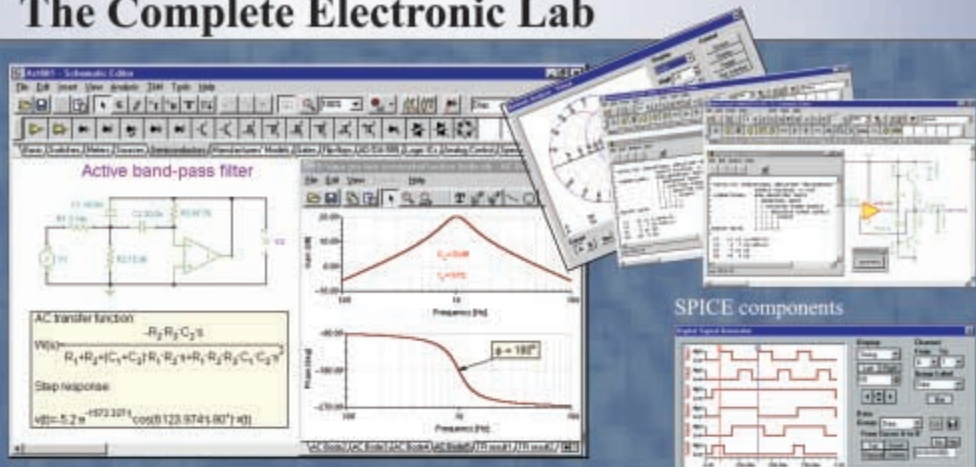


Figure 3—*The FPGA implements a subset of the SED133x logic. Sheet 1 contains the microprocessor interface and emulation registers. Sheet 2 contains the video memory interface, and sheets 3 and 4 contain the LCD interface.*

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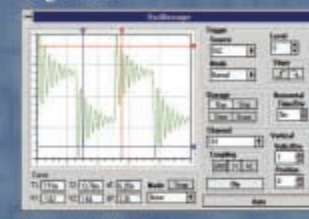
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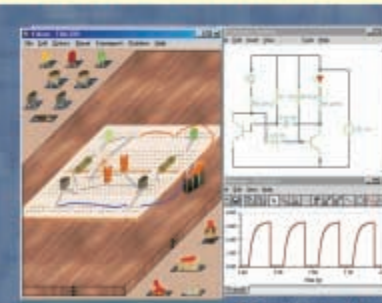
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clock can be used, making the implementation even more EMC compliant.

COMMAND SET

The FPGA emulation implements just four of the SED133*x* commands: system set (with 8 bytes of data), display on/off control, set cursor address, and memory write. Although the system set command only implements three of the parameter registers, they're located in the same positions as on the SED133*x* in order to maintain software compatibility between the two implementations. The parameters supported are C/R, TC/R, and LF. The C/R parameter sets the address range covered by one display line; in other words, the number of bytes for one display line. Similarly, the TC/R parameter sets the total time for a line (including retrace), and it must contain a minimum value of C/R + 4.

The Set Cursor Address command stores the address for the next display update in a counter, which increments for every byte written by the Memory Write command. This effectively moves the cursor to the right as bytes are written. Clearly, this is simpler than the four possibilities offered by the SED controller (up, down, left and right), but I felt that the computational capabilities of the microcontroller linked to the display controller are more than sufficient to make up for this. Today's microprocessors are more powerful than the ones available when the SED133*x* was first designed.

Listing 1—*This excerpt from the FPGA timing report shows the good news about the bus interface.*

```
Setup/Hold to clock $Net00004_
---------------+------------+------------+
               |  Setup to  |  Hold to   |
Source Pad     | clk (edge) | clk (edge) |
---------------+------------+------------+
$Net00011_     |     1.641(R)|   10.799(R)|
$Net00001_     |     4.590(R)|   10.549(R)|
$Net00005_     |     6.486(R)|    8.653(R)|
$Net00021_     |     0.327(R)|    2.903(R)|
$Net00023_     |     0.335(R)|    2.895(R)|
$Net00024_     |    -3.641(R)|    8.223(R)|
$Net00006_     |    -4.100(R)|    7.936(R)|
$Net00007_     |     2.523(R)|    8.270(R)|
$Net00008_     |     0.672(R)|    6.785(R)|
$Net00009_     |    -3.263(R)|    5.981(R)|
---------------+------------+------------+
```

BOARD-LEVEL SCHEMATIC

The PCB schematic is simple (see Figure 4). The Xilinx Spartan XCS10 FPGA is in an 84-pin package. The signals to the Hitachi SP14Q002 LCD are buffered by a 74HC244 to provide greater drive for potentially long cables. A Maxim MAX629 provides the negative V_{EE} supply for the LCD.

A 10-kΩ trimmer is used to set the

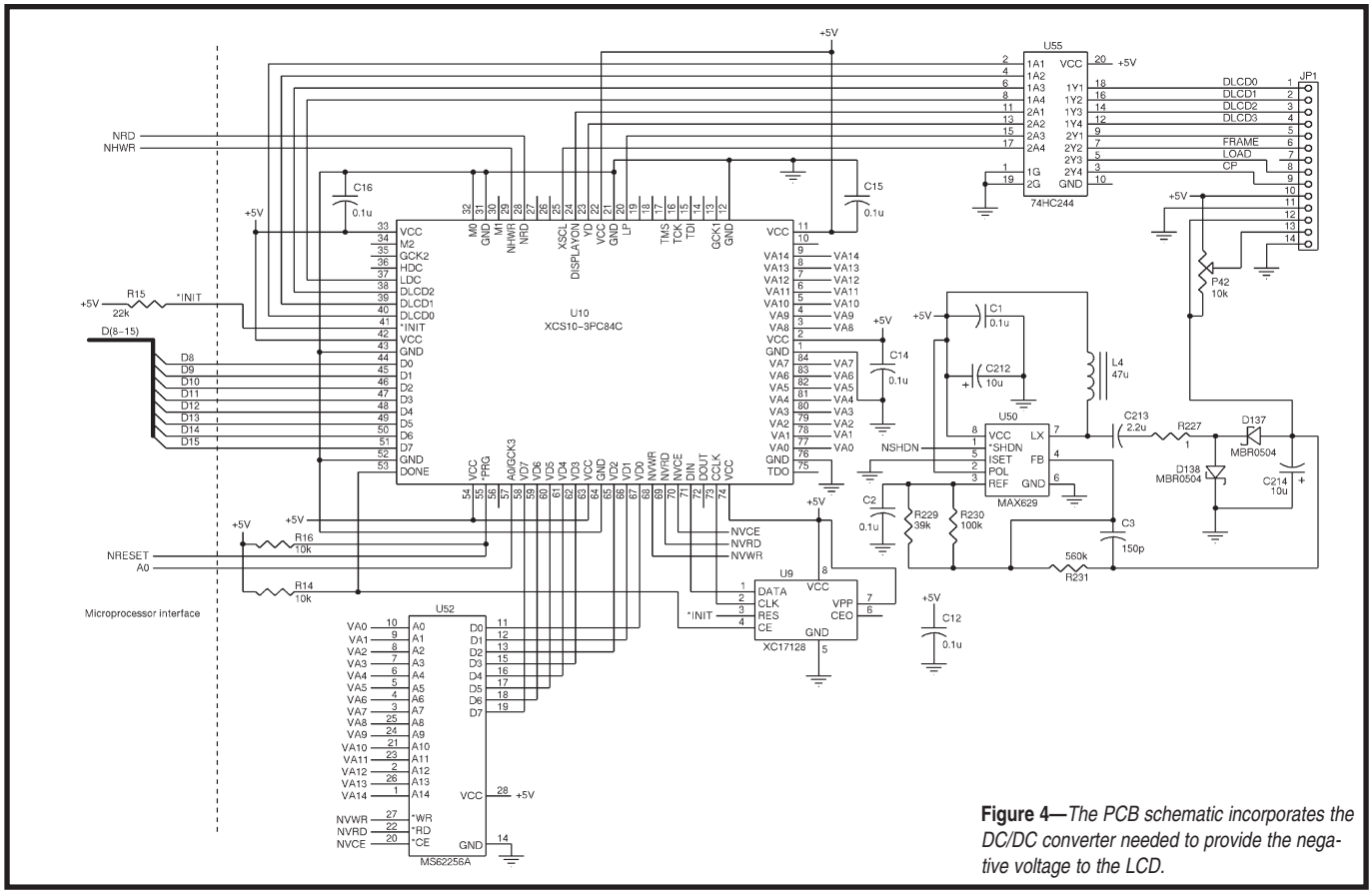


Figure 4—*The PCB schematic incorporates the DC/DC converter needed to provide the negative voltage to the LCD.*

Description	Symbol	Speed grade –4		Speed grade –3	
		Minimum	Maximum	Minimum	Maximum
Setup times (TTL inputs)					
Clock enable (EC) to clock (IK), no delay	T_{ECIK}	1.6	N/A	2.1	N/A
Pad to clock (IK), no delay	T_{PICK}	1.5	N/A	2.0	N/A
Hold times					
Clock enable (EC) to clock (IK), no delay	T_{IKEC}	0.0	N/A	0.9	N/A
All other hold times	T_{ECIK}	0.0	N/A	0.0	N/A

Table 2—*The raw timing specifications of the FPGA promise high performance.*

display contrast. If the microprocessor has a PWM or D/A output, it can be filtered and combined with the trimmer voltage in order to provide a software-controlled contrast adjustment. The PWM could also be implemented in a spare section of the FPGA; after all, 50% of the XCS10 is still available. Other application-specific features can be incorporated into the FPGA as well.

If you need more FPGA space and you know up front the initialization parameters for your LCD, you can hard-wire the values and eliminate most of the logic associated with the System Set command and its parameter registers. This will also simplify the software driver.

Another interesting possibility is to mount the LCD upside-down. This can be accomplished by subtracting every address setting from 9599 (320 × 240 – 1), swapping each bit in a byte (reversing the bus order reading from the video memory, using RAMBUS[0:7] instead of RAMBUS[7:0]) and using a down counter instead of the up counter for the write address register.

Roberto Ferrabone earned a BSEE from the Politecnico di Torino in Turin, Italy. He co-owns Siro Automazione Srl. You may reach him at roberto.ferrabone@sirioautomazione.it.

PROJECT FILES

To download the code, go to ftp.circuitcellar.com/pub/Circuit_Cellar/ 2002/147/.

SOURCES

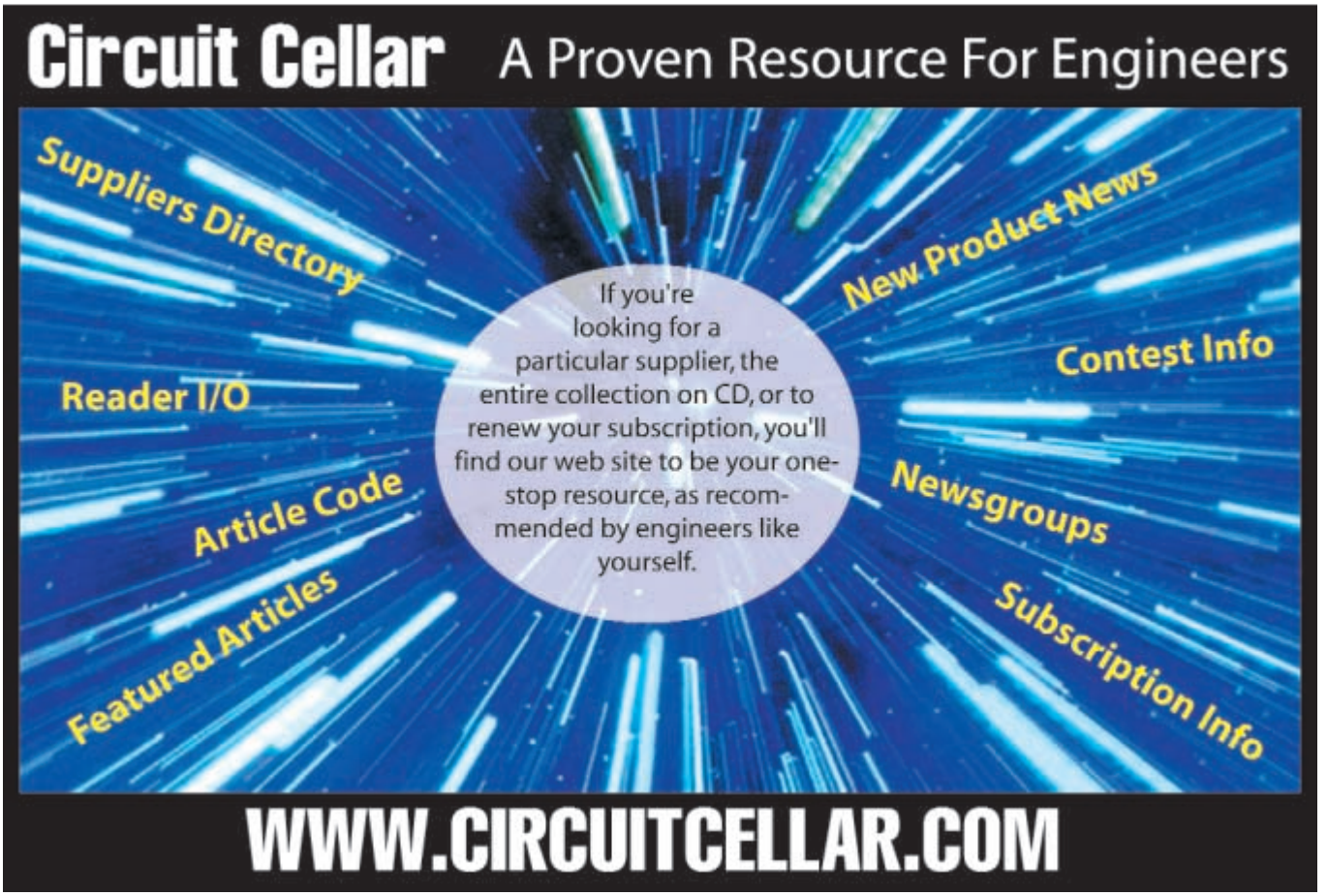
SP14Q002 display
Hitachi America, Ltd.
www.hitachi.com

MAX629
Maxim Integrated Products, Inc.
www.maxim-ic.com

74HC244 Octal buffer/line driver
Philips Semiconductor
www.semiconductor-philips.com

SED133*x* LCD controller
Seiko Instruments USA, Inc.
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Spartan FPGAs
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www.xilinx.com



Ed Nisley

Audio Transformation

If you've ever had a problem connecting your PCs to a sound system, and chances are you have, then listen up. In this article, Ed shows us how he took the mystery out of audio transformation by building an isolated mixer for PC sound card audio. So, get ready to connect.

Surely, you've encountered one of these problems: you have more audio sources than your PC has line-in jacks, or you'd like to connect all of your PCs to a sound system with real speakers. In either case, you cannot simply solder the offending outputs together and stuff them into one input jack, although I've seen that done by folks who should have known better.

You need what's called an audio mixer, which is a device that combines two or more audio input signals into a single output. The word "mix" has two different meanings in the analog domain, however. When you mix audio signals, their amplitudes add up to produce a linearly related output signal. When you mix RF signals, their amplitudes multiply in a decidedly nonlinear and highly useful manner. We'll use linear mixing now and discuss nonlinear mixing in a later column.

As you saw in my August column (*Circuit Cellar* 145), audio signals have large dynamic ranges, low average levels, and a distressing propensity for noise. Anyone who's ever tried to wire an audio system has uncovered the clearly audible hum that simply won't go away. An isolating transformer can pass the audio signal while eliminating the galvanic connection between equipment, thus breaking the ground loop that produces the noise.

Transformers in general, and signal transformers in particular, seem to be a mystery to many engineers. Let's take a look at them with a straightforward application: an isolated mixer for PC sound card audio.

TRANSFORMER 101

Nowadays, transformers are used only when no feasible alternatives exist. Those hulking iron lumps in old electronic gear have largely given way to fiercely complex chips that simply wouldn't work if you built them from discrete parts. Apart from wall warts and Ethernet jacks, transformers are hard to find these days.

Contrary to popular belief, though, you don't need many turns of wire or a metallic core to form a transformer. All it takes is one wire, called the primary, and another, called the secondary, in reasonable proximity to each other. Passing an alternating (or at least changing) current through the primary wire creates a magnetic field that transfers energy to the secondary wire. That's all there is to it.

Everything else is in the nature of fine-tuning: multiple turns of wire increase the coupling, a metallic core concentrates the field, and specialized materials tailor the transformer's characteristics for specific applications. You can make it as complex as you like, which can be very complex indeed.

A fundamental understanding of transformer action requires getting up close and personal with folks named

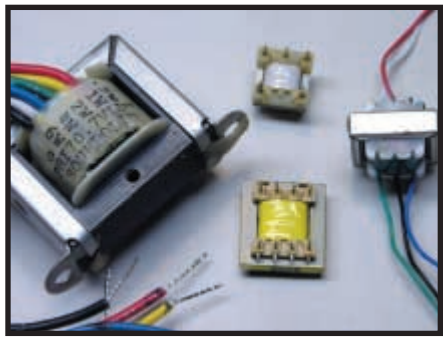


Photo 1—*A 6-W audio line transformer dwarfs telephone and 8-Ω:1-kΩ output-matching transformers. Note that a larger core volume implies a higher power handling capability.*

Ampere, Faraday, Biot, Savart, Lenz, and Maxwell. For the purpose of this article, however, some simple assumptions and approximations will suffice.

Dividing the number of turns in the secondary winding by the number of turns in the primary winding will give you the turns ratio of a transformer. Usually expressed in primary:secondary form (e.g., 1:1, 2:3, or something similar), the turns ratio is a transformer's single most important parameter.

If you assume the primary winding transfers energy to the secondary winding with 100% efficiency, which is actually a pretty good assumption, and that the transformer doesn't really care which coil you call the primary, then most of the useful transformer formulas fall out almost immediately.

Magnetic coupling depends, reasonably enough, on both the AC current flowing in the winding and the number of turns in the field, which is known as ampere-turns. For example, 1 mA in 100 turns generates the same field as 10 mA in 10 turns, or 100 µA in 1000 turns. Thus, a given primary current produces a secondary current scaled by the turns ratio:

$$i_s = i_p \times \frac{n_p}{n_s} \qquad [1]$$

You may have seen transformers with a single-turn secondary used in spot-welding applications that use 50 kA at a fraction of 1 V. In the opposite direction, a heavy single-turn primary with a multiple-turn secondary appears in current-sampling applications such as feedback control of DC-DC converter power supplies.

Knowing the input (and output) power and the output current gives you the output voltage:

$$v_s = v_p \times \frac{n_s}{n_p} \qquad [2]$$

Note of the order of the subscripts in the turns ratio part of Equations 1 and 2. The secondary current decreases and the secondary voltage increases with the number of secondary turns.

An exaggerated example of voltage step-up appears in neon-sign transformers that produce 15-kV voltages at a few milliamps, and in automotive ignition coils that fire spark plugs from a 12-V source.

Because those two relations apply at the same time, you can figure out the impedance relationship across the transformer with:

$$\frac{v_s}{i_s} = \frac{v_p}{i_p} \times \left(\frac{n_p}{n_s}\right)^2 \qquad [3]$$

Despite a common notion, a transformer does not have an inherent impedance of its own, at least to a first order approximation. It does, however, enforce a relation between the primary and secondary windings that can be satisfied by specific external impedances related by the square of the turns ratio.

Thus, neither winding of an 8-Ω to 1-kΩ impedance-matching transformer measures what you might expect, and no parameter of a 600-Ω isolation transformer works out anywhere near 600 Ω. DC resistance measurements reveal only winding resistances that bear no relation to the AC impedances.

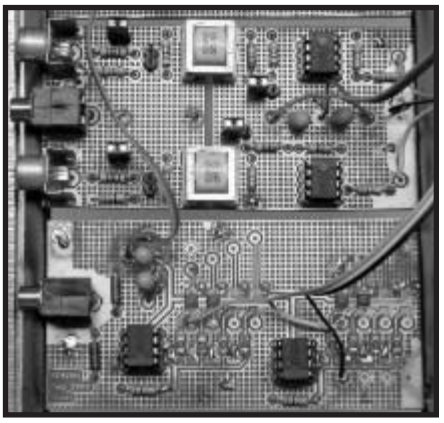


Photo 2—*An input board's audio transformers link signals across the separated ground planes, shown at the top of this photo. The mixer board at the bottom had only two pairs of analog switches installed for testing.*

Not surprisingly, however, even though transformers are optimized for one application, they can be transplanted into other circuits. Just by looking at Photo 1, you can tell that a small audio transformer won't work for AC power, nor should you use a wall wart for audio. You can, however, use a nominal 600-Ω telephone isolation transformer in an audio circuit with similar impedances.

With all of that in mind, let's see how it works out in practice.

AUDIO INPUTS

I built an audio mixer that combines PC audio outputs for my outboard sound system. As Photo 2 shows, an input board handles one stereo signal from a single 3.5-mm stereo plug or two RCA-style plugs, while the lower board does the audio switching and mixing. The complete system has four input boards (one more than I need!), one mixer board, and a power-supply board.

Figures 1 and 2 show the right channel of the input and mixer boards, respectively, with the missing left channel looking just the same. The power supply board, which I don't have room to discuss here, holds a straightforward linear

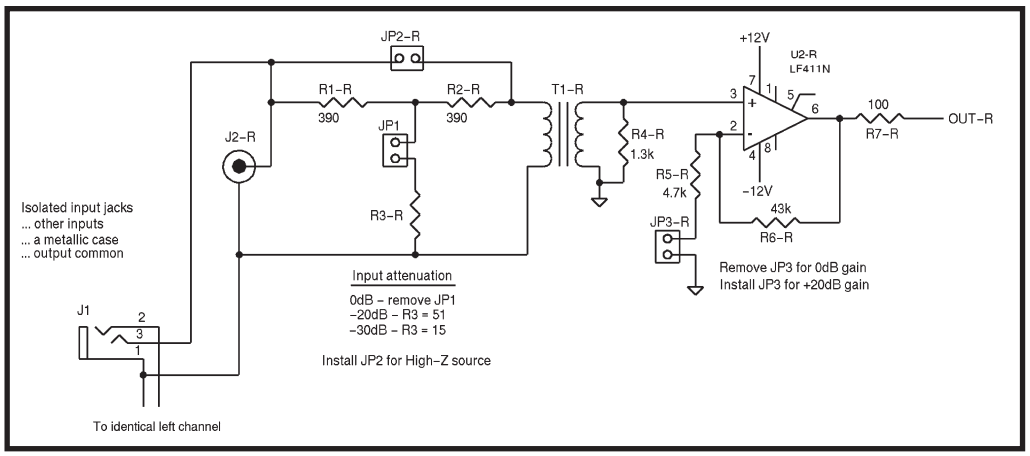


Figure 1—*Input can come through either a 3.5-mm jack or two RCA jacks. The input common connection must be isolated from all other circuit commons to avoid ground loops and their resultant noise. The jumpers and resistors allow many different input impedances, but remain fixed after you find the proper configuration for your source.*

supply producing ±12 V and 5 V from a center-tapped 22-VAC wall wart.

My usual volume settings produce a 75-mV_P signal into the external amplifier's Line-In jack. Shoving the PC Volume Control sliders to the top boosts that to 1.5 V_P, which is a 26-dB increase and louder than even my ears can tolerate for long periods of time. I used that range to determine what the mixer had to handle; your PC should be similar, but measure before building.

Because every input and output gizmo already had volume adjustments, I needed a unity gain device that simply added the signals together. Thus, unlike commercial sound mixers, this one doesn't have adjustable volume or tone controls, just an analog switch to mute each input signal.

Even low-level sound has a high crest factor, so the common 5-V single-supply op-amps don't have the input or output range required for peak signals. In my parts box, I had a stock of LF411 op-amps, which are decent performers with a moderate input noise spec. Given the audio quality going into the mixer, though, they're adequate.

Although I didn't need it in my application, Figure 1 includes a resistive attenuator to cut high-level audio down to size. You can pick the resistors to suit your situation; I simply installed JP2 to pass the signal straight through to the transformer.

I used a pair of 600-Ω 1:1 audio transformers to isolate the input signal's common connection from the mixer circuitry. The transformers, originally designed for a modem, are being used outside of their original specifications, but their frequency response turned out to be surprisingly good.

The output impedance of my various PC Line-Out and Speaker-Out amplifiers lies in the 3- to 5-Ω range, so the input board looks like a high impedance to the PC. The secondary side sees a low impedance, effectively in parallel with the 1.3-kΩ resistor.

Why not use an 8-Ω to 1-kΩ matching transformer? That implies a turns ratio of 1:11, which would step up my usual 75-mV_P input signal to 800 mV_P and the 1.5-V_P maximum to 16 V_P. Can you see why even transistorized audio amplifiers use high supply voltages? I decided to use 1:1 transformers.

My cheerful "ideal transformer" assumption breaks down at low frequencies where the slowly varying magnetic field cannot induce enough secondary current to maintain the transformer action. As the frequency decreases, the primary side sees an increasing load that eventually leads to severe distortion.

The cure involves either a larger core that can carry more magnetic flux without saturating, or a lower signal level to fit the available flux limit. The low-frequency limit at 75 mV_P is about 5 Hz; at 1.5 V_P it's 50 Hz, which is good enough for this application. The original modem application handled 1-V phone line signals with a low-frequency spec of about 300 Hz.

At sufficiently high frequencies, a transformer's intra- and inter-winding capacitances affect its response. That isn't a problem in this application, because the circuit's response is flat to about 100 kHz. I should probably roll off the op-amps well before that!

AUDIO MIXING

Figure 2 shows you that audio mixing involves nothing more complex than adding all of the signals together with an op-amp. That's something of a letdown, no?

The advantage of an inverting op-amp adder lies in the fact that its negative feedback holds the summing node, the point where all of the input signals combine at 0 V. This ensures that the input signals cannot creep back out through their neighbors and cause problems upstream. The op-amps on each input board prevent that situation in this circuit, but it's something to consider for more complex mixers.

Mixers with numerous input channels must have summing amplifiers that can drive enough current through the feedback resistor to handle the maximum input current through all of the channels. A 32-channel mixer with 1-kΩ input resistors (for lower noise) and a 1-V_P input level could have up to 32 mA flowing into the summing node, which would pose a major problem for any of the common op-amps.

Of course, the input currents

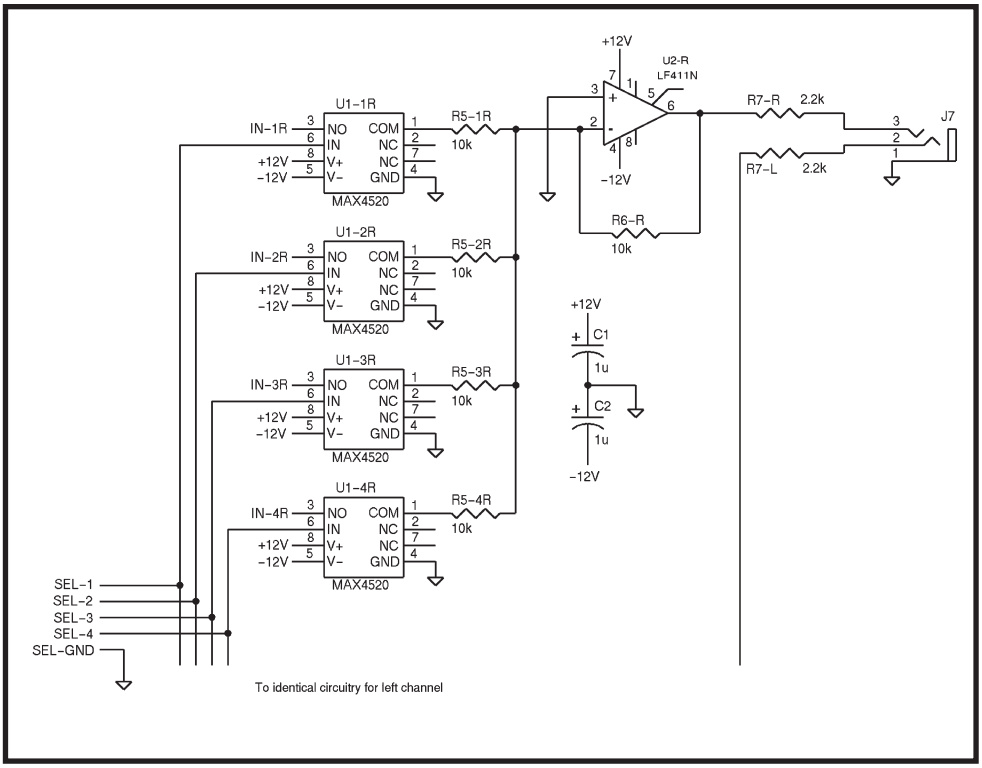


Figure 2—*The right channel of the audio mixer combines signals from up to four input boards. The LF411 op-amp adds the input signals and must have headroom of at least a factor of four (12 dB) over the maximum input signal.*

would almost never add up that way because they're uncorrelated. You must, however, ensure that the summing amplifier can handle whatever you define to be the maximum current. That's another way of saying that the output voltage is the sum of the input voltages. If you run the mixed audio into an ADC, you must allow for enough headroom to handle those additive peaks. Digital clipping sounds more annoying than analog clipping, so you may wind up feeding only 13 bits of input signal voltage into your fancy 16-bit ADC to allow a mere 18 dB of headroom.

The MAX4520 analog switches pass rail-to-rail voltages under the control of a TTL logic signal. They are normally open, so a high logic terminal mutes the audio. You can drive these from a simple mechanical switch or, as you'll see in my next column, from something a bit more complex.

A larger mixer would use SPDT switches to short the inputs to ground and eliminate their input noise. If the inputs are capacitively coupled, you must also hold their DC level at ground to eliminate a nasty pop when you un-mute the inputs.

Audio purists will horripilate when they discover that this mixer inverts the incoming signal phase. If it's any consolation, not all sound cards produce phase-correct outputs, nor are all the outputs necessarily of the same phase. Adding a unity-gain inverting buffer to the mixer board will let you drive a low-impedance device directly from the mixer, but this certainly isn't intended as a speaker amplifier!

CONTACT RELEASE

You can also use this mixer on the other side of the PC audio chain to combine external inputs for the PC's Line-In jack. Although you might consider building the input and output mixers in a single cabinet, you'll be connecting the PC's common to the audio amp's common through the mixer power supply. Investigating this is worthwhile, but don't bend any sheet metal until you verify it!

My tastes in PC audio seem to be fairly limited by contemporary standards, particularly because I don't listen to anything that requires more than stereo sound. Also, even though I can report the frequency response of these circuits, I can't tell you how they sound because two years ago a (biological) virus rolled off my ears by about 25 dB above 2 kHz. Although I don't need hearing aids, my graphic equalizer looks like an old dot-bomb financial chart: two rows of LEDs rising dramatically to the right.

Ed Nisley, PE, is an electrical engineer and a ham radio geek (call sign KE4ZNU). You may contact him at ed.nisley@ieee.or.

PROJECT FILES

To download the schematics and board layouts, go to ftp.circuitcellar.com/pub/Circuit_Cellar/2002/147/.

RESOURCES

Audio isolation transformers
www.jeffrowland.com/tectalk2.htm

Electrical Engineering course notes
Brigham Young University
maxwell.byu.edu/~spencerr/websumm122/web.html

Department of Electronics
Carlton University
www.doe.carleton.ca/~gauthier/97315/labs/97315_lab_03.pdf

Jensen Transformers, Inc.
www.jensen-transformers.com/apps_wp.html

Midcom, Inc.
www.midcom-inc.com/pdf/TN69.pdf

SoundCraft mixer design
Shure, Inc.
www.dself.demon.co.uk/ampins/mixerdes.htm

SOURCES

MAX4520 Analog switch
Maxim Integrated Products, Inc.
(408) 737-7600
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Transformer testing tutorial
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Build an Ethernet Controller

Fred first introduced us to the STK500 starter kit. Now he's back with the newest tool in his Atmel toolbox, the STK501. In this project, he combines the STK501 daughterboard with the STK500 and ASIX Ax88796 to build a 10/100-Mbps Ethernet controller.

As microcontrollers and their supporting parts move from the classic DIP and leaded packages to the realm of SMT, the tools that support them must also make that migration. Proof in point is this month's subject matter.

The Atmel ATmega128 MCU can be had only in a 64-pin TQFP configuration. I was drawn to this part by its high I/O pin count, speed, and large amounts of internal SRAM and program flash memory. To experiment with the ATmega128, I had to come up with a way to get at its power without having to solder one down every time I changed applications.

After some thought, I came up with the package you can see in Photo 1. My aim was to use a standard and commonly available through-hole IC socket that could carry the ATmega128 and a PCB that would extend the ATmega128's pins out to larger hard points. The 64-pin IC socket that supports the ATmega128/PCB duo is the same one that carries the venerable 68000 series of micros.

Because I'm from the South, I spend a lot of time on the interstate highway system traveling between Florida and Tennessee. Of course, when you think of an interstate you think of trucks and trailers. The resulting PCB and ATmega128 perched atop the 64-pin IC socket reminded me of a big old flatbed tractor-trailer rolling down the highway. So, the contraption you see in Photo 1 is dubbed "Flatbed." The Flatbed lash-up works well, and I have an eight-lane Pinewood Derby race timer running with the ATmega128/carrier board/64-pin IC socket combination on-line out there in Boy Scout land to prove it.

Although Flatbed serves its purpose well, there are situations when the standard-voltage or commercial-temperature ATmega128 isn't suitable for the environment the microcontroller is going to reside in. Therefore, you have to build a fleet of Flatbeds with each little truck carrying a low-power ATmega128L-8AC or industrial temperature-rated ATmega128-16AI.

ATMEL'S STK501

To avoid having to put together a fleet of Flatbeds, Atmel offers the STK501, which is an add-on product for the STK500 AVR development system. As you can see in Photo 2, the STK501 is a daughterboard that couples to the original STK500 via the expansion headers. A TQFP ZIF socket, which is a mechanical marvel in its own right, takes all of the pain out of switching between the various types of ATMega128 devices. The ATmega128 TQFP ZIF socket is spring-loaded, and it has fingers for each pin that move out of the way to allow the ATmega128 to be inserted and removed.

The STK501 is not just a home for an ATmega128. The ATmega128 has three additional I/O ports (i.e., E, F, and G), and the STK501 pins them out. There's also an additional serial port that must be accommodated; the STK501 pins it out as well. For convenience, the STK501 includes a MAX3232E RS-232 converter IC and nine-pin shell connector that are tied directly to the extra ATmega128 serial port.

The ATmega128 has the ability to use a 32.768-kHz crystal that can be tied across the TOSC pin set. A slide switch on the STK501 switches the on-board 32.768-kHz crystal in and out of this circuit arrangement.

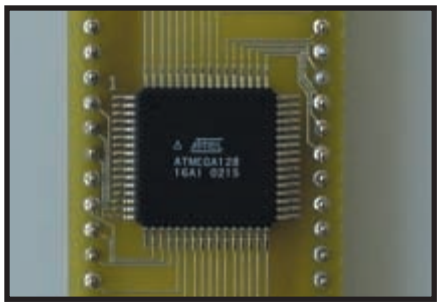


Photo 1—*This is a handy 64-pin IC socket package because you can throw it in a socket and wire wrap or solder it into your project.*

Other features of the STK501 include solder pads for an additional ATmega128 test socket and external SRAM or flash memory. A 6-pin connection is provided to allow a programming cable to be fitted between the STK500 and STK501 ISP programming headers. For JTAG ICE users, the STK501 has a JTAG pin set that mates perfectly with the Atmel JTAG ICE header. Take a look at Photo 3 to see the STK500/STK501 configuration I used for this project.

DRIVING THE TOOL SET

The STK500, STK501, and JTAG ICE all are designed to be driven using hooks in Atmel's AVR Studio. After connecting the STK500/STK501 hardware to my PC's serial port, I downloaded the latest version of AVR Studio from Atmel's web site. After discovering the STK5*xx* hardware, AVR Studio requested that I update the STK500's firmware to enable the enhancements offered by the new version of software. Likewise, AVR Studio performed a similar upgrade to the JTAG ICE firmware.

I'm in the process of evaluating a new Ethernet IC from ASIX. The part I'm looking at is the AX88796 three-in-one Local Bus Fast Ethernet Controller. I will need a minimum of three of the ATmega128's I/O ports to provide address, data, and control signals for the AX88796. The port set included with the STK500 becomes an extension of the ATmega128 port set when the STK501 daughterboard is attached. This gives you I/O ports A, B, C, and D on the STK500, and I/O ports E, F, and G on the STK501. Each port is pinned out identically (i.e., pin 1 of the I/O port header is bit 0, pin 2 is bit 1, and so forth). This consistent pinout allows for the use of simple 10-pin female-to-female ribbon cables as the I/O signal carriers between the STK boards and between the STK boards and external hardware under development.

To complement the services provided by AVR Studio, I will be using the ImageCraft ICCAVR Professional C compiler to produce the firmware for the new Ethernet IC. Because I will be porting code in the Ethernet application, I don't plan to employ the services of the JTAG ICE unless things get really sticky. I'll debug using the second serial port of the ATmega128L running at 57.6 Kbps. The pins for the primary serial port will be used for ISP (in-system programming). I've already written a module that will allow me to use `printf` statements aimed at the secondary serial port. According to the AX88796 datasheet, the AX88796 is compatible with the NE2000 register set, which means I can use most of the same code that makes the RTL8019AS-based Packet Whacker hum. [1]

OK, it looks like I now have all of the necessary AVR tools assembled on the bench to begin working with the AX88796. The next step in the process is to gain easy access to the 128 pins that hang off the AX88796 LQFP package.

DEVELOPMENT BOARD

The AX88796 development board is designed to be easily interfaced with the Atmel STK500 and STK501 AVR development boards. All of the AX88796 development board's address, data, and control lines are pinned out to 10-pin male headers. The pinout of the AX88796 development board headers matches the header pinout pattern of the STK boards. In addition to providing a means of easy access to digital signals on the development boards, each male header includes pins that transport power and ground as well. Pin 9 is ground; pin 10 is VTG (V Target).

The AX88796 is a 3.3-V part with 5-V tolerant I/O. Therefore, a couple of things must happen on the STK500/STK501 end to accommodate this. First, the STK500 AVR target voltage (VTG) must be set for 3.3 VDC in AVR Studio. Second, the standard ATmega128-16AC must be replaced by the ATmega128L-8AC because the ATmega128-16's operating voltage range is 4.5 to 5.5 VDC. The L version of the ATmega128 extends the voltage range down to a 2.7-VDC minimum.

Another trade-off for moving to the L version of the ATmega128 is that the maximum clock speed decreases from 16 to 8 MHz. Neither the need for the L version of the ATmega128, the 3.3-VDC operating voltage, nor the microcontroller speed is a showstopper with the STK500/STK501 tool set. Even at 8 MHz, the ATmega128L is speedy, and the 8-MHz speed limit is more than fast enough for this application. In fact, I'll use a 7.3728-MHz crystal to clock the ATmega128L. That's as close to 8 MHz as I can get and still clock the data rate generator accurately.

Obtaining the 3.3 VDC for the AX88796 is as simple as a mouse click inside AVR Studio. The spring-loaded ZIF allows the ATmega128 to be replaced by an ATmega128L in seconds.

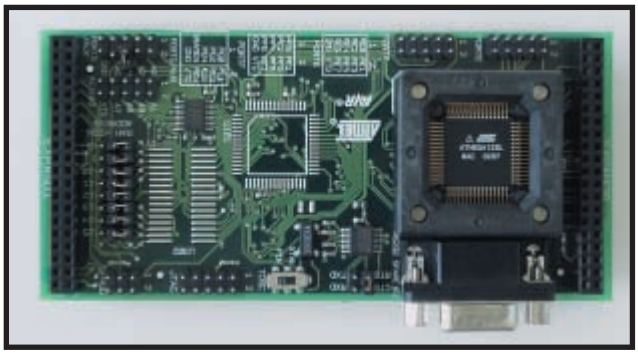


Photo 2—*The addition of the STK501 allows the STK500 to support all of the Atmel 8-bit microcontrollers with a single development board.*

As you can see in Photo 4, the AX88796 development board has four 10-pin male headers. One header pins out five of the AX88796's 10 address lines. The lower five address lines are used to access the AX88796's internal NE2000 (MAC) register set. The remaining address lines are hardwired to a base address of 0x200, which is the default base address for the AX88796. Using the

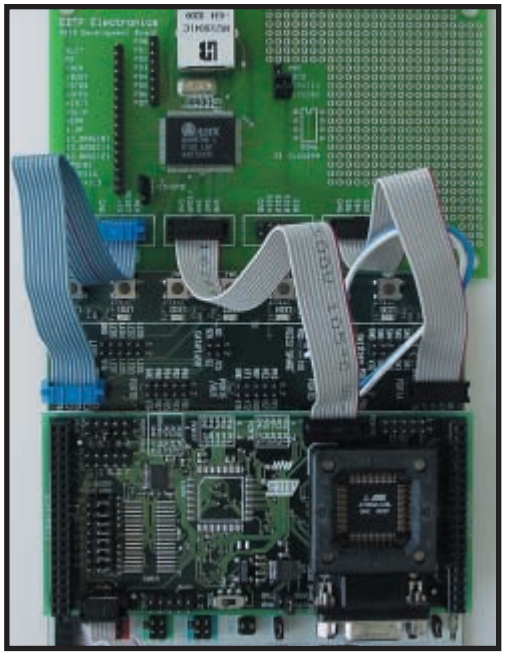


Photo 3—*The standardization of the 10-pin headers on the STK500 and STK501 made for a clean I/O connection to the AX88796 development board.*

default address allows the three base address pins (i.e., I/O_BASE[0], I/O_BASE[1], and I/O_BASE[2]) of the AX88796 to be left unconnected and follow their internal pull-up and pull-down circuitry. The address header also pins out the *IORD and *IOWR I/O control signals and the interrupt request line (IRQ).

The ATmega128 is an 8-bit microcontroller, and the AX88796 is designed to run in 8- or 16-bit mode. So, there is a header for the lower eight data bits and another for the upper eight data bits of the AX88796. Data bits 8 through 15 are pinned out on the AX88796 development board for those of you who want to operate in 16-bit mode. Setting a bit in the AX88796's data configuration register (DCR) selects 8- or 16-bit mode.

The fourth header contains pins for the ISA mode AEN and RDY signals. The AX88796 is billed as a Local Bus Ethernet Controller, and CPU[0] and CPU[1] pins on the AX88796 can be configured for one of four local bus CPU modes. These modes include ISA, 80186, 68K, and 8051. The AX88796 pins morph with the CPU selection. For instance, in 8051 mode, the AEN pin becomes the PSEN signal. When the CPU[X] pins are jumpered for 68K mode, the RDY line becomes the DTACK line and address line SA[0] doubles as the LOWER DATA STROBE (LDS) signal. AX88796 chip select (CS) and RESET can be accessed on the header. To accommodate 16-bit designs, the BUS HIGH ENABLE (BHE) signal is also pinned out to this header. AX88796 CS also can be permanently enabled with a jumper or controlled by the AVR at the header.

In addition to being a 10/100-Mbps Ethernet controller, the AX88796 can be configured to interface to a printer. All of the standard printer control lines, including a bidirectional data bus, are pinned out on the AX88796 development board. These lines double as media-independent interface (MII) signals by default. When MII signals are activated, an external PHY can be accessed to implement other types of networks. In either mode, special-purpose registers inside the AX88796 manipulate the feature signals.

Moving to the opposite side of the printer interface pins, you can see a socket area for an 8-pin EEPROM. Unlike the RTL8019AS, the AX88796 does not automatically look for this EEPROM at power-up. Instead, the EEPROM is placed under your control, and it's accessed with an internal AX88796 EEPROM register set.

The AX88796 development board's magnetics are housed within the NU1S041C-434 Lan Mate. The NU1S041C-434 complies with the IEEE 802.3u standards. The Lan Mate is configured with a 1:1 center-tapped turns ratio, and it incorporates all of the necessary electronics to interface to the in-can RJ45 connector.

In addition, the NU1S041C-434 includes three in-can status LEDs. You may download a diagram of the NU1S041C-434 from the *Circuit Cellar* ftp site (it's included in the schematic for the main AX88796 development board).

BOARD MEETING

Now that you're familiar with all of the development boards, let's put them together and explore the AX88796's internals. Of course, I always begin with a smoke test. In my haste, I attached the AX88796 development board to a 5-V VTG STK500/ STK501 system. To my amazement, nothing was damaged on the AX88796 development board. That was a good omen.

According to the AX88796's datasheet, you should be able to port NE2000-compatible code to the AX88796 with little pain and no tears. I'm going to test this because I plan to use much of the same code that the now world-traveled RTL8019AS-based Packet Whacker (it's also hooked up to a web cam) employs.

After reviewing the datasheet for the AX88796, I determined that I had to make some minor changes in the MAC register definitions. I also had to add some definitions because the AX88796 includes registers and bits that the RTL8019AS does not have. The MAC core register set is identical in the buffer ring control areas. The same page start, page stop, current page, and boundary registers described in the National Semiconductor documents exist on the AX88796. The SRAM buffer area is also mapped to the standard NE2000 location of 0x4000 through 0x7FFF. I was pleasantly surprised by the inclusion of content in the AX88796's datasheet that is similar to the original National Semiconductor datasheet content describing the ins and outs of using the buffer ring and DMA resources of the NIC.

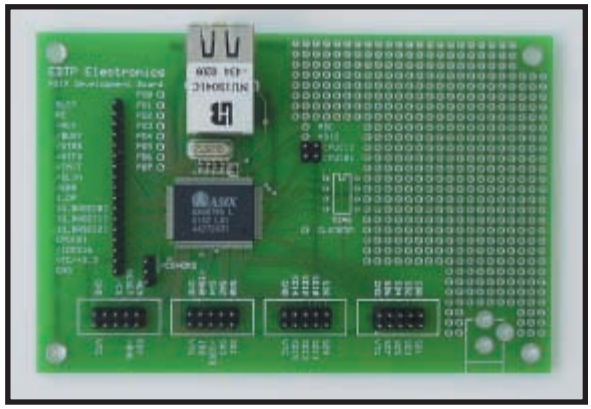
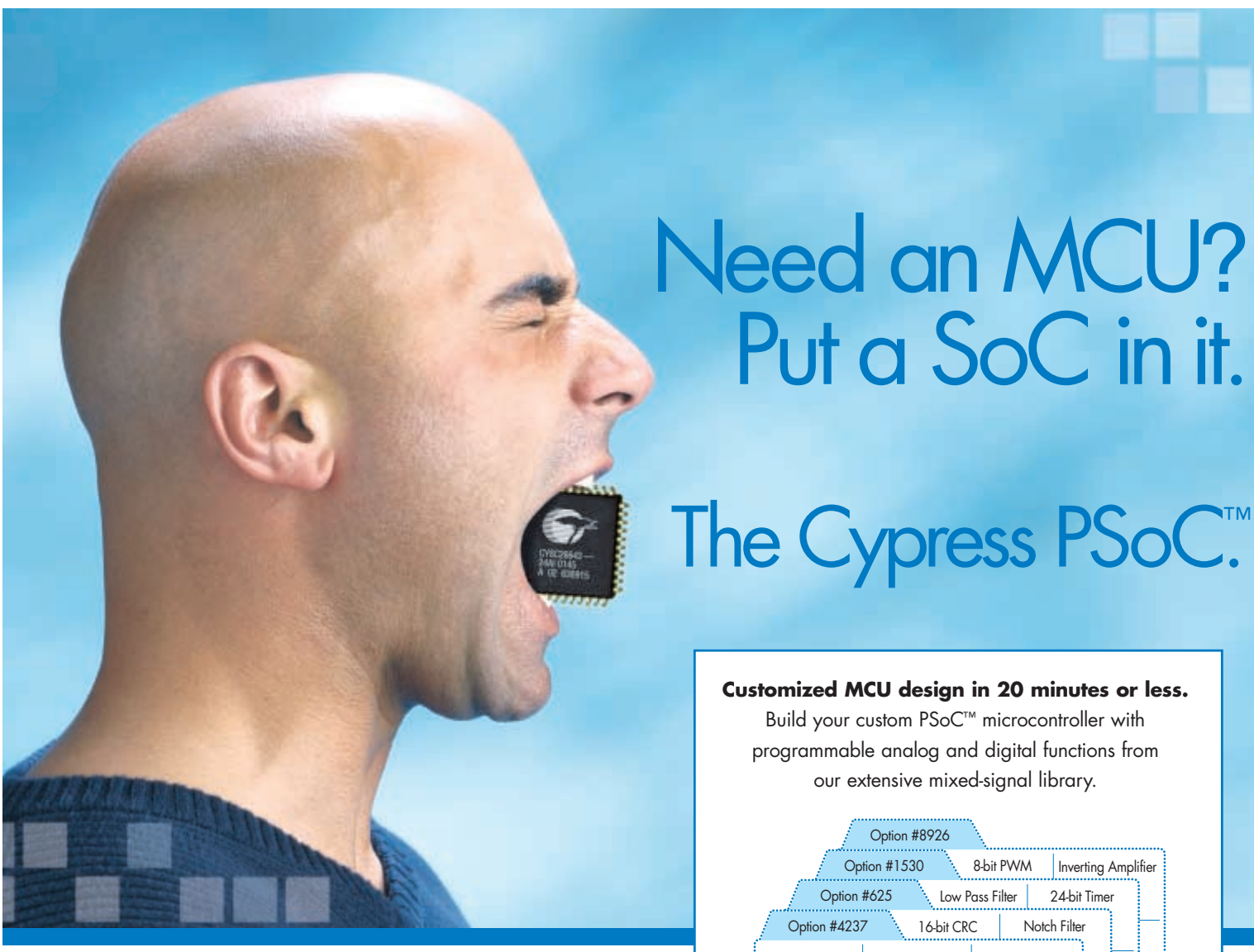


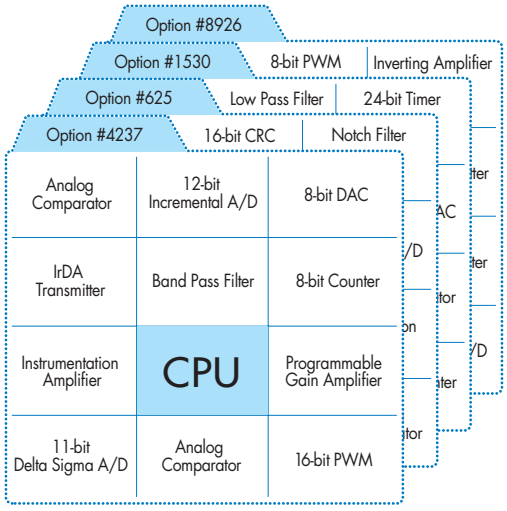
Photo 4—*Every pin that isn't tied to a power rail is pulled out to the header pins. Because I'm new to this IC, I wanted everything to be accessible.*



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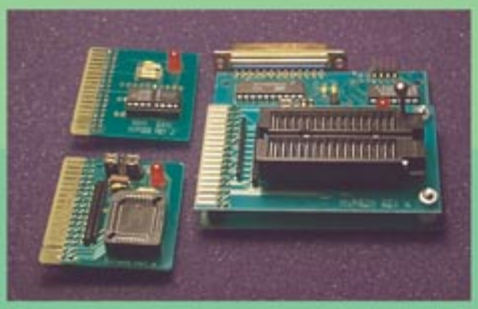
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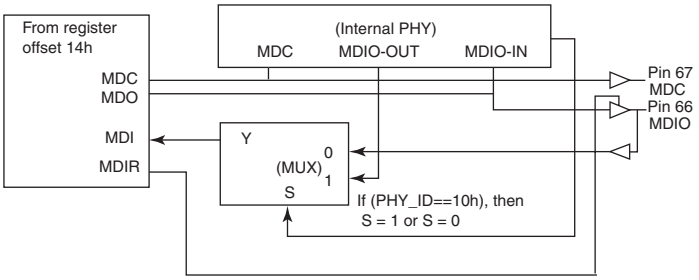
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Unlike the RTL8019AS, there are no pages two and three of the AX88796 MAC register set. That's because the EEPROM is not automatically accessed, so there is no need to reserve space for that "expected" data. Also, Duplex mode is easily selectable using bits in the transmit configuration register (TCR) in the MAC/MII register area. The RTL8019AS contains this mode and the LED activity mode stuck in a hard-to-reach page-three area of the MAC. The LED mode for the AX88796 is pin-selectable by using the I_OP pin of the AX88796.

A notable difference between my original Packet Whacker code and the AX88796 ported code is the way the AX88796 handles NIC reset. The RTL8019AS uses the interrupt status register (ISR) RST bit to indicate when the NIC is out of reset. The AX88796 RST bit is simply an indicator that is set when reset is entered; it's cleared when a start command (0x22) is issued to the command register (CR).

There are many other interesting ways to monitor reset on the AX88796. To accomplish this, the AX88796 adds a test register (TR) at MAC register offset 0x15. Within the TR register are four bits: 100BASE-TX in reset, 10BASE-T in reset, Reset Busy, and Auto-Negotiation Done. Some of the reset results are based on the auto-negotiation process. Reset Busy or RST_B is the replacement for the RST bit in the ISR, and it indicates whether or not the AX88796's PHY is in reset. Because the AX88796 can operate in 10BASE-T or 100BASE-TX mode, the PHY contains logic for both modes with the modes being mutually exclusive.



Field	Description
Pre	Preamble—the PHY will accept frames with no preamble. This is indicated by a 1 in register 1, bit 6.
ST	Start of frame—indicated by a 01 pattern
OP	Opcode—10 for a read; 01 for a write
PHYADD	PHY address—5 bits, allowing for 32 unique addresses. The first PHY address bit transmitted and received is the MSB. A station mangement entity that is attached to multiply PHY entities must have prior knowledge of the appropriate PHY address for each entity.
REGAD	Register address—5 bits, allowing for 32 unique registers within each PHY. The first register address bit transmitted and received is the MSB of the address.
TA	Turnaround—2-bit time spacing between the register address field and the data field of a frame to avoid drive contention MDIO during a read transaction. During a write to the PHY, these bits are driven to 10 by the station. During a read, the MDIO is not driven during the first bit time; it is driven to a zero by the PHY during the second bit time.
DATA	Data—16 bits; the first bit transmitted and received will be bit 15 of the register being addressed.
IDLE	Idle condition—the idle condition on MDIO is high-impedance state. All three state drivers will be disabled, and the PHY's pull-up resistor will pull the MDIO line to logic 1.

Read/Write (R/W)	Pre	ST	OP	PHYAD	REGAD	TA	DATA	IDLE
R	1…1	01	10	AAAAA	RRRRR	Z0	DDDDDDDDDDDDDDD	Z
W	1…1	01	01	AAAAA	RRRRR	Z0	DDDDDDDDDDDDDDD	Z

Figure 1—*Although I slowed the clock to 1-s intervals to watch the LEDs, this interface can run at 12.5 MHz against the internal PHY.*

Auto-negotiation is a means of establishing the highest performance link between stations on a network. For instance, if a station on a network can operate only in 10BASE-T Half-Duplex mode, the auto-negotiation process determines this and sets up the link accordingly. Each node knows about the other through advertisements of each node's abilities. These advertisements are transmitted using fast link pulses, or FLPs. An FLP burst contains 33 link pulses that occur at the same intervals as 10BASE-T normal link pulses (NLPs).

NLPs occur every 16.8 ms. Each FLP burst is 100 ns wide. FLP bursts interleave clock pulses with data pulses. The 17 odd link pulses are clock pulses, and the 16 even link pulses are the data. The absence of a pulse following a clock pulse encodes a logic 0. Conversely, a pulse within the time window following a clock pulse encodes a logic 1. This invisible encoding process ultimately becomes a 16-bit word or link-code word (LCW). Bits within the LCW represent the abilities of the nodes that are establishing the communications link. Using the datasheet, you can see the AX88796's abilities listed in the MR1 register of the AX88796's embedded PHY register set.

I wrote some simple code to read the TR register bits and connected the AX88796 development board to a 10BASE-T network. After performing an NIC reset, reading the TR register indicated that the 100BASE-TX logic was in reset. I then connected the AX88796 development board to a 100BASE-TX network and performed a NIC reset. Just as I expected, the 10BASE-T logic was in reset when connected to the 100BASE-TX net-

work. In both cases, the PHY reset bit was set and later cleared, indicating that the PHY reset successfully. So far, so good.

Although accessing the MII is not required, I thought that it would be a good idea to have AVR code to read and write the AX88796's embedded PHY registers. As it turns out, if I want the AX88796 to behave, I must be able to write to the MII's MR0 control register. There's a statement in the datasheet that basically says you must put the AX88796's embedded PHY in Power Down mode for 2.5 s, and then restart the auto-negotiation process to assure that a good link is established. To do this, you must write two sequences to the MR0 embedded PHY register. This brought about the addition of another MAC register, the MII/EEPROM Management Register (MEMR), at offset 0x14, to my original MAC definitions.

The MEMR register is the origin and endpoint of data going to and from the AX88796 embedded PHY and the external 8-pin EEPROM. The upper four bits of the MEMR represent all of the EEPROM signals—EECLK, EEO, EEI, and EECS. The lower nibble of the MEMR is dedicated to the MII interface. Follow along using Figure 1 as I describe how to interface with the AX88796's embedded PHY.

Notice that pins 66 and 67 can be used to communicate with an external PHY. These pins also can be used during debugging. I connected them to a couple of LEDs on the STK500. The clock for the communications session is provided by alternately loading the MDC bit (bit 0) of the MEMR with a one and zero. I slowed down this clock to 1-s intervals in order to observe the clock and data activity on pins 66 and 67. Everything is synchronized to the rising edge of the MDC clock pulse.

So, to send a one to the embedded PHY, simply set the MDO bit (bit 3 of the MEMR) and write a one-zero sequence to the MDC bit location. To read a bit from the PHY, you must clock the MDC bit and check the status of the MDI (bit 2) bit of the MEMR. The secret to success,

Listing 1—*The ability to read and write the MII interface is a plus because you have access to information about the auto-negotiation process and what the PHY is really doing.*

```
//Write to MII registers
void write_mii(unsigned char phyad,unsigned char regad,unsigned int
mii_data)
{
 unsigned char mask8;
 unsigned int  i,mask16;
 mii_write;            //Macro that sends ST and OP for write operation
 mask8 = 0x10;
 for(i=0;i<5;++i)      //Send 5 bits of PHY address
 {
  switch ((mask8 & phyad))
  {
   case 0:
    clr_mdo;           //Macro clears MDO bit
    break;
   default:
    set_mdo;           //Macro sets MDO bit
  }
    mii_clk;           //Macro clocks bits out of MDC by setting and
                           clearing the MDC bit
    mask8 >>= 1;
 }
 mask8 = 0x10;
 for(i=0;i<5;++i)      //Send 5 bits of PHY register address
 {
  switch ((mask8 & regad))
  {
   case 0:
    clr_mdo;
    break;
   default:
    set_mdo;
  }
   mii_clk;
   mask8 >>= 1;
 }
 mii_w_ta;             //Macro that drives two turnaround bits 10
 mask16 = 0x8000;
 for(i=0;i<16;++i)     //Send 16 bits of data to PHY
 {
  switch (mask16 & mii_data)
  {
   case 0:
    clr_mdo;
    break;
   default:
    set_mdo;
  }
 mii_clk;
 mask16 >>= 1;
 }
}

//Read the MII registers
unsigned int read_mii(unsigned char phyad,unsigned char regad)
{
 unsigned char mask8,i;
 unsigned int  mask16,result16;
 mii_read;             //Macro that sends ST and reads OP bits
 mask8 = 0x10;
 for(i=0;i<5;++i)      //Send 5 bits of PHY address
 {
  switch (mask8 & phyad)
  {
   case 0:
    clr_mdo;
    break;
   default:
```

(Continued)

Listing 1—*Continued*

```
set_mdo;
  }
 mii_clk;
 mask8 >>= 1;
 }
 mask8 = 0x10;
 for(i=0;i<5;++i)              //Send 5 bits of PHY register address
 {
  switch (mask8 & regad)
  {
   case 0:
    clr_mdo;
    break;
   default:
    set_mdo;
  }
 mii_clk;                      //Sets, and then clears MDC bit,
                                   providing the clock
 mask8 >>= 1;
 }
 mii_r_ta;                     //PHY output buffer turnaround time
 mask16 = 0x8000;
 result16 = 0x0000;
 for(i=0;i<16;++i)             //Read 16 bits of data from PHY
 {
  mii_clk;
  read_rtl(MEMR);
  switch (byte_read &= 0x04)
  {
   case 0:
    nop;
   break;
  default:
   result16 |= mask16;
  }
 mask16 >>= 1;
 }
 return result16;
}
```

when reading and writing the embedded PHY, is to know that it's addressed as 0x10.

The bottom of Figure 1 contains the frame format used to communicate with the embedded PHY. The preamble is not required because a bit (bit 6) is set in the MII MR1 register to bypass it by default. A simple start-of-frame sequence is clocked in (ST) followed by the read/write opcode (OP). The bits are clocked in just as you see them, from left to right.

So, to talk to the embedded PHY, 10000 is clocked in as the PHY address. There are 5 bits in both the PHY address (PHYAD) and PHY register address (REGAD). This allows 32 PHY addresses to be defined, and it gives access to 32 registers within each of the 32 PHYs. Note that a PHY address of 0x10 muxes the embedded PHY's output to the MEMR. Any other PHY address would mux the input from pin 66 into the MEMR. The GPO and Control (GPOC) register (another addition to the MAC register definitions) allows you to choose between an external and the internal PHY. The AVR code to access the embedded PHY is shown in Listing 1.

REGISTER TO WIN

It's pretty obvious that you can easily control the AX88796 if you know how to manipulate its registers. I also added the SPP Data Port Register (SPP_DPR) at offset 0x18, the SPP Status Port Register (SPP_SPR) at offset 0x19, and the SPP Command Port Register (SPP_CPR) at offset 0x1A to support bit banging from the AX88796's bidirectional I/O printer port.

You may download the complete AX88796 AVR code from the *Circuit Cellar* ftp site. For more information about the AX88796 development board, head over to the EDTP Electronics web site (www.edtp.com).

Now that you know how to read and write the AX88796's MAC and MII registers with an ATmega128L, you too can be on your way to building a 100-Mbps Ethernet using an 8-bit AVR microcontroller, proving along the way that it doesn't have to be complicated to be embedded.

Fred Eady has more than 20 years of experience as a systems engineer. He has worked with computers and communication systems large and small, simple and complex. His forte is embedded-systems design and communications. Fred may be reached at fred@edtp.com.

PROJECT FILES

To download the code and board schematic, go to ftp.circuitcellar.com/pub/Circuit_Cellar/2002/147/.

REFERENCE

[1] ASIX Electronics Corp., "AX88796 L 3-in-1 Local CPU Bus Fast Ethernet Controller," AX796-18, V1.8, June 2002.

SOURCES

AX88796 Ethernet controller
ASIX Electronics Corp.
886 3 5799500
www.asix.com.tw

ATmega128 Microcontroller, STK500/STK501
Atmel Corp.
(408) 441-0311
www.atmel.com

ICCAVR C compiler
ImageCraft Creations, Inc.
(650) 493-9326
www.imagecraft.com

MAX3232E
Maxim Integrated Products, Inc.
(408) 737-7600
www.maxim-ic.com

RTL8019AS Ethernet controller
Realtek Semiconductor Corp.
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Mad Dash for Flash Cash

FROM THE BENCH

Jeff Bachiochi

12, 16, 18, Hike!

Dashing for Flash Cash



Whether you're gearing up to participate in the Microchip 2002 design contest or getting ready to follow the action from your favorite recliner, now is the perfect time to tune in for Jeff's pregame analysis.

In the past few issues while covering my SmartMedia project, I've been talking about Microchip's PIC18F252. I didn't spend much time discussing the processor then, but it's an apropos topic now that *Circuit Cellar* is kicking off the Mad Dash for Flash Cash Microchip Design Contest 2002. In addition, to give you a leg up in the contest, I'll cover the rest of the Microchip product basics in this article.

RISC-based MPUs began like most with ROM parts for production and EPROM-based parts for development. Although EPROM (windowed) parts are erasable via UV, one-time programmable (OTP) parts don't have a window and cannot be erased even though they're conveniently user-programmable. For many years, development was accomplished with expensive emulators or blow-and-go, using slow-turnaround (erase time) EPROM-based parts. Some frustrated engineer asked about using the new EEPROM/flash memory technology in a micro, allowing it to be quickly erased electrically. Although the packaging would not require the expense of a ceramic-windowed part, using the part only for development would keep volumes low and costs high. Because cost was of great concern, it was deemed foolhardy to consider a flash memory part for production use. After all, when the code works, there's no need for further tweaking and higher costs for erasable parts.

Upgrading a product with external program space consists of replacing the code-bearing ROM/EPROM devices. Thanks to the companies that used socketed parts, this replacement was easy even though it was expensive. When a product used a microprocessor with internal code, the costs were higher, even if it was socketed. On the production line, it took months to use up the old revision stock. This, of course, would lead to unhappy customers further down the road. In terms of inventory, there were advantages to using a reprogrammable part in production, such as the lack of waste and immediate revision updates without the loss of stock.

Early programmable parts required special voltages for the programming process and high programming currents prevailed. Although using internal voltage-boost converters hid some of this, flash memory technology has now advanced to the point where devices are fully reprogrammable in-circuit, even using normal operating voltages. Today, a product can be updated without having to remove the processor from the circuit. In fact,

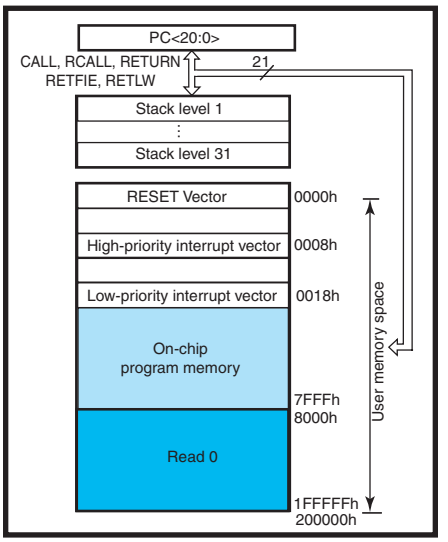


Figure 1—*Program memory space for the PIC18Fx52 is a full 32 KB of flash memory. That's up to 16K single-word instructions. A separate stack space allows 31 levels of calls and interrupts.*

many products that are currently on the market can be updated through a phone/cable/network connection.

DRIVING DOWN COST

OK, so it doesn't start out that way. Investing in technology costs money; however, when the long-term benefits outweigh the costs, the end product's cost can go down. For example, take the PIC16C6*x*/7*x*, which is one of Microchip's most useful parts. It was redesigned using flash memory technology, and now it sells for about half of the original OTP part and one-third the cost of the EEPROM version. Essentially, you're getting a better part for a cheaper price.

From day one, Microchip's top priority was to keep future products code-compatible. Their "seamless migration path" objective is not an easy one to obtain. Even though the word "seamless" probably originated in Microchip's marketing department, the engineering department has obviously attempted to hold onto this mantra with both hands.

LINE 'EM UP

The product lineup began with 12-bit instruction products using only 33 instructions (i.e., the 16C5*x*-series parts). The industry's first 8-pin micro also used this 12-bit RISC instruction set, which is referred to as the 12-series. (Remember asking yourself, "What good is a micro with only six I/Os?")

New devices bragged an increase in instructions to 35 with an increase in instruction width to 14 bits and the addition of interrupts. Reprogrammable parts began to hit production (the PIC16C84) and simplify development. Success triggered a natural progression toward a 16-bit instruction set that used 58 instructions. As a result, the 17-series was born.

C compiler-optimized architectural enhancements gave rise to the 18-series micros and an increase of the instruction set to 77. Meanwhile, flash memory technology has been applied to many devices in the 12-, 16-, and now 18-series of micros.

Instruction	Description
INDF*x*	Moves data to the location pointed to by the FSR*x*H/L pair
POSTDEC*x*	Moves data to the location pointed to by FSR*x*H/L, then decrements the FSR*x*H/L pair
POSTINC*x*	Moves data to the location pointed to by FSR*x*H/L, then increments the FSR*x*H/L pair
PREINC*x*	Increments the FSR*x*H/L pair, then moves the data to the location pointed to by FSR*x*H/L
PLUSW*x*	Moves data to the location pointed to by the combination of the WREG and FSR*x*H/L pair

Table 1—*Use direct addressing to move your data. Indirect addressing is the proper method when you need to move based on a register's value.*

PIC18F252

The PIC18F252 is one of the newest members of Microchip's PIC18F*xxx* family of micros. Let's get more familiar with the processor before you dash off to start your contest entry (see Photo 1).

If you take a look at Figure 1, you'll see some of the important features associated with the program memory organization. The 'F252 has 32 KB of code flash memory, 1536 bytes of data RAM, and 256 bytes of data EEPROM. There are also 31 levels of hardware stack space available in the micro. And, because the stack pointer is read/write, you can set up a software stack in RAM if you need more space. Speaking of RAM, banks of RAM are much easier to use with the PIC18F252.

Figure 2 shows six 256-byte banks of RAM. Note that one bank of RAM is identified by a bank select register (BSR). Alternately, there's an access register bank that always contains the first 128 bytes of RAM (from bank 0) plus the last 128 bytes from bank 15 (i.e., the special function registers, or SFRs). The SFRs are RAM used by the CPU for core functions; peripheral modules use SFRs for control functions.

The data EEPROM is a single bank of 256 bytes. This might be used as configuration data for a sensor that's incorporated in your application. The configuration data might need to be changed; however, it must be nonvolatile in nature.

The PIC chips incorporate a few safety techniques to assure this memory isn't changed arbitrarily by errant code. First, the EEPROM data area is not mapped into the data (register) space. To read from the EEPROM block, you must place the address of interest into the EEADR register in the FSR bank. Note that the EEPGD bit must be cleared to point to the EEPROM area, and the RD bit must be set to enable a read. Both bits are found in the EECON1 register located in the FSR

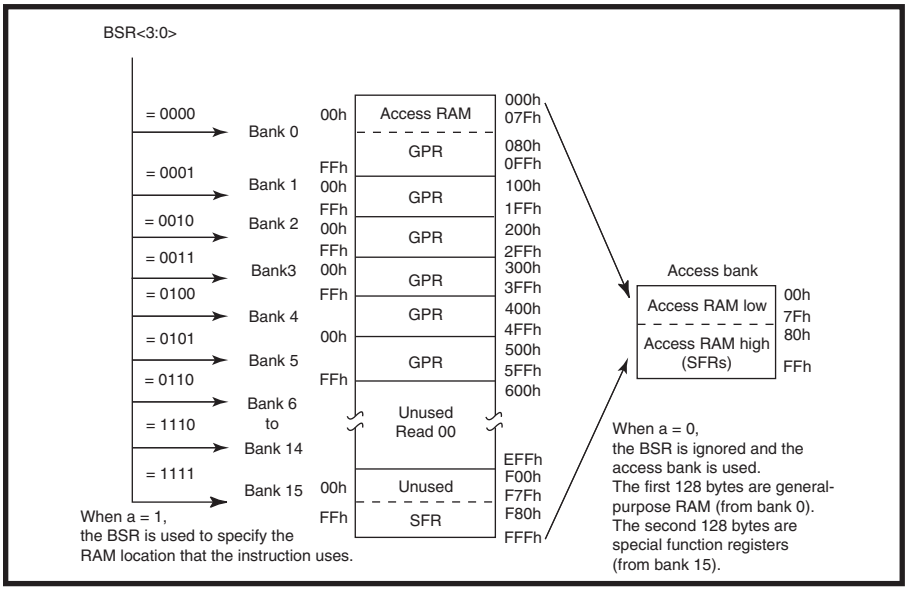


Figure 2—*Data memory is divided into 256-byte static RAM banks. Data addressing is available via the access bank or through the bank select register (BSR). The BSR's lower nibble selects one of the 16 RAM banks (0 to 15). The access bank is always available. It consists of the first half of RAM in bank 0 plus the special function registers (SFR) in the last half of bank 15.*

bank. The data stored in the EEPROM at address EEADR is available in the EEDATA register in the FSR bank.

Writing an address in the data EEPROM involves a similar process. Place the address of the write into the EEADR register. Then, insert the data to be written into the EEDATA register. The EEPGD bit must be cleared to point to the EEPROM area, and the WREN bit must be set to enable a write. Next, disable the global interrupt to prevent interference by any other peripheral. The following sequence must be executed exactly: Write 0x55 to the EECON2 register; write 0xAA to the EECON2 register; set the WR bit in the EECON1 register to begin the actual write; and then execute an NOP instruction. The global interrupt can be enabled once again. It's a good practice to clear the WREN bit when finished writing data to the EEPROM data area.

ADDRESSING

If you've had the privilege to program 12- or 16-series PICs, you're probably familiar with the page-

Mnemonic, Operands		Description	Cycles	16-bit instruction word MSb			LSb	Status affected
Byte-oriented file register operations								
ADDWF	(f, d, a)	Add WREG and f	1	0010	01da	ffff	ffff	C, D, Z, OV, N
ADDWFC	(f, d, a)	Add WREG and carry bit to f	1	0010	00da	ffff	ffff	C, DC, Z, OV, N
ANDWF	(f, d, a)	AND WREG with f	1	0001	01da	ffff	ffff	Z, N
CLRF	(f, a)	Clear f	1	0110	101a	ffff	ffff	Z
COMF	(f, d, a)	Complement f	1	0001	11da	ffff	ffff	Z, N
CPFSEQ	(f, a)	Compare f with WREG, skip =	1 (2 or 3)	0110	001a	ffff	ffff	None
CPFSGT	(f, a)	Compare f with WREG, skip >	1 (2 or 3)	0110	010a	ffff	ffff	None
CPFSLT	(f, a)	Compare f with WREG, skip <	1 (2 or 3)	0110	000a	ffff	ffff	None
DECF	(f, d, a)	Decrement f	1	0000	01da	ffff	ffff	C, DC, Z, OV, N
DECFSZ	(f, d, a)	Decrement f, skip if 0	1 (2 or 3)	0010	11da	ffff	ffff	None
DCFSNZ	(f, d, a)	Decrement f, skip if not o	1 (2 or 3)	0100	11da	ffff	ffff	None
INCF	(f, d, a)	Increment f	1	0010	10da	ffff	ffff	C, DC, Z, OV, N
INCFSZ	(f, d, a)	Increment f, skip if 0	1 (2 or 3)	0011	11da	ffff	ffff	None
INFSNZ	(f, d, a)	Increment f, skip if not 0	1 (2 or 3)	0100	10da	ffff	ffff	None
IORWF	(f, d, a)	Inclusive OR WREG with f	1	0001	00da	ffff	ffff	Z, N
MOVF	(f, d, a)	Move f	1	0101	00da	ffff	ffff	Z, N
MOVFF	(f_s, f_d)	Move f_s (source) to first word f_d (destination) second word	2	1100 1111	ffff ffff	ffff ffff	ffff ffff	None
MOVWF	(f, a)	Move WREG to f	1	0110	111a	ffff	ffff	None
MULWF	(f, a)	Multiply WREG with f	1	0000	001a	ffff	ffff	None
NEGF	(f, a)	Negate f	1	0110	110a	ffff	ffff	C, DC, Z, OV, N
RLCF	(f, d, a)	Rotate left through carry	1	0011	01da	ffff	ffff	C, Z, N
RLNCF	(f, d, a)	Rotate left (no carry)	1	0100	01da	ffff	ffff	Z, N
RRCF	(f, d, a)	Rotate right through carry	1	0011	00da	ffff	ffff	C, Z, N
RRNCF	(f, d, a)	Rotate right (no carry)	1	0100	00da	ffff	ffff	Z, N
SETF	(f, a)	Set f	1	0110	100a	ffff	ffff	None
SUBFWB	(f, d, a)	Subtract f from WREG with borrow	1	0101	01da	ffff	ffff	C, DC, Z, OV, N
SUBWF	(f, d, a)	Subtract WREG from f	1	0101	11da	ffff	ffff	C, DC, Z, OV, N
SUBWFB	(f, d, a)	Subtract WREG from f with borrow	1	0101	10da	ffff	ffff	C, DC, Z, OV, N
SWAPF	(f, d, a)	Swap nibbles in f	1	0011	10da	ffff	ffff	None
TSTFSZ	(f, a)	Test skip if 0	1 (2 or 3)	0110	011a	ffff	ffff	None
XORWF	(f, d, a)	Exclusive OR WREG with f	1	0001	10da	ffff	ffff	Z, N

Figure 3—*Byte-oriented instructions manipulate a RAM or SFR.* f *is the register file,* d *is the destination bit, and* a *is the RAM access bit.*

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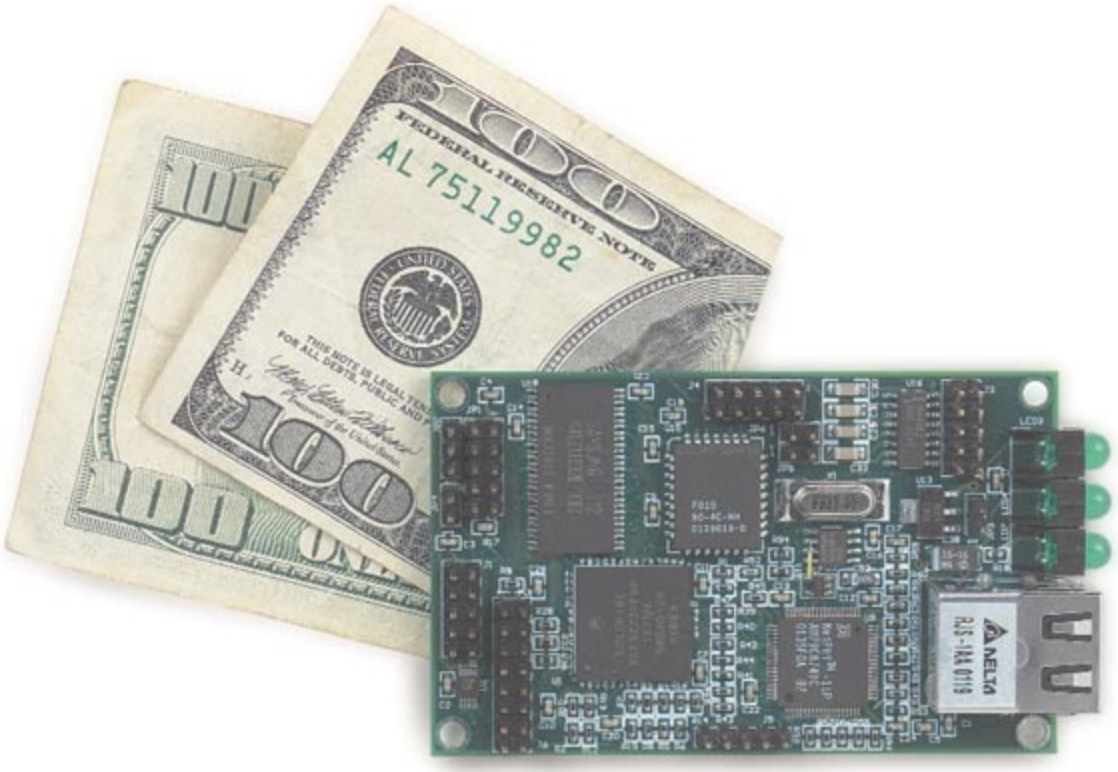
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switching requirement that's the result of the limited width of the address field in single-word GOTO and CALL instructions. A larger 21-bit program counter provides a linear reach of 2 MB. And the paging ugliness has been done away with, thanks to multi-word GOTO and CALL instructions.

Program memory is handled in byte increments instead of the previous word-sized (12, 14, or 16 bits) increments. Although this means the PC is now incremented by two for each instruction or four for each two-word instruction, the instruction flow (i.e., the use of pipelining) still exists. This allows each instruction to be executed in a single execution cycle (after an initial fetch) except for any instruction that changes the PC (i.e., a branch instruction), which requires a new fetch to fill the pipe again.

Direct addressing is used for most data moves—get this here, put that there. The moves are based on a fixed location. Indirect addressing is handy when you need to move dynamically, based on a register's value as opposed to the register itself. Although the original PICs had a single indirect register, the 18-series has three sets of indirect registers. Each set contains a register pair, FSR*x*H and FSR*x*L (x = 0–2), where the registers hold a 12-bit address covering the total RAM space.

In addition to this pointer pair, five other registers are used to access the data being pointed to, and they potentially affect the pointer pair (see Table 1). The indirect registers work the same way when retrieving data from them (i.e., the location pointed to by the FSR*x*H/L pair). Notice any similarity to C operators here?

Mnemonic, Operands	Description	Cycles	16-bit instruction word				Status affected	Notes
			MSb			LSb		
Bit-oriented file register operations								
BCF (f, b, a)	Bit clear f	1	1001	bbba	ffff	ffff	None	1, 2
BSF (f, b, a)	Bit set f	1	1000	bbba	ffff	ffff	None	1, 2
BTFSC (f, b, a)	Bit test f, skip if clear	1 (2 or 3)	1011	bbba	ffff	ffff	None	3, 4
BTFSS (f, b, a)	Bit test f, skip if set	1 (2 or 3)	1010	bbba	ffff	ffff	None	3, 4
BTG (f, b, a)	Bit toggle f	1	0111	bbba	ffff	ffff	None	1, 2

Figure 4—*Bit-oriented instructions manipulate a single bit within a RAM or SFR.*

Even though the FSR*x*H and FSR*x*L cover the data area, another useful set of registers cover the code area. This is useful for retrieving table information stored in code space. It works a bit differently from the indirect addressing registers. Because the code area is much larger than the RAM area, three address registers are needed TABPTRU/H/L. A single register TABLAT is used to hold the table read's data. Instead of using registers to read the table data, there are four TABRD instructions you can use. Each instruction will affect the TABPTRU/H/L register differently (see Table 2).

Remember that these instructions are performing access to the code area. Normally, with non-flash memory parts, the data in the code area is read-only. Flash memory parts open Pandora's box because the code area can be reprogrammed using the TABWR instructions similar to the TABRD instructions. If you recall from



last month how a byte of a sector of a SmartMedia block is changed, then you can already guess how reprogramming a byte in code space must be handled.

A byte of code area (flash memory) that's not erased cannot be written on a byte or word basis; it requires an erasure of a 64-byte block (e.g., TBLPTRU/H/L uses only bits 6 to 21, bits 0 to 5 are ignored). This means that if data in the other 63 bytes is important, you must have a 64-byte RAM buffer set aside to read the 64-byte block into before erasing it or the data stored there is lost.

To erase a 64-byte block of the code area, place the address of the block into the TBLPTRU/H/L registers. The EEPGD, WREN, and FREE bits must be set to point to the flash memory area to enable a write and an erase. All bits are found in the EECON1 register located in the FSR bank.

Next, disable the global interrupt to prevent interference by any other peripheral. Then, execute the following sequence to begin the internal erasure process: Write 0x55 to the EECON2 register; write 0xAA to the EECON2 register; set the WR bit in the EECON1 register to begin the actual erase; and then execute an NOP instruction.

Further instructions will be halted until the internal process is complete. The global interrupt can be enabled at that time. After the data is in RAM, bytes can be changed and the block written back into the code space. But wait, writing to the code area writes 8 bytes (i.e., a partial block) at a time, so the write process must be done eight times to completely write the 64-byte block back into the code area.

Instruction	Description
TABRD	Retrieves data from the location pointed to by the TABPTRU/H/L registers
*TABRD–	Retrieves data from the location pointed to by the TABPTRU/H/L registers, then decrements the FSRxH/L pair
*TABRD+	Retrieves data from the location pointed to by TABPTRU/H/L registers, then increments the FSRxH/L pair
*TABRD+	Increments the FSRxH/L pair, then retrieves data from the location pointed to by the TABPTRU/H/L registers

Table 2—*These are the four instructions you can use to read the table data.*

To write to the flash memory, the TBLPTRU/H/L registers are set to the beginning address of one of the partial blocks (the LSb would be xxxxx000). Eight writes to the TABLAT (using *TABWR+, post-increment) actually write to eight holding registers. These registers will be used by the hardware when the programming takes place. To initiate the write to flash memory, the EEPGD, WREN, and FREE bits must be set to point to the flash memory area to enable a write and an erase.

Next, disable the global interrupt to prevent interference by any other peripheral. Now, the following sequence is executed to begin the internal programming process: Write 0x55 to the EECON2 register; write 0xAA to the EECON2 register; set the WR bit in the EECON1 register to begin the actual write; and then execute an NOP instruction.

Further instructions will be halted until the internal process is complete. The global interrupt can be enabled once again. This entire process is repeated eight times for the remaining data bytes in the block. Note that it requires about 18 ms to update the whole block.

INSTRUCTION SET

Instructions are grouped into five categories: byte-oriented, bit-oriented, literal, control, and table-oriented. The byte-oriented operations are listed in Figure 3. They contain an opcode and up to three operands: a file register (f), a destination bit (d), and a RAM access bit (a).

The file register is the location in a RAM bank on which the operation is to be performed. The destination bit indicates where the result of the operation will be placed. When d = 0, the result goes into the WREG. When d = 1, the result is put back into the file register. The RAM access bit indicates where the file register will be found. When a = 0, the file register is taken from the access register bank. If a = 1, the file register is taken from the RAM bank indicated by the BSR. Note that this is a source of confusion, so it must be chosen wisely.

For instance, if the file register of interest is the SFR TXREG, you may use a = 0 to indicate it's in the access bank. If the BSR = 0x0F, you may use a = 1, otherwise using a = 1 (RAM bank) when BSR points to any other bank will make use of the wrong register (see Figure 2).

Most byte-oriented instructions are single-word instructions that execute in a single instruction cycle (except where the PC is altered). In the byte-oriented category, there's also a register-to-register move, which requires two words because it's a direct move avoiding the use of bits a and d. As such, it must contain the 12-bit address of each register. This instruction takes two instruction cycles to execute.

The bit-oriented instructions are listed in Figure 4. These contain an opcode and three operands: a file register, a bit position (b), and a RAM

Mnemonic, Operands	Description	Cycles	16-bit instruction word MSb			LSb	Status affected	Notes
Literal operations								
ADDLW (k)	Add literal and WREG	1	0000	1111	kkkk	kkkk	C, DC, Z, OV, N	
ANDLW (k)	AND literal with WREG	1	0000	1011	kkkk	kkkk	Z, N	
IORLW (k)	Inclusive OR literal with WREG	1	0000	1001	kkkk	kkkk	Z, N	
LFSR (f, k)	Move literal (12-bit) second word to FSRX first word	2	1110 1111	1110 0000	00ff kkkk	kkkk kkkk	None	
MOVLB (k)	Move literal to BSR<3:0>	1	0000	0001	0000	kkkk	None	
MOVLW (k)	Move literal to WREG	1	0000	1110	kkkk	kkkk	None	
MULLW (k)	Multiply literal by WREG	1	0000	1101	kkkk	kkkk	None	
RETLW (k)	Return with literal in WREG	2	0000	1100	kkkk	kkkk	None	
SUBLW (k)	Subtract WREG from literal	1	0000	1000	kkkk	kkkk	C, DC, Z, OV, N	
XORLW (k)	Exclusive OR literal with WREG	1	0000	1010	kkkk	kkkk	Z, N	

Figure 5—*Literal instructions involve a constant in the manipulation of a register, usually WREG.*

Interrupt source	Description
TMR0	Timer 0 overflow
TMR1	Timer 1 overflow
TMR2	Timer 2 overflow
TMR3	Timer 3 overflow
RB	Port B change of state
INT0	External interrupt 0
INT1	External interrupt 1
INT2	External interrupt 2
PSP	Parallel slave port (PIC18F4*x*2 only)
AD	End of A/D conversion
RC	USART Receive
TX	USART Transmit
CCP1	Capture compare PWM 1
CCP2	Capture compare PWM 2
EE	EEPROM/flash memory write complete
BCL	Bus collision
LVD	Low-voltage detect
SSP	Synchronous serial port

Table 3—*Interrupts make coding a much easier process. Here are the interrupt sources for the '18Fxx2.*

access bit (a). The file register is the location in a RAM bank on which the operation is to be performed. The bit position specifies on which bit (from 0 to 7) the operation is to be performed. The RAM access bit indicates where the file register will be found.

When a = 0, the file register is taken from the access register bank. And when a = 1, the file register is taken from the RAM bank indicated by the BSR. All bit-oriented instructions are single-word instructions and execute in a single instruction cycle (except where the PC is altered).

The literal instructions are listed in Figure 5. These contain an opcode and one or two operands: a constant (k) and an FSR (f). In most cases, an operation is performed using an 8-bit constant and the WREG, with the result being placed back into the WREG. One instruction uses an FSR to point to one of the three indirect file register sets, which will accept the 12-bit direct RAM memory address (k). This move is a two-word instruction requiring two instruction cycles.

Control operations have to do with instructions that can change the path of execution. These contain an opcode and up to two operands (see Figure 6). Opcodes without operands have direct operations like CLRWDT (clear watchdog timer), NOP (no operation), and SLEEP (go into a Standby mode). There are both direct and relative GOTO (BRA) and CALL (RCALL) instructions. The direct instructions require two words. Because all of them affect the PC, they all require two execution cycles. Even though all conditional branch instructions are single words, they too affect the PC, and as such, they require two execution cycles.

The eight table operations were discussed earlier and are listed in Figure 7.

INTERRUPTS

If you've worked with the 12-bit PICs, then you know it's not easy coding without interrupts. Even with the advent of interrupts, many applications suffer from long interrupt latencies (i.e., the time from the initial interrupt event to the time when the interrupt is actually serviced). This might be the result of having to save registers, poll the interrupt register, or another interrupt routine having control at the time. The 18-series micros have a number of latency-reducing features.

The first is two levels of priority. Often, your project will include more than one interrupt routine. When all of the interrupts are equal, a pending interrupt must wait for any in-process interrupt to complete. Eighteen-series interrupts can be optionally defined as either high or low priority (see Table 3). Each priority has a separate interrupt vector address. A high-priority interrupt can interrupt a low-priority interrupt immediately. Therefore, a high-priority interrupt has the lowest interrupt latency.

An interrupt automatically saves the WREG, STATUS, and BSR bits into a one-level fast stack. The control instruction RETFIE (return from interrupt) has an s operand that controls whether or not the return from the interrupt is with or without restoring these registers from the fast stack. Care must be used because the fast stack is only one level. If a high-priority interrupt interrupts a low-priority routine, the low priority's automatic save is overwritten when the high-priority interrupt begins. The control instructions CALL and RETURN also have the s operand and can make use of the fast stack, but should be used only if interrupts are disabled or not used.

CLOCK OSCILLATOR

The PIC18F*xx*2 micros support eight oscillator modes. The low-power (LP) mode supports crystals up

Mnemonic, Operands	Description	Cycles	16-bit instruction word MSb			LSb	Status affected
Control operations							
BC (n)	Branch if carry	1 (2)	1110	0010	nnnn	nnnn	None
BN (n)	Branch if negative	1 (2)	1110	0110	nnnn	nnnn	None
BNC (n)	Branch if not carry	1 (2)	1110	0011	nnnn	nnnn	None
BNN (n)	Branch if not negative	1 (2)	1110	0111	nnnn	nnnn	None
BNOV (n)	Branch if not Overflow	2	1110	0101	nnnn	nnnn	None
BNZ (n)	Branch if not zero	1 (2)	1110	0001	nnnn	nnnn	None
BOV (n)	Branch if overflow	1 (2)	1110	0100	nnnn	nnnn	None
BRA (n)	Branch unconditionally	1 (2)	1101	0nnn	nnnn	nnnn	None
BZ (n)	Branch if zero	1 (2)	1110	0000	nnnn	nnnn	None
CALL (n, s)	Call subroutine first word	1	1110	110s	kkkk	kkkk	None
	second word		1111	kkkk	kkkk	kkkk	
CLRWDT	Clear watchdog timer	1	0000	0000	0000	0100	*TO, *PD
DAW	Decimal adjust WREG	1	0000	0000	0000	0111	C
GOTO (n)	Go to address first word	2	1110	1111	kkkk	kkkk	None
	second word		1111	kkkk	kkkk	kkkk	
NOP	No operation	1	0000	0000	0000	0000	None
NOP	No operation (Note 4)	1	1111	xxxx	xxxx	xxxx	None
POP	Pop top of return stack (TOS)	1	0000	0000	0000	0110	None
PUSH	Push top of return stack (TOS)	1	0000	0000	0000	0101	None
RCALL (n)	Relative call	2	1101	lnnn	nnnn	nnnn	None
REST	Software device RESET	1	0000	0000	1111	1111	All
RETFIE (s)	Return from interrupt enable	2	0000	0000	0000	000s	GIE/GIEH, PEIE/GIEL
RETLW (k)	Return with literal in WREG	2	0000	1100	kkkk	kkkk	None
RETURN (s)	Return from subroutine	2	0000	0000	0001	00ls	None
SLEEP	Go into Standby mode	1	0000	0000	0000	0011	*TO, *PD

Figure 6—*Control instructions alter the execution of a program or perform a given task.*

to 200 kHz. Crystals or resonators up to 4 MHz can be used with XT mode. For frequencies up to 20 MHz, the high-speed (HS) mode is used.

To reduce EMI, the PLL mode accepts crystals or resonators up to 10 MHz and internally multiplies them by four. These modes require both OSC1 (input) and OSC2 (output) pins. The RC resistor/capacitor (RC) and external clock (EC) modes require only the OSC1 input. The OSC2 output will have a clock output derived by an OSC1 divided by four. Alternatively, the OSC2 output can be disabled and the pin used as an extra I/O with RCIO and ECIO modes. Timer 1 can be configured as a low-power clock by attaching a 32-kHz watch crystal to its oscillator pins. The system clock can be sourced and switched between either of these oscillators, making for some rather interesting speed/power trade-offs.

RESET

Numerous sources can cause a reset, so knowing where the reset came from can often allow an application to respond differently based on the cause. Table 4 lists the functions that can cause a reset.

To ensure that the power supply and internal functions have stabilized, special power-up delays are invoked depending on the mode of the micro. If MCLR is tied to V_{CC} (i.e., no RC delay has been applied to the MCLR pin), the power-up timer (PWRTE) can be enabled to hold the micro in reset for an initial fixed 73-ms delay. If a crystal or resonator is used, the micro is held in reset for an additional delay of 1024 oscillator cycles to ensure that the oscillator has stabilized. When configured for PLL, the delay is extended for another 2 ms to allow the phase loop to fully lock.

When enabled, the brownout detector can be set for one of four voltages (2, 2.7, 4.2, or 4.5 V). Any time V_{CC} falls below this level, the micro is held in reset for a total power-up delay after V_{CC} has been restored. On a wake-up from sleep or an oscillator source switch, further execution can be delayed by 1024 oscillator cycles plus 2 ms, depending on the mode.

Bit	Function	Register location
STKFUL (7)	Stack overflow	STKPTR
STHUNF (6)	Stack underflow	STKPTR
RI (4)	Software reset	RCON
TO (3)	Watchdog time-out	RCON
PD (2)	Power down	RCON
POR (1)	Power-on (hardware) reset	RCON
BOR (0)	Brownout	RCON

Table 4—*There are several functions that can cause a reset.*

HARDWARE MULTIPLY

Math-intensive applications can benefit from the hardware multiply function included in the 18-series PIC processors. WREG is multiplied by any 8-bit register to produce a 16-bit result in a single instruction cycle. This unsigned function saves about 68 instruction cycles over using a software routine. For signed and other larger multiplies, including the hardware multiply, the algorithm will reduce execution time by a factor of seven to 15 times.

PORTS

Like many micros, some port I/O pins are multiplexed for alternate peripheral functions. Each port has three registers associated with it. These registers are PORT*x*, TRIS*x*, and LAT*x* (where x = A/B/C for the PIC18F2*x*2 and D/E for the '18F4*x*2).

The TRIS*x* register is a read/write register that determines the direction of each port pin. When a bit position equals one, the corresponding I/O pin is configured as an input (high impedance). When a bit position equals zero, the corresponding I/O pin is configured as an output, and the logic level of the corresponding data latch bit is placed on the I/O pin. Writing data to the LAT*x* or PORT*x* will update a data latch. Reading the LAT*x* register retrieves the present state of the data latch. Reading the PORT*x* register retrieves the present state of the port's I/O pins (not the data latch).

Even though it's only available on the PIC18F4*x*2, which uses PORTD and PORTE, the parallel slave port (PSP) is worthy of being mentioned here. This peripheral allows the micro to be interfaced directly to another processor's data bus. The 8-bit data port and three control signals (CS, RD, and WR) camouflage it as a peripheral chip. This little gem lets you design custom smart peripherals.

TIMERS

Four 16-bit counter/timers are included in the PIC18F*xx*2 microcontroller. Each has several special features associated with it. Timer 0 is selectable as an 8- or 16-bit timer with appropriate rollover interrupt; it has a dedicated 8-bit prescaler and clock edge selection when clocked externally.

Timer 1 and Timer 3 have dedicated 3-bit prescalers and clock edge selection when clocked externally. Their clock source can also come from the auxiliary low-power external oscillator and synchronized to the system clock. Both timers can be cleared by a trigger from the CCP module (Compare mode).

Although Timer 2 has an 8-bit timer register (TMR2), it can achieve a 16-bit count with the 4-bit prescaler and 4-bit postscaler. A second 8-bit period register (PR2) is compared to the TMR2 and used as a reference. When the registers match, the TMR2 register is cleared (data rate generator).

Prescalers are normally cleared with a write to the lower byte of any timer.

CCP

Each PIC18F*xx*2 contains two identical CCP*x* modules (where x = 1 or 2). In Capture mode, a 16-bit timer count (Timer 1 or Timer 3) is transferred into a 16-bit CCPR*x*H/L

Mnemonic, Operands	Description	Cycles	16-bit instruction word MSb			LSb	Status affected
Data memory ↔ Program memory operations							
*TBLRD	Table read	2	0000	0000	0000	1000	None
*TBLRD+	Table read with post-increment		0000	0000	0000	1001	None
*TBLRD–	Table read with post-decrement		0000	0000	0000	1010	None
*TBLRD+	Table read with pre-increment	2 (5)	0000	0000	0000	1011	None
*TBLWT	Table write		0000	0000	0000	1100	None
*TBLWT+	Table write with post-increment		0000	0000	0000	1101	None
*TBLWT–	Table write with post-decrement		0000	0000	0000	1110	None
*TBLWT+	Table write with pre-increment		0000	0000	0000	1111	None

Figure 7—*Table instructions allow the program memory space to be read or modified.*

register pair on a selected event. An event is defined as every falling edge, every rising edge, every fourth rising edge, or every sixteenth rising edge.

In Compare mode, the value in the 16-bit CCPRxH/L register pair is compared to a 16-bit timer count (Timer 1 or Timer 3). A match initiates an interrupt and triggers a clear to the counter/timer. A match can also toggle an output pin or produce a rising or falling edge on a match.

Timer 2 is used for the PWM period timer servicing both PWMs. When implemented as the PWM period timer, two additional least significant bits are used, either from the Timer 2 prescaler or the Q clock when the prescaler is 1:1, to produce a 10-bit value. When Timer 2 matches (TMR2 = PR2), TMR2 is cleared, the CCP output pin is set, and a CCP reload is triggered. The duty cycle period is determined by the 8-bit value in CCPRxL + 2 bits from the CCPxCON register. This 10-bit reference value is loaded into the 8-bit CCPRxH + 2-bit internal latch by the Timer 2 trigger. This 10-bit value is compared with Timer 2's 10-bit register (TMR2 + 2 bits). A match between these 10-bit registers clears the CCPx output pin.

So, the period equals the amount of time it takes TMR2 to count up to PR2. The on (i.e., CCP*x* output pin is high) time is the time it takes TMR2 to match CCPRxH. If the CCPRxH is zero, the output never gets set. If CCPRxH is greater than TMR2, the output never gets cleared because CCPRxH will never match TMR2.

SERIAL PORT

The synchronous serial port (SSP) module can be configured to support SPI or I²C. The SPI supports Master and Slave modes. Master mode provides a synchronous clock out to support data output and input pins. Slave mode accepts a synchronous clock to support data output and input pins. The clock comes from the system, prescaler, or Timer 2.

The I²C interface uses two bidirectional pins, data and clock. In Master mode, a clock output is supplied and data flows in and out of the data pin. In Slave mode, the clock becomes an input and the data flows in and out of the data pin. Multimaster mode allows masters to compete for the bus, with the loser(s) of arbitration allowing the winner to complete its message. The clock for the I²C interface comes from a dedicated data rate generator (BRG). This is an auto-reload 8-bit counter with an optional divide-by-16 prescaler off of the system clock.

The universal synchronous asynchronous receiver transmitter (USART) module can be configured for both sync and async modes. Both modes use BRG as the clock source. Asynchronous mode allows data to flow independently in both directions (TX and RX) at the same time.

Because Synchronous mode supplies a clock (by the master on TX), data can flow only in one direction at a time on RX. The data format is the

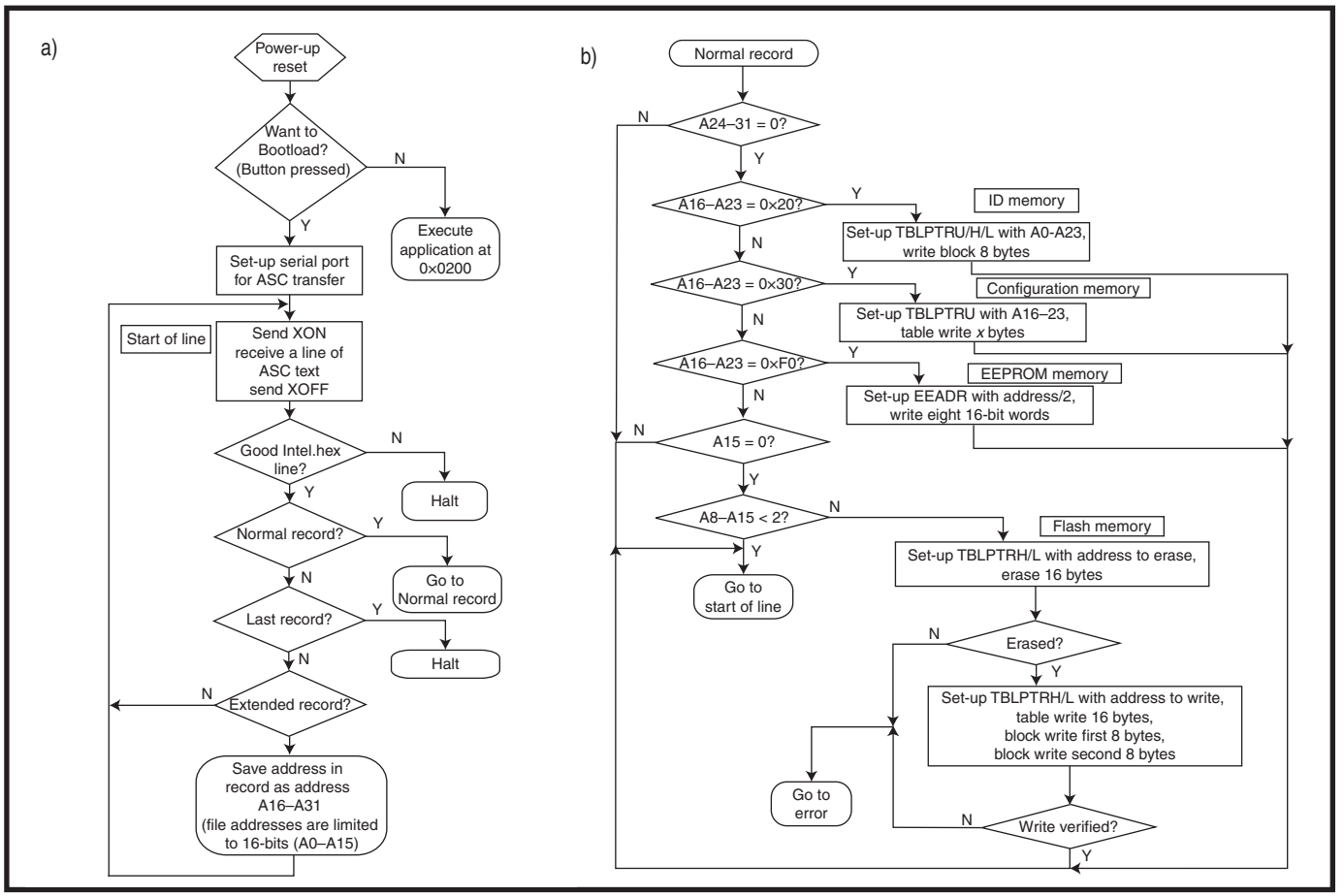


Figure 8—*This flowchart will help you write your own boot load application.*

same for both modes: 8(9) data bits per byte, with the asynchronous mode requiring one start and one stop bit per byte sent.

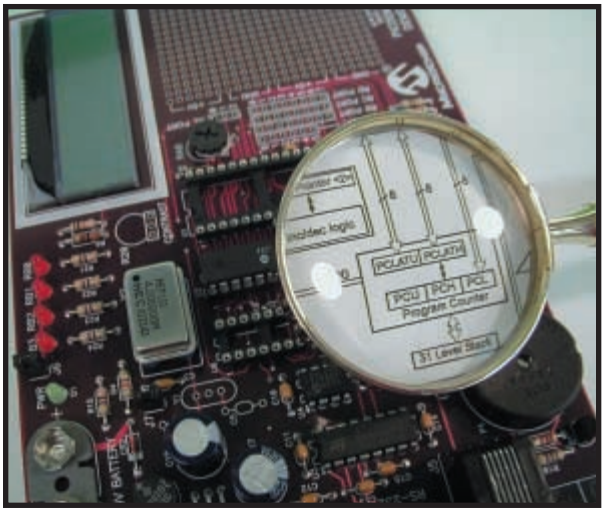


Photo 1—*Look inside before taking your first step in the dash for flash cash.*

A/D

Between the eight-channel multiplexer ahead of the 10-bit analog-to-digital converter module and the ability to choose whether or not pins are configured as digital, analog, or reference, this module is highly user-friendly. Both the upper and lower references for the analog-to-digital converter can be configured for internal V_{DD} and V_{SS} or external voltages via port pins. This allows the input span to be carefully tailored for maximum resolution. The 10-bit A/D result can be right or left justified in the 16-bit register pair, making it easy for a single-byte read to retrieve the 8-MS or least significant bits of the result.

It's recommended that the analog source impedance be less than 2.5 kΩ. This will allow the converter to meet the specified accuracy by permitting the internal sampling capacitor to charge fully in a predetermined amount of time (i.e., a minimum acquisition time).

After a channel is selected, the application must wait this acquisition time before beginning a conversion (setting the GO bit in ADCON0). The GO bit will be cleared when the conversion result is ready. You may wish to set up CCP*x* and TIMER1 (or 3) to provide an acquisition delay and automatic conversion start.

LOW-VOLTAGE DETECTOR

When using batteries, it's often necessary to prepare the application for shutdown by executing housekeeping tasks. Sure, the brownout detector can stop execution before things go haywire, but how do you prepare for this?

A low-voltage detector can be set somewhere above the brownout voltage so that it gives warning of impending doom with time to make ready. The detector in the PIC18F*xx*2 can be set to one of 14 levels or through an external pin (LVDIN). These levels are tapped off of a voltage divider powered by V_{DD}. The level is compared to a 1.2-V internal reference also powered by V_{DD}. Therefore, the LVDCON register has a bit (IRVST) that indicates when you can trust the detector's output and enable the interrupt.

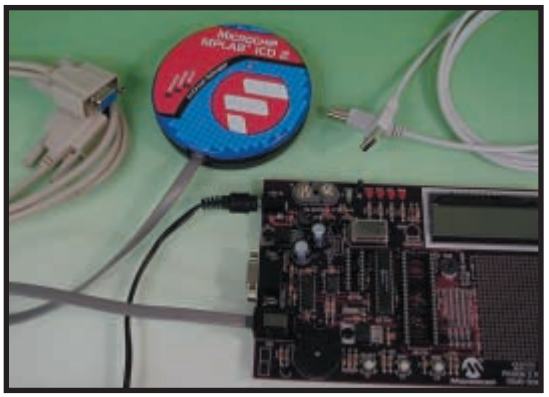


Photo 2—*I've used Microchip's IDC1 before, but the IDC2 would have made some of my earlier projects a little easier.*

WATCHDOG TIMER

Watchdog timers (WDT) are used to grab hold of an application that's executing errant code stuck in never-never land, and then reset the system to regain control. The '18F*xx*2 has a watchdog timer that uses a completely autonomous RC oscillator.

If the device is configured with the watchdog enabled, it can be arbitrarily enabled and disabled using the

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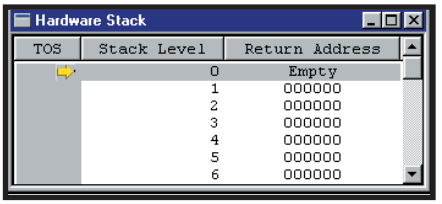


Photo 3—*A view into the hardware stack will give you important feedback as to the depth of the nested call and interrupt routines.*

SWDTEN bit in the WDTCON register. If it's configured as off, it cannot be controlled through software. The nominal watchdog time out is 18 ms. A 7-bit postscaler can extend this time to over 2 s if required. A WDT overflow will reset the microprocessor. If it's sleeping, it will wake up and continue execution. To prevent the WDT from timing out, the application must issue a CLRWDT instruction periodically.

SLEEP

A power-down mode is entered when the SLEEP command is executed. The oscillator is stopped, but all I/O remains in its present state. An MCLR will reset the micro, but all of the other system events will wake up the processor and restart the oscillator, allowing execution to continue where it left off. Wake-up events can come from WDT, INT*x*, RB, PSP, TMR1, TMR3, CCP, SSP, USART, ADC, EEPROM/flash memory write, and LVD.

CODE PROTECTION

The code space within a PIC18F*xx*2 is divided into blocks. The first 0x200 bytes are considered the boot block, and the following 0x1E00 bytes belong to block 0. The remaining address space is divided into 0x2000 byte blocks.

Each block can be protected in three ways. The CP*x* bit prevents the code from an associated block from being read by an external source. Because code can be modified by executing code, two additional protection bits are included. The WRT*x* bit prevented a table write to an associated block. The EBTR*x* bit prevents a table read from outside of the associated block. Table reads within the block are always allowed. Protection bits are enabled (cleared) during the programming. After they're programmed, protection cannot be removed from any block unless the chip or block is totally erased.

IN-CIRCUIT

The PIC18F*xx*2 parts offer a few additional and significant features: in-circuit serial programming (ICSP), in-circuit debugging (ICD), and low-voltage in-circuit serial programming (LVICSP).

ICSP is a five-wire connection to the micro: SCLK, SDATA, V_{DD}, V_{SS}, and MCLR (V_{PP}). The micro automati-

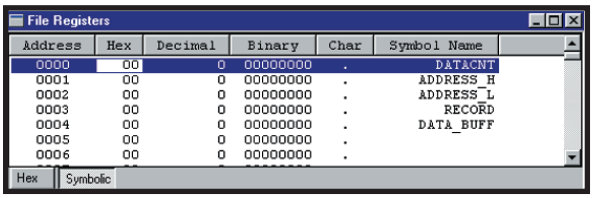


Photo 4—*The file register window shows the RAM locations, including any defined variables. You can create a watch window to hold a group of specific registers. When debugging, limiting the registers of interest will reduce the time it takes to update registers upon a code execution break.*



cally enters ICSP mode at power-up if SCLK and SDATA are held low while V_{DD} rises and MCLR is raised to V_{PP}. The serial format consists of 20-bit instructions, with the first 4 bits identifying a command, and the following 16-bit data to be acted on.

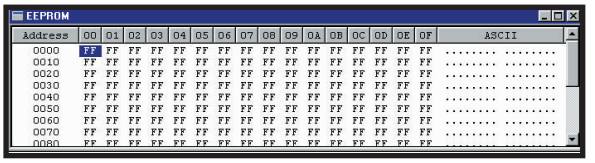


Photo 5—*The EEPROM window displays values stored into any of the 256-byte nonvolatile EEPROM data bank.*

Nine out of the 10 commands are table read and write commands for moving data in and out of code memory. The tenth command (core command) allows actual microcontroller instructions to be executed by the micro. This allows register setup for the table commands. Note that the low-voltage programming (LVP) bit in the CONFIG4L register can only be cleared in ICSP mode. Clearing the LVP bit will prevent the LVICSP mode from being used; therefore, additional programming can only be done in ICSP mode.

For the micro to power-up in LVICSP mode (LVP bit must not be equal to zero), an additional signal PGM is used (this brings the programming connection to six wires). If the PGM signal is held high while the micro is powering up with the same signal requirements as ICSP mode above (with the exception of MCLR requiring V_{CC} instead of V_{PP}), the micro will enter LVICSP mode. The format usage is the same as ICSP mode, but the difference is that the programming voltage V_{PP} isn't needed.

The ICSP interface makes an ideal connection to do helpful debugging. In fact, a special debugging mode is built in to the PIC18F*xx*2 devices. Clearing the BKBUG bit in the CONFIG4L register enables this mode. Background debugging using Microchip's in-circuit debugger (ICD) uses the ICSP interface and requires a 10-byte RAM space, two stack levels, and 512 bytes of code space on the target microcontroller to perform its magic.

ICD2

I've been using Microchip's ICD1 for a long time now. Because I'm a crash-and-burn kind of guy, using Microchip's integrated development environment (IDE software) in conjunction with a flash memory part and the in-circuit debugger really lets me develop in a designer-friendly way (see Photo 2). With this setup, I get to interrogate registers within the working device. This allows me to learn about the foolish mistake I've made that's causing a crash.

The design of the ICD2 integrates a DB9 for those of you who still require RS-232 serial. In addition, the ICD2 has an alternate USB interface. Your target connection is through an RJ-11 jack. Designing an RJ-11 into your PCB will literally make interconnections a snap.

I wish I had an ICD2 available for my SmartMedia project. I guess that's one of the downsides of trying to stay on the cutting edge. Now, with support for the PIC18F*xxx* parts, the ICD2 is destined to be one of those must-have items.

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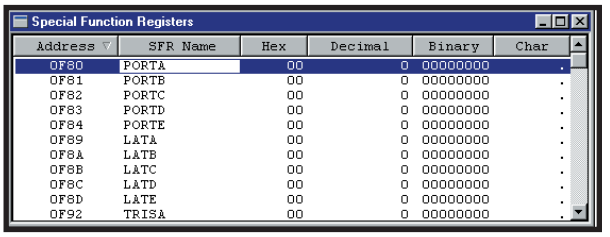


Photo 6—*The special function registers are the interface between the user and all of the microcontroller's core and peripheral functions. The SFRs are grouped by function.*

To use the debugger, you must make sure that your application doesn't use any of the resources required for the debugger. With the resources available to the PIC18F*xxx* parts, this is hardly a problem. The debugger resources use only minimal upper RAM and program memory, in addition to two levels of stack. When your code is written and compiled using the IDE, you can transfer the hex file to the target device either with or without the debug code.

Without the debug code, the target can run your application at reset. With the debug code, you'll be ready to run or step through your application. With the run command, execution can be halted at any time. Step will execute a single instruction and then halt. Whenever the target execution is halted, the IDE is updated with the present value of every register, including the stack space (see Photo 3), RAM (see Photo 4), EEPROM (see Photo 5), and special function registers (see Photo 6).

Also, execution can be halted at a match of address (see Photo 7). With breakpoints, you have control over when the program halts, so you can check register values at that critical point in your application.

BOOT LOADER

OK, you know that these PIC18*Fxxx* parts can reprogram their own code space. How can this be used to update an application? Well, the device can be totally reprogrammed using ICSP. What about the user who may not have programming tools available? The low-voltage programming option along with a simple boot application affords you reprogramming capabilities. You have to use a serial connection on the target system along with a terminal program on the PC.

Microchip's bootload.asm program can be used to accomplish this. Although it was written for use on the PICDEM 2 PLUS demo board (push buttons), it can be altered. In fact, you'll notice it was written for a 10-MHz oscillator and uses a BRG_VAL constant of D'10' (56 Kbps). My PICDEM 2 has a 4-MHz oscillator, so I

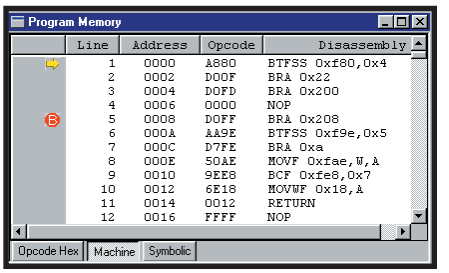


Photo 7—*The program memory window lists the program instructions and indicates which instruction is next to execute. The ICD's breakpoint is also displayed (if it's used). This window shows the bootload.asm program following reset with a breakpoint set at the high-priority interrupt, which is redirected to 0x0208.*

Frustration? No, thanks.
Fun? Yes, please.

NEW VERSION

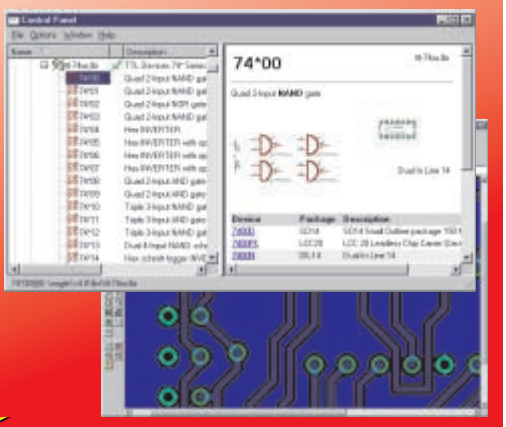
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changed the BRG_VAL to D'12', which at 4 MHz sets up communication for 19.2 Kbps. Note that lowering the oscillator to 3.579 MHz would allow 56 Kbps with a BRG_VAL of D'3'.

The code fills about three-fourths of the boot block from 0x0000 to 0x0200. Both interrupt vectors are redirected from 0x0008 and 0x0018 to 0x0208 and 0x0218. This means that any application that needs to be boot loaded must be ORG'd for 0x0200. If the boot load code finds (in this case) a high on PORTA.4, it will transfer execution to address 0x0200 (i.e., the programmed application). If PORTA.4 is low at reset, the boot load application executes. Figure 8 is a flow diagram of the boot load application. You can use this as a guide for writing your own boot load application. Note that this is the point where the code protect bits really come into play.

Because the boot load application requires less than 0x200 bytes and resides in the boot block, full code protection will prevent inadvertent application-controlled code memory erasure and writes in this block. At the same time, it allows the boot load application to erase and rewrite the remaining blocks of code memory.

GETTING TOOLS

I've written and debugged plenty of code with Microchip's free simulator (part of the IDE). But, if you wish to put that code into a device, you'll need some kind of programmer capable of handling the device you are designing with. There are many PIC programmers on the 'Net, but few can boast about being able to program the newest PIC18F*xxx* devices. Refer to the microEngineering Labs and New Found Electronics web sites to learn more about two programmers (i.e., EPIC Plus and WARP-13) that cost less than $100.

Microchip has a complete line of tools, including the free IDE software suite and reasonably priced development and production programmers, emulators, and debuggers.

I've been told that Microchip has put together a small kit of parts for the contest. My scouts indicate that it includes the newbie PIC18F252 micro, in addition to a V_{OUT} temperature sensor (TC1046AVNBTR), op-amp (MCP6022-I/P), ADC (MCP3302-BI/P), digital potentiometer (MCP42100-I/P), and V_{REF} (MCP1541-I/TO). How cool is that? So, all you designers out there get ready, get set, dash for flash cash.

Jeff Bachiochi (pronounced BAH-key-AH-key) is an electrical engineer on Circuit Cellar*'s engineering staff. His background includes product design and manufacturing. He may be reached at jeff.bachiochi@circuitcellar.com.*

SOURCES

ICD1/2, MCP1541/3302/42100/6022, PIC16C6*x*/7*x*, PIC18F*xx*2, TC1046, PICSTART PLUS, PROMATE II
Microchip Technology, Inc.
www.microchip.com

EPIC Plus programmer
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SILICON UPDATE

Tom Cantrell

Watch Me Pull A Rabbit Out of My Hat



It's clear that the Rabbit 3000 is an improved 8-bit micro. But how "new" is it? In this article, Tom takes a look at the micro's history, focusing on the evolutionary track leading up to its current features.

As you'll see, no one can argue that the new and improved Rabbit 3000 8-bit micro doesn't live up to the latter expectation.

How new it is, though, is another question. The silicon may be hot off of the assembly line, but the 3000 has roots that go way back.

Flash back to the mid-'70s. Messrs, Faggin, Shima, Mazor, et al of Intel sit down to craft a follow-on to their 4004 calculator chip and 8008 terminal chip. The result—the 8080—is a big hit in spite of management's skepticism. After all, companies like IBM and the "BUNCH" (Burroughs, Univac, NCR, CDC, and Honeywell—remember them?) don't sell that many computers, so just how many computer chips can we expect to unload?

Meanwhile, those cowboys in Texas are making hay with their 6800. The 8080 crew goes to their battle stations ready to craft a new version of the 8080 that will send the Motorola horse to the glue factory for good.

But wait, Intel management is starting to get it about these newfangled microchips. From on high, word comes down that it's 16 bits or bust. Yeah, we'll let you make a new 8080, which subsequently appeared as the 8085, but it's just a holding action until we get our 8086/88 act together.

Faggin, Shima, and the others aren't happy. Be the 16-bit and beyond world as it may, there's still great untapped potential for better 8-bit chips. A new company, Zilog, and a new chip, the Z80, are born.

In the late '70s and early '80s, while Intel and Motorola battled for dominance in the nascent PC business, Zilog was cranking 8-bit Z80s and peripheral chips into embedded applications like there was no tomorrow.

If Zilog had stayed focused, the story might have turned out differently. But instead they repeatedly fell victim to all manner of self-inflicted, ill-conceived product strategies and corporate machinations. The founders left, an oil company took over, the Z8000 choked, and, though sales continued coasting along, Zilog fiddled while the Z80 burned.

The next chapter in the saga comes from overseas where Hitachi, looking for a way out of a messy love-hate relationship with Motorola, came up with the HD64180, a spiffed-up Z80-compatible CPU with handy built-in glue logic and I/O functions. Subsequently, Hitachi moved on with their H8 architecture, and Zilog remains as the source for the Z180 and it's derivatives along with their own eZ80 next-generation design (*Circuit Cellar* 139).

I suppose with all of the excitement over the years, it's no surprise that a long-time Z80/180 customer, the aptly named Z-World, decided to take matters into their own hands. Enter Rabbit Semiconductor, a sister company created to carry forward the 20-plus-year legacy of the 8080/Z80/180.

And lest you think a legacy is more like baggage, just remember that while new players (e.g., the Atmel AVR and aforementioned Hitachi H8) are starting to get traction, the 8-bit market is still well served by long-in-tooth classic architectures.

RABBIT 3000

Fortunately, the history and basic features of the Rabbit design are excellently documented in the pages of *Circuit Cellar*, including words of wisdom from one of chip's developers, Monte

Dalrymple, and a five-part article series from our own Fred Eady. [1, 2] You can check them out (not to mention the copious documentation on the Rabbit web site) for the inside story.

Perhaps the Rabbit 3000 is easiest to understand as the next step in the evolution of the '80 species (see Figure 1). At each chip along the way between the 8080, Z80, '180, and now the Rabbit 3000 (and EZ80), designers figured out ways to add new and improved features while retaining the essence that made the predecessor popular in the first place.

On this historic scale, basic evolutionary trends can be seen in the instruction set, performance, peripherals, glue logic, and interfacing. As you examine each trait, you can see how the Rabbit Semiconductor 3000 continues along the trajectory set by the '80 chips of yore.

NO-RISK CISC

The Rabbit 3000 is by no means object-code compatible with the Z80/180, because a number of opcodes were deleted or moved around. I don't really consider this a problem and indeed argue that the ostensible virtue of object-code compatibility is overblown in the embedded world.

For embedded applications, you almost always have to change your software when you use a new chip. As a practical matter, with software defining so many of an embedded product's features, the scenario is usually, new chip = new product = new features = new software.

And even if you really want the new chip to run old software, you're going to have to tweak the files at least a little bit. For instance, the Z180 is considered object-code compatible with the Z80 because all of the opcodes are the same. But still, to upgrade from a Z80 you would have to add some '180-specific initialization code and be ready to hack around subtle changes in timing.

What matters isn't compatibility, but rather familiarity. Z80/180 users will feel right at home with a Rabbit 3000, and it's easy to discern the relatively few significant changes.

One of the novel features added to the Z80 was an extra register bank, which is a concept that remains popular to this day. The premise behind the scheme was that it would allow faster interrupt response by virtue of simply switching between register banks rather than pushing and popping all of the registers on and off the stack.

This makes a lot of sense in principle, but how about in practice? As someone who's dabbled a fair bit with Z80s and Z180s over the years, I personally can't recall ever using the alternate register set in this manner, or in fact at all.

Similar experience presumably inspired the Rabbit designers to make better use of these valuable, underutilized regis-

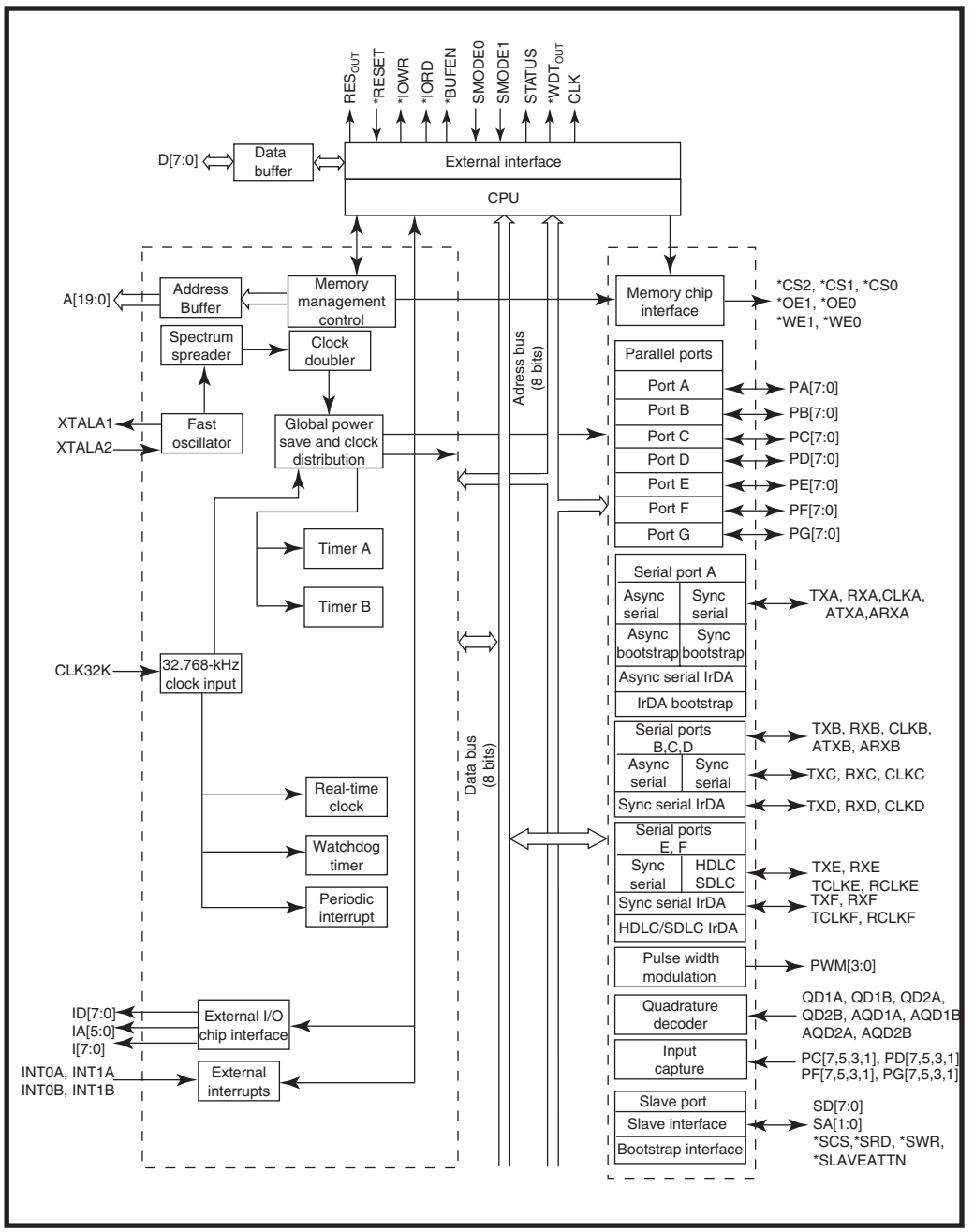


Figure 1—*The Rabbit 3000 is the latest in a long line of '80 chips that goes all the way back to the dawn of micros.*

ters. Instead of being restricted to just exchanges, the alternate registers can be accessed directly by using an alternate destination (ALTD) prefix (e.g., via loads and stores and pushes and pops).

Another use of the prefix trick is with I/O, which is handled in a different manner than before. On the earlier Z80/180 models, I/O devices were accessed with unique opcodes (IN, OUT, and variations). I'm not sure that this was ever a good idea to begin with, but it's certainly archaic at this point. Instead, for the Rabbit 3000, an I/O prefix (IOI for internal and IOE for external I/O) can be used with any conventional memory access instruction to cause the memory address to be interpreted as a 16-bit I/O address.

Going way back, the 8080 did have an advantage over other 8-bit chips at the time; it had the ability to perform some 16-bit operations (e.g., load, store, add, etc.), albeit a limited set. Rabbit has boosted the 16-bit capability significantly to include, for example, shifts and other logical operations such as AND and OR.

There's also the interesting new BOOL instruction that works with the 16-bit HL register pair, the de facto 16-bit accumulator. It's really simple: `BOOL HL` sets HL to one if the contents of HL are nonzero and leaves it zeroed otherwise. This proves useful to the C compiler for handling conditional evaluation; it also provides the basis for short instruction sequences that perform 16-bit signed and unsigned compares.

The traditional vector table interrupt system is enhanced with a four-level priority scheme. The worst-case interrupt latency for the highest priority is just the length of the longest instruction (or longest sequence of uninterruptible instructions), which is approximately 20 clocks.

The MMU is tweaked to manage the 1-MB address space differently than before. The basic notion that a 64-KB portion of the physical memory is always present remains the same. However, the details have been changed to better suit the memory management strategy employed by the C compiler.

PECK-O-PERIPHS

The Rabbit 3000 has 128 pins to play with. That's 28 more than the Rabbit 2000, twice as many as the '180, and more than three times the 40-pin originals.

Two-dozen of them are devoted to power and ground, notably because of the fact that separate power supplies (though both 3.3 V) are used for the processor core and I/O. That minimizes the leakage of EMI generated by the former out of the latter. Note that inputs are 5-V tolerant, which is something that's still useful in the embedded world.

The remaining pins are divided between the external memory bus and various I/O functions.

As for the former, the Rabbit 3000 is designed to use standard byte-wide memories, typically SRAM and flash memory. The 20-bit address bus and 8-bit data bus are supplemented with the familiar control lines (*CS, *OE, *WE) for direct no-glue connection to as many as six commodity memory chips.

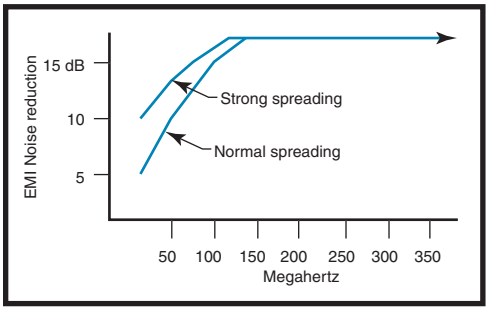


Figure 2—*Three spread-spectrum settings (i.e., off, normal, and strong) are available. Spreading interference around isn't the same as reducing it, which makes the technique a bit controversial, though it no doubt facilitates meeting FCC regulations.*

Note that support for dynamic RAM, which made sense in the old days when DRAM densities were measured in kilobits, is arguably no longer relevant for 8-bit chips and has been eliminated.

The on-chip I/O functions are given seven 8-bit ports (A through G) to play with. As usual, particular ports can take on dedicated I/O functions or be used as generic parallel I/O.

If you've ever wished you had an extra serial port (and who hasn't?), the Rabbit 3000 is the chip for you with a whopping six on tap. Now, it isn't likely that you'll need to use all six as UARTs (with IRDA format thrown in for good measure), so four of them can work as SPI clocked serial ports instead. This is especially handy for using multiple clocked serial peripheral chips without having to multiplex the connection externally. Furthermore, two of the ports even include SDLC/HDLC capability for applications that need to connect to the wider world of LANs and WANs.

Another I/O option is a slave interface comprised of an 8-bit bidirectional port and a few address and control lines. This provides a handy way to connect a Rabbit 3000 to another processor, which could be another Rabbit 3000, but doesn't have to be. A simple dual-port register mechanism makes it as easy to talk to the CPU as any conventional peripheral chip.

Historically, external I/O and memory chips all would connect to the same data and address

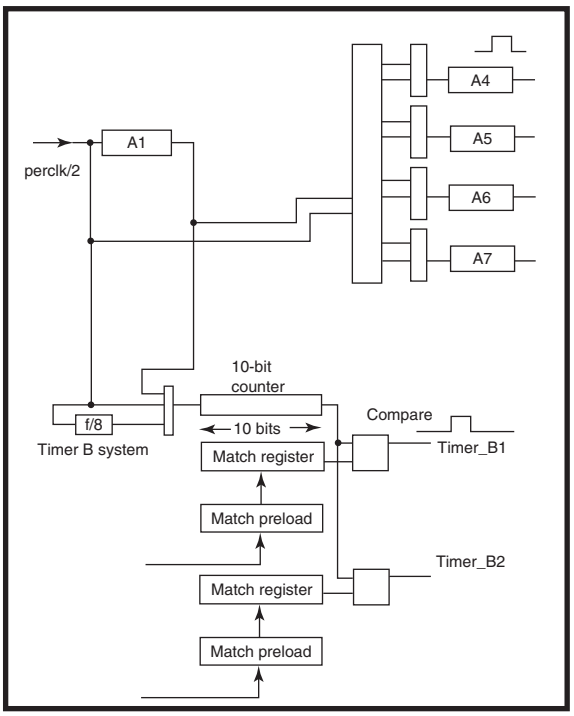
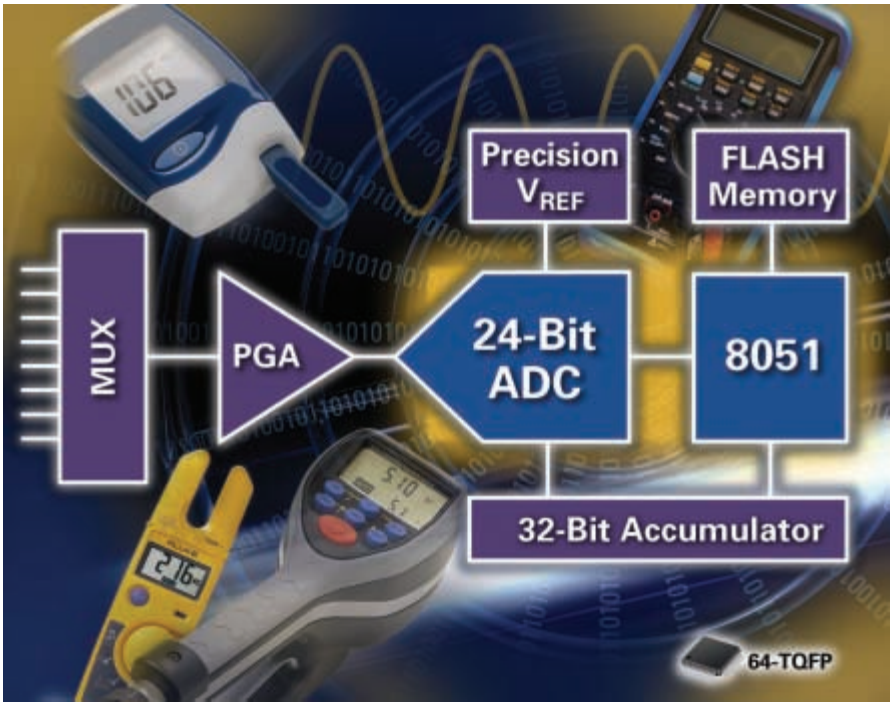


Figure 3—*Besides handling the mundane chores such as serial data rates, the Rabbit 3000 timer subsystem goes well beyond the typical MCU's reload timer with features like high-speed input capture, PWM, and quadrature decode.*

Lowest noise precision data acquisition system on a chip.



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lines. That option is available for the Rabbit 3000, as well; however, the chip also offers an auxiliary I/O bus mode that splits I/O operations onto their own 8-bit data/6-bit address bus.

This provides benefits that may prove compelling in certain designs. For example, if top performance is your goal, you'll likely find (as usual) that memory access time is a concern. Moving I/O devices onto their own bus reduces capacitive loading on the memory bus that would otherwise slow things down.

Similarly, although the Rabbit 3000 can tolerate 5-V inputs, a particular 3.3-V memory chip might not be so obliging. If mixing 3.3-V memories and 5-V I/O chips on the same bus proves to be problematic, then splitting the busses is the way to go.

Finally, practical product evolution and packaging considerations often call for an I/O bus or backplane that is physically accessible and expandable. Both of these criteria can compromise critical memory bus performance and raise EMI concerns. With the split bus

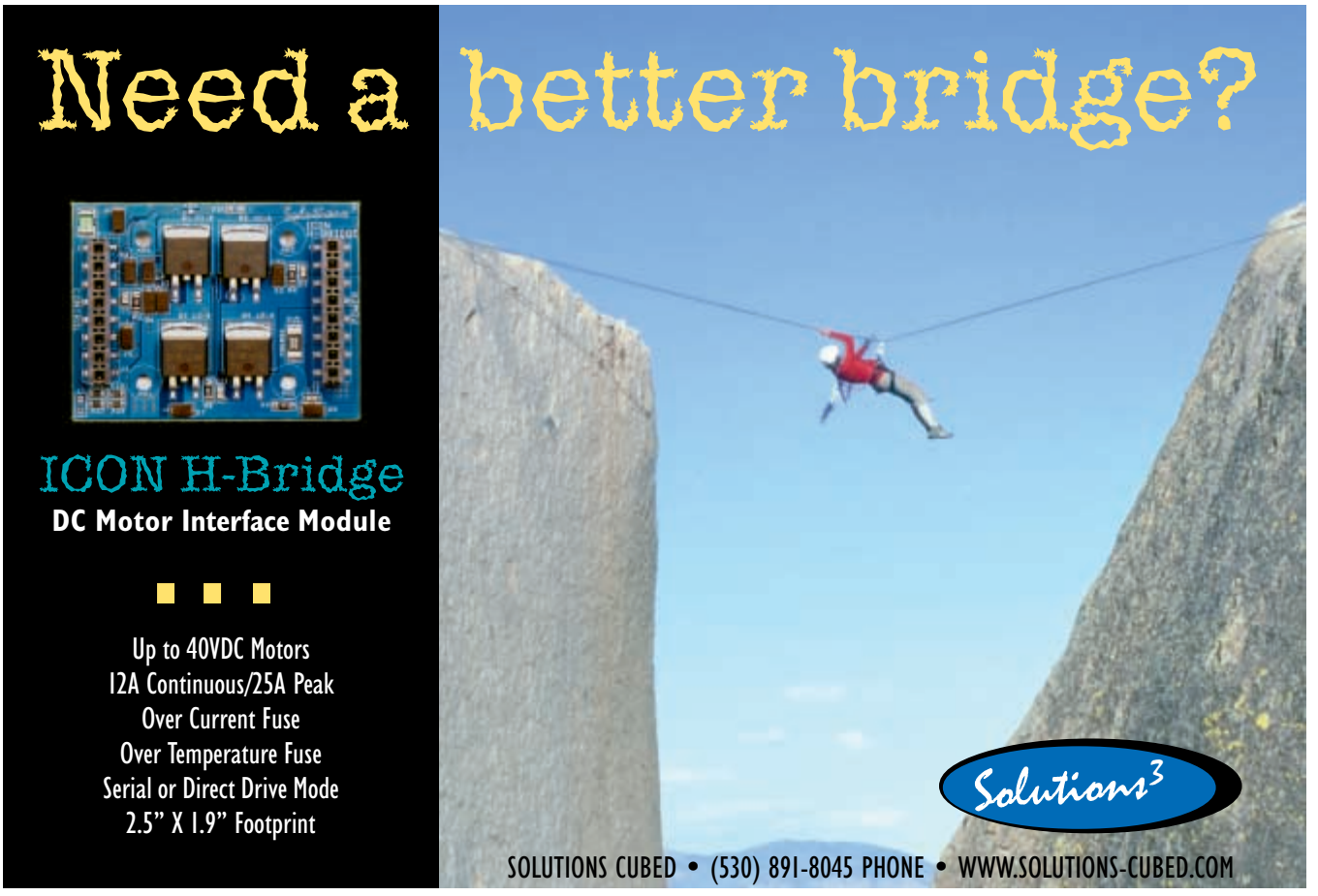
Listing 1—*Language purists will have none of it, but I like the fact Dynamic C is custom tailored to the hardware with language extensions for I/O, interrupts, memory management, and, in this case, multitasking.*

```
main()
{
      initPort();                    //Initializes port G only
      while (1)
      {
         costate
         {                           //DS1 LED
             DS1led(ON);             //On for 50 ms
             waitfor(DelayMs(50));

             DS1led(OFF);            //Off for 100 ms
             waitfor(DelayMs(100));
         }

         costate
         {                           //DS2 LED
             DS2led(ON);             //On for 200 ms
             waitfor(DelayMs(200));

             DS2led(OFF);            //Off for 50 ms
             waitfor(DelayMs(50));
         }
      }
}
```

Operation/program	Dhrystone 1.1 1000 loops per second	Whetstone 1000 loops per second	Sieve (milliseconds)
Rabbit 3000 at 50-MHz Dynamic C	6570	813	53
AMD 188ES at 40-MHz Borland 3.31 C	3603	61	120
Zilog eZ80 at 40-MHz Zilog C compiler	2914	20	158
Dallas DS80C320 (8051) at 33-MHz Keil C	1251	140	160
Phillips 80C51 at 33-MHz Keil C	598	61	350

Table 1—*As usual, a simple benchmark summary raises as many questions as it answers. Nevertheless, it's clear that the combination of the Rabbit 3000 and Dynamic C is no tortoise when it comes to floating point.*

Application timing tasks are well served by a plethora of clocks, counters, and pins. In this case, a picture is easily worth the thousand words it would take to describe all of the options (see Figure 3). It's definitely a sophisticated and high-resolution setup compared to run-of-the-mill 8-bit micros.

A registered output option means even parallel output gets precise. You can configure output port updates to trigger off timers for superior timing precision without the CPU having to babysit the port in software.

scheme, the relatively quiet auxiliary I/O bus can act as the backplane for external add-ons, while the faster and noisier memory bus can be kept tight and light (i.e., in close proximity with the CPU and minimally loaded with only a few memory chips).

TIME TRAVELER

The Rabbit 3000 has a lot of features in the time domain, starting with the clock pins. Make that clocks, because the chip provides connections for separate low- (32.768 kHz) and high-speed (up to 30 MHz) inputs. An on-chip doubler boosts the clock rate to the 50-MHz-plus maximum specification.

The low-speed input (i.e., watch crystal) drives the real-time clock (implemented as a 48-bit counter with dedicated battery backup pin) and watchdog timer while the high-speed clock drives the processor and peripherals.

The low-speed clock can also drive the processor and peripherals, which is the basis for the low-power Sleepy mode that can throttle the CPU down to almost 2 kHz (i.e., 32.768 kHz divided by 16). Slowing the clock to reduce CPU power consumption isn't a new concept, but Rabbit shows attention to detail with short and self-timed chip-select options that minimize memory chip power consumption as well.

EMI reduction is a hot topic that I predict will only get hotter. The Rabbit 3000 is one of the first micros to incorporate spread-spectrum clocking as an option. When enabled, pseudo-random jitter is automatically injected into the clock, spreading the radiated noise (see Figure 2).



ONE-STOP SHOPPING

Yes, the Rabbit 3000 is a neat chip, but there are a lot of those on the market to choose from these days.

What I really like about the Rabbit 3000 isn't merely the chip itself, but the entire package—documentation, tools, libraries, and so on—that make for a successful project.

Notably, Rabbit gains a lot of synergy by virtue of supplying both the chip and C compiler. Way back when, this was common, but it fell out of favor as chip companies' afterthought in-house compilers fell to superior third-party offerings.

But remember that Rabbit/Z-World was doing C compilers long before they did their own chip. The result is a fine mesh between hardware and software that's rare to find in an era of promiscuous couplings between standard tool suites ported to any and all chips.

When it comes to performance, a good compiler can do wonders. Even though the Rabbit 3000 is a frisky chip, it is, after all, still a CISCy beast. Instructions can easily balloon into double-digit clock cycles, depending on how baroque they are (i.e., fancy addressing modes, multiple memory accesses). Nevertheless, even with all of the usual benchmarking caveats, it's safe to say the Rabbit/Z-World compiler brings it on, especially when it comes to floating point (see Table 1).

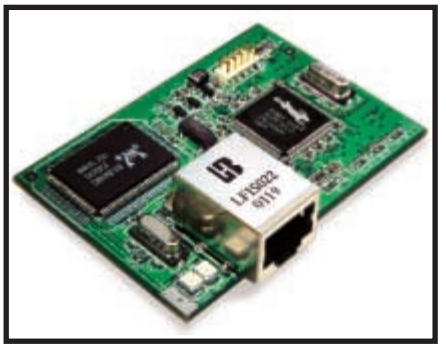


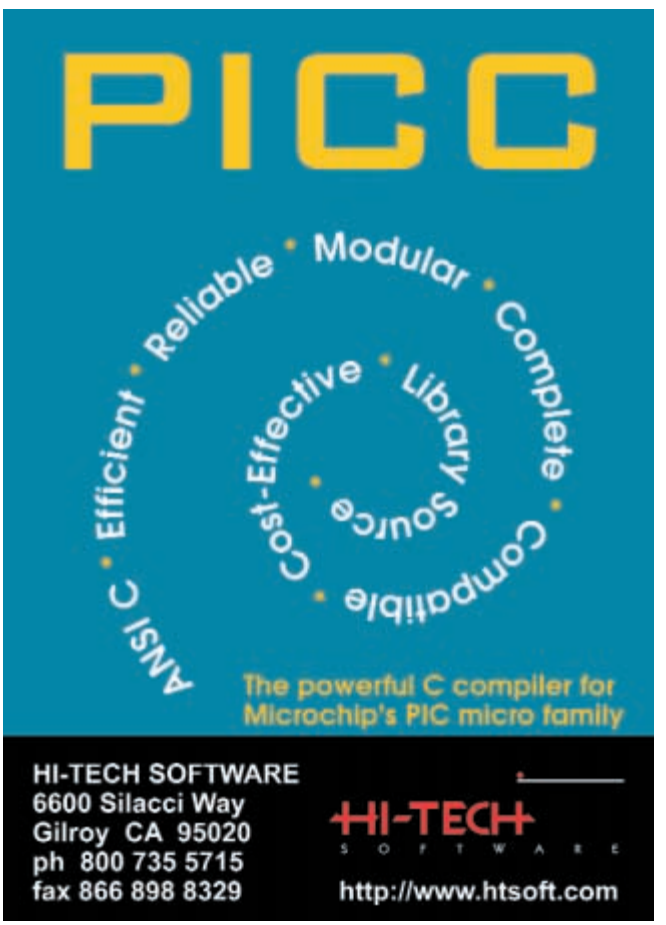
Photo 1—*The Rabbit Core Module (RCM) 3000 serves as the basis of the $299 development kit. With built-in Ethernet (using a Realtek PHY) and up to 512 KB each of flash memory and SRAM, it's a natural for embedded web applications too.*

Even if you don't care about performance or Rabbit's claims, there are other big advantages to one-stop compiler and chip shopping. Have you ever struggled to make a C compiler deal with an interrupt? Access an I/O device? Store a variable in flash memory rather than RAM? Perform multitasking (see Listing 1)? For C on the Rabbit, these are all built-in and blessedly easy to use.

I had the chance to plug and play with the Rabbit 3000 development kit, which I found to be polished, user-friendly, and a relative bargain at $299, considering that the C compiler is included. As you can see in Photo 1, the kit is based on the Rabbit Core Module 3000 (RCM), a viable contender for embedded Internet applications thanks to the built-in Ethernet interface and royalty-free (source code is included) protocol stacks.

Although I'm not in a position to make an authoritative statement about correctness and performance, the Rabbit networking support feels relatively comprehensive, credible, and confidence-inspiring. That's





more than I can say for a lot of the mini-me network stuff I run across, too much of which borders on snake oil. Kudos to Rabbit Semi for offering more hope and less hype when it comes to putting embedded gadgets on the I-way.

Not that Rabbit 3000 support is an entirely in-house proposition. There's also a chip-specific port of MicroC/OS-II, the popular RTOS written by Jean Labrosse, and a C compiler from Softools. [3]

KEEP MOTORING

About 25 years ago, I was running machine language blink-em programs on my beautifully LED-laden IMSAI 8080. That puppy must have weighed 50 pounds, thanks largely to the 100-W boat anchor power supply. All that big iron got you was barely more than 1 MHz and few kilobytes of RAM and ROM.

Today, I'm looking at a few square inches, a couple of ounces, and less than 1 W delivering MIPS and memory, not to mention I/O, that the old IMSAI could have only dreamed about. And whether you're using C or ASM, even the most die-hard designer must admit it's a step up from toggling front-panel switches.

Yeah, there have been plenty of twists and turns, not to mention a few fender benders, along the Route '80 way. But there always comes a time when I look forward to zooming up the next on-ramp in a shiny new chip. Thanks for the ride, Rabbit.

Tom Cantrell has been working on chip, board, and systems design and marketing for several years. You may reach him by e-mail at tom.cantrell@circuitcellar.com.

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[2] F. Eady, "Rabbit Season," Parts 1-5, *Circuit Cellar* 123-127.

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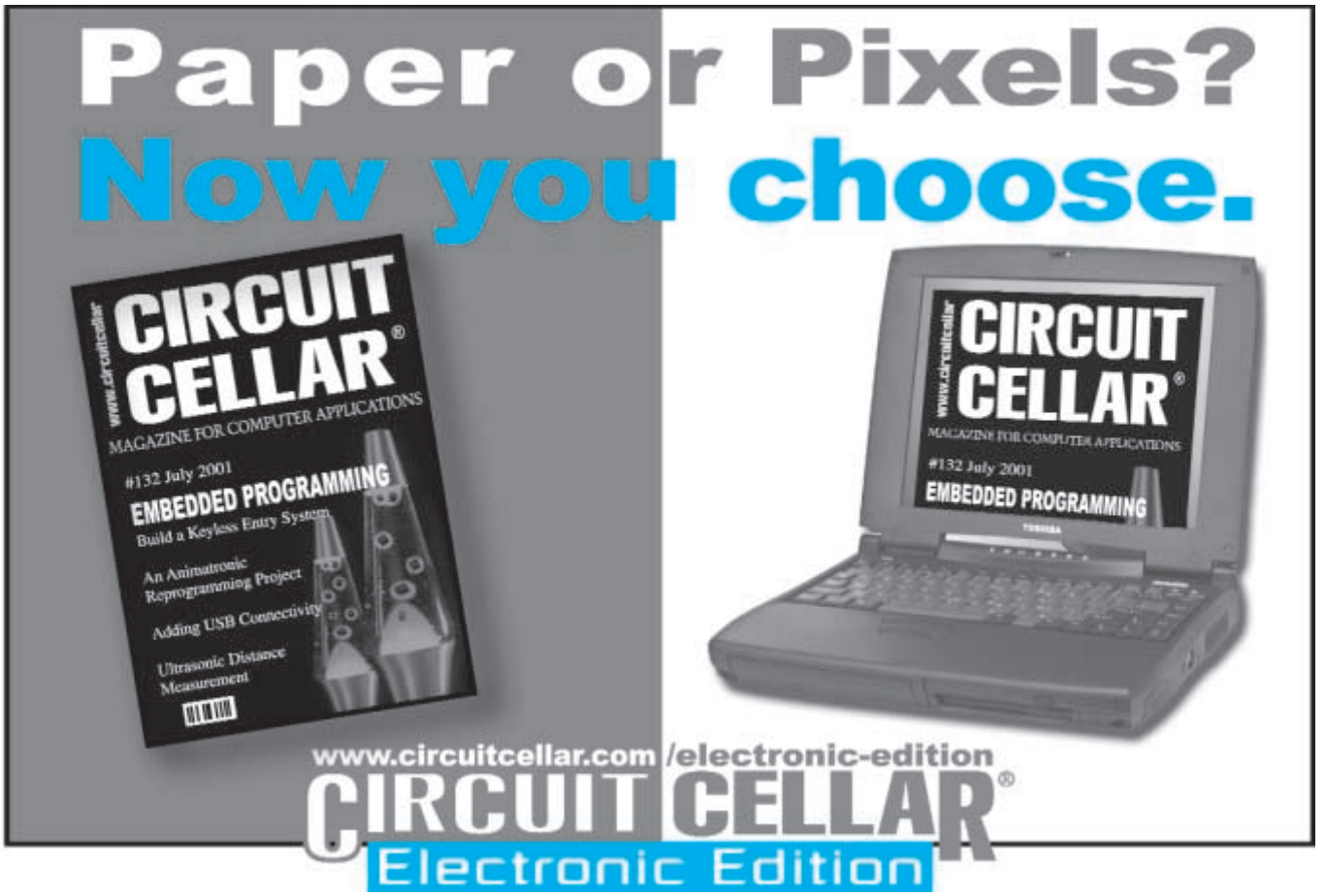
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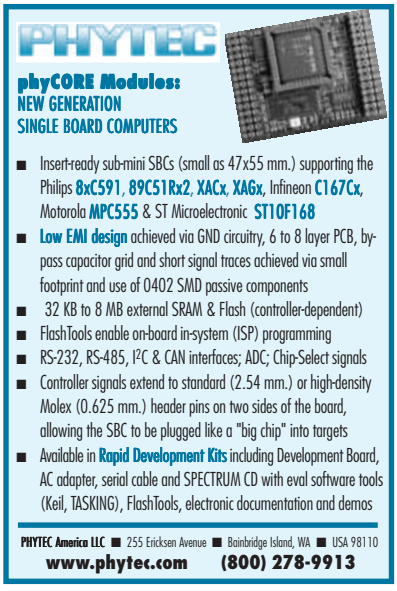
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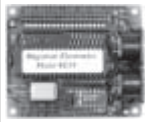
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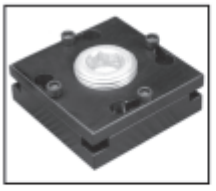
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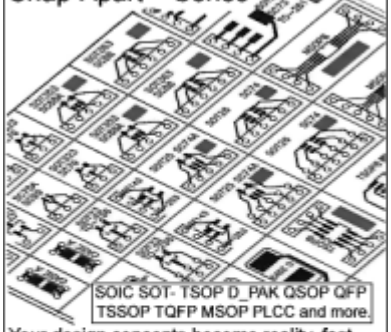
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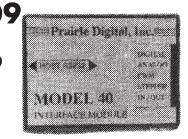
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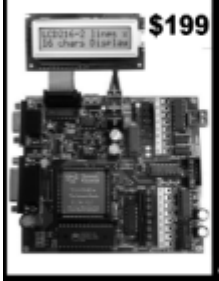
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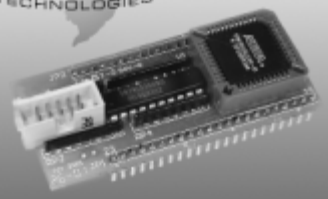


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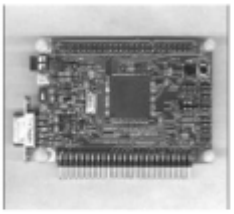
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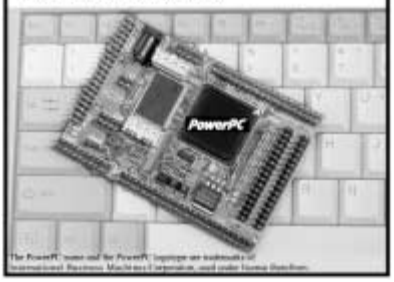
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The LAB-X1 is a pre-assembled experimenter's platform. It provides a testbed containing most of the circuitry commonly used with PICmicro microcontrollers (MCUs). Possible applications include calculator, voltmeter, LCD backpack, tone dialer, and RC servo control. The LAB-X1 can run programs written in Assembly, C, PicBasic, or PicBasic Pro. (requires 40-pin MCU)

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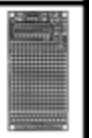
EPIC Plus PICmicro Programmer



The pocket-sized EPIC Plus Programmer quickly and easily programs the following PICmicro microcontrollers: PIC12Cxxx, 12CExxx 14C000, 16C505, 16C55x, 6xx, 7xx, 84, 92x, 16CE62x, 16F62x, 7x, 8x, 87x, 17C7xx, and 18Cxxx (some MCUs require an additional adapter). Interactive software included for Windows and DOS. Requires two 9V batteries or AC adapter (not included).

Bare PCB w/software - **$34.95**, Assembled - **$59.95**
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PICProto Prototyping Boards - $8.95 to $19.95



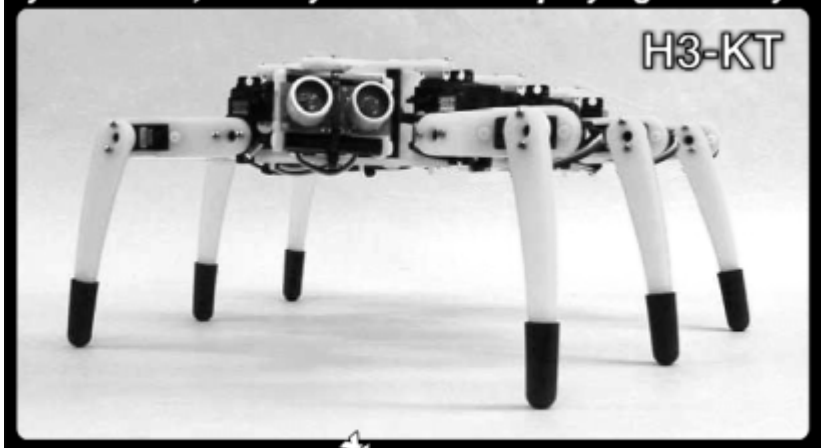
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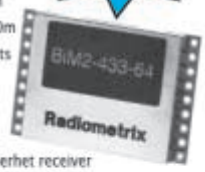
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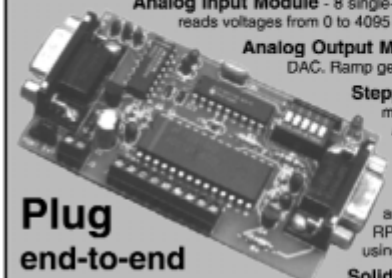
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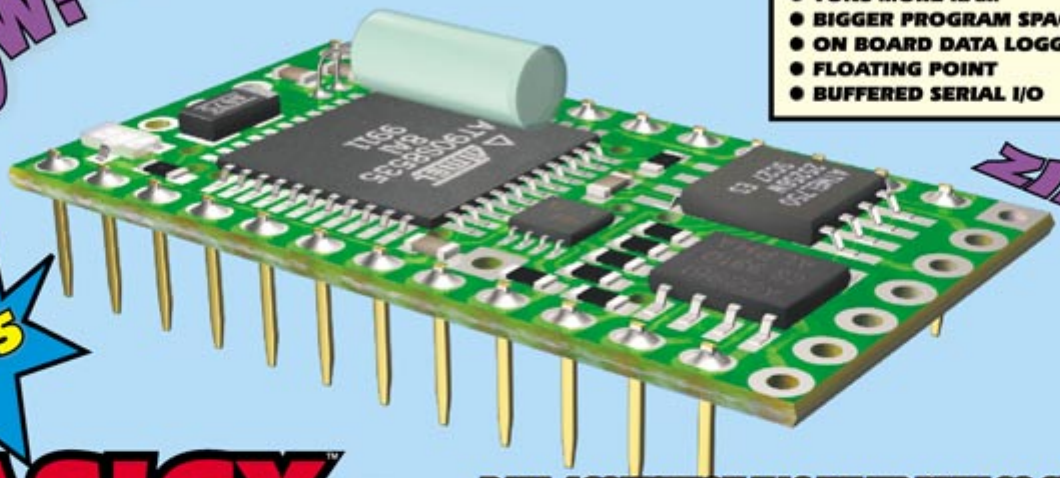
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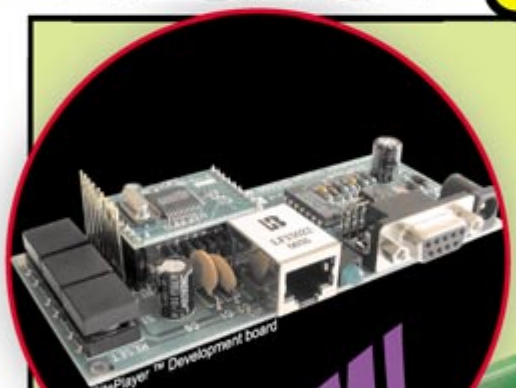
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Linguini with Clam Sauce



As most of you know, I lead a fairly reclusive lifestyle. Yes, by central Connecticut's standard of shopping malls and condos, we rustic upstate Yankees live in the boonies among the trees. Of course, someone from Washington state would laugh at what we call the woods. On the other hand, a New York City native living only 100 miles away would think he was on a wilderness trek when visiting our part of Connecticut. It's all relative.

While I live in a wooded area, about the only thing around here that's really rustic are the trees. Our house is a hexagonal California redwood contemporary that exemplifies the personal style and expression of a mad scientist with carpentry tools. Think of a wooden octopus and you have a reasonably accurate description of the ground plan. It would look out of place next to a traditional New England saltbox or Cape Cod, but, isolation has its advantages (very few neighbors). And, to me it's always been the official Circuit Cellar.

Being an engineer whose expertise is embedded process control has left its mark. Our home contains about as much copper as wood. There are wires everywhere. The security system connects to the home control system; the driveway sensors talk to the video and security system; the video and entertainment electronics talk to the home control and lighting system, and so on. Everything was mostly direct-wired, so the result is one gigantic wiring maze.

In all the time I've lived there, I've installed computerized controls on everything except the heating and air-conditioning systems. It's not that I can't instrument them, but rather that I've had little success proving enough tangible benefit to justify complicating an otherwise uncomplicated environmental system.

We just built a large kitchen addition, and I thought I would try it once again. As the contractor was constructing the kitchen, I added what seemed like another mile of copper for temperature sensors, heat and vent controls, and a shade canopy extension. In combination with sensors detecting outside temperature and humidity, I presumed I could calculate heating and cooling ramps and anticipate demand more efficiently. Then, I could tie it all into the home control system and let it control everything.

When the crew finished, I was ready to begin doing my thing. Typically, that means blowing holes in the walls for the control devices, kludging control schemes for equipment that wasn't originally intended to be computerized, and stringing yet more wires. Ten years ago this would have been a no-brainer. I would have jumped right in and then written articles about the electronic transformation. Today, I'm a little more practical about such adventurous ideas. This time, I decided to make linguini with clam sauce (it's a kitchen after all) and think about it for a while. In fact, I decided to cook for a couple of months.

It was déjà vu all over again. I could rip apart the whole place and call it "computerized," but in this particular Connecticut location, I doubt that I'd see a significant advantage over traditional controls. The benefit provided by trees that give shade, extending the shade canopy, and opening a few windows seemed to be adequate for all but extreme weather. The real extremes I hadn't encountered before, however, were the ones the kitchen created.

Kitchen vent hoods have reached new levels of performance. While they certainly exhaust smoke and smells efficiently, it's what they don't tell you in the kitchen store that you have to be careful about. When my 1300-CFM blower winds up, if it hasn't sucked everything including the furnace out the vent, somewhere between the first and second flips of the steak au poivre, it's dropped that cozy kitchen about 30° in the middle of January. Of course, the opposite can be true in the summer. Turning on a six-burner Viking stove is about the same as firing up a medium-sized furnace in the middle of your kitchen. Ultimately, the environmental control solution isn't a duel between Linux and Windows CE. The solution is straightforward: Add about 60′ of baseboard heating and a 2-ton air conditioner.

The primary lesson I learned during the couple of months of gathering data was basically that I like to eat too much. Being able to claim that it's all computerized won't make it a better place to cook and entertain. As for the environment, it seems that the extremes are the dominate issue, and centralized environmental control wouldn't add any advantage over the distributed individual heating and cooling controls standard with conventional installations. Every time I've tried to justify it, I've come away with the same answer: In this tech-crazy world it's hard to admit it, but, if it ain't broke, don't fix it.



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