#139 FEBRUARY 2002

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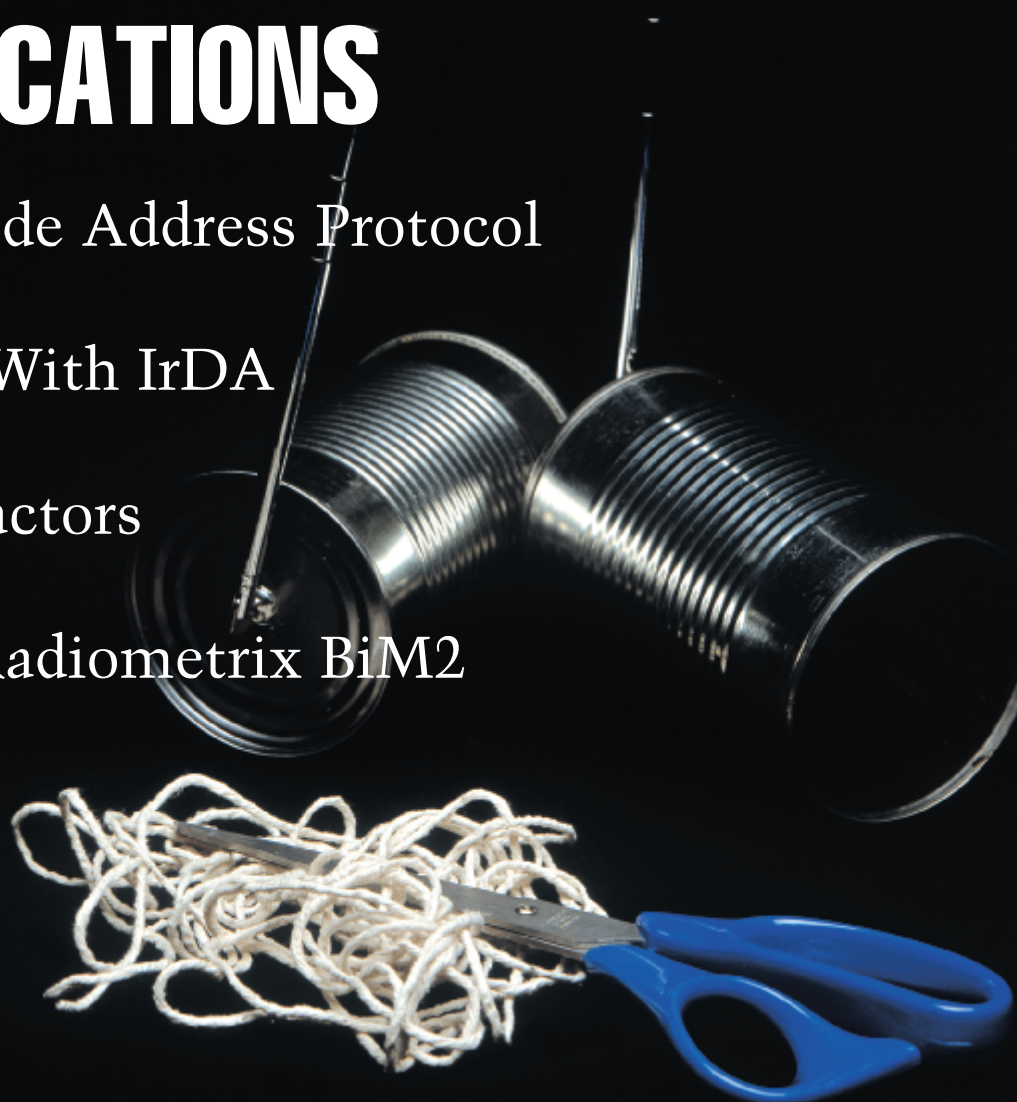
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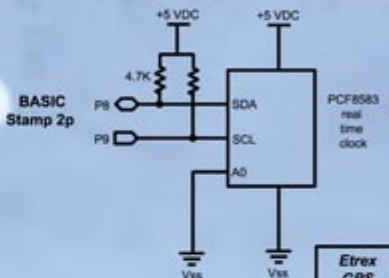
It's the unique applications and ease of use that have put the BASIC Stamp in all corners of the world. With over 50,000 customer web links and millions of BASIC Stamps in the field, chances are you can find an example of the project you want. Below is a sampling of applications available from our web site (www.parallaxinc.com).



TIME



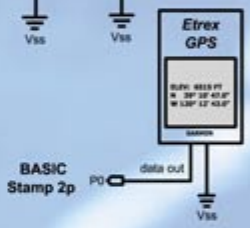
Project: Set and measure time with the Phillips 8583 I²C protocol real time clock chip
Hardware: BASIC Stamp 2p module and Plus Pack
Application: www.parallaxinc.com/pluspack



LOCATION



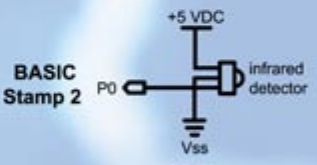
Project: Log latitude and longitude records from a commercial GPS unit in EEPROM every two seconds
Hardware: BASIC Stamp 2p module and Etrex GPS
Application: www.parallaxinc.com/GPS



INFRARED



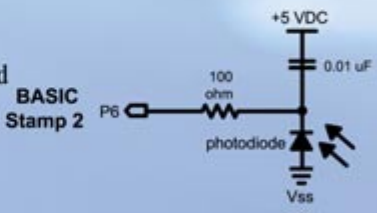
Project: Read infrared remote control signals from a Sony-compatible handheld controller or detect nearby objects
Hardware: BASIC Stamp 2, universal remote and an infrared detector
Application: www.parallaxinc.com/infrared



LIGHT



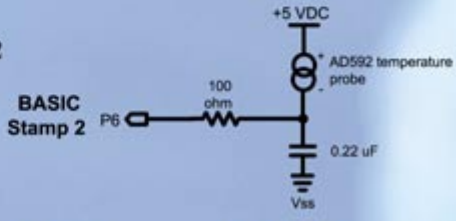
Project: Measure and calibrate light levels using the sun and a photodiode in a resistor/capacitor circuit
Hardware: BASIC Stamp 2 and photodiode
Application: www.parallaxinc.com/earthmeasurements



TEMP.



Project: Construct a mini probe with an Analog Devices 592 to measure micro-climate and fluid temperatures
Hardware: BASIC Stamp 2 module and AD592 in resistor/capacitor circuit
Application: www.parallaxinc.com/earthmeasurements



Visit our website to view the above projects and their corresponding products. Also, take advantage of our free documentation and software downloads.

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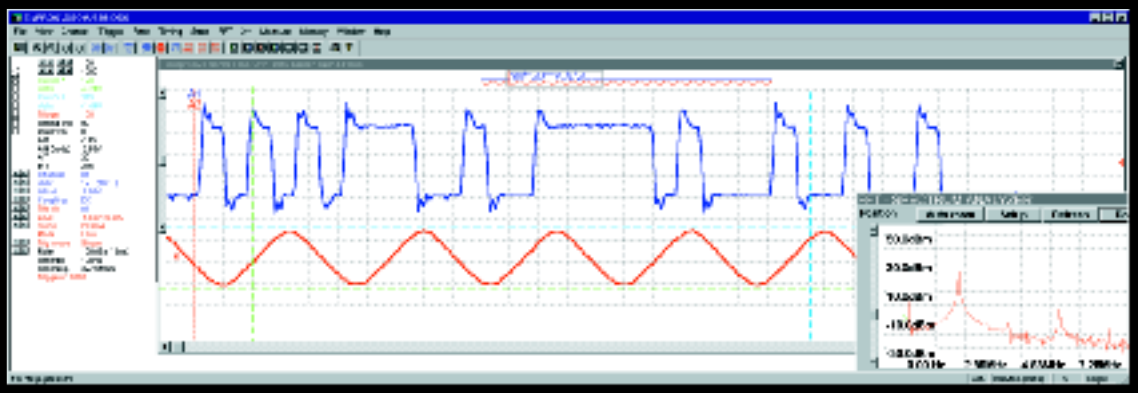
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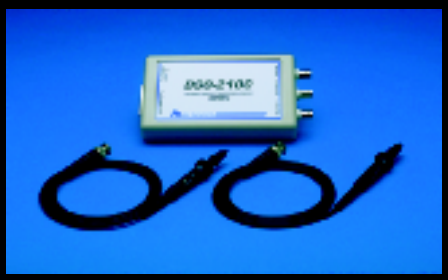
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Digital Oscilloscopes

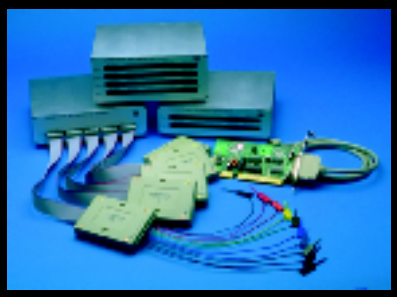


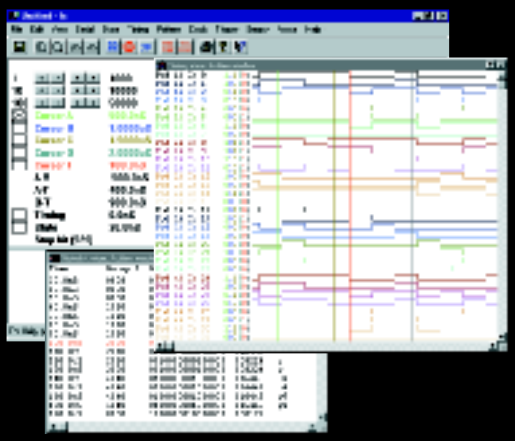
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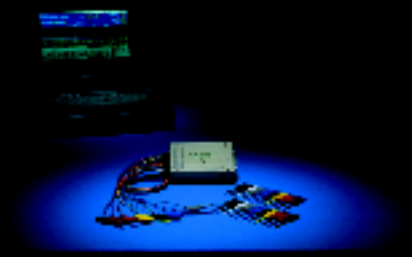


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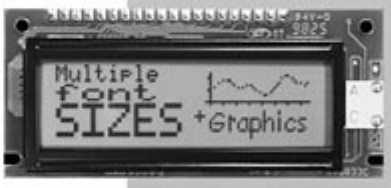
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RESOURCES

Each month *Circuit Cellar*'s Resource Links provide helpful links and information on a variety of featured topics.

- **Stream Control Transmission Protocol**
  Brant Schroeder
- **Organic Light Emitting Diodes**
  Brant Schroeder

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Circuit Cellar Online offers articles illustrating creative solutions and unique applications though complete projects, practical tutorials, and useful design techniques.

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DO YOU EXCEL IN ELECTRONICS?

Part 1: Learning the Basics of Excel
by Aubrey Kagan
Although you usually hear of Excel being used for business or home finances, in his series, Aubrey shows us that engineers can benefit by using the program to make the design process easier. This month, he takes us through the basic techniques of Excel, including naming cells, look-up tables, costing a product, and more. January 2002

GO

SCOPE IT OUT

Building an MPC555-Based Oscilloscope
by Daniel Mihalik
With a detailed description of how to use the QADC and SCI on the MPC555, Daniel shows us how to create our own simple oscilloscope. He even includes the source code needed for the design. In the end, we wind up with a useful debug tool. And that's just the beginning. With a few software upgrades, the opportunities are limitless. January 2002

GO

GETTING INTO A ROUTINE

Setting Up an Integer Print Routine
Lessons from the Trenches—*by George Martin*
As you know, the slightest bump in any routine can cause chaos. George finds himself needing a formatted printing routine, and only perfection will do. The answer to his prayers? A simple modification to Turbo C's *printf* and *sprintf*.
January 2002

GO

USB—IT'S NOT JUST A BUS, IT'S AN ADVENTURE

Silicon Update Online—*by Tom Cantrell*
Hardhearted, cynical, pessimistic. Sounds like a description of the Grinch or Ebeneezer Scrooge, right? More like engineers when it comes to PCs. This month, Tom pours out his frustrations with PCs and the software/hardware upgrades that invariably follow. He also sings his praise of one thing about PCs that's yet to let him down, USB. January 2002

GO

THE eZ80 WEBSERVER

An 8-Bit CPU Takes on the Internet
Technically Speaking—*by James Antonakos*
James likes doing what the majority of engineers enjoy most—discovering new hardware and software. And this month, he got a real kick out of Zilog's new eZ80 Webserver microprocessor. Along with the many design ideas he came up with, he also got an idea for a contest. Check it out and then enter!
January 2002

GO

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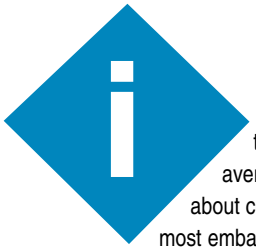
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TASK MANAGER

Care to Try Some PSoC?



It's an unfortunate but mostly true fact that the average American maintains a shallow knowledge about countries and cultures beyond our shores. The most embarrassing aspect is that most of the uninformed are satisfied with their ignorance. Content to let the rest of the world convert its currency to dollars and its measurements to inches. Unless, of course, we happen to be taking military action in a particular region or the latest summer blockbuster is set in an exotic locale (i.e., not America), then we're spoon-fed some facts by news anchors and it's off to the water cooler to drop some terminology that hints at our cultural awareness.

Not that I approve of such cultural ignorance, but in our defense, the country was started by a handful of colonies that decided they didn't care how things were done in England. So from the beginning, the American way was to do things the way Americans thought they should be done, regardless of whose cultural traditions we stepped on in the process.

Aside from military conflicts and movies, food is probably the most common source of cultural experience for Americans. During one semester in college, I had a roommate from Hawaii and a roommate from Guam, and although the U.S flag flies over both of those locations, I quickly learned that outside of speaking the same language, our lifestyles, traditions, and tastes were worlds apart. I developed a whole new appreciation for steamed rice and even grew to like the taste of salted seaweed sheets. However, when it came to the main course, raw seafood just did not appeal to me. After all, I'm from New England where seafood is served either deep fried or in chowder.

The typical American way of dealing with new foods is to ask, "What is it?" (even though in many cultures this can be taken as an insult). I guess it's just the American way to question the unknown, but not until the unknown is about to have a direct personal effect on us. As a designer of any nationality, if you look at page 7 and find yourself asking what a Cypress MicroSystems PSoC component can do, I hope you'll take a few moments to find out. After all, a part of $17,000 in cash prizes could directly affect you if you submit one of the top entries to the latest design contest from *Circuit Cellar* and Cypress MicroSystems!

With the growth of the Internet, information about any culture or region of the world is only a Google search away. And finding out more information about Cypress' line of PSoC components and the PSoC 2002 Design Challenge is even easier than that. Just point your browser to www.circuitcellar.com/psoc2002 and you'll find all of the information you'll need. While you're there, be sure to sign up for the free contest Development Pak that we'll be distributing while supplies last.

Besides, getting involved in a *Circuit Cellar* design contest will help you expand your global cultural awareness. After all, you could find yourself joining a group of engineers from Bolivia, Canada, Romania, South Africa, India China, France, Belgium, Australia, Spain, and the United States who have won prizes in recent design contests.



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PSoC™ Design Challenge 2002

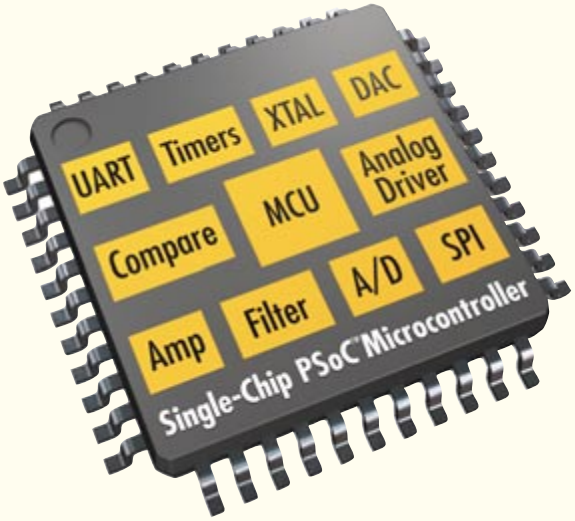
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For complete rules and entry form

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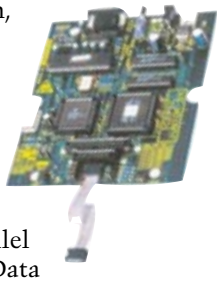
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NEW PRODUCT NEWS

Edited by John Gorsky

PC/104 COMPUTER-ON-A-BOARD

The **Prometheus** is a PC/104 embedded computer-on-a-board. It combines the integrated ZF Micro Devices ZFx86 FailSafe embedded PC-on-a-chip with a 10-Mbps Ethernet port, data acquisition, serial ports, and additional features in the PC/104 form factor. It integrates three standard boards into one.



The board can perform as a stand-alone unit or as the baseboard. It features a 100-MHz 486-DX2 processor, 32-MB RAM, floppy and IDE-HDD controllers, four serial ports, one parallel port, two USB ports, and an IrDA port. Data acquisition functions include 16, 16-bit analog inputs with programmable gain, four 12-bit analog outputs, 24 digital I/O lines, and two counter/timers. A panel board and enclosure are also available to eliminate all I/O cables.

The Prometheus costs **$700**.

Diamond Systems Corp.
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www.diamondsystems.com

CAPACITIVE PROXIMITY SENSOR

The **QF 5.5** ultra-thin 5.5-mm (0.22″) capacitive proximity sensors can be mounted in small areas. The sensors also have a long sensing range relative to their size: either 5- or 10-mm flush mountable range, depending on model.

Mounting is facilitated with several holes and slots in the sensors that allow multiple mounting options. The sensors detect all metallic and nonmetallic materials, including water, metal, wood, glass, cardboard, plastic, concrete block, glue, thin wire, silicon wafers, and numerous other materials. QF 5.5 sensors are available with or without a sensitivity potentiometer to adjust the range of the sensor.

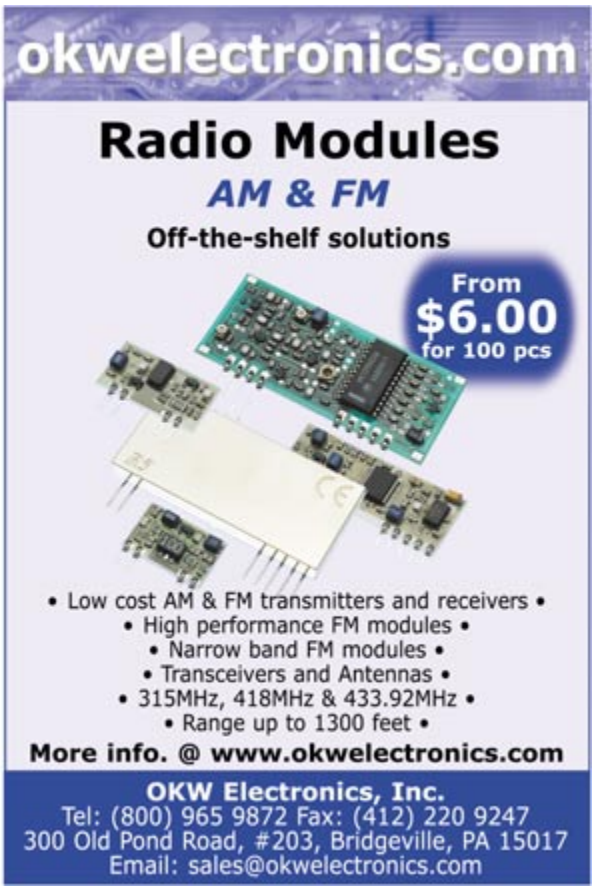
The 10- to 30-VDC sensors are can be embedded in steel depending on sensitivity adjustment and are available with NPN (sourcing) or PNP (sinking), normally open or normally closed outputs.



List prices begin at **$75**.

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www.turck.com

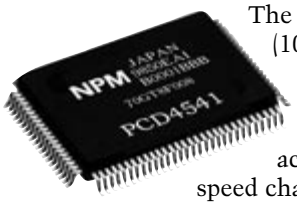




NEW PRODUCT NEWS

MOTION CONTROL CHIP

The **PCD-4541** is a four-axis motion control chip designed for two-phase unipolar or bipolar stepper motors. The PCD-4541 can output CW/CCW pulses or excitation signals directly to drive chips because sequence logic for Full and Half Step modes is built-in.



The main features of PCD-4541 (100-pin QFP package) are four independent axes control, simultaneous start and stop of all axes, linear or S-curve acceleration and deceleration, speed change on the fly, idling pulse output for start, and various limit signals.

The PCD-4541 makes multi-axis stepper motor systems easier and cost-effective. Major applications for this product are semiconductor manufacturing and inspection equipment, robots, analyzers, medical examination equipment, and automatic handling equipment.

Pricing for 500-piece quantities is **$18**.

Nippon Pulse Motor Co., Ltd.
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Fax: (540) 633-1677
www.pulsemotor-usa.com

30-V POWER MOSFETS FOR 2.5-V GATE DRIVES

The **Si7494DN**, **Si3434DV**, and **Si6404DQ** are 30-V power MOSFETs specified for gate drives down to 2.5 V. The new n-channel TrenchFETs (in TSOP-6, TSSOP-8, and PowerPAK 1212-8 packages) are designed for battery charger switching and protection applications in portable electronics and 26- to 28-VAC adapters.

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The devices are aimed at battery switching applications. The Si7404DN combines on-resistance of just 22 mΩ at a 2.5-V gate drive with a low thermal resistance package. The Si3434DV provides an on-resistance of 50 mΩ at 2.5 V. The Si6404DQ has on-resistance of 14 mΩ at a 2.5-V gate drive.



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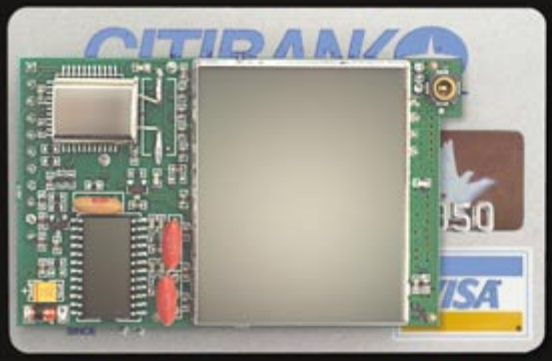
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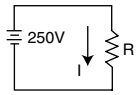
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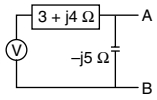
Draw a phasor diagram that explains the special characteristics of the waveform.

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Problem 4—Highlight the differences between ripple counter and synchronous counters.

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FEATURE ARTICLE

Colin O'Flynn

It's a SNAP

A Flexible Communications Protocol

Finding the right communications protocol is an important step in the design of a network project. There are plenty of options to choose from, but Colin took a look at the Scalable Node Address Protocol (SNAP) and found out that it met all of the needs for his project.

Whether you are designing a system to monitor the temperatures in a nuclear reactor or a home automation system, a communications protocol is needed. There are hundreds of different communications protocols, each one perfect for a different use. I was looking for one that's usable for most projects. It would have to be simple, secure, expandable, and easy to implement in a microcontroller. I discovered Scalable Node Address Protocol (SNAP), which was developed by High Tech Horizon for use with its power line modems.

SNAP is useful not just for the power line modems but also for any network. This protocol is flexible and can support from two to 16.7 million nodes. It also supports up to eight different error detection methods, so you don't have to use overkill to transmit data 3 cm. However, SNAP isn't a solution for every communications problem.

The protocol specifies only how the data is laid out, not the physical layer. This can be both an advantage and a disadvantage because you cannot guarantee that two different SNAP networks will work together. You may define high as 5 V but someone else may define high as 25 V. Also, SNAP can use both synchronous and asynchronous data transfer. Synchronous needs another line that has the clock pulse on it; asynchronous does not (an ordinary serial port is asynchronous) and has only a data line.

If you're looking for a protocol that's easy to use and implement, SNAP fits the bill. Each packet can vary from a few bytes to a few hundred bytes. The structure of each packet is illustrated in Figure 1. The sync byte starts the packet. Next comes the HDB2 byte (see Figure 2). Although I won't get into the details, note that you may also put some preamble bytes before the sync byte.

The destination address bytes (DABs) tell the receiver the packet's intended direction. The number of nodes you need determines how many DABs you will need. If only 255 nodes are needed, then only one DAB is needed. If you plan on using all 16.7 million nodes, then you'll need all three DABs. The system is similar with source address bytes (SABs). Only 1 byte is required if you need less than 255 nodes. Three bytes are needed if all nodes will be used.

The protocol-specific flag bytes are not supported in the current version of SNAP (V.1). Note that they will define things such as remote resets and packet priority.

The ACK and NAK bits define the ACK request, ACK response, and NAK response. These bits indicate if the sender is requesting an ACK response. Then, they determine whether the packet is an ACK or NAK response (see Figure 3).

After the SYNC and HDB2 bytes comes the HDB1 byte. The HDB1 byte defines whether or not the byte is in Command mode. HDBI also defines the kind of error detection and the number of data bytes (see Figure 4).

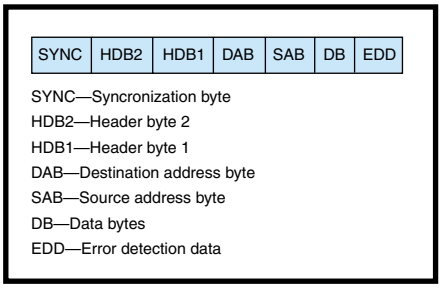


Figure 1—*The packets are layed out as shown.*

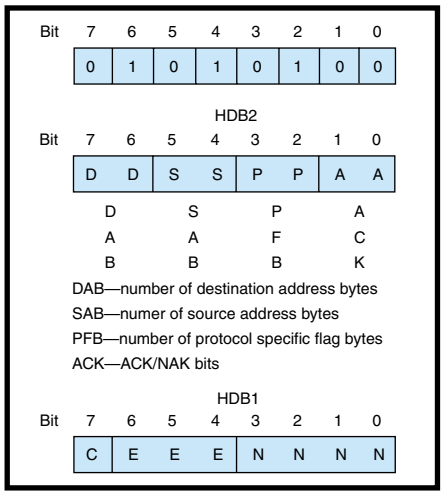


Figure 2—*The sync byte comes first in the packet, followed by the HDB2 packet. HDB1 is next in line. It contains information regarding the length of the packet.*

The Command mode bit defines if this packet is a Command mode packet or normal data packet. Command mode is only minimally supported in SNAP V.1, thus it's marginally useful. Keep checking the High Tech Horizon (HTH) web site catalog for future releases that will offer more support for Command mode.

The next few bits define the error detection method (EDM) used. Error detection is used in communications to figure out if there are any problems with the packet. Figure 5a displays the many EDM supported by SNAP. You can also choose to use none of these methods, which works fine for some applications. However, I suggest using one when you want to make sure the data is correct. You may easily implement any of these EDMs on a microcontroller. Let's discuss the methods from the most simplistic to the most complicated.

The three-times retransmission method is simple; logically it retransmits the same packet three times. If the receiver gets the same packet at least twice, the data should be OK.

Another fairly simple EDM is the 8-bit checksum. It works well for times when corruption isn't likely. The checksum result is 1 byte added at the end of the packet.

The 8-bit CRC (CRC8) method is more advanced than the 8-bit checksum, so it is more unlikely that a bad packet will slip by. For this method, 1 byte is added to the end of the packet.

At the most complicated end of the scale is the 16-bit CRC (CRC16) EDM. It is extremely unlikely that a bad packet will slip by the CRC16 unnoticed. The CRC16 is 16 bits in length, so it adds 2 bytes to the end of the packet. (As an aside, CRC32 is better but hard to put in a small microcontroller.)

The last four bits of HDB1 determine the number of data bytes. There can be up to 512 data bytes. For a breakdown of how the bits and bytes look, check out Figure 4b. As you can see, you cannot specify just any amount of data bytes. However, the amount is nicely divided up to still allow a good selection.

Following these bits are the destination address bytes (DABs). If more than one DAB is sent, they must be sent in descending order (i.e., DAB3, DAB2, DAB1). Next comes the source address bytes (SAB). Again, the bytes must be sent in descending order if more than one is sent.

The next segment of the packet will be the data bytes. You don't need to have any data bytes (e.g., ACK and NAK packets are handled entirely within the header), however, the packet won't be too useful. Once again, the sending in descending order applies to sending data bytes. This part of the packet is straightforward.

Error detection data bytes comprise the final one or two bytes. These last bytes will be the result of the checksum, CRC8 or CRC16. Later in the article, I'll discuss the mechanics of calculating error detection.

USE WITH BASCOM-AVR

As I said, SNAP is easy to implement in any language and with any controller. I use BASCOM-AVR, which is a BASIC compiler that works with the Atmel AVR series of microcontrollers. I recommend downloading the source code for the project I'll describe next; it provides many useful (and working) examples. The following isn't an example program, simply some quick snippets of code that show you how to implement the SNAP network. This is why it's important to download the source code, so you can figure out how these snippets of code go together. The first step in any program is to identify the variables you will be using. Table 1 lists some variables that will be used in the code bits.

You will need to load the HDB2 and HDB1 with data. These will be stored in Message(1) and Message(2), respectively. Suppose you have the number of DAB loaded in `Ndab` and the number of SAB loaded in `Nsab`. Information regarding whether or not you have an ACK request is loaded in `Ackm`. Then, you can simply use a shift command to get the data bits set to the right spot. Use the logic OR command to OR the two registers together. Listing 1 is an example of how to load HDB2.

You can load HDB1 in the same way, by shifting `Edm` left four bits, and then using a logic OR to combine it with `Dbn`. It's a good idea to use temporary registers (unless you are extremely short on space) to prevent corruption. However, this isn't necessary if you are careful.

Next, you should load information about where the packet is to and from into the Message(3) and Message(4) registers. After that, load the data bytes you will use. Remember to load them in the order they will be sent, so DB2 goes in Message(5) and DB1 goes in Message(6).

Error detection is the next step and also the most complex. If you're having trouble with a SNAP program, it's probably because of something in this area. You can get the complete subroutines for error detection from the source code for the SNAP analyzer. As stated earlier, the easiest EDM is three- times retransmit; simply repeat the transmission routine three times:

```
For Threetrans = 1 to 3
  TRANSMISSION ROUTINE
Next Threetrans
```

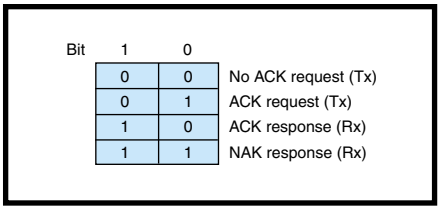


Figure 3—*The ACK/NACK setup is fairly simple.*

The next EDM is 8-bit checksum. This method too is pretty simple. All of the bytes except SYNC are added, and the total is divided by 256. The remainder is the checksum (see Listing 2). The number of added bytes could exceed 255, so you use a word. In this case, I used the variable *Crc* to store the result. I chose the name because it is a word variable, not because checksum is related to CRC. Always make sure you reset variables such as *Crc* before use, otherwise they will contaminate the result.

Next is the CRC8 method, which is better than 8-bit checksum, but not as good as CRC16:

```
Temp3 = 6
Temp2 = Crc8(message(1) ,
Temp3)
Message(7) = Temp2
```

BASCOM-AVR has a built-in CRC8 command so it's easy to use. `Temp3` is loaded with how many bytes to read from the array, starting at `Message(1)`. `Temp2` has the result of `CRC8`, which is then transferred to `Message(7)`. The final EDM is CRC16, which is extremely reliable.

The top snippet in Listing 3 loads the temp1 register with the value to be put into the CRC16 algorithm, and then calls the subroutine below it. Carefully place this subroutine in the program so the program won't run into it unless it's meant to.

a)

Bit 6	5	4	
0	0	0	No error detection
0	0	1	Three times retransmit
0	1	0	8-bit checksum
0	1	1	8-bit CRC
1	0	0	16-bit CRC
1	0	1	32-bit CRC
1	1	0	FEC (specific FEC standard to be determined)
1	1	1	User specified

b)

Bit 3	2	1	0	
0	0	0	0	0 bytes
0	0	0	1	1 byte
0	0	1	0	2 bytes
0	0	1	1	3 bytes
0	1	0	0	4 bytes
0	1	0	1	5 bytes
0	1	1	0	6 bytes
0	1	1	1	7 bytes
1	0	0	0	8 bytes
1	0	0	1	16 bytes
1	0	1	0	32 bytes
1	0	1	1	64 bytes
1	1	0	0	128 bytes
1	1	0	1	256 bytes
1	1	1	0	512 bytes
1	1	1	1	User specified

Figure 4a—*There is a host of EDM available. You have to figure out which one is best for your application.* **b**—*The number of data bytes is encoded in a binary-style code.*

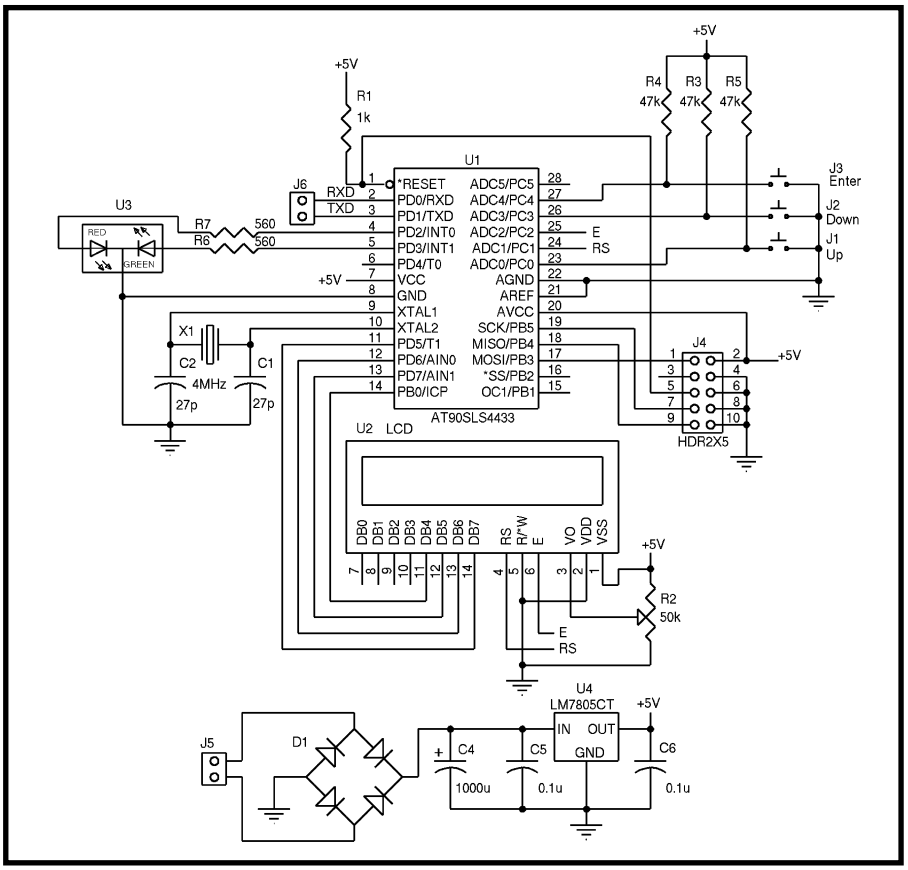


Figure 6—*As you can see from this schematic, the SNAP analyzer isn't complicated.*

Sending the data should be simple, but sometimes this is a difficult process. You have to make sure that the data is outputted in the correct direction and in the correct format. Don't try to use `printbin` directly with an array, as it will output all of the elements of the array (i.e., `Message(1)` to `Message(6)`, not just `Message(1)`). Listing 4 shows the correct way to accomplish this task.

So, now you know what's involved with sending data. How the program executes is essential, so again I stress the importance of looking over the source code and the official SNAP.

Inputting data is the opposite of sending. To input data, use the `Inputbin` command. Use this command with care because it, like `printbin`, will try to fill the entire array if you use it with an array.

Listing 5 shows the code that checks for the sync byte, and then inputs HDB2, HDB1, DAB, and SAB. You can use similar code to input the rest of the data bytes. Check that the SAB matches "my address" so you receive the packet:

```
If Message(4) <> Myaddress
then Goto Waitfordata
```

After you input all of the data you expect, run the error detection on the newest data. Then, check the result you calculate against the result you inputted. If you need some more examples, the SNAP analyzer source code is useful for this.

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Variables	Descriptions
Temp	Byte
Temp1	Byte
Temp2	Byte
Temp3	Byte
Message(8)	Byte, defines an array. Eight elements in the array message( )
Crc	Word, used by CRC16 calculation
Tmpw1	Word, used by CRC16 calculation
Tmpw2	Word, used by CRC16 calculation
Dbn	Byte, number of data bytes (also could be called NDB)
Edm	Byte, error detection method used
Ackm	Byte, ACK/NAK request/response
Nsab	Byte, number of source address bytes
Ndab	Byte, number of destination address bytes
Myaddress	Byte, what is my address?
Error	Bit, error detected?
Threetrans	Byte, used for three retransmissions

Table 1—*These variables are used in the examples.*

BUILDING THE ANALYZER

This project is useful not only as a way to send and receive SNAP packets, but also to gain experience working with the SNAP network. The analyzer doesn't support all of the SNAP features, however, the code may be modified easily to support whatever features you need. Let me go through the list of what the analyzer does support.

The analyzer supports sending and receiving data up to four data bytes long, up to 255 addresses when sending and receiving, and the four EDMs for sending data discussed earlier. The EDMs for receiving data that are supported include 8-bit checksum, CRC8, and CRC16. ACK/NAK responses when receiving data are supported, as well.

On the other hand, ACK requests when sending data, Command mode, protocol-specific flags, and preamble bytes are not supported. Lastly, the analyzer doesn't support sending or receiving more than four data bytes.

If you need to push your SNAP network to the limit, you can get a free SNAP Lab from the HTH web site (www.hth.com/snap). It runs on your PC and supports everything about the SNAP network. You need this software to test the SNAP analyzer you'll build for this project.

The analyzer code isn't complicated, however, it takes up almost the whole space in the chip! The microcontroller of choice here is an Atmel AVR AT90S4433. The AT90S4433 has 4 KB of space for the code as well as several onboard timers and an ADC (which isn't used in this project). The chip is in-system programmable so you don't have to remove it from the board to program it. This is an important advantage for an application like this, as the code on the chip can be changed and loaded quickly and easily.

Figure 5 displays the SNAP analyzer. Either an AC or DC supply may power the unit. The supply should be 7.5 to 20 V, which is regulated down to the 5 VDC needed by the unit. The heart of the circuit is an AT90S4433 by Atmel running at 4 MHz.

Any 2 × 24 LCD will display the output well. The LCD runs on a 4-bit interface. The voltage on VO controls the contrast of the LCD. A bicolor LED is also used as an indicator, signifying if the unit is receiving, transmitting, or waiting for data.

A 10-pin header serves as the programmer connection. The programmer allows you to program the chip in-circuit and connects to your computer's parallel port. You can either buy or make a programmer. The connection to the SNAP network is up to you. Here, I used a simple TTL level out. If you're connecting this to your computer, instead use an RS-232-to-TTL level converter, such as MAX232. You could also use an op-amp, zener diode, or optoisolater for input and output.

You may build the SNAP analyzer on perf board or a PCB. If you want to go the latter route, download the PCB design and parts placement diagram from the *Circuit Cellar* ftp site. You can also download both of these from the HTH web site.

The PCB is single sided with one jumper. There are two spots on the board marked NC and two marked NO. You have to jumper these pads depending whether you use NC or NO switches. This makes sure that you can use either type of switch and still pull the input high.

After you solder down all the components except the microcontroller, it's time to power up the unit. Check that the microcontroller socket has 5 V between the VCC and GND pins. Then, make sure that there are no shorts in the PCB or on the perf board. Finish the assembly by installing the microcontroller and connecting the hardware.

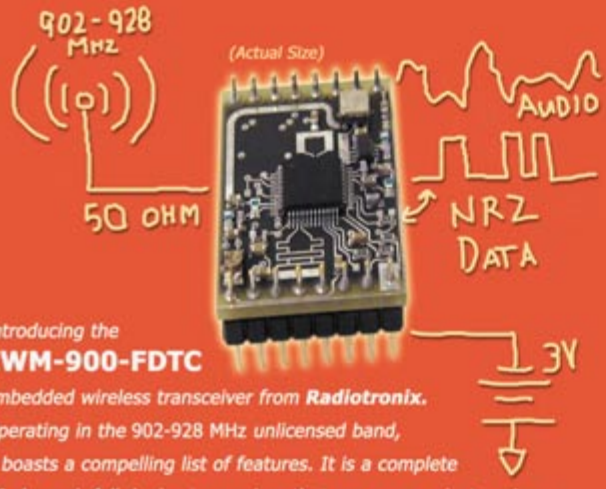
Listing 1—*HDB2 is loaded from other variables, so the value of HDB2 can be easily modified.*

```
Temp = Nsab
Temp1 = Ndab
Temp2 = Ackm
Shift Temp1, left, 7
Shift Temp , left, 5
Temp3 = Temp1 OR Temp
Temp3 = Temp3 OR Temp2
Message(1) = Temp3
```

Listing 2—*The checksum is an easy-to-implement yet reliable EDM.*

```
Crc = 0
For temp1 = 1 to 6
Crc = Message(temp1) + Crc
Next temp1
Temp2 = Crc MOD 256
Message(7) = temp2
```

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To do further work on the unit, you'll have to get an ISP and programming software. If you get BASCOM-AVR, it has programming software built in. BASCOM-AVR will also allow you to modify the source code for the programmer. Atmel offers free programming software on its web site. Keep in mind though, if you get only the free software from Atmel, you are limited to the code already provided and compiled for you.

Listing 3—*CRC16 is a reliable EDM, however, it's processor-intensive.*

```
Crc = 0
Temp = 6
For Temp2 = 1 To Temp
Temp1 = Message(temp2)
Gosub Cacl_crc
Next Temp2
Message(7) = high(Crc)
Message(8) = low(Crc)
Calc_16:       //CRC16 calculations
  Tmpw1 = Temp1 * 256
  Crc = Tmpw1 Xor Crc
  For Temp4 = 0 To 7
     If Crc.15 = 0 Then Goto Shift_only
     Tmpw2 = Crc * 2
        Crc = Tmpw2 Xor Crcpoly
        Goto Nxt
Shift_only:
  Crc = Crc * 2
Nxt:
  Next
Return
```

Listing 4—*Transmitting the data is the easy part, just make sure you output the data in the correct order.*

```
Temp = Message(1)
Temp1 = Message(2)
Temp2 = Message(3)
Temp3 = Message(4)
Printbin Sync ; Temp ; Temp1 ; Temp2 ; Temp3
Temp = Message(5)
Temp1 = Message(6)
If Dbn > 0 Then Printbin Temp
If Dbn > 1 Then Printbin Temp1
Temp = Message(7)
Temp1 = Message(8)
If Edm > 1 Then Printbin Temp
If Edm > 3 Then Printbin Temp1
```

Listing 5—*Inputting data is similar to outputting data. Again, make sure the data is in the right order.*

```
Waitfordata:
Inputbin Temp3
If Temp3 <> Sync Then Goto Waitfordata
Inputbin Temp1
Message(1) = Temp1
Inputbin Temp1
Message(2) = Temp1
Inputbin Temp1
Message(3) = Temp1
Inputbin Temp1
Message(4) = Temp1
```

You need an ISP to download the code to the chip. The ISP connects from the parallel port of your computer to the chip through a few wires. You can either buy or make one. If you wish to make an ISP, use Figure 6. Make sure to match the output lines on the schematic to the matching pins on the chip (note that CLOCK is the same as SCK). The ISP connects to the unit via a 10-pin header, and this connector should be accessible from outside the case.

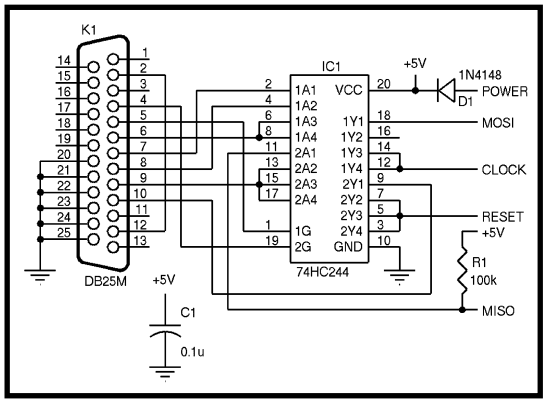


Figure 6—*The ISP for the Atmel AVR runs off the parallel port.*

Now, start up BASCOM-AVR or your programmer software. Connect the ISP to your parallel port and to the SNAP analyzer, then apply power to the analyzer. Load a file to program and click auto-program. You will receive a message if there is a problem programming it. If the chip won't program, check the software settings and check all of your hardware for shorts or other problems.

If the chip was programmed properly, you should see a message on the LCD. If you don't see a message, check that the LCD is connected properly and that the contrast is well adjusted (the lower the voltage on the VO pin, the higher the contrast). The crystal also can be picky; you must match the crystal with the proper size capacitors. Try a slightly different size capacitor on one side of the crystal, say 22 pF or 24 pF. Also double check that the code was properly downloaded to the chip. You can test this by clicking Verify (ISP must be connected) in your programming software. This function will read the code in the chip and check it against the code it programmed in.

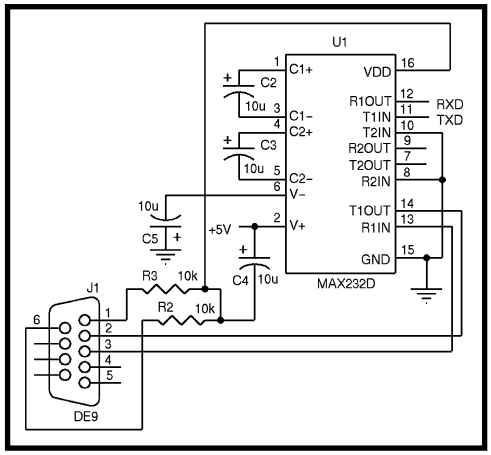


Figure 7—*The MAX232 provides fairly simple TTL-to-RS-232 conversion to connect the analyzer to your computer.*

USING THE ANALYZER

The analyzer is easy to use, just connect the TXD and RXD lines to the SNAP network. To send data, just use the arrow buttons to change data and hit enter when the data is correct. When the analyzer sends the data, it will display the data sent. Hit Enter to exit this screen. To receive data, again use the arrow buttons to change data, and press Enter when the data is correct. When the bicolor LED turns orange, it is waiting to receive data. The analyzer will wait until it receives a sync byte, then input the data that was sent. It does an error check and displays the data. Again, hit Enter to exit this screen.

You will set up a sample SNAP network to test the analyzer. First, you need to download SNAP Lab from the HTH web site. Run this program and click on the Connection tab to set up which port you plan to use. Set the serial data rate to 4800 bps and click connect.

You'll need a MAX232 level converter to connect the analyzer and your computer. Note that RS-232 voltages aren't compatible with TTL or CMOS levels, and will destroy a TTL or CMOS part directly connected to RS-232 (see Figure 7).

Power up the SNAP analyzer and select send. Enter in any data, address, and error detection. The data will be sent and show up on the computer screen. If nothing happens, use a logic probe to make sure that data is being sent. Check the MAX232, cable, computer port, and SNAP Lab.

After you get it to send bytes, set the analyzer to receive. If you set the sender address to zero, the analyzer will receive data from any source. If you set "my address" to one and hit Enter, it will wait for data. Set up the SNAP Lab software to send a packet with 1 data byte using CRC8. Set the destination address to one and click Send Packet. Some data should appear on your LCD. Now that everything is tested, you can start making networks!

THE FINAL PACKET

This article showed you some examples for using SNAP and what it is about. Hopefully, you'll find SNAP useful for your applications. Try writing some simple SNAP nodes and making them communicate with the SNAP analyzer or lab.

Colin O'Flynn is a student in Ontario, Canada. He started working with microcontrollers when he was 10 years old, and now works with many different types of electronics, including microcontrollers and CPLD. You may reach him at coflynn@newae.com.

SOFTWARE

To download the code, go to ftp.circuitcellar.com/pub/Circuit_Cellar/2002/139/.

SOURCES

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FEATURE ARTICLE

Robert Lacoste

A Tracking Lab Power Supply

Stable and reliable, that's how we like our power supplies. The question is, how do you build one that meets the criteria? Going back to his engineering roots, Robert revisits building completely with analog devices. His creation is more than reliable, it's bulletproof.

What are the two common factors of every electronic project, from RF transceivers to microcontroller-based meteorological stations, from FPGA experimentation to washing machine controllers? First, they all need more power than their designers initially expected. Second, it isn't unusual to spend days trying to debug them only to then discover that the problem was simply an imperfect power supply, either not stable enough or full of spurious signals.

I used to test my prototypes with a big power supply built when I was 16 (yes, that was a long time ago), using a used arc-welding transformer. The power supply was able to supply 25 A without a glitch, but has only one output and an approximate regulation. It was fine for 74LS00-based designs, but today circuits often need several different voltages in the low range (e.g., 5, 3.3, 2.7 V). Rather than adding several power supplies on my bench, which is already a little overcrowded, I decided that is was time for a new one. As usual, I didn't find on the market exactly what I was looking for and decided to take the do-it-yourself approach.

THE CONCEPT

I will probably use this new power supply for decades, so I decided to build a flexible one based on three entirely isolated sections. This arrangement allows you to connect two or three sections in parallel to increase the maximum current or in series to increase the maximum voltage or provide bipolar voltages. Another useful configuration is to connect two sections in series to power the device under test and to use the third one as a floating voltage source (e.g., to polarize a transistor somewhere).

I decided that each section should be a stable 0- to 20-V source, 0 to 3 A for sections one and two, and 0 to 2 A for section three (auxiliary). These sections should be able to work in Constant Voltage mode as well as in Constant Current mode, both with perfect regulation. So I will be able to get up to 60 V at 2 A or up to 8 A at 20 V, which should be enough.

In order to add complexity and justify a homemade design, I also included three more requirements to my wish list. To facilitate serial/parallel configurations, I wanted to have a tracking mode. In this mode, one section should automatically follow the voltage of another section, without any sacrifice on the 100% isolation between sections. I also wanted to have a way to measure the selected maximum current without having to short circuit the outputs. And, last but definitely not least, I wanted a compact design.

Have a look at Figure 1 and you'll see the final block diagram of this dream power supply. Then, take a look at Photo 1, which shows that the resulting prototype is indeed compact.

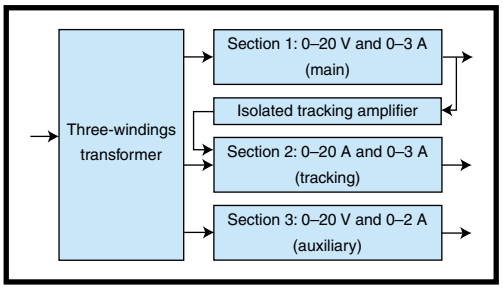


Figure 1—*The power supply is built around three independent, isolated, 0- to 20-V sections. An isolated amplifier allows you to implement a tracking mode.*

OPERATIONAL AMPLIFIERS

OK, now let's open the box and check out the schematics. The three sections are identical. I'll start by describing one of these sections, then spend some time discussing the isolated tracking amplifier and the global assembly of the power supply.

As shown in Photo 2, I've used a three-output torus transformer, providing one 40-VA and two 60-VA windings. These transformers are common in hi-fi amplifiers, and provide good decoupling from power line transients. Figure 2 shows the schematic of the high-current part of a regulation section.

The AC voltage from the transformer is rectified and then filtered with a decent, large capacitor (no less than 10,000 µF for each output). Next, it goes through a couple of ballast BD649 transistors in parallel, which will implement a classic Serial mode regulation. A buffer, made with a quarter of a LM324 quad operational amplifier, drives these transistors.

On the output side, the resistor bridge R6/R7 provides a measure of the output voltage (USENSE signal) and the serial shunt R8 provides a measure of the output current (ISENSE). Perspicacious readers will notice that USENSE is not exactly proportional to the output voltage, because there is a voltage drop in the shunt resistor, namely ISENSE. However, you can try different solutions, and will quickly discover that there is no solution that gives both an exact voltage and exact current proportional signals, each referenced to ground. Usually this problem is solved with a current shunt on the positive line, but this causes difficulty in implementing a good current regulation because the signals have a high common voltage. So instead, I'll just correct the USENSE signal with some analog arithmetic.

Figure 2 also shows that I've included a couple of auxiliary voltage regulations in order to power the LCD displays (9 V) and to get a good reference voltage (2.5 V) for the main regulation. A discrete half-bridge inverter built around C2, C3, and diodes D1 and D2 provides a negative voltage. The voltage is regulated to –3 V with the D3 zener diode without requiring another winding on the transformer.

The negative voltage drives the negative power inputs of the operational amplifiers and allows the outputs to be properly regulated down to exactly 0 V. I tried to eliminate the need for these parts using rail-to-rail operational amplifiers, but the result was not satisfactory; these chips, even if they are more expensive than standard ones, are too imprecise when their inputs and outputs are in the tens of millivolt range.

The main regulation stuff is shown on Figure 3. Let's start with the current limitation: the actual current (from ISENSE) is amplified by U4.A and compared by U4.B to the maximum allowed current, selected by the P2 potentiometer. Notice the small feedback capacitor, C11, on comparator U4.B. C11 reduces the gain of the comparator in high frequencies and suppresses high-frequency oscillations that were occasionally present without it. The output of U4.B goes low if the actual current exceeds the preset limit.

The voltage regulation section is a little more complex. The USENSE signal is first corrected to get a signal exactly proportional to the output voltage. Let's look at how. You have:

$$\text{USENSE} = U_{OUT} \times \frac{R7}{R6 + R7}$$

thanks to the R6/R7 bridge, where U_{OUT} is the voltage between the ground and positive output line. But, as there is a voltage drop equal to ISENSE in the R8 shunt (i.e., between the ground and negative output line), the voltage available on the output connector is $U = U_{OUT} - \text{ISENSE}$, so $U_{OUT} = U + \text{ISENSE}$

So, replacing U_{OUT} with this expression produces:

$$\text{USENSE} = (U + \text{ISENSE})\left(\frac{R7}{R6 + R7}\right)$$

After performing some elementary math, you get:

$$U = k\left(\text{USENSE} - \frac{R7}{R6 + R7} \times \text{ISENSE}\right)$$

So, to get a voltage proportional to the actual output voltage U, you have to reduce ISENSE with a resistor bridge

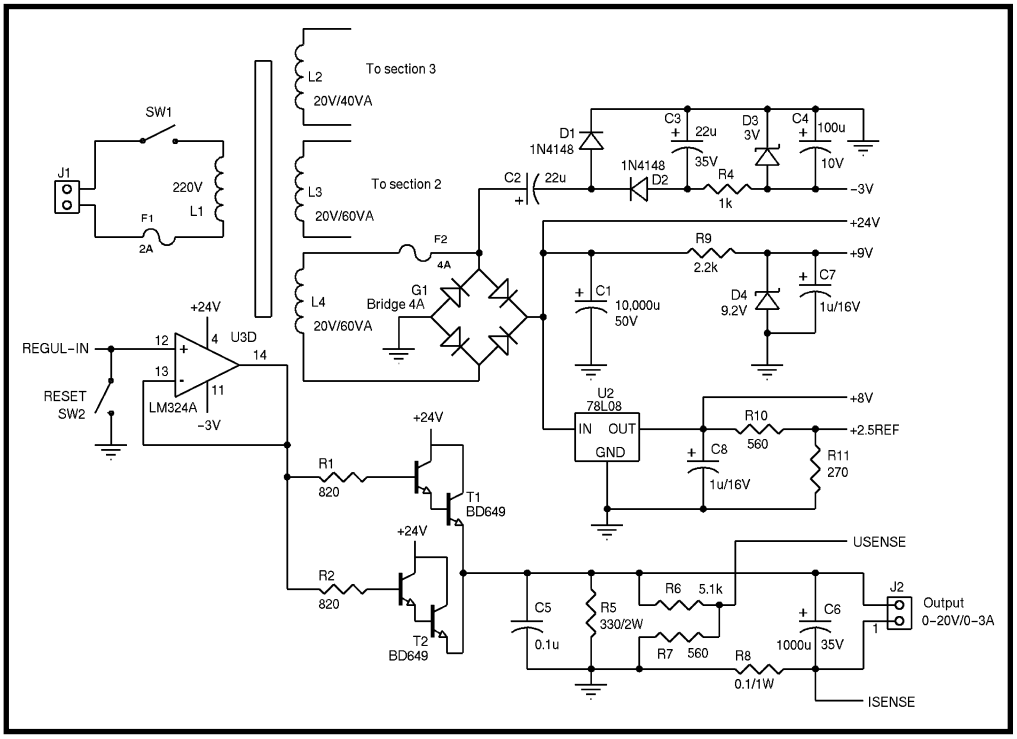


Figure 2—*Secondary power regulations provide the –3, 9, 8, and 2.5 V needed by the main regulation circuitry and LCDs.*

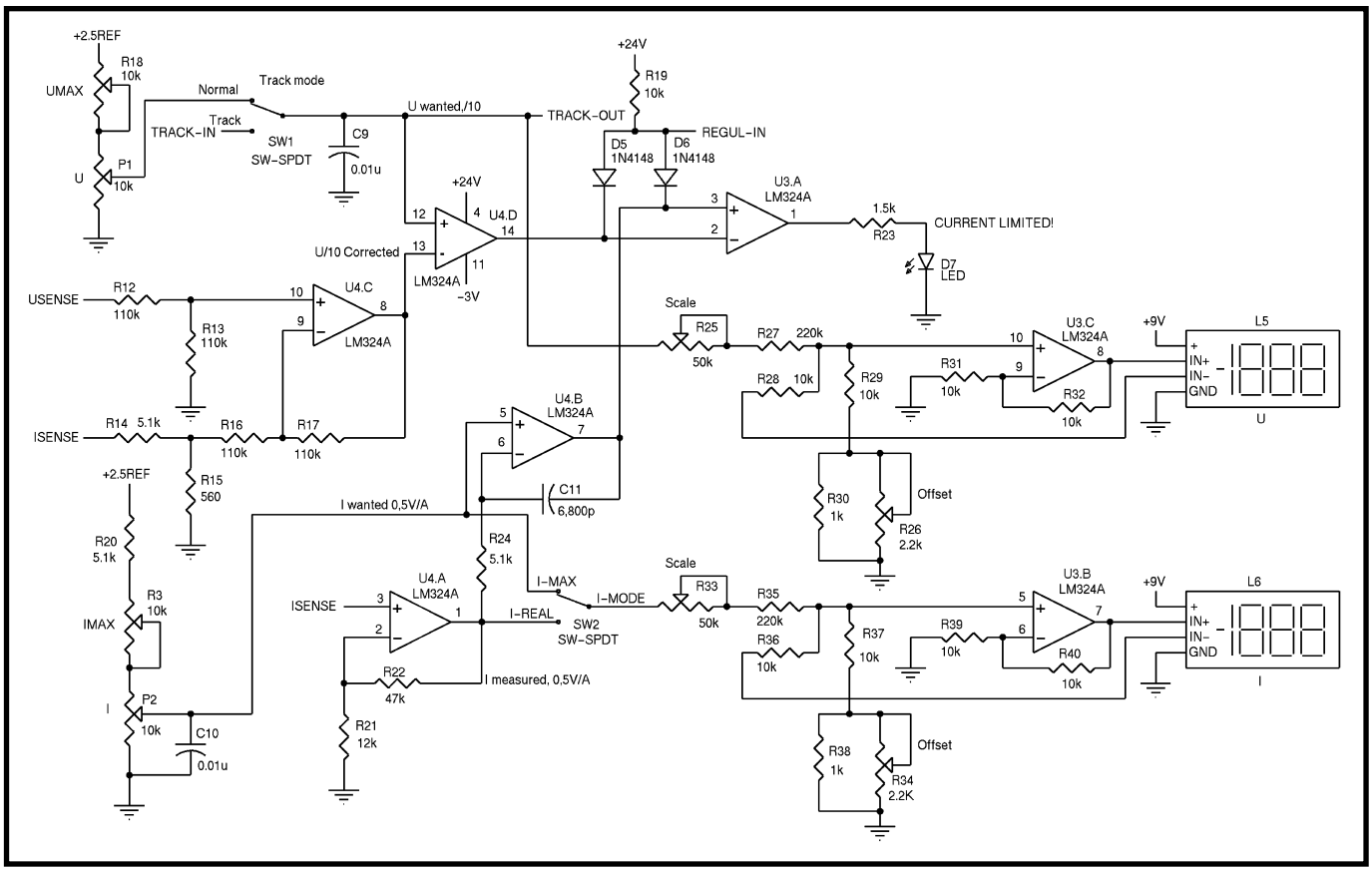


Figure 3—*The main regulation circuit is a good "operational amplifiers for dummies" exercise. It includes noninverting amplifiers, comparators, adders, and subtractors.*

equivalent to R6/R7, and then substract the result from USENSE. R14/R15 and then U4.C do this. If you're unfamiliar with adders, subtractors, comparators, and inverting and noninverting amplifiers built around analog amplifiers, I strongly recommend reading the handbook provided on the Texas Instruments web site. [1]

Then, U4.D compares this signal to the required output voltage, either from the 10-turns precision potentiometer, P1, or the tracking amplifier output. The output of U4.D goes low if the actual output voltage exceeds the preset limit.

The voltage-regulation output and the current-regulation output are ORed with D5 and D6. The analog mode OR is taking the minimum of the signals. The ORed control then drives the ballast transistors through U3.D. A last comparator, U3.A, lights the D7 LED when the output is current-limited. Use manual switch SW2 to reset the output and implement Standby mode (see Figure 2).

LCD

I wanted to have dedicated 3.5-digit voltage and current displays for each output. LCD voltmeters are not exactly the least expensive stuff you can buy, so I looked around for the lowest cost solution. I ended up with some really nice and inexpensive units commercialized in Germany by Conrad. These voltmeters accept a ±200-mV signal and are powered by a 9-V supply. And, did I mention they're inexpensive?

However, there is one issue with them: the input signal must be floating relative to the power supply, because the voltmeters have differential IN+ and IN– inputs and can't connect IN– to ground. Because I didn't

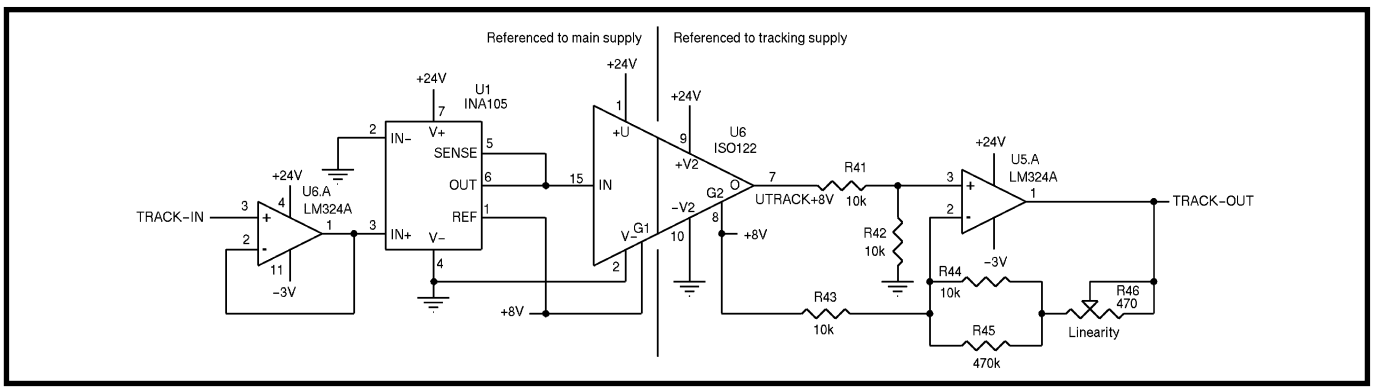


Figure 4—*The tracking section is built around a TI ISO122 isolated amplifier, driven by an INA105 unity gain amplifier. Care should be taken to keep isolation between sections.*

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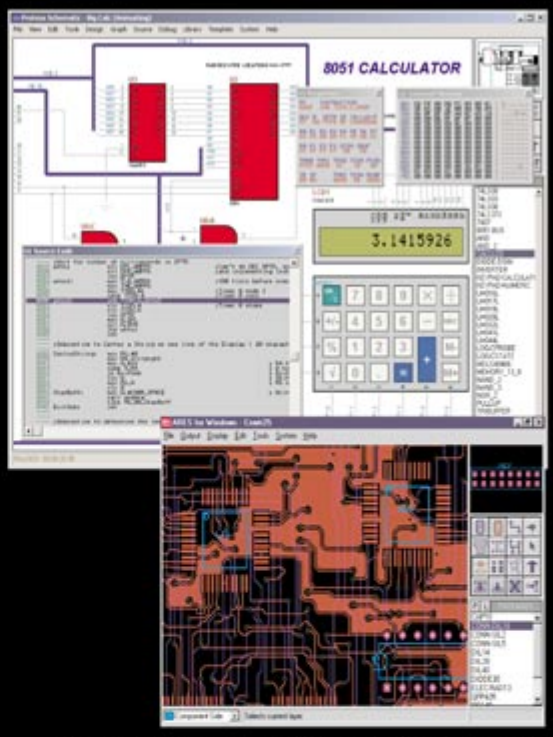
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Photo 1—*A compact design, isn't it? The transformer and filtering capacitors are below the PCB and the power transistors are on the large heat sink at the back of the device.*

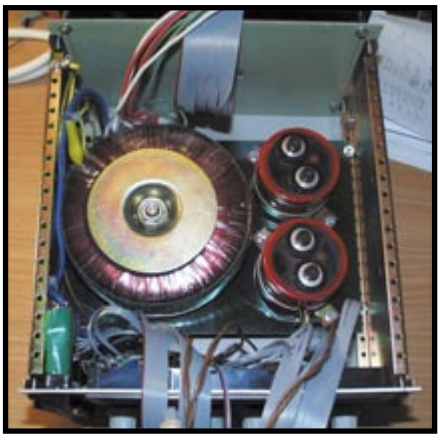


Photo 2—*A close-up view shows the two more important pieces of a good power supply. The generous transformer is a 200-VA transformer. The filtering capacitors are generous as well, at two times 10,000 µF for the two main sections.*

want to add three more floating power supplies or batteries, I decided to add more operational amplifiers—U3.B and U3.C. Both of these amplifiers implements an analog adder and transforms the unipolar voltage to be measured into a differential voltage simply adding to it the voltage available at the IN– input of the voltmeters. The only complexity is that, because I didn't want to use high-precision resistors, I needed to add offset and scale-adjustable resistors for each display.

You may think that I'm starting to have an unreasonable number of operational amplifiers, but do the math. Up until now, you've had eight amplifiers per section, but that is only two 14-pin LM324 quad amplifiers, or far less than $1 on the bill.

LET'S TRACK IT

Now, let's talk about the high-tech stuff. How do you implement the tracking mode? How do you measure the output of section one and use it as a reference for section two without losing the isolation between the two sections?

The first idea I had in mind was to use some digital devices—an ADC, optocoupler, and DAC. And some synchronization signals. And some clocks. Well, it got slightly complicated.

Then, I considered dedicated chips and found the TI ISO122 chip (formerly of Burr-Brown), and decided to go with it. In fact, this chip integrates my discrete solution and provides an isolated voltage-copying channel (see Figure 4). TI also provides an application note explaining how to use it with unipolar power supplies, thanks to a precision INA105 unity gain amplifier. Read the datasheets of these components for more information. [2, 3]

A last operational amplifier, U5A, helps to reduce the offset on the output. Of course, take care while using these devices in order to keep a good isolation between the two sides. In particular, don't forget to split the power planes.

BUILD IT

Photos 2 and 3 show the assembly of my prototype. I used a 20 cm × 12 cm × 24 cm (roughly 8″ × 4.7″ × 9.5″ in strange standard U.S. units) metallic enclosure. I affixed the transformer and two main capacitors on an epoxy blank plate, which was affixed a couple of millimeters above the base of the enclosure. All the components except the power transistors were assembled on a prototype board and connected to the front panel and transistors thanks to ribbon-type connectors. For high-current signals, a couple of ribbon wires were used in parallel.

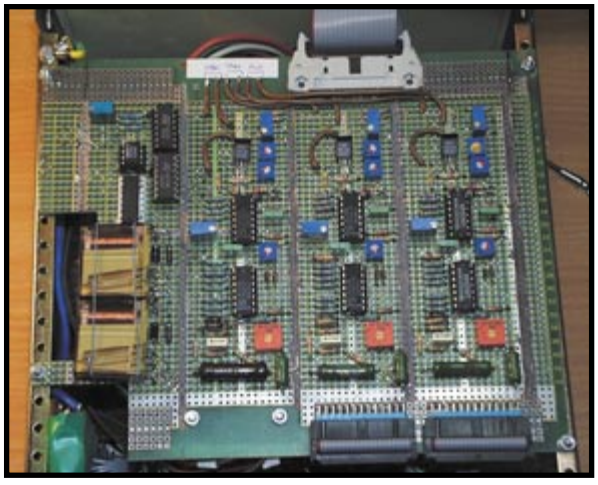


Photo 3—*The components are assembled on a prototype board. The three identical sections are clearly visible, each of them using two quad analog amplifiers. The tracking amplifier is at the top left, just above the relays.*

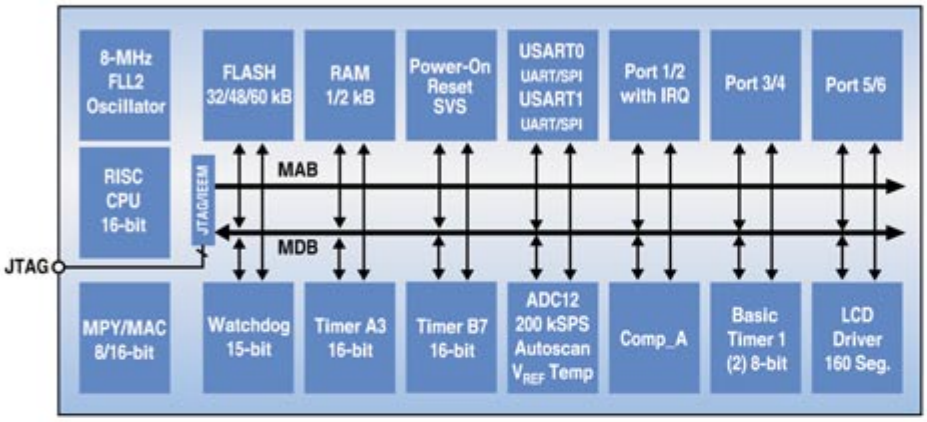
Regarding the Standby and I-MAX switches, I first looked at 3RT switches in order to drive the three sections simultaneously without losing isolation. However, I didn't find any that were small enough for my packaging. So, I used standard 2RT switches, one RT driving the main power supply section and the second RT driving a small 2RT relay, which drives the two other power supply sections. Not the simplest solution, but an effective one.

The power transistors are fixed on a heavy heat sink (see Photo 1). However, I discovered during the tests that this heat sink was not simply heavy enough, as it can climb up to 100°C when the three outputs are short-circuited with maximum current. For safety, I fixed a thermal switch on this heat sink to disconnect the AC power when it gets too hot. However if you build this device, just buy a larger heat sink….

LET'S SEE WHAT IT CAN DO

The performance of this power supply is better than what I was looking for. The voltage drop from zero to maximum current is less than 40 mV on all three outputs, and the current Regulation mode is always better than 0.2%. The residual oscillation is perhaps a little high (around 30 mV under worst-case con-

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ditions), but is probably linked to the assembly on a prototype board.

Regarding the tracking mode, the linearity is better than 1%, as shown in Photo 4. Last but not least, I measured the dynamic performances of the regulation, thanks to a pulse generator driving an external transistor used as a load, and the result is more than satisfactory. You can see the evidence in Photo 5. The thermal stability of the outputs is excellent; no noticeable variation is measured with a 5.5-digit meter. However, the onboard LCDs do have a visible variation in temperature (up to 0.5% error) shared between the differential amplifiers and LCD voltmeters, but this does not affect the output voltage.



Photo 4—*With the power supply at work, the tracking mode is selected and provides a satisfactory performance (less than 1% error). The I-MAX button is also selected so that the current meters show the maximum currents and not the actual currents.*

POWERING DOWN

Designing and building this power supply was fun. Between two projects based on the latest high-end, multi-MIPS microcontroller, it's refreshing to go back to the basics and use 100% analog devices. I'll be fully honest though, the first block diagram I wrote for this power supply was around a microcontroller. Well, three microcontrollers—one per section—with some optoisolated serial links between them. Then, I checked the added value of these micros and decided to sacrifice half of the features and build discretely. Discrete but bulletproof, as a power supply must be.

Robert Lacoste lives near Paris, France. He has 12 years of experience with real-time software, embedded system developments, and business management, and continues to love building innovative microcontroller-based devices after-hours. He is currently working for Nortel Networks. You may reach him at robert_lacoste@yahoo.fr and visit his web site at www.geocities.com/robert_lacoste.

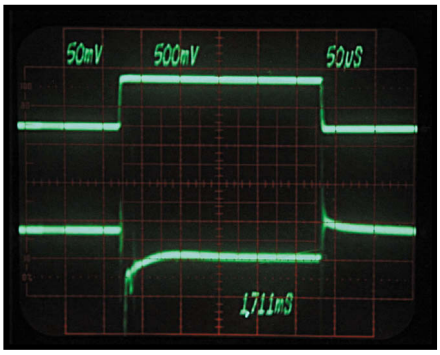


Photo 5—*A dynamic response is captured using a power transistor as a load, driven by a pulse generator. With abrupt load change (here from 0 to 1 A), the output voltage stabilizes in less than 50 µs and the voltage error is around 40 mV, including losses in the connecting cables. Overshoots when the current goes back to zero are almost nonexistent (plot taken on a Tek 7834 oscilloscope). The bottom trace is 50 mV/div.*

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[2] Burr-Brown Corp. (now Texas Instruments, Inc.), "Precision Lowest Cost Isolation Amplifier," ISO122, November 1993.

[3] ———, "Precision Unity Gain Differential Amplifier," INA105, August 1993.

SOURCES

DVM210 LCD meters
Conrad Electronic GmbH
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ISO122 chip, INA105
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FEATURE ARTICLE

Robert Bowen

Developing with Open-Source TCP/IP

Getting PCs and SBCs to reach their full communication potential is important. Robert says that more information about the essential components is always the best route to success, and he provides the info you'll need to get your Ethernet interface to speak TCP/IP.

The RS-232 serial port is still one of the most commonly used hardware interfaces. With a low cost and reduced pin count, it isn't surprising to find this interface built into most microcontrollers sold today. My favorite handheld Fluke 189 digital multi-meter proudly boasts an RS-232 connection.

In the past, I have faithfully used the serial or parallel port on a desktop computer to communicate with embedded devices. This decision was not made by accident. Listing 1 reveals how easy it is to move data across a parallel port of a PC using a high-level language such as Visual Basic.

The advantages are clear. There is less software overhead. Direct access to the hardware interface is offered. In addition, no communication protocol is required to send and receive command data.

Today, most embedded PCs and SBCs sport an Ethernet interface. Transmitting and receiving data through this hardware interface requires more than simply addressing a direct I/O port. It involves the use of a communication protocol.

In this article, I'll focus on the essential components required to transmit and receive data via UDP datagrams across an Ethernet interface. First, I will introduce a well-known and free TCP/IP protocol stack from Waterloo and port it to the MicroC/OS-II real-time kernel. Next, with just a little extra effort, I'll transfer the kernel application to the TS-2800 embedded PC from Technologic Systems (see Photo 1). Finally, I'll create a network application (GUI) on a desktop PC to communicate with the TS-2800 via Ethernet for control and monitoring purposes.

OPEN-SOURCE TCP/IP

The key to writing any network application is utilizing the network programming library, more commonly referred to as the Application Program Interface (API). In the Windows environment, most people refer to this library as the WinSock API.

WinSock was designed to create a standard programming interface for TCP/IP on all versions of Windows OS. You'll examine the WinSock API when developing your network GUI. The first order of business is to find a socket API suitable for DOS. Luckily, I didn't have far to search. The folks over at Technologic Systems were kind enough to ship a copy of the WATTCP TCP/IP protocol stack (including source code) with the TS-2800 embedded PC. You may download a complete copy of the WATTCP TCP/IP stack from the Internet.

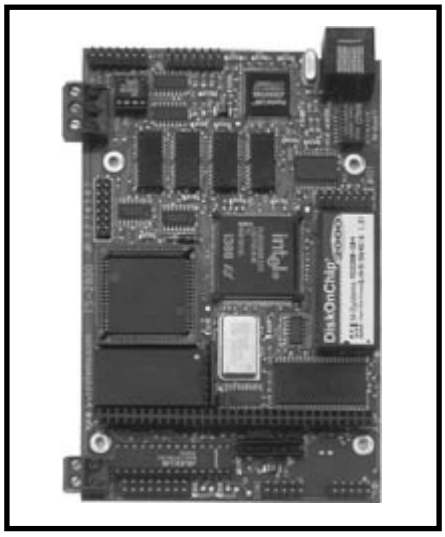


Photo 1—*The TS-2800 sports the usual embedded goodies including an ADC, LCD interface, flash memory disk from M-Systems, and digital I/Os. Hiding behind the RJ-45 connector is a 10BaseT Ethernet port powered by the CS8900A Ethernet controller from Cirrus Logic.*

Erick Engelke originally wrote and released the WATTCP TCP/IP stack in 1989. It was designed specifically to work within limited memory and to support multi-tasking applications, making it well suited for your selected RTOS.

Listing 1—*Under Windows 95/98, sending and receiving data through the parallel port on a PC is a trivial task. Software overhead is low. Direct access to the port is accessible using a high-level language like VB.*

```
Public Declare Function Inp Lib "inpout32.dll" _
Alias "Inp32" (ByVal PortAddress As Integer) As Integer
Public Declare Sub Out Lib "inpout32.dll" _
Alias "Out32" (ByVal PortAddress As Integer, ByVal Value As
Integer)

DataPort = &H378              //Base address
StatusPort = &H379            //Base address plus one
ControlPort = &H37A           //Base address plus two
CmdData = Inp(DataPort)       //Read data from 8-bit data port
Out (DataPort, 12)            //Write data (12) to the 8-bit
data port
```

Listing 2—*The WATTCP TCP/IP socket is not reentrant. The socket is initialized and all socket calls are handled in Task 1.*

```
sock_init();
udp_open(&TASK1_UDP_DATA, localport, remote,remoteport,NULL);
sock_mode(&TASK1_UDP_DATA, UDP_MODE_NOCHK);
sock_puts(&TASK1_UDP_DATA,"SocOpening Socket().Connection
Successful!");
data    = data;
  while (1) {
    rxmsg = (char *)OSMboxPend(TxMbox,0,&err);
    sock_puts(&TASK1_UDP_DATA,rxmsg);
    OSMboxPost(AckMbox, (void *)1);
    n = sock_dataready(&TASK1_UDP_DATA);
    if (len >sizeof(buffer))
    len = sizeof(buffer);
    sock_read(&TASK1_UDP_DATA, buffer,len);
    buffer[len]=0;
    cmd = *buffer;
```

Listing 3—*First, the channel of the ADC is sampled and the readings are posted into a mailbox. The results are then sent to Task 1 for transmitting to the host computer via UDP datagrams.*

```
while (1)  {
//Channel 1 ADC reading
    outp(0x078, 0x11);
    OSTimeDlyHMSM(0, 0, 0, 5);
    msb = (inpw(0x79));
    lsb = (inpw(0x78));
    ADCReading = (((msb | lsb) * FullScale)/Resolution);
    sprintf(s, "CH1 %5.3f",ADCReading );
//Send CH1 reading to task 1 for Tx via UDP to host PC
    OSMboxPost(TxMbox,(void *)&s);
    OSMboxPend(AckMbox,0,&err);
//Display CH1 reading on LCD
    OSSemPend(LCDSem, 0, &err);
    DispStr(1, 0, s);
    OSSemPost(LCDSem);
```

The WATTCP TCP/IP protocol suite supports both TCP and User Datagram Protocol (UDP). TCP is considered a reliable protocol because packets are retransmitted if they are lost or corrupted. UDP is considered an unreliable protocol because there is no guarantee that a datagram will arrive. Moreover, if a datagram does arrive, there is no guarantee that the response will be received. However, software overhead is higher when developing with TCP. For this application, you'll use UDP.

The `TCP.H` include file contains the definitions and function prototypes of all the socket calls. Further examination of the header file reveals the programming syntax for each function call. The WATTCP socket calls used in this real-time application are `sock_init()`, `udp_open()`, `sock_mode()`, `sock_read()`, and `sock_puts()`.

Porting the library to the MicroC/OS-II kernel is straightforward and completely painless. First, you will include the `TCP.H` header file in your main `INCLUDE.H` file. Next, compile. Then, link the `WATTCPLG.LIB` file to the MicroC/OS-II application.

You may download a drawing of the component architecture from the *Circuit Cellar* web site. DOS loads both the kernel application and packet driver. The library communicates with the packet driver, which in turn talks directly to the TS-2800 Ethernet hardware.

THE KERNEL APPLICATION

A word of caution, the WATTCP TCP/IP library is not reentrant (software that can be executed multiple times simultaneously). Nevertheless, you can easily work around this limitation by creating a mailbox to handle all incoming and outgoing Ethernet traffic.

A mailbox is a service provided by the kernel. It allows a task to send a pointer to another task. The pointer can point to any application-specific data, but take note that both the sender and receiver need to agree about the data being pointed to.

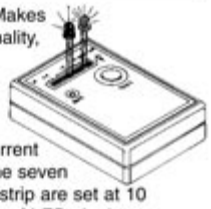
Your application will have two tasks. The first, Task 1, will be the

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highest priority task and be responsible for handling all of the Ethernet UDP datagrams between the TS-2800 and host computer. The second task, Task 2, will take on the challenge of reading the onboard ADC, monitoring digital inputs one through four, and displaying the results on the LCD. You may download a list of the tasks and their priorities.

Listing 4—*The WATTCP TCP/IP stack does not talk directly to the network card. It communicates through a packet driver interface.* `AUTOEXEC.BAT`*, as shown here, can be written to load the packet driver after DOS starts. The last line is the packet driver and software interrupt address.*

```
echo on
path =
a:\util;a:\ethernet;a:\dos;c:\util;c:\dos;c:\ethernet;c:\rtos;
prompt $p$g
set DIRCMD=/ogn
epktisa 0x60
```

Listing 5—*You need to tell WATTCP a little about your network. This is done by creating an ASCII file (*`WATTCP.CFG`*) and storing it on the TS-2800 flash memory disk. After the packet driver is loaded and the network socket is initialized, data is free to flow through the Ethernet port.*

```
//Substitute with your IP
print="Embedded MicroC/OS-II TCP/IP"
my_ip=192.168.0.7
hostname="mts.com"
netmask=255.255.255.0
```

Listing 6—*The network GUI application is not much different than using the RS-232 serial port. Data can be sent and received. This is just a little faster.*

```
Private Sub LedOff_Click(Index As Integer)
RTOS_UDP.SendData "b"          //Turn off LED
End Sub
Private Sub LedOn_Click(Index As Integer)
RTOS_UDP.SendData "a"         //Turn on LED
End Sub
Private Sub RTOS_UDP_DataArrival(ByVal bytesTotal As Long)
Dim strData As String
  RTOS_UDP.GetData strData
  Select Case Left$(strData, 3)
     Case "01A"
        Reading = Mid$(strData, 4, 9)
        Label18.Caption = Reading
        Case "CH1"
              Reading = Mid$(strData, 4, 7)
              Label8.Caption = Reading
        Case "CH2"
              Reading = Mid$(strData, 4, 7)
              Label11.Caption = Reading
        Case "ST1"             //Kernel statistics
               Reading = Mid$(strData, 4, 7)
               Text1.Text = Reading
        Case "ST2"
               Reading = Mid$(strData, 4, 7)
               Text2.Text = Reading
        Case "ST3"
End Select
```

Let's examine Listing 2, which explains the details of Task 1. Task 1 starts by initializing the WATTCP socket library by calling `sock_init`. The `udp_open` function configures the socket on which to send and receive UDP datagrams. The IP address and port number of the host computer are defined in this function call.

Next, use the `sock_mode` function to enable or disable checksums on each data packet that is sent and received. Checksums are enabled by default. However, you'll disable checksums in this application to speed up both local and remote processing of datagrams. Following this step, the kernel application is now prepared to start passing Ethernet data. The `sock_puts` and `sock_read` functions are used to transmit and receive UDP datagrams, respectively.

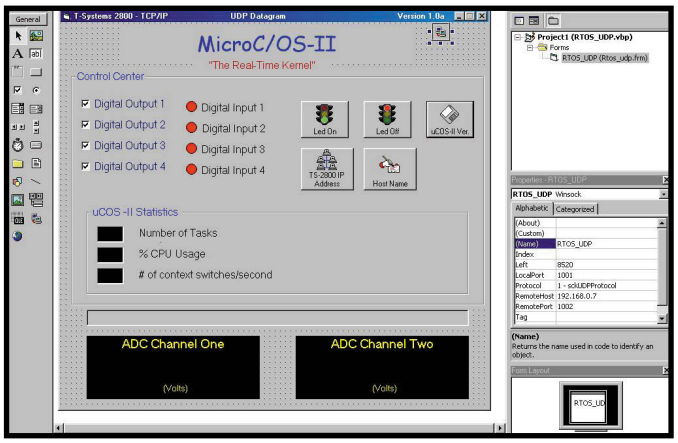
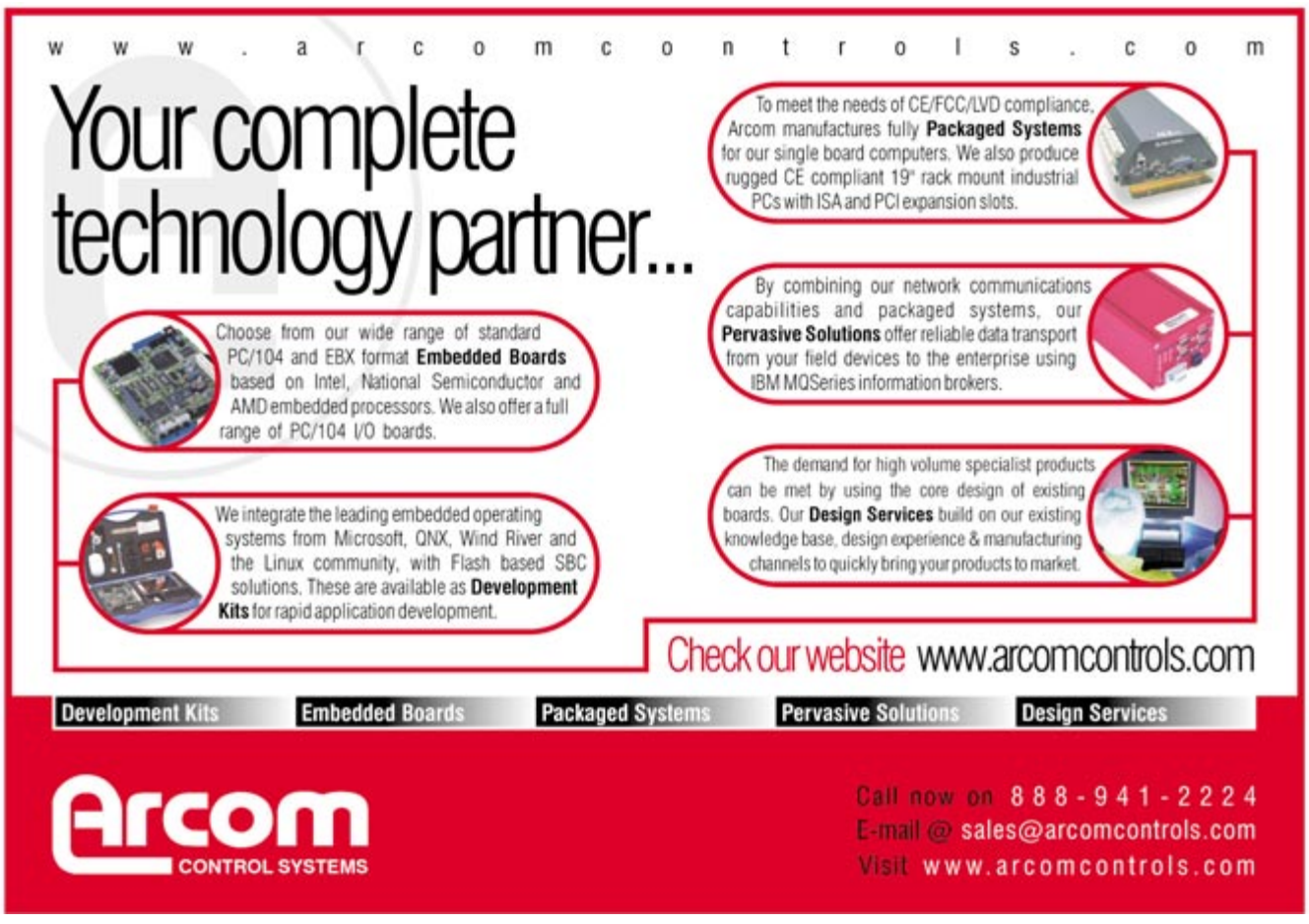


Photo 2—*Visual Basic provides an easy IDE for the network programmer. By simply adding the Visual Basic WinSock component to the main form, your application is ready to talk TCP/IP. Simply type in the local port, protocol, remote port, and IP address and Visual Basic handles all of the low-level WinSock calls.*

Task 2 (see Listing 3) is responsible for acquiring the A/D readings. Next, digital inputs one through four are sampled and the results are placed into a mailbox and sent to Task 1. Finally, the LCD is updated with current A/D readings from channels one and two.

Before launching the MicroC/OS-II application, you need to address a couple of maintenance items on the TS-2800. First on the list to address is the WATTCP TCP/IP socket, which does not talk directly to the network hardware. Instead, WATTCP TCP/IP communicates with a packet driver. Again, I didn't have far to search to solve the problem. A packet driver from Crynwr Software was included on my utility disk from Technologic Systems. Listing 4 shows how to include this packet driver into the `AUTOEXEC.BAT` file for automatically loading at boot-up.

To handle the final maintenance item, you need to educate WATTCP about your network with details such as the IP address, host name, and net mask. The `WATTCP.CFG` file contains the settings to configure the TCP/IP protocol stack for your network. A sample of the `WATTCP.CFG` file is shown in Listing 5. Now, the kernel application is complete and ready for



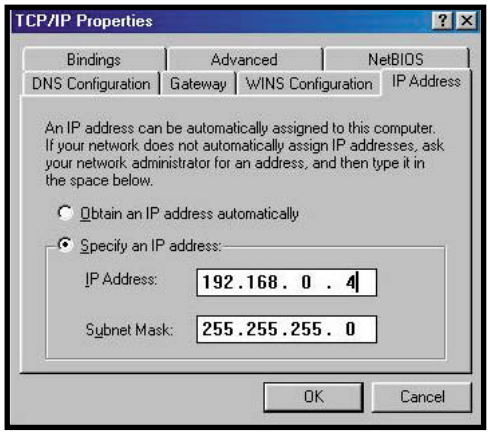


Photo 3—*Configuring a NIC card in a desktop PC to talk TCP/IP is completely painless under Win95/98. Simply edit the TCP/IP properties IP address tab and assign your IP address and sub-network mask.*

uploading to the TS-2800 for execution. It's time to build the network GUI.

SOCKET PROGRAMMING

While I was developing the MicroC/OS-II kernel application, I used the WATTCP socket library. An understanding of the WATTCP macros and programming syntax were necessary to build the kernel application. I'll take a slightly different approach developing the network GUI. Rather than using direct WinSock API calls, I plan to use the WinSock OCX component. By simply adding this OCX object to the main form of the application, all of the low-level function calls are transparent to the programmer.

Photo 2 is a snapshot of the Visual Basic IDE. After defining a few parameters to the WinSock, your application is ready to pass UDP datagrams. Listing 6 provides the source code for the network GUI. As you will notice when building your own system, sending and receiving data through an Ethernet interface is not much different than with the familiar RS-232 serial port.

CONFIGURING THE PC

A simple `WATTCP.CFG` file located on the TS-2800 flash memory disk provided all of the necessary network information. As shown in Photo 3, configuring the desktop PC is just as effortless (thanks, Microsoft). Under control panel/network, enter the TCP/IP properties for your network. The network GUI now has a ticket to the Ethernet gateway and is free to roam.

The network application GUI shown in Photo 4 presents a clean interface while demonstrating some simple control and monitoring techniques. Commands are sent from the PC to the TS-2800 to control the onboard LED and the digital outputs. The two panel meters update automatically with the A/D readings from the embedded device as well as the status of the digital inputs.

A green light indicates an active-high output and a red indicates a logic low. Notice the two buttons labeled "TS-2800 IP Address" and "Host Name." Pressing these buttons will return the IP address and host name of the TS-2800.

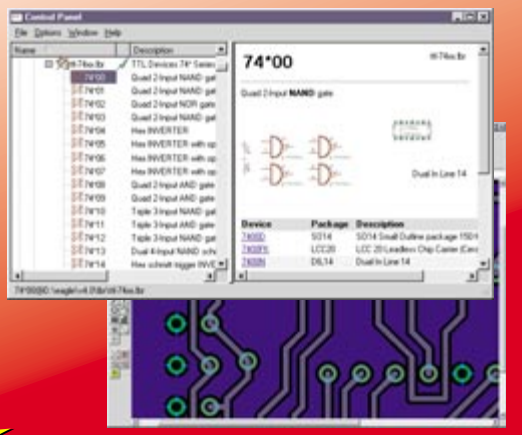
TCP/IP EMBEDDED STYLE

This article focused on UDP/IP for embedded systems as well as provided an introduction to WinSock pro-

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Photo 4—*The GUI resides on the host computer. All of the real-time work is handled on the TS-2800, which is powered by the MicroC/OS-II application.*

gramming. If you are developing network applications for a desktop PC, your perception of TCP/IP may be quite different from an embedded engineer's understanding. However, regardless of your background, the programming concept is the same. Both are easily implemented through standard socket API calls.

Whether you're designing an Internet appliance or looking for a substitute for RS-232 connectivity, TCP/IP certainly has its advantages. Imagine designing your next high-speed data acquisition controller that allowed several concurrent connections to the same box. Sound too perfect? It's possible with TCP/IP.

The WATTCP TCP/IP protocol stack is an alternative to rolling your own or purchasing a commercial suite and can be ported to your favorite kernel. Whether your embedded device is standalone or computer-controlled, TCP/IP is just a socket call away.

Robert Bowen has an Associates Degree in Electronic Technology and Electronic Engineering. He has worked for AT&T Consumer Products designing test equipment. Currently, he works for MTS Systems Corp. as a field service engineer designing automated calibration equipment and developing testing methods for customers involved in the material and simulation testing fields. In his spare time, he enjoys being an amateur radio operator (call sign N0PAU) and tinkering with Linux.

SOFTWARE

To download the code, go to ftp.circuitcellar.com/pub/Circuit_Cellar/2002/139/.

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J. Labrosse, *MicroC/OS-II, The Real-Time Kernel*, CMP Books, Gilroy, CA, November 1998.

R. Bowen, "Porting MicroC/OS-II to the TS-2800 Embedded PC," *Circuit Cellar Online*, June 2001.

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CS8900A Ethernet controller
Cirrus Logic
(800) 888-5016
(512) 445-7222
www.cirrus.com

WATTCP TCP/IP
Erick Engelke
www.wattcp.com

TS-2800 Embedded PC
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FEATURE ARTICLE

John West & Mark Stachew

Using a Median Filter

Understanding when to use median filters can save you time and money in the long run. As John and Mark describe, the applications of median filters range from automotive misfire detection to image processing software, but getting the numbers right is critical.

Picking the one in the middle may not be a surefire way to beat your friend's latest card trick, but it is a classic approach to removing noise from a signal. Of course, the median filter is used in applications ranging from image processing to automotive misfire detection. The median filter is the simple technique of using the median value of a set of data points as the signal data. For an ordered array of *n* data points, the median value is the data point at indices:

$$\frac{n}{2} \quad \text{and} \quad \frac{n+1}{2}$$

where *n* is an even number an odd number, respectively. The first index is when *n* is an even number. The second index is when *n* is an odd number. Consider the following set of data points: 47 19 32 64 34. Rearranging in ascending order we get: 19 32 34 47 64. The number of points (or rank) is five, so,

$$\frac{n+1}{2} = 3$$

and the median value for the set of points is 34. This sounds easy.

Although simple in concept, a software median filter can be expensive to implement in terms of execution time. The larger the number of data samples outside of the desired band, the larger the number of points required for the filter, and the longer the execution time. This result is largely because the data must be sorted to obtain the median value. Sorting means a lot of comparisons, and for a pipelined machine, a lot of pipeline flushes resulting from wrong branch predictions.

IN CASE OF...

Averaging filters are used in many software applications because of the ease of implementation and fast execution time. But an averaging filter may not be suited to your application's needs. A simple averaging filter is a low pass filter that smoothes out the noise in a signal. It also smoothes out the actual signal.

Consider a five-point averaging filter applied to a step input signal. As shown in Figure 1a, the filter has the effect of transforming the step into a linear ramp. If your application needs to capture fast edges of an input signal, then the median filter offers a better alternative. Figure 1b shows the output of a five point median filter applied to the same step input signal as given in Figure 1c. The output of the median filter preserves the step input, but output delays the input by three sample periods.

One of the drawbacks of averaging filters is that data points well outside the normal range affect the output of the filter. This is not the case for the median filter. Outlying data points only affect the output of the median filter if they occur at least:

$$\frac{n}{2-1} = 3$$

times within n data points, where *n* is the size or rank of the filter.

This article proposes a software algorithm for fast execution of a software median filter for a one-dimensional data set. The algorithm is a generic algorithm that is not optimized for any specific class of microprocessors. This algorithm was developed for an auto-

motive misfire detection system, which required a filter of 125 16-bit unsigned data points. Average execution time was not important so the algorithm only had to meet a worst-case execution time requirement. When execution time is the main focus, you'll find that size, readability, portability, maintainability, and such are optional at best. When your customer tells you that you have a fixed timing budget for a software implementation, or custom hardware has to be developed, you make sacrifices.

ALGORITHM OVERVIEW

The algorithm can be broken down into three sections. The first section implements a circular buffer in order to insert each new data sample in place of the oldest data sample. The second section of the code implements a modified binary search algorithm to locate the index of the old data value in a sorted array. The modified binary search simultaneously locates the index to insert the new data value in the sorted array. The last section shifts the sorted array in order to remove the oldest data value and insert the newest value. Now let's take a look at each section of the algorithm in detail.

BUFFERS

The median filter data is processed as a FIFO. A circular buffer with a size equal to the rank of the filter is used to store each new data value read by the system. Each new data value replaces the oldest value in the buffer. This requires that an index to the oldest data value be maintained. Each new data value is stored at the current index into the circular buffer, and then the index is incremented. When the index overflows the buffer size, it is set back to zero.

A second array is used to store the values in the circular buffer in a lowest to highest value arrangement. The size of the sorted array is also equal to the rank of the filter.

The circular buffer is used because minimal effort is spent determining the oldest value in the data set. The index increment and overflow check must be done only once for each new data value. The circular buffer could be removed by keeping track of the oldest value in the sorted array, but this would require much more effort because the sorted data has no relation to the order in which the data is received. The extra memory usage for the two arrays is sacrificed in order to speed execution.

To initialize the median filter, the index to the oldest value is set to the beginning of the circular buffer and the circular buffer and sorted array are zeroed. The initialization is performed on the first call of the median filter routine. The check for the first call could be removed in a number of ways.

Listing 1—*This array initialization code can be removed if the array is initialized another way. Notice the circular buffer code used to store the items in array in the order they are received.*

```
//this isn't ideal but does initialize the arrays
   if (!first_time)
   {
     first_time = 1;
     in_order_inx = 0;
     for(i=0;i<RANK;i++)
     {
       in_order[i] = 0;
       sorted[i] = 0;
     }
   }
//Stick in new point and find the oldest point
   oldest = in_order[in_order_inx];
   in_order[in_order_inx] = datum;

   if (in_order_inx >= (RANK - 1))
     in_order_inx = 0;
   else
     in_order_inx++;
```

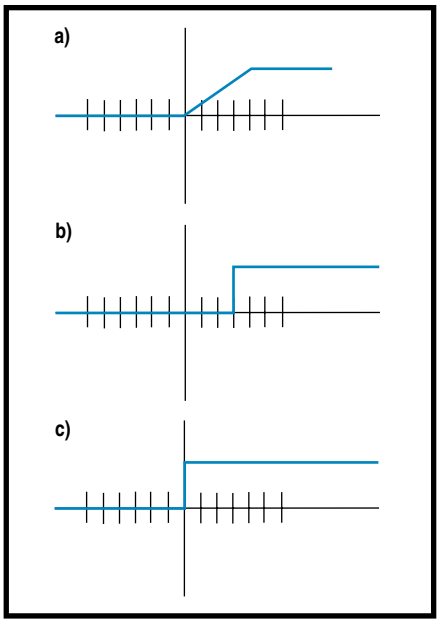


Figure 1—*You can easily see the difference between the output of a five-point averaging filter (**a**) and a five-point median filter (**b**) for the step input signal shown (**c**).*

A valid median is not guaranteed until the buffer has been filled completely. The code for the circular buffer is shown in Listing 1. The output of this section of code is the value of the oldest data point, which along with the new data point are the search items for the next section of the code.

SEARCH ALGORITHM

Now that you have a new data point stored in the circular buffer, you need to insert it into the ordered array and remove the oldest entry. Listing 2 shows the classic binary search, which is a fast way to search a sorted list.

A binary search compares the middle element of the array with the input value, if the input is less than the middle element, then searching continues only on the lower half of the array, otherwise search only the upper half. This process of halving the array continues until the element is found or the array can no longer be divided in half, indicating the element is not in the array.

The classic binary search can find any element in an *n* element array in log_2(n) iterations. This fact allows flexibility in deciding the number of points needed. Because log_2(64) = 6 and log_2(128) = 7, an array with 65–128 points will have the same worse-case search timing (seven iterations).

You have to execute this loop twice because you need to find both the oldest entry and where to insert the new entry. Any improvements to the loop will double the execution time savings, improving your overall worst-case timing. The loop has three separate areas—array-halving logic, the three-way decision requiring two checks, and the loop overhead. The array-halving logic is simple math and is the key to the search, so there's not much to optimize there. However, the other two areas do have room for optimization.

Because you're designing for the worse case, you can assume the classic binary search will search 2 × log_2(n) times to find both the new and old element. Log_2(n) iterations seems likely for a new element that can be in the array only if multiple elements have the same value. So, your best case, as well as the average for two searches, would be performing log_2(n) iterations only once and finding both values.

With that in mind, you can design an optimized loop with *n* iterations. However, on closer examination of the classic loop you can see that the last iteration is only used to break out of the loop and provide the appropriate return value. The old element is in the array and you don't care if the new element is in the array or not because you are simply looking for the insertion point. Now you can eliminate the last loop and run the loop n – 1 times.

The three-way decision in the classic search is designed to determine which half of the array to continue searching or to exit if the element is found (see Figure 2). In this case you have decided to find two elements with one loop and run for n – 1 iterations, so you don't need the three-way search. The search will continue whether the element is found or not, which means that you can simplify the loop with an if-else.

Listing 3 shows the code to perform the two binary searches with one loop. There are two identical binary searches within the loop, each converging on their own data point. Notice the two cleanup statements outside the loop, these are necessary for the n – 1 iteration technique.

Listing 2—*It's as simple as a classic binary search.*

```
int bin_search(int tbl[], int x, int n)
{
 int lo = 0;
 int hi = n - 1;
 int mid;

 while(lo <= hi)
 {
   mid = (hi+lo) >> 1;
   if (x < tbl[mid])
     hi = mid - 1;
   else if (x > tbl[mid])
     lo = mid + 1;  continue
   else
     return(mid);  /* match */
 }
 return(-1);  /* no match */
```

Listing 3—*By performing the loop once, you can find two data elements in log_2(n) iterations rather than 2 × log_2(n).*

```
low = zero;
 low1 = zero;
 hi = RANK - 1;
 hi1 = RANK - 1;

 // find the oldest and new spot
 for(m=0;m<LOOPS;m++)
 {
   // oldest
   i = (hi + low) / half;
   if (sorted[i] > oldest)
     hi = i;
   else
     low = i + one;

   // new spot
   j = (hi1 + low1) / half;
   if (sorted[j] > datum)
     hi1 = j;
   else
     low1 = j + one;
 }

 i = low - 1;
 if (datum < sorted[j]) j--;
```

Listing 4—*Depending on the compiler you're using, this simple method for shifting elements in an array may or may not be efficient.*

```
//shift data
If (oldInx >= newInx)
{
 for (i = oldInx, ++newInx; i > newInx;i--)
 {
   sorted[i] = sorted [i - 1];
 }
 sorted[i] = newData;
}
else
{
 for (i = oldInx; i <newInx; i++)
 {
   sorted[i] = sorted [i + 1];
 }
 sorted[i] = newData;
}
```

In embedded applications there are times when it's more efficient to do the work than to check and see if it needs to be done. For example, checking to see if a bit is set before setting it can be a waste of time, simply set the bit and if it's already set there's no harm done. In this case, by running the loop with no early out for finding the element, you're able to maximize your workload per iteration and reduce your worst-case timing.

INSERTION ALGORITHM

After the indices to the old and new data points have been determined by the binary search, the old data must be removed from the array, and the new data is inserted. This must be done while keeping the data in the array in ascending or descending order so that the median value remains in the median position of the array. We started with the simple method of shifting the data in the array to accomplish this.

Listing 4 gives a snippet for a simple shift of the data in the array to remove the old data point and insert the new. The number of shifts required is simply the difference between the indices to the old and new data points.

Shifting begins at the index of the old data value. If the old data point is greater than the new, then data is shifted upward in the array (from lower indices to higher). Otherwise, data is shifted downward (from higher indices to lower). After shifting reaches the index of the new data, the new data is inserted at that index.

A shifting example is shown in Figure 3. In the example, the value 8 is the oldest data value, and the value 3 is to be inserted into index three of the sorted array. The value of 8 is located at index seven of the sorted array. As shown in Figure 3, the data at indices three through six is shifted to indices four through seven. The new value of 3 is then inserted into index three to complete the shift operation.

The code in Listing 4 is straightforward and did the job, but a funny thing happened on the way home from the compiler. After inspecting

Array	x	n
2	5	3
4		
6		

	Iter1:	Iter2:	Iter3:
High =	2	2	1
Low =	0	2	2
Mid =	1	2	

Figure 2—*Here's the worst-case search path for a three-element array using the classic binary search method shown in Listing 2.*

the assembly listing we noticed some strange things going on with this previously simple code.

In the automotive misfire application, the initial thought was to make some optimizations in the insertion algorithm. The application required 125 16-bit unsigned data points. In the worst case, that could be a lot of data shifting of the array. Because a 32-bit PowerPC was our target processor, we decided that shifting two 16-bit data points at a time would cut the number of shifting loops in half.

So, we wrote the code and it worked, but we didn't see any improvement in execution time! Knowing this was impossible, we quickly found ourselves looking at the assembly listing for the code in Listing 4. Strangely enough, the compiler had done the same optimization itself. It doubled up on the data for each shift, thereby reducing the number of loops by a factor of two. Some housekeeping was added to prevent from shifting past the desired point if the number of shifts is an odd number.

Even though we had done the same thing, we quickly concluded that we couldn't rely on other compilers to act the same way, so we kept the double shifting in our algorithm. Listing 5 gives the insertion code, which shifts two 16-bit values at a time.

Let's step through the insertion code for the case where the index to the new value is greater than the index to the old. In this case you will start at the old value index and shift data down in the sorted array until you reach the index of the new value. The code is essentially the same for the opposite case where the old index is greater than the index of the new value.









Start by checking to see which direction the shifting will occur. The number of shifts is calculated as the difference between the old and new data indices. Next, a check for a one in the least significant bit of the number of shifts is done to determine if the number of shifts is odd. If the number of shifts is odd, then we shift a single 16-bit value and increment the index to the old value by one before beginning the double shifts.

The number of shifts is then divided by two to account for the double shifts. A destination pointer is set to the index of old value, and a source pointer is set to the index one greater than that. The pointers are 32-bit pointers, so in the loop, two 16-bit values are shifted each iteration of the loop.

Although the primary performance improvement comes from the loop executing half of the iterations, you should take a quick look at the bus activity. Using 32-bit pointers to move 16-bit data by one array element involves accesses that are not aligned. In this case, you read the data on a 32-bit boundary and write it to a 16-bit boundary resulting in a mis-aligned access.

In many processors a 32-bit mis-aligned access is broken into two 16-bit accesses. So in this case you have one read to get the data and two writes (mis-aligned 32-bit broken up into two 16-bit), totaling three accesses. Using 16-bit pointers you would need four accesses (two for reading and two for writing). In theory you have a 25% saving.

There are processors that either require extra cycles for mis-aligned accesses or do not allow them at all. In those cases, you can modify Listing 5 to perform two 16-bit reads or writes inside the loop. After

Listing 5—*This code performs the same shifting as the code in shown in Listing 4, but doesn't rely on the compiler to make the optimizations.*

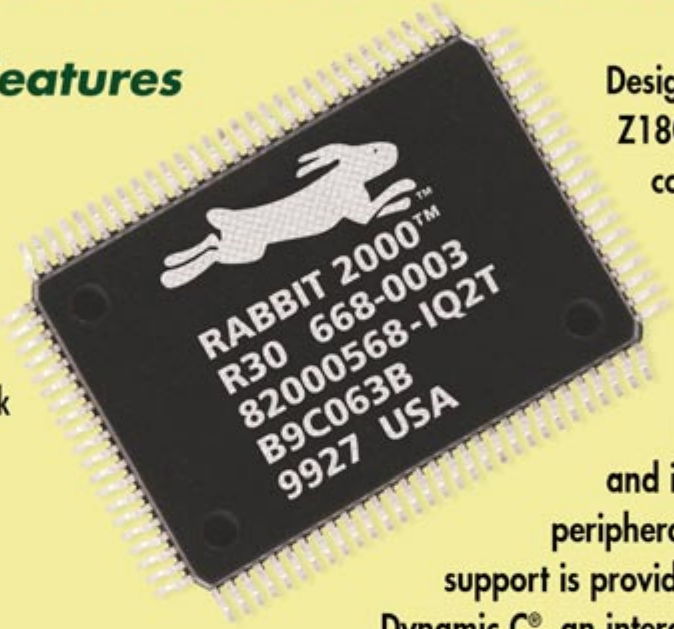
```
if (j >= i)
{
 hf = j - i;
 if (hf & 0x01)
 {
   sorted[i] = sorted[i+1];
   i++;
 }
 hf >>= 1;
 from_ptr = (long *)&sorted[i+1];
 to_ptr = (long *)&sorted[i];
 for(;hf > 0; hf--)
 {
   *to_ptr = *from_ptr;
   to_ptr++;
   from_ptr++;
 }
 sorted[j] = datum;
}
else
{
 j++;
 hf = i - j;
 if (hf & 0x01)
 {
   sorted[i] = sorted[i-1];
   i--;
 }
 hf >>= 1;
 from_ptr = (long *)&sorted[i-2];
 for(;hf > 0; hf--)
 {
   *((long*)((short int *)from_ptr+1)) = *from_ptr;
   from_ptr--;
 }
 sorted[j] = datum;
}
```

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Median	Time (µs)
15 rank	04.46
31 rank	05.80
63 rank	07.98
125 rank	11.76

Table 1—*Here are a few examples of the worst-case execution times of the filter using different ranks. Timing was performed on the Motorola MCP565 running at 56 MHz.*

the loop completes, the new data value is written to the sorted array.

The shifting works easily with 32-bit pointers when shifting downward in the array. It doesn't work quite as well when shifting upward because pointers don't address backwards! In the case where the old index is greater than the new, interesting type casting is needed to shift the data. First, the source pointer is set to two locations prior to the index of the old value. Then the line:

```
*((long*)((short int *)from_ptr+1))
  = *from_ptr;
```

takes the 32-bit value from that location and moves it one array index upward. The type cast to `short int *` is necessary to make `from_ptr+1` point to one 16-bit location past `from_ptr`. It must be then cast back to a `long *` to transfer the 32-bit value. It's not pretty, but it works.

This concept can be extended for further increases in the processor bus width as compared to the data size. For example, if your data contained 8-bit values, you could shift four values at once. The drawback is that now you could potentially shift three places past the desired point. Additional housekeeping is required to correct this and the simplest way is to use two loops.

Using the example of shifting four values at once, the first loop shifts four values at a time, and executes the number of shifts divided by four times. The second loop shifts single data values and executes the number of shifts modulus four times. This method will pay off in execution time if the rank of the filter is large and therefore, a large number of points must be shifted.

If your filter only had a small number of data points, the overhead for shifting multiple values would be too costly. A quick play of the numbers shows that when average execution time is critical, the number of points in the filter should be three times greater than the number of values shifted at once to see a performance improvement. For worst-case execution time, the filter should have twice the number of points as the number of values shifted.

If the data size equals the bus width of the processor, you may be able to normalize the data to a smaller size and still shift multiple values. This will depend on the application. Keep in mind that normalizing data acts as a filter!

PERFORMANCE DATA

Although there are many ways to implement a median filter, few are optimized for embedded applications concerned with worst-case scenarios. Perhaps the simplest and most popular type of algorithm is the find *m* element method, in which sorting is performed every time. Obviously, this type of approach can never meet the demands of embedded applications (even using sorting methods like quicksort), and often takes hundreds of milliseconds. At first glance, a linked-list approach seems popular, like the one seen in the October 2000 issue of *Embedded Systems Magazine*. Linked lists provide an easy way to insert and remove elements, however the searching has a worst-case equivalent of a linear search.

For example, a median filter with a rank of 125 would, in the worst case,

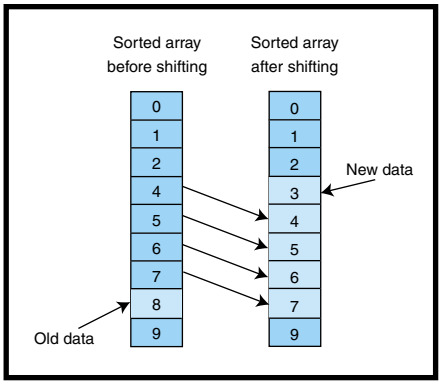


Figure 3—*After the old and new data elements are found, the data is shifted and the new element is inserted.*

do 125 comparisons to locate the oldest element to remove and find the insertion spot for the new element. It also must perform the pointer manipulation needed for insertion/deletion (minimal). Compare this to the modified binary search of seven iterations for finding both the oldest and new spot, and you'll see that in the worst case, the shifting loop executed 64 times. Test data taken on a Motorola MPC565 shows that this method is approximately 2.5× faster than the linked-list version, at least for the worst case.

Table 1 shows the worst-case execution times of the filter. Notice that as the number of points double, the execution time does not. An 8× increase in the number of points only increases the execution time by 2.64×. The RAM required is 3 + (rank(data size × 2)).

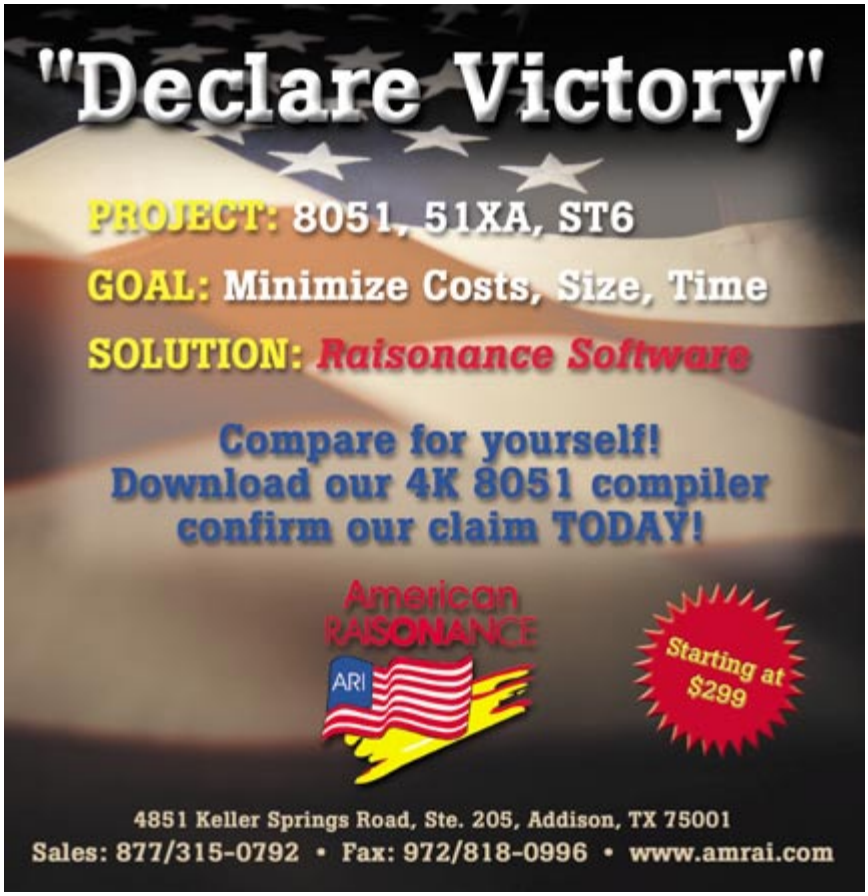
As with any embedded application, the trade-offs must be made among efficiency, size, readability, portability, maintainability, and other features. If you're looking for a higher performance worst-case optimized median filter, we hope this article has provided all of the information you need.

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SOFTWARE

To download the complete software listing, go to ftp.circuitcellar.com/pub/Circuit_Cellar/2002/139/.





FEATURE ARTICLE

Stuart Ball

Inside a Digital Joystick

All work and no play is boring. Stuart's latest project brings us back to why many of us started down the engineering path: it's fun! In the process, he uncovered plenty of useful information about designing with switches, magnets, sensors, and other such joystick innards.

Let's build a digital joystick. The first question to ask is why? There doesn't seem to be any economic reason to build your own joystick. You can buy a cheap one for $15 and a good one for $30. Your assumption is right, there isn't a reason. Well, except for the same reason you would make your own wooden chessboard or hot-rod: because I wanted to build it.

Actually, my kids have worn out a number of joysticks and I was tired of replacing them. The problem with a traditional joystick is that it consists of two potentiometers (variable resistors) that are normally used in things like volume controls. They aren't designed for continuous, repetitive action like you find in a joystick. If you are old enough to remember the time before every electronic device used remote controls, you probably remember that volume controls went bad even with the limited usage they had in that application. The usual symptom was a scratchy sound when you changed the volume.

The plan for this joystick was fairly simple. Build a joystick that didn't use potentiometers for the x-axis and y-axis controls, and do it without purchasing a complete machine shop. I did make a concession and use potentiometers for the trim controls. Trim controls don't see continuous use, so the reliability of a potentiometer is acceptable there.

I considered a couple of approaches for the joystick. I originally investigated the use of a reflective optical sensor, which would take minimal hardware to implement. The sensor would be mounted on the stick and look at a strip with varying reflectivity; the resulting signal would be used to drive the gameport inputs. The problem with this approach is that it is difficult to completely eliminate wobble in the stick, and the wobble affects the optical output.

I also tried a pair of stacked sliding plates controlled by a stick. A reflective optical sensor looked at a wedge-shaped reflector on the plates to generate an output. This worked and solved the stick wobble problem, but it was difficult to make the plates slide freely without being too loose. Additionally, the entire arrangement requires a lot of space.

The approach I finally settled on was to attach a couple of magnets to the moving parts and use Hall effect switches to generate the outputs (see the "The Hall Effect" sidebar). The Hall effect switches were arranged in an arc that matches the magnet swing. Many of the problems with the optical approach were eliminated by the built-in hysterisis of the switches.

The resulting output has 16 discrete states instead of true continuous operation, but none of the software I've tried it with seems to care. An Atmel AT90S4414 or '8515 microcontroller reads the switches and generates the resulting output values. The Atmel code is simple and uses only a fraction

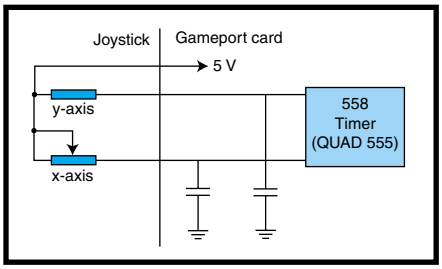


Figure 1—*An ordinary joystick has two potentiometers connected between a 5-V power supply and the inputs to the gameport. The potentiometer's resistance controls the width of a timing pulse in the gameport circuitry.*

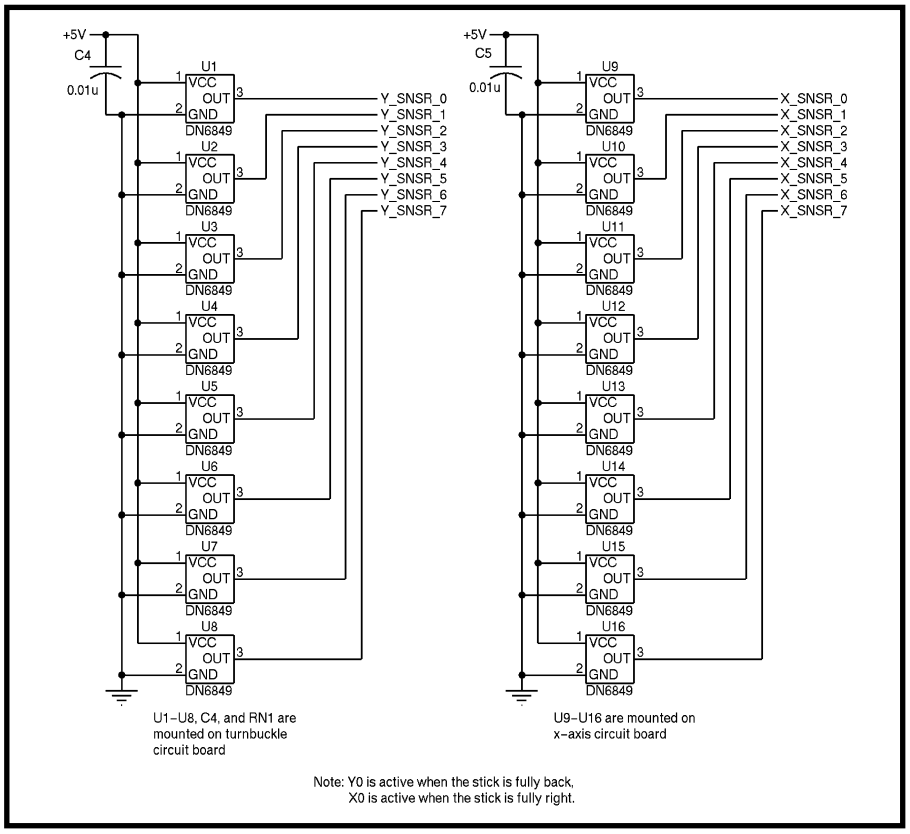


Figure 2—*Hall effect switches are mounted on two boards, one each for sensing x-axis motion and y-axis motion.*

of the available code space. The large 40-pin device is used because of the number of I/O pins required.

HOW IT WORKS

For a better understanding of how the joystick works, take a look at Figures 1, 2, and 3. A normal joystick has a pair of potentiometers connected between the 5-V supply and the timing capacitors on a 558 timer on the gameport board. One potentiometer rotates as the stick is moved from front to back (y-axis) and the other rotates as the stick is moved right to left (x-axis). As the joystick is moved, the resistance of the x- and y-axes potentiometers changes in value. This changes the length of the pulse generated by the 558 timer.

The CPU in the PC reads the position of the stick by triggering the 558 and measuring how long it takes each timer to expire. The resulting timing value varies with the values of the potentiometers, the temperature of the timing capacitors, and the resolution of the counters the PC uses to make the measurement. This is accurate enough for game play, probably not something you would want to use for precision analog measurements.

As already mentioned, the drawback to this scheme is wear on the resistive elements in the potentiometers. Using magnets and Hall effect switches eliminates this problem. The magnets move across the faces of the Hall effect switches, turning them on in sequence. The microcontroller continuously reads the state of the switches on ports B and D, using a look-up table to generate the outputs.

The outputs of the microcontroller, on ports A and C, consist of a bank of resistors that is isolated with diodes. When the microcontroller drives a port bit high, current flows through the corresponding isolation diode, through the resistor, and to the timer circuit on the gameport board. Two or more resistors can be turned on simul-

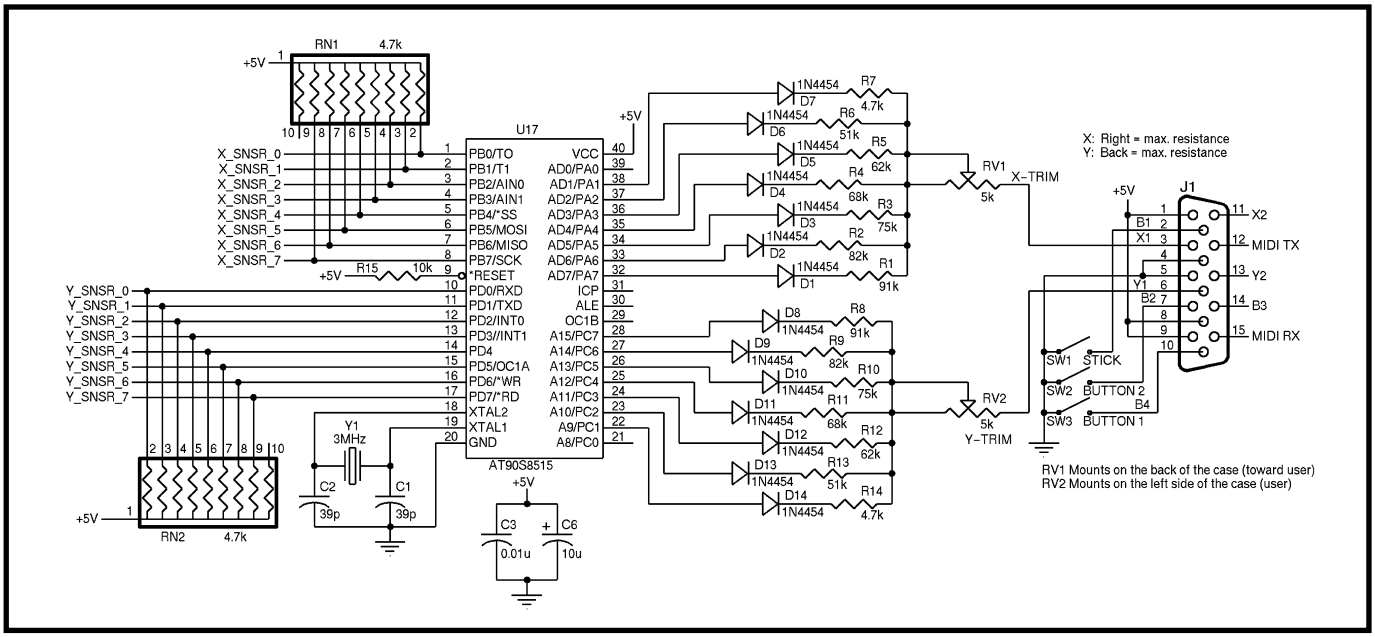


Figure 3a—*The microcontroller reads the inputs from the Hall effect switches and turns on output bits to generate analog outputs to the gameport. (See Figure 3b on page 45.)*

taneously to increase current flow. Isolation diodes are needed so that only the high state of the outputs affects the effective resistance. Without the diodes, a low microcontroller output would drag down the voltage available to the 558 timer. If the voltage across the timing capacitor can't reach two thirds of the supply voltage, the 558 timer will never complete its timing cycle.

The microcontroller outputs don't quite go all the way to the supply voltage, and the drop across the diodes further reduces the voltage available to charge the timing capacitor, but there is sufficient voltage to make everything work. Table 1 shows which microcontroller output bits are turned on to generate specific resistance values. The actual equivalent value presented to the gameport inputs will vary somewhat from these values because of resistor tolerances and varying drops across the isolation diodes.

The microcontroller firmware takes only a fraction of the available code space. The firmware continuously reads the state of the switches, uses a look-up table to get the corresponding output value, and writes that to the output port. The same table is used for both x- and y-axis outputs.

Outputs activated (port A or C)	Resistors activated (in kilohms)	Equivalent resistance (in kilohms)
D7	91	91
D6	82	82
D5	75	75
D4	68	68
D3	62	65
D2	51	51
D7, D6	91, 82	43
D6, D5	82, 75	39
D5, D4	68, 75	35
D2, D3	51, 62	27
D4, D3, D2	51, 62, 68	19
D6, D5, D4, D3, D2	51, 62, 68, 75, 82	13
D7, D6, D5, D4, D3, D2	51, 62, 68, 75, 82, 91	11
D1	4.7	4.7
D7, D6, D5, D4, D3, D2, D1	4.7, 51, 62, 68, 75, 82, 91	3.2

Table 1—*To build your own joystick, you'll have to know the output resistance values and corresponding microcontroller control bits. The actual values vary because of resistor tolerances and drops across the isolation diodes.*

CONSTRUCTION

Mechanically, I built the stick around a small aluminum turnbuckle, which you can get at your local hardware store. A 0.25" thick aluminum bar serves as the joystick handle. A wooden handle extension is added to the handle to provide better grip and a place to mount a fire switch. The aluminum bar swivels on a 6-32 bolt that runs through the turnbuckle (see Figures 4, 5, and 6). If you want a more rugged construction, use a larger turnbuckle and an 8-32 bolt (the entire assembly will be larger). The y-axis motion is achieved by the aluminum bar swiveling on its mounting bolt in the turnbuckle. The x-axis motion is achieved by rotating the turnbuckle/bar assembly from side to side.

Switches are momentary contact, normally open push buttons. The trim potentiometers are 5-kΩ, linear taper pots mounted to the case.

The components are mounted on three perfboards: one for the y-axis Hall sensors, one for the x-axis sensors, and one for everything else, including the microcontroller. The board containing the y-axis Hall switches swivels right and left with the turnbuckle assembly. Make the 10 leads coming off this board long, with a big loop, so the stress is distributed over the wire length and not over a small portion of the wire. Another important point is to make sure the wire bundle doesn't hang up on anything.

The prototype was built using an AT90S4414 because I had one laying around. The '4414 is obsolete now, but the AT90S8515 will work as well. The value of the crystal, Y1, is not critical. I used a 3-MHz part because I had more of those than anything else in my box of crystals. Anything between about 2 and 8 MHz will work as long as it will oscillate in the circuit. If you use the 4-MHz version of the microcontroller, of course, you can go up to only 4 MHz for Y1.

Pick magnet diameters so that the Hall effect switches turn on like this as the magnet moves across the arc: U1 on; U1 and U2 on; U2 on; U2 and U3 on; U3 on, and so on.

THE HALL EFFECT

Dr. Edwin Hall discovered the Hall effect in 1879. He determined that if a magnetic field is placed perpendicular to one face of a thin gold sheet and current is flowing in the sheet, a voltage will appear across the sheet. The resultant voltage is proportional to the current flowing in the sheet and the magnetic flux density.

Hall effect sensors are made from silicon. The voltage produced in silicon is only a few microvolts per volt per gauss. They include an integrated high gain amplifier to bring the signal level to a useable level. You can choose from two different types of sensors. One comes with analog outputs that are proportional to the magnetic field; the other comes as a switch that changes state when the magnetic field exceeds a certain level.

There are two varieties of Hall effect switches. Bipolar switches turn on in the presence of a south pole magnetic field and require a reversed (north pole) field to turn off. Although they turn on in a south pole magnetic field, unipolar switches turn off when the field drops below a certain level; in these cases, no reversal is needed.

The joystick project uses unipolar switches with open-collector outputs.

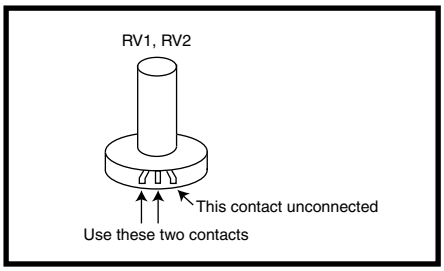


Figure 3b—*When wiring trim potentiometers RV1 and RV2, only two of the pins are used.*

This gives 16 combinations using only eight switches, and ensures that there are no dead spots where no switches are on. If you find dead spots, either move the switches or use a bigger magnet. I don't recommend using those tiny, rare earth magnets such as the ones at Radio Shack. They have plenty of magnetic strength, but they are too small to get the right on/off pattern. If you want to use a rare earth magnet, get a bigger one.

Don't worry if the magnet and switch arrangement results in three switches being on at some positions. The software handles that condition by treating the three-switch-on condition as if just the middle switch is on. On the prototype, one of the magnets is large enough so that I never have just one switch turned on, and the unit works fine. Note that a 0.5″ magnet diameter is about right.

Make sure the magnet spacing doesn't result in magnets scraping across the tops of the switches, or you will eventually damage them. You must have the south side of the magnet facing the switches and the switches mounted with the beveled side facing out, or it won't work at all.

The DN6848 switches are made by Panasonic and are available from Digi-Key. You can substitute other Hall effect switches, just be sure they are unidirectional switches (not bipolar switches or sensors with analog outputs) and that you can turn them on with a magnet of reasonable strength. If you use a different switch, it should have an output that goes low when activated by the magnetic field.

Handle centering is accomplished with two springs attached to a screw threaded into the bottom of the aluminum bar and attached to the two ends of the mounting box. This provides more resistance in the horizontal plane than in the vertical plane but it still centers the stick. The springs are a bit noisy, so an alternative would be to use rubber bands or O rings. I've even considered using a large weight on the bottom of the stick, but I haven't tried it. If you use a deeper box, you might be able to mount a single spring from the bottom of the stick to a rail that runs across the box.

The joystick is mounted in a 5″ × 7″ × 3″ box from Radio Shack. Cut a rectangular or circular hole in the bottom of the box and attach everything inside. The removable top of the box becomes the bottom in the finished project. You could make a sliding plate that fits over the handle to cover the hole, but I left it open with the turnbuckle exposed. Of course, if anybody drops a paper clip into the prototype, smoke may roll out.

The 6′ long DA15 connector on the prototype was cut from a worn out joystick. If you don't want to make a cable, you could mount the connector to the enclosure and use a joystick extension cable to connect to the PC.

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The wooden handle extension has to be drilled for the fire switch that mounts on top. Clamp a 0.25″ piece of wood into the slot so you can drill into something solid. The switch wires need to be routed in a big loop (like the y-axis wires) so they don't tangle or flex over only a small portion of their length.

The simplest way to mount the handle extension is to drill and tap six or eight mounting holes in the aluminum bar before mounting it on the turnbuckle. Mark and drill corresponding holes in the two sides of the wooden handle before gluing the three pieces of the handle together. I recommend using countersunk screws to attach the handle to the bar.

Finally, use a lockwasher (metal or chemical) to hold the bolt that passes through the turnbuckle and the aluminum bar in place. If you use a chemical locking compound, such a Loctite, don't get any in the threaded hole through the aluminum bar. Put a drop of oil in that hole to prolong the life of the threads in the bar.

Most programs let you adjust joystick parameters, so you could probably eliminate the trim controls. On the other hand, they're fairly cheap. If you do decide to leave them out, just connect the resistor banks directly to the x- and y-axes connections.

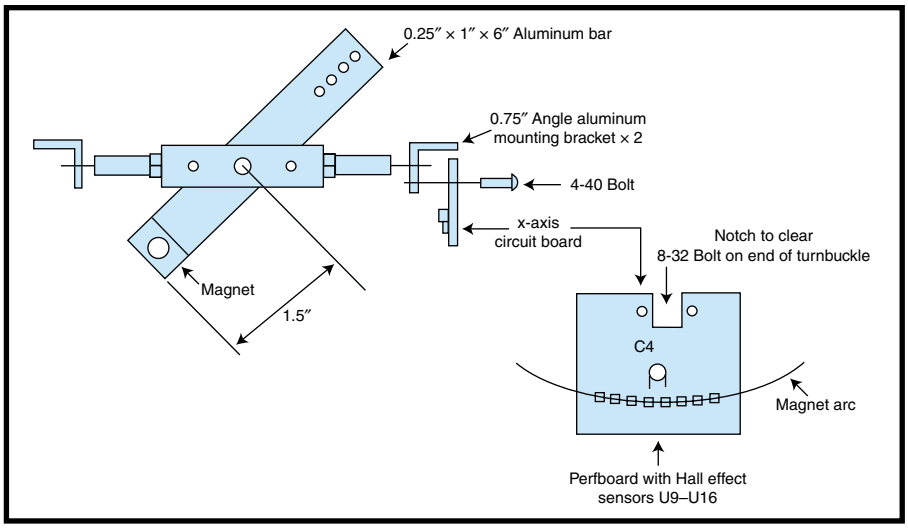


Figure 4—*The mechanical assembly shows the details of the joystick.*

CHECKOUT

I recommend verifying circuit operation before hooking it to a PC. Otherwise, if you have a wiring error, you can short out the power supply in your PC. Start by connecting a 5-V supply to the DC inputs and verifying that the ICs, including the sensors, have power. You can connect directly to the circuit board, but if you connect through the DA15 connector, you can ensure that it is wired correctly at the same time.

Verify that moving the joystick activates the Hall effect switches in the right sequence. This is easiest if you hook an LED with a 1-kΩ limiting resistor to each switch so you can watch all the sensors at once. Do this by connecting the LED cathode to the switch, connecting the anode to 1-kΩ resistor, and connecting the other end of the resistor to 5 V. Although it's more tedious, you can use a voltmeter if you don't want to use eight LEDs just to check out everything. Check both x- and y-axis motion. Be sure there aren't any dead spots. Remember that the Hall effect switches are on when low (<1 V) and off when high (>4 V).

To check the outputs, connect a 10-kΩ resistor from the x-axis output (pin 3 of the DB15) to ground. As you move the joystick from right to left you should see increasing voltage across the 10-kΩ resistor. Move the stick slowly to see each of the transitions, so you can verify that the steps are always in the correct direction. If you find a step that is the wrong way (e.g., the voltage goes down instead of up), one of the switches or output resistors was probably wired wrong.

After the x-axis is squared away, repeat this test for the y-axis output on pin 6 of the DA15. On the y-axis, voltage should be increasing moving forward (stick fully forward means maximum voltage, fully backward means minimum voltage). If you get no output at all, verify the microprocessor connections, especially the crystal. Make sure none of the sensor inputs are grounded.

There is one more test to administer after you finish the previous output tests. Check the switches by verifying that they connect the appropriate pins on the DA15 connector to ground when pressed.

My kids insist that the new joystick works better than any of the joysticks we've had in the past. They say it has more precise control. I suspect this is because many manufacturers save money by using log potentiometers instead of linear potentiometers. And, there is always a little slop in transferring the joystick motion to the pots.

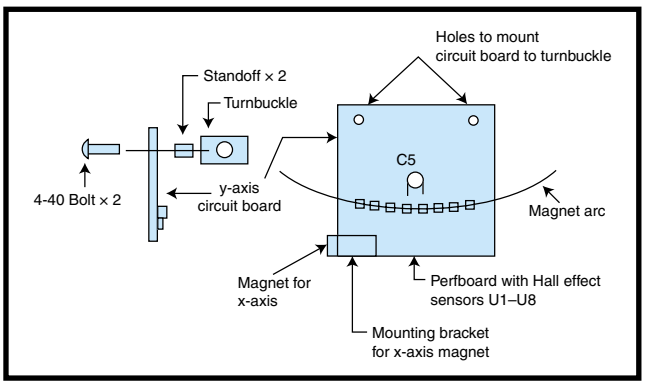


Figure 5—*The perfboard with the y-axis sensors mounts to one side of the turnbuckle. Use stand-offs as needed so the magnet clears the sensors.*

OTHER IDEAS

Instead of magnets and Hall effect switches, you could use an ultrasonic or optical sensor to measure the distance of a flag attached to the joystick handle. You should be able to make this work with no flexing wires. Of course, using an ultrasonic or optical sensor requires a different output circuit. It's possible to avoid using a microcontroller if you use a constant-current circuit to drive the x- and y-axes outputs.



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Use digital output optical potentiometers instead of analog pots. This is expensive but worth it because it's simple. You might even be able to find a joystick with a mechanism that will accept the optical pots in place of the existing ones, so you don't have to build the turnbuckle assembly. Note that this approach requires different microcontroller software.

Finally, the threads will last longer if you use a steel bar instead of aluminum. Steel is harder to work with, however, and you have to keep the magnet physically isolated from the bar to avoid magnetizing it.

Stuart Ball, a registered Professional Engineer, is an electrical engineer with 20 years of experience. He has written numerous articles and three books about microprocessor-based designs, all published by Butterworth-Heinemann (www.bhusa.com).

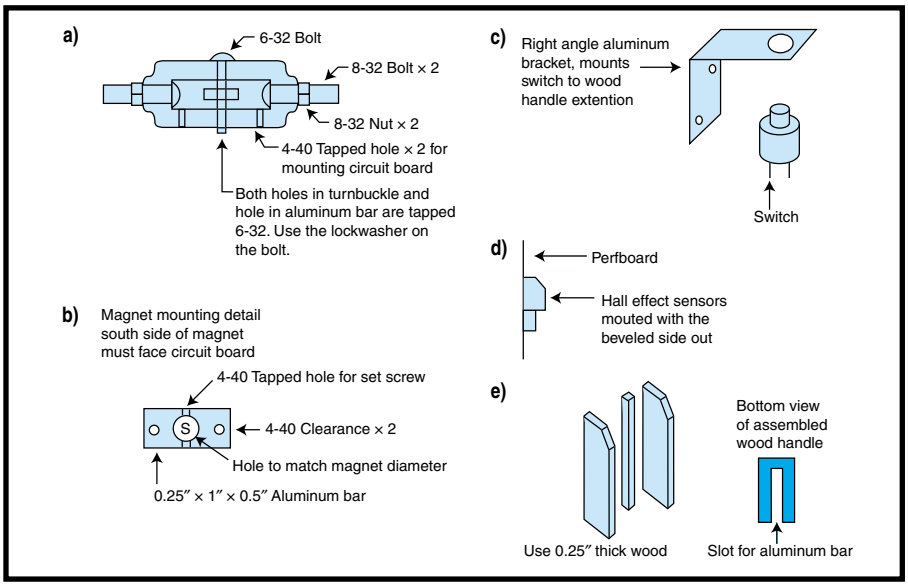


Figure 6a–e—*Check out the details of the mechanical parts used to mount all of the pieces.*

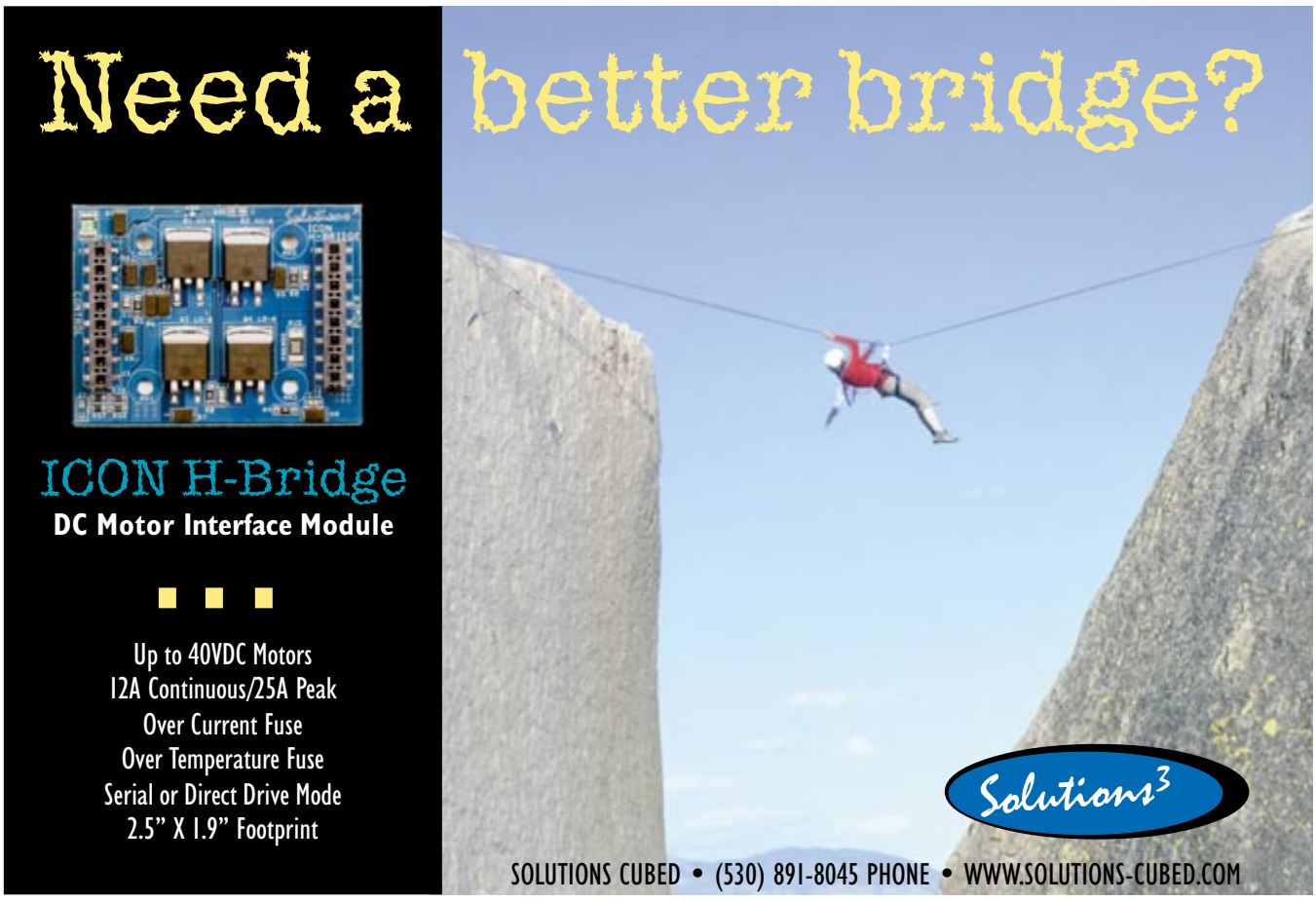
SOFTWARE

To download the code, go to ftp.circuitcellar.com/pub/Circuit_Cellar/2002/139/.

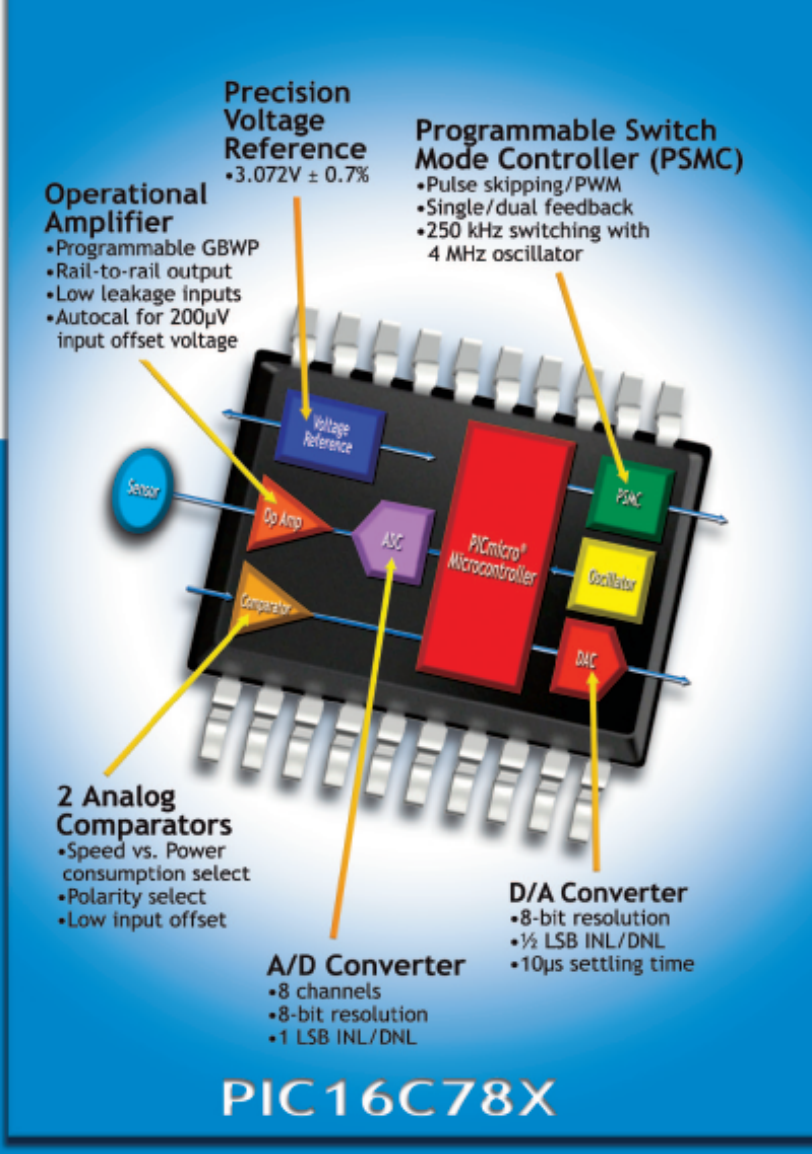
SOURCES

AT90S4414 Microcontroller
Atmel Corp.
www.atmel.com

DN6848 Switches
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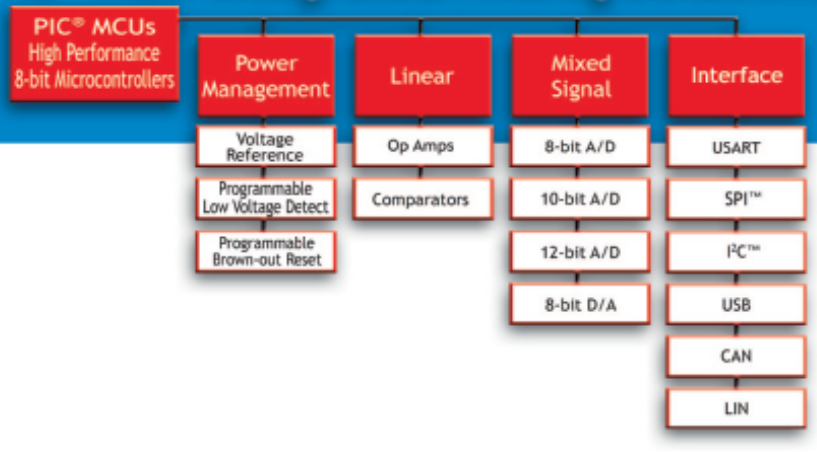
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FEATURE ARTICLE

Stefan Hollos & Richard Hollos

A Guide to Varactors

Variable reactors turn up in most of today's radio and RF circuits, but they do more than just replace mechanical variable capacitors. Stefan and Richard explain some of the characteristics of varactors and how they handle capacitance, bias voltage, and distortion.

The word varactor comes from the term "variable reactor." It can be used to refer to any electronic component whose reactance can be varied, usually electronically. This includes nonlinear inductors, in which the inductance is controlled by a current, and nonlinear capacitors, in which the capacitance is controlled by a voltage. The word varactor, however, is most commonly used today to refer to a variable capacitance diode. These diodes also may go by the names: varicap, tuning diode, and voltage variable capacitor. In this article we will use the term varactor to refer to these diodes exclusively.

Varactors can be found in most modern radios and RF circuits. They are the solid state answer to the mechanical variable capacitor found in older radios. They take up much less space, are less expensive, and they can be integrated. Because the capacitance of a varactor can be controlled electronically, automatic circuit tuning becomes practical.

A varactor is simply a diode in which the P and N regions are doped in such a manner that the capacitance that normally forms near the PN junction can be precisely controlled by a reverse bias voltage. There is an inverse relationship between the capacitance of a varactor and the applied voltage: a small reverse bias gives a big capacitance, and a large reverse bias gives a small capacitance.

In this article we will describe how varactors work, and show how the capacitance changes as a function of the bias voltage. We will discuss the varactor's circuit model and show how to bias a varactor. We will talk about the distortion that can be caused by varactors and how it can be minimized. Finally we will show a few applications of varactors.

HOW DO THEY WORK?

To understand how varactors work it will be helpful to start with a quick review of capacitors and the concept of capacitance. We can define a capacitor as any two-terminal device that stores energy in an electric field. The electric field is created by two spatially separated regions of opposite electric charge between which no appreciable current can flow. The amount of charge (Q) stored in either of the regions, will be some function of the voltage (V) applied across the terminals of the device: charge = Q(V). A capacitor's capacitance (C) is then defined as the ratio of the charge to the applied voltage:

$$C = \frac{Q(V)}{V} \qquad [1]$$

To analyze the behavior of a capacitor in a circuit, you need a relationship between the current and voltage across it. The current (I) is equal to the time rate of change of the stored

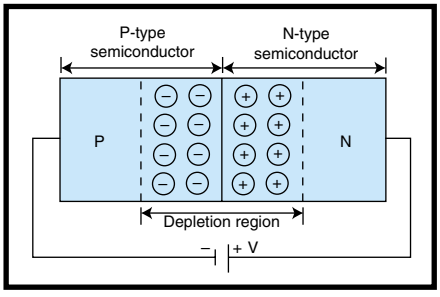


Figure 1—*The depletion region consists of two layers of fixed negative and positive charges. Increasing voltage increases the width of the depletion region.*

charge. This relationship can be expressed as follows:

$$I = \frac{dQ}{dt} = \left(\frac{dQ}{dV}\right) \times \left(\frac{dV}{dt}\right) = C(V) \times \frac{dV}{dt} \qquad [2]$$

where C(V) = dQ/dV is the incremental capacitance, which is important in varactor circuit design. It is possible to have a capacitor with a small capacitance and a large incremental capacitance.

In most circuit design, you deal with linear or nearly linear capacitors, in which the charge is directly proportional to the applied voltage:

$$Q = Co \times V \qquad [3]$$

where *Co* is constant. In this case the incremental capacitance is equal to the capacitance:

$$C(V) = \frac{dQ}{dV} = Co \qquad [4]$$

and is independent of the voltage. There are devices, however, for which the stored charge is a nonlinear function of the voltage. The incremental capacitance then will be a function of the voltage. One such device is the varactor.

The charge in a varactor is stored in the depletion region that forms at the PN junction of a semiconductor diode. To understand what this means, let's first review a few basic facts about these diodes. A P-type semiconductor is doped with impurity atoms called acceptors that lack an electron needed to complete bonds with neighboring atoms. An N-type semiconductor is doped with impurity atoms called donors that have an extra electron, not needed in bonds with neighboring atoms. Note that, even though the impurities are said to either lack an electron or have an extra electron, the two semiconductor types are electrically neutral (i.e., they have no net charge).

This is not true, however, at the PN junction of a diode. Here the extra electrons from the donor atoms on the N side of the junction diffuse across the junction and attach themselves to the acceptor atoms on the P side. In the process, the acceptor atoms, near the junction, acquire a net negative charge while the donor atoms left behind by the electrons acquire a net positive charge. The build up of charge at the junction creates an electric field that eventually stops the diffusion of more electrons across the junction. These two oppositely charged regions on either side of the junction together form what is called the depletion region (see Figure 1).

The name derives from the fact that the region is depleted of free charge carriers. No appreciable current can therefore flow across the junction. You can see then that the depletion region, according to our previous definition, constitutes a capacitor.

CAPACITANCE

The width of the depletion region can be changed by applying a voltage across the diode. Applying a positive voltage to the N side of the diode and a negative voltage to the P side will cause the width of the depletion region to increase. This is called a reverse bias. The opposite voltage polarity, called forward bias, will cause the width of the depletion region to shrink. We will limit our discussion to the reverse bias case because this is the way varactors are almost always used.

The width of the depletion region usually is a nonlinear function of the applied voltage. The exact functional form depends on the density of impurity atoms on the two sides of the junction. Three common density profiles used are graded, abrupt, and hyperabrupt (see Figure 2). In a graded junction, the density of impurity atoms increases linearly as you move away from the junction. In an abrupt junction, there is an approximately constant density of donor and acceptor atoms on the two sides of the junction. In a hyperabrupt junction, the density decreases as you move away from the junction.

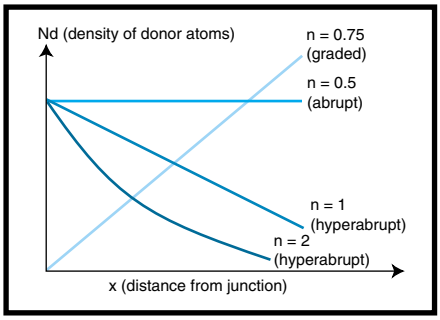


Figure 2—*There are three common impurity density profiles for varactors: graded, abrupt, and hyperabrupt.*

Given the density profiles, finding the width of the depletion region as a function of the applied voltage is actually a straightforward electrostatics problem. We will skip the details of solving the problem, however, and just note that after you have the width as a function of voltage, you can get the total charge on either side of the depletion region by a simple integration. Now you have the charge as a function of voltage, Q(V). This is really all that is needed to characterize a capacitor. From this you can get expressions for the incremental capacitance. Leaving out the details of the derivation [1, 2], the expressions for the different doping profiles all have the following form:

$$C(V) = \frac{Co}{\left(1 + \frac{V}{Vo}\right)^n} \qquad [5]$$

Vo is the junction potential with no bias voltage applied and is usually in the range of 0.5 to 0.7 V. You will not find the value of *Vo* on a datasheet, but you can easily determine it by measuring

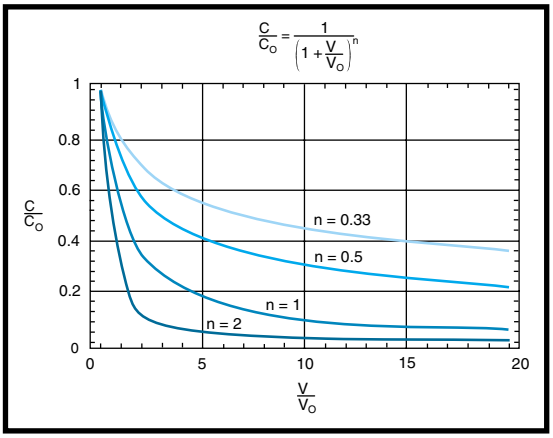


Figure 3—*In this example, you can see capacitance as a function of voltage for different types of junctions.*

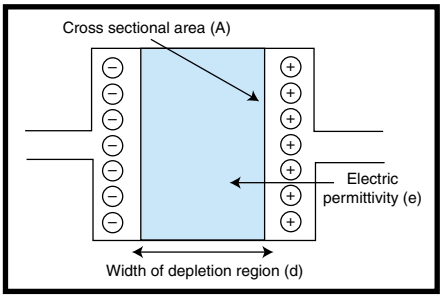


Figure 4—*Check out the parallel plate capacitor.*

the voltage drop across the diode when it is conducting under forward bias. *Co* is the capacitance with zero bias voltage. The value of exponent *n* depends on the doping profile: n = 0.33 for a graded junction n = 0.5 for an abrupt junction n = 1 to 2 for a hyperabrupt junction.

V is the applied voltage; it's positive for reverse bias and negative for forward bias. Equation 5 does apply for forward bias voltages but only up to about V = Vo/2. It's possible to derive an expression for *Co*, but in practice the value of *Co* usually has to be determined experimentally. The value of *n* for an abrupt junction varactor will be close to half but the exact value for a particular varactor has to be determined empirically. For a hyperabrupt varactor, the value of *n* can range from one to two and the exact value must once again be determined experimentally. The value n = 2 for a hyperabrupt varactor can be useful when the device is used as part of an LC resonant circuit in a voltage-controlled oscillator (VCO) because the oscillation frequency then will be a linear function of the voltage (more on this later). Most manufacturers do not provide values for *Co* and *n*. Usually only a graph of C(V) is given from which you can determine *Co* and *n*. Figure 3 shows how the capacitance varies as a function of voltage for the different junction types.

HELPFUL ANALOGY

It's possible to draw an analogy between a varactor and a parallel plate capacitor. [3] A parallel plate capacitor (see Figure 4) consists of two parallel conducting plates of area (A) separated by a slab of dielectric material of thickness (d). If *e* is the electric permittivity of the material, then the capacitance is:

$$C = e \times \frac{A}{d} \qquad [6]$$

The capacitance is a constant, which is independent of voltage applied across the plates.

The expression for the capacitance of a varactor also can be written in this form. In the case of a varactor, *e* would be the electric permittivity of the semiconductor (usually silicon or germanium), *A* would be the cross sectional area of the diode, and *d* would be the width of the depletion region. The width of the depletion region is a function of the voltage:

$$d(V) = do \times \left(\frac{1 + V}{Vo}\right)^n \qquad [7]$$

Then, the varactor capacitance can be written as:

$$C(V) = e \times \frac{A}{d(V)} \qquad [8]$$

which is similar in form to Equation 6. Keep in mind though that this is an incremental capacitance and is a function of the applied voltage, whereas Equation 6 is the actual capacitance and is independent of the voltage.

DATASHEETS

Datasheets regarding varactors normally specify the capacitance at one or more bias voltages. They also note tuning and capacitance ratio parameters. This is just the ratio of the capacitance at two specified voltages. For example, the MV2115 datasheet lists the tuning ratio as C2/C30 = 3.0, which means that the capacitance at 2-V bias is three times the capacitance at 30-V bias. [4] Other commonly listed parameters are the reverse breakdown voltage and the reverse leakage current. Like any diode, the reverse bias on a varactor can be increased only so far before it begins to conduct heavily and it no longer acts like a capacitor. Even with a reverse bias below the breakdown voltage, there will be some current through the capacitor. This is called the reverse leakage current and is usually specified at a particular voltage. From this parameter you can get an idea of the size of the resistance that's parallel to the junction capacitance in the varactor circuit model, which we'll discuss in a minute.

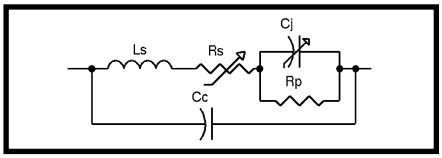


Figure 5—*Let's look at the high-frequency model for a varactor. Ls and Cc are important at high frequencies.*

Another important parameter is the quality factor (Q). While varactors can replace variable mechanical capacitors in most circumstances, an important difference between the two is the lower *Q* of the varactor. The *Q* is equal to the ratio of the energy stored (imaginary part of the impedance) to the energy dissipated (real part of the impedance) in a component. If the component is intended for use as a reactance or energy storage element, then the higher the *Q*, the better. The *Q* of an ideal capacitor is infinite. In datasheets, the *Q* is usually listed at the frequency and reverse bias for which it is a maximum. If you use the device at another frequency or bias, you can expect a lower *Q*.

CIRCUIT MODEL

The high-frequency circuit model for a varactor is shown in Figure 5. *Ls* is the lead inductance and *Cc* is the package capacitance. These components become significant only at very high frequencies, and we'll ignore them in the following discussion.

The model we will analyze is shown in Figure 6a. [1] *Cj* is the junction capacitance that varies with the applied voltage per Equation 5. The series resistance (Rs) is a result of the resistance of the semiconductor material of which the diode is made as well as any lead and contact resistance. Only the part of the diode that isn't part of the depletion region contributes to this resistance. This means that *Rs* is a function of the bias voltage.

As the reverse bias is increased, the depletion region gets larger and *Rs* gets smaller and vice versa. The parallel resistance (Rp) represents the reverse leakage current. Generally, it varies somewhat with the applied

voltage, rapidly decreasing near the reverse breakdown voltage. You can assume that it is constant though.

Using the circuit model shown in Figure 6a, the normalized impedance is:

$$\frac{Z}{Rs} = \frac{\left(B + 1 + x^2 - j \times B \times x\right)}{\left(1 + x^2\right)} \quad [9]$$

where:

$$B = \frac{Rp}{Rs} \text{ and } x = w \times Rp \times Cj \quad [10]$$

From this equation, you can see that both the resistive (real) and reactive (imaginary) parts of the impedance depend on frequency. The effective resistance reaches a maximum of Rs + Rp in the low frequency limit (x = 0), and a minimum *Rs* in the high frequency limit (x = ∞). The effective capacitive reactance goes to zero in both the low and high frequency limits. Its maximum is x = 1, or:

$$f = \frac{1}{2\pi \times Rp \times Cj} \quad [11]$$

The *Q* is given by:

$$Q = \frac{B \times x}{B + 1 + x^2} \quad [12]$$

The *Q* has a maximum value, which you can calculate by using either of the following:

$$\frac{\frac{B}{2}}{\sqrt{B + 1}} \quad [13]$$

$$\text{at } x = \sqrt{B + 1} \quad [14]$$

$$\text{or } f = \frac{\sqrt{B + 1}}{2\pi \times Rp \times Cj} \quad [15]$$

This circuit model also can be applied to any fixed or mechanical capacitor. However, note that the series resistance for a varactor is typically higher than for a mechanical capacitor. This gives the varactor a lower *Q* than a mechanical capacitor, resulting in less gain when using the varactor in a resonant tank LC circuit and poorer frequency selectivity.

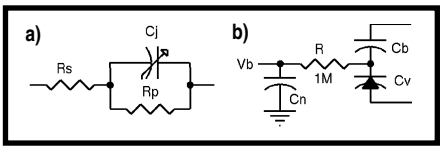


Figure 6a—*Compare the high-frequency model for a varactor in Figure 5 with this low-frequency model. Also note the basic circuit for using a varactor in* **(b)**.

BIASING, DISTORTION, AND Q

The basic circuit for using a varactor is shown in Figure 6b. Capacitor Cb blocks the DC bias voltage preventing it from affecting the rest of the circuit. It is in series with the varactor, therefore it would reduce the effective capacitance of the varactor unless it is made much larger than the varactor capacitance. Capacitor Cn and the 1-M resistor help isolate the RF and bias circuits. The 1-M resistor also prevents destruction of the varactor if the bias voltage becomes larger than the reverse breakdown voltage of the varactor.

The capacitance of the varactor is a function of the total voltage across it. This means that not only the bias voltage but also the level of the RF signal itself will determine the capacitance. To prevent the RF signal from modulating the capacitance, it should be kept much lower than the bias voltage. A good rule to use is to keep it less than 15% of the bias voltage. [1] For example, if you have a bias voltage of 2 V, the RF signal level should be less than 300 mV. Using an RF signal larger than this will make the varactor behave as a nonlinear capacitance, which means that it will generate harmonics of the RF signal and, thus, cause distortion.

If distortion is a problem, putting the varactors in a back-to-back configuration will allow RF signals to be much larger before distortion begins. Figure 7a shows the basic circuit for reducing distortion. This circuit works because when the RF signal level is rising, the total voltage across one varactor is increasing, which reduces its capacitance. At the same time, the total voltage across the other varactor is decreasing, which increases its capacitance. The net effect is less capacitance modulation and, therefore, less distortion. This circuit, though, provides only half of the capacitance of a single varactor. If you need to keep distortion down and also keep the full capacitance of a single varactor, you could use the circuit of Figure 7b.

APPLICATIONS

Varactors are found in most modern televisions, radios, cordless phones, cell phones, and other wireless communications devices. Their most common use in these devices is in frequency selective or resonant circuits. The varactor can be combined with either an inductor or crystal to create a resonant circuit. In some cases the varactor is part of an integrated circuit with the inductor or crystal connected to it externally. In an LC resonant circuit, the varactor is put either in series or in parallel with an inductor. In the series configuration, the impedance goes to a minimum at the resonant frequency. In the parallel configuration, the impedance goes to a maximum at resonance. The resonant frequency in both cases is:

$$f = \frac{1}{2\pi \times \sqrt{L \times C}} \quad [16]$$

LC resonant circuits are found in voltage-controlled oscillators (VCO), tuned amplifiers, and tunable band-pass filters.

In a VCO, the control voltage is usually used to bias the varactor in an LC circuit. The resonant frequency of the LC combination then determines the oscillation frequency. Figure 8 is an example of a VCO, this one is based on a Colpitts oscillator. The frequency of oscillation for this circuit is given by Equation 16, where *C* is the combined equivalent capacitance of the DC blocking capacitor Cb in series with the varactor capacitance (Cv). If Cb is much larger than *Cv*, then *C* will be approximately equal to just *Cv*. Because the capacitance

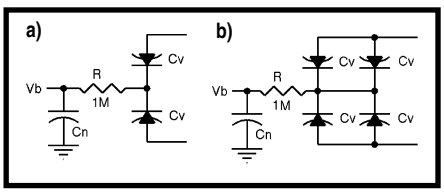


Figure 7a and b—*These circuits reduce distortion. The first provides only half the capacitance of a single varactor but the second provides the full capacitance of one varactor.*

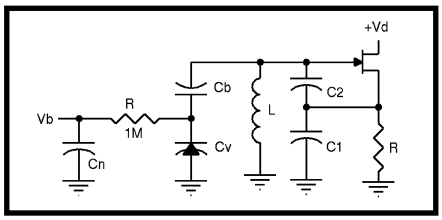


Figure 8—*This VCO is based on a Colpitts oscillator.*

of *Cv* depends on the bias voltage (Vb), the oscillation frequency is controlled by voltage.

In some cases, it's nice to make the oscillation frequency a linear function of the voltage. You can do this by using a hyperabrupt varactor with exponent *n* = *2* (see Equation 5). The capacitance then becomes:

$$C = Cv = Co \times \left(1 + \frac{V}{Vo}\right)^{-2} \qquad [17]$$

Substituting this into the equation for the oscillation frequency gives:

$$f = \frac{1 + \frac{V}{Vo}}{2\pi \times \sqrt{L \times Co}} \qquad [18]$$

which is a linear function of the voltage. A VCO with linear tuning can be used to create a frequency-modulated signal. In this case, the voltage is composed of a signal added to a DC bias voltage, which determines the center frequency.

You also may use a parallel LC resonant circuit containing a varactor in a tuned amplifier (see Figure 9). The LC combination takes the place of the drain resistor in a common source amplifier. The LC impedance is high only near the resonant frequency, so only signals near that frequency are amplified. By varying the bias voltage, you can tune the amplifier to different frequencies. Using a microcontroller and a digital-to-analog converter, you can set the varactor bias to tune the amplifier to preset frequencies.

One of the more exotic uses of a varactor is in a parametric amplifier, which takes advantage of its nonlinear characteristics. However, implementing a good parametric amplifier with a varactor can be tricky. We will not go into the details here; the following is just a general description of the concept from which you can hopefully see how a varactor might be used.

In a parametric or reactance amplifier, the value of a circuit parameter (capacitance or inductance) is modulated at twice the signal frequency. In its simplest form, if the modulation is in just the right phase with respect to the signal, energy will be pumped into the signal and amplification will occur. A familiar example of this phenomenon is a child on a swing. The child lowers and raises his center of gravity twice during each complete swing, thereby transferring energy into the swinging motion.

In the electrical case, consider an oscillating LC circuit (assume no resistance) with a parallel plate capacitor in which the plate separation can be changed. The capacitance decreases and the voltage as well as the energy of the capacitor increase if the capacitor plates are pulled apart when the charge on the plates reaches a maximum. If they're pushed back together again when there is no charge on the plates, the capacitance increases again but there is no change in the energy. There is then a net flow of energy into the circuit and the oscillation amplitude will increase.

In spite of the shortcomings of a lower *Q* than variable mechanical capacitors, varactors are indispensable in modern radio frequency devices because of the ease with which their capacitance can be changed and because they're much smaller size is perfect for portable devices. If you have an interest in making RF devices, getting to know varactors is well worth your time.

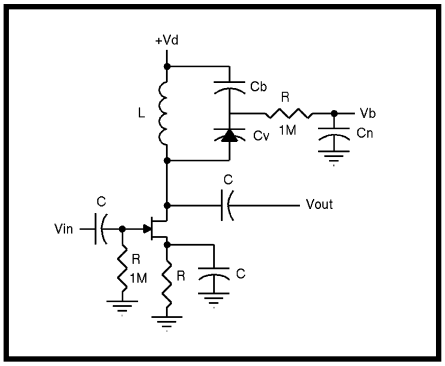


Figure 9—*One option is to use a parallel LC resonant circuit with a varactor in a tuned RF amplifier.*

Stefan Hollos and Richard Hollos design nuclear magnetic resonance (NMR) spectrometers and magnetometers at the company they founded, Exstrom Laboratories LLC. They each have degrees in both physics and electrical engineering. Stefan is like the professor on Gilligan's Island, who can make a radio with a coconut and a few scraps of wire. Richard is more like Gilligan, the essential human element in the realization of the professor's ideas.

SOFTWARE

To download the parts list, go to ftp.circuitcellar.com/pub/Circuit_Cellar/2002/139/.

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Ed Nisley

UHF Voice Radio

Continuing to look at the Radiometrix radio transceiver module, Ed considers some of the ins and outs of working with the BiM2 setup. Tune in and you'll get plenty of useful information not only about this project, but about radio design considerations, as well.

Deeply embedded radios have a special place in the radio world: they're invisible, so people forget they exist. I'm sure you recall the surprise shown by folks when they discovered that their cordless and cellular telephone conversations could be monitored, recorded, and played back to the world, regardless of any legalities.

Engineers working with embedded radios have an obligation to hide the usual control knobs and dials, if only because users have no interest in the RF part of the equipment. For example, a radio amateur may have the time and patience to select an appropriate operating mode and frequency, but a police officer needs information on his laptop concerning a suspected felon immediately.

The Radiometrix BiM2 FM radio transceiver module provides a bidirectional, low-power RF data link with a minimum of external hardware (see Photo 1). In fact, there are only three inputs (data, transmitter enable, and receiver enable) and three outputs (data, audio, and carrier detect). The digital signals are compatible with CMOS inputs and currents.

Although intended as a data radio, the BiM2 can also transmit and receive analog signals. I decided to see how it works as a simple, fixed-frequency voice radio that might be suitable for a bicycle/mobile intercom. Although it may seem silly to push voice through a data radio, doing so ensures a certain simplicity that helps focus attention on the analog and RF issues rather than the firmware required for digital data.

Along the way, we'll look at frequency modulation and deviation, signal level matching, what happens when there's no signal, and some of the nuances of breadboarding small parts. Pay attention and you'll save some time and effort when your next radio project comes along.

THE BIG PICTURE

In simplest terms, the circuitry shown in Figure 1 converts the audio signal from an electret microphone to the appropriate input voltage of the BiM2. The circuitry in Figure 2 reverses the process to produce an audible signal from the analog output of the BiM2. As in any design, it's the nuances that count.

The BiM2 operates at 433.92 MHz in the UHF band. It draws about 14 mA while transmitting 10 mW of RF power

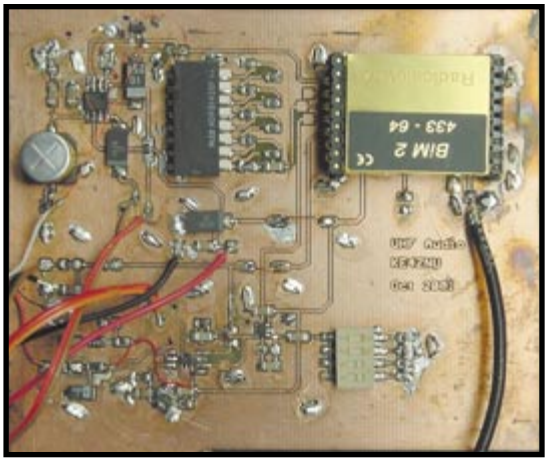


Photo 1—*The Radiometrix BiM2 UHF data radio can also transmit analog voice signals. The surrounding circuitry interfaces an electret microphone and an earbud to the analog I/O pins. Yes, the BiM2 module is plugged into its socket correctly, and, yes, the tiny red wires go to SOT23 packages epoxied dead-bug style to the board.*

and 18 mA while receiving, both from a nominal 5-V power supply. The supply ripple must be less than 20 mV_{PP}, which requires fairly good regulation on an AC-powered supply.

I was thinking of a portable application, so I decided to use the simplest possible power source. A 4.8-V, 850-mAh NiMH battery pack and a small trickle-charger board fit neatly into a dicast metal case. The charger schematic and layout are available on the *Circuit Cellar* ftp site, because I don't have room to discuss them in this column.

I reused the directional discontinuity ring radiator antenna you saw in my December column by trimming its ground plane to fit the top of the 4.5 square inch dicast metal case. A half wavelength of RG-174 connects the radio to the antenna. The ground plane dimensions changed, so the 50-Ω feedpoint also moved slightly.

You should also recall that although the BiM2 has been approved under European regulations, its 10-mW output power far exceeds the limits of the Part 15 rules imposed by the U.S. Federal Communication Commission. I am using it under the restrictions of an amateur radio license.

WHAT GOES IN...

The BiM2 radio was designed to transmit binary data, so its analog input expects high-level digital signals rather than low-level analog voltages. The RF output frequency depends on the instantaneous input voltage, which is the definition of frequency modulation.

The nominal output frequency, 433.92 MHz, lies near the center of the actual range of frequencies produced by the BiM2. The specifications allow an initial frequency error of ±50 kHz and a maximum overall error of ±100 kHz from the transmitter.

The initial receiver frequency error is ±50 kHz, so the maximum total error of ±150 kHz lies within the 400-kHz bandwidth of the receiver (200 kHz on either side of the actual center frequency). As a result, no tuning is required between any two BiM2 units using binary data. However, if you intend to use a BiM2 with other radios, you may need to adjust it to match their expectations. The deviation used for narrow-band FM voice in the amateur service is ±5 kHz around the center frequency and voice channels are separated by 15 to 25 kHz, so the actual transmit frequency of the BiM2 may appear on any one of several separate channels.

The nominal frequency deviation of the BiM2 is 30 kHz. That figure represents the total deviation rather than plus or minus around the 433.92-MHz center frequency. One of my units produced 433.896 MHz with 0-V input and 433.927 MHz at 5 V, which is a range of 31 kHz. At 2.5 V—half of the power supply—the output frequency was 433.909 MHz. Applying 4.5 V tuned it to 433.920 MHz.

Because the input signal cannot exceed the supply voltage or go below 0 V, a DC offset not at the midpoint reduces the AC modulation range available to your data. For example, a 4.5-VDC bias reduces the maximum AC modulation range to only ±500 mV.

A straight-line fit to my measurements (or simple division of the specification sheet values) reveals a slope of about 6 kHz/V. That is, changing the input voltage by 1 V changes the output RF frequency by 6 kHz. Looked at another way, achieving a 10-kHz total RF modulation range requires 1.67 V peak-to-peak or 0.83 V peak.

If you must set your ham voice transceiver to exactly 433.920 MHz, you can't tune the BiM2 radio I used to that frequency and adequately modulate the signal. On the other hand, there's no reason you can't set the transceiver to, say, 433.91 MHz, apply just over 2.5 VDC to the BiM2, modulate it at 1.7 V_{PP}, and live happily ever after. You must simply understand what the specification means in real life.

Trimpot R8A in Figure 1 adjusts the DC bias voltage by 1 V to tune the output through a 6-kHz range. Typical FM UHF radios have a 5-kHz tuning step, so you can tweak the output frequency to the nearest step. As you can tell from the "A" part number suffix I gave the trimpot, it's a convenience rather than a necessity. There's more to the tuning story, but let's follow the audio signal through the remaining circuitry first.

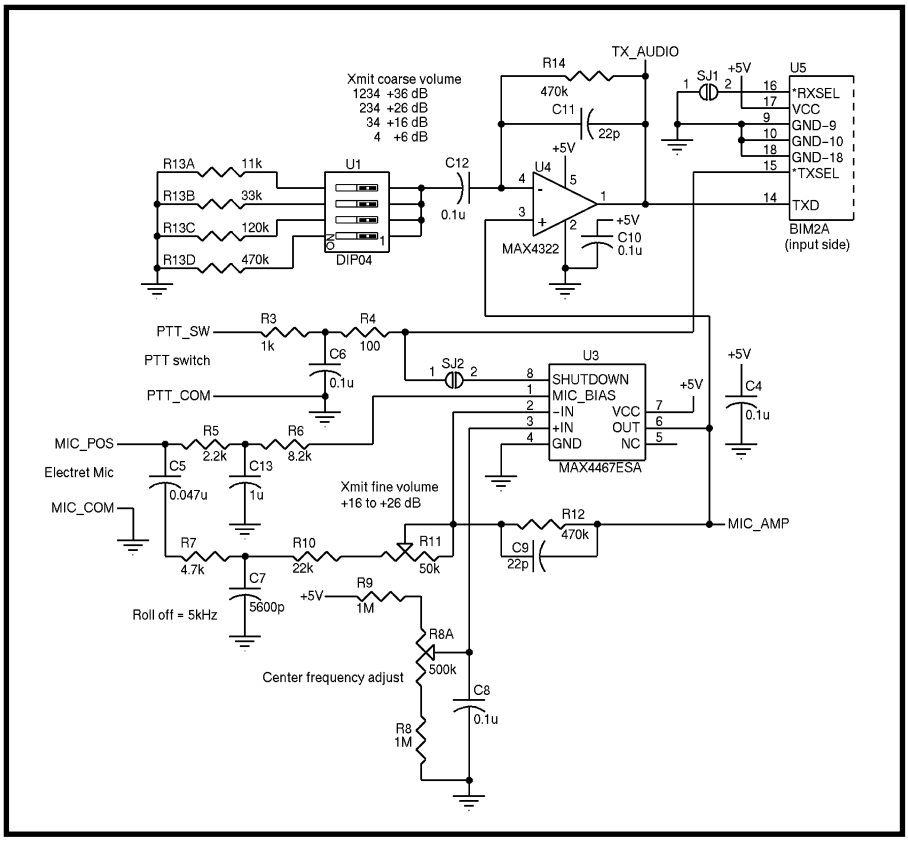


Figure 1—*The electret microphone signal requires about 30 dB of amplification to produce an adequate FM deviation. A Push-to-Talk switch activates the MAX4467 mic amplifier and enables the BiM2 RF transmitter. R8A sets the transmit frequency, which is nominally 433.92 MHz ±150 kHz*

U3, a MAX4467 microphone amplifier, includes a FET that controls the microphone bias and shuts down the internal op-amp. By controlling the mic's power with the push-to-talk signal, you can reduce the total power drawn by the circuit when it isn't actually transmitting. Given that you spend most of your time listening rather than talking, that makes perfect sense.

At least that's what I planned to do. As it turned out, the samples from Maxim were something else entirely, in a SOT23-8 package rather than the SO8 I expected. Surface mount parts are too small to display a part number, so Maxim uses a three- or four-letter "topmark" instead. The topmark, AAII, didn't correspond to any known part and, when I hand-wired one into the circuit dead-bug style (epoxied upside-down to the board on its back, with teensy wires soldered to its legs), it didn't play.

So, I replaced it with a MAX4322 SOT23-5 op-amp and that worked fine. The board and schematic show a MAX4467 in the SO8 package, which I'll use in the next iteration of my board.



Photo 3—*The yellow arrow marks a pin pushed out of position after nearly two years of bicycle/mobile use.*

DIP switch S1 and trimpot R11 adjust the input gain over a 40-dB range, which covers the wide variety of electret mics in my collection and also allows for considerable deviation tweaking. You have the option of setting the gain precisely if you have an FM deviation meter, but simply adjusting the gain so you sound about as loud as when you talk on a standard transceiver will suffice.

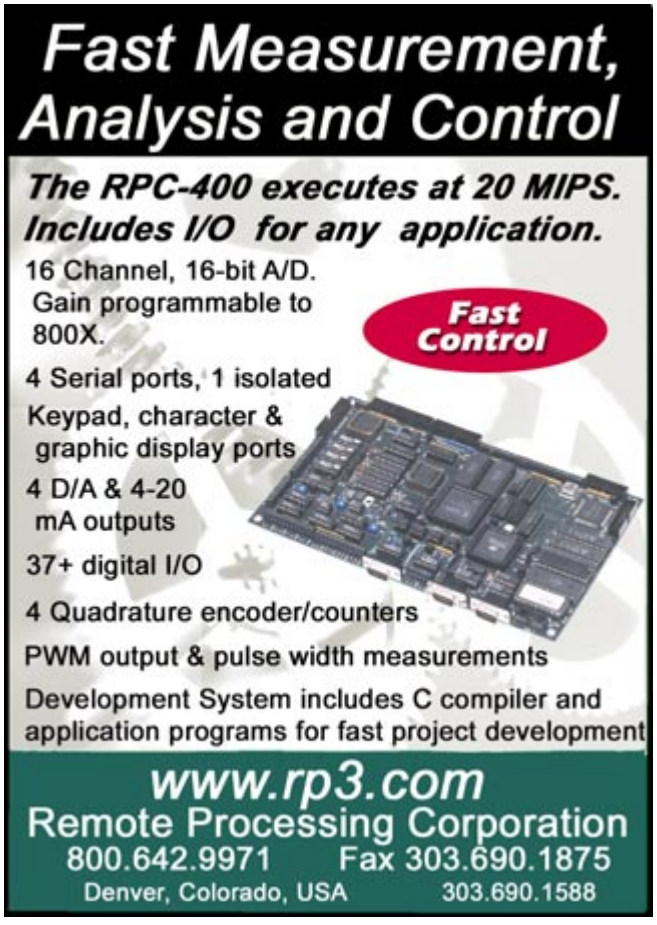
The remaining input circuitry rolls off the audio frequency response on both ends, protects the inputs from static zaps and RFI, and generally handles the minutiae of getting outside signals into the box. I've covered these topics in previous columns, so there's little new ground to cover here.

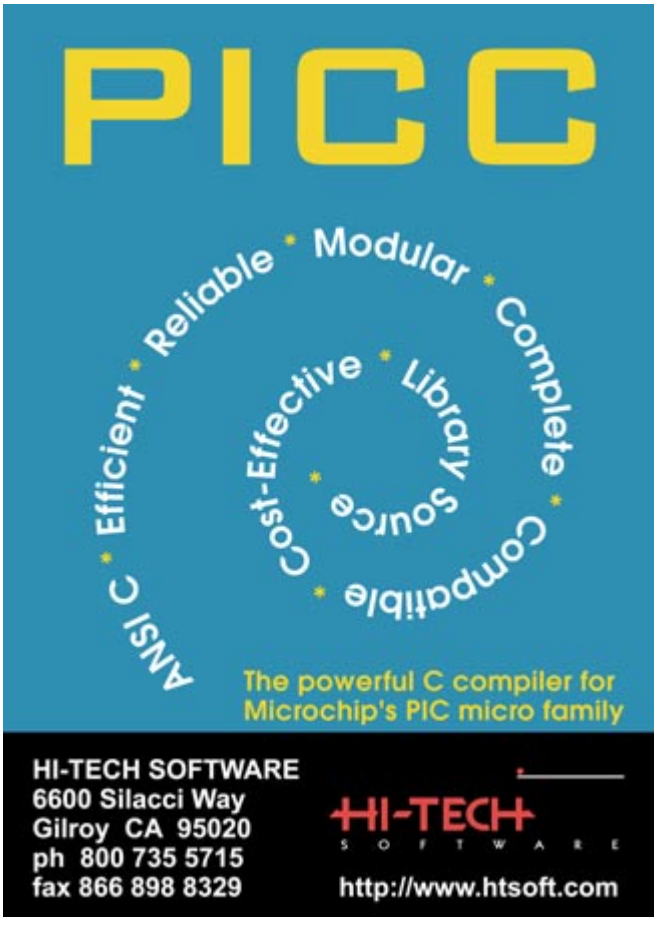
Having launched the RF into the ether, let's see what happens when it hits the antenna. Incidentally, the BiM2 receiver can be active simultaneously with its transmitter, meaning you can listen to what you transmit. Use an earbud to prevent feedback through the mic.

...MUST COME OUT

As shown in Figure 2, the BiM2 has one output for digital data and another for the corresponding analog signal. Most data radio applications use RXD, which comes from a comparator that slices the signal around its short-term average value. The input to that comparator, the analog output from the FM demodulator, appears on the audio frequency (AF, which is radio jargon for the audio output) pin. The specs call for a 400-mVAC signal with a 1.25-VDC bias, which presumably occurs at the nominal 30-kHz deviation.

Therefore, the 10-kHz total deviation produced by ham radio transceivers will result in a 130-mV_{PP} out-





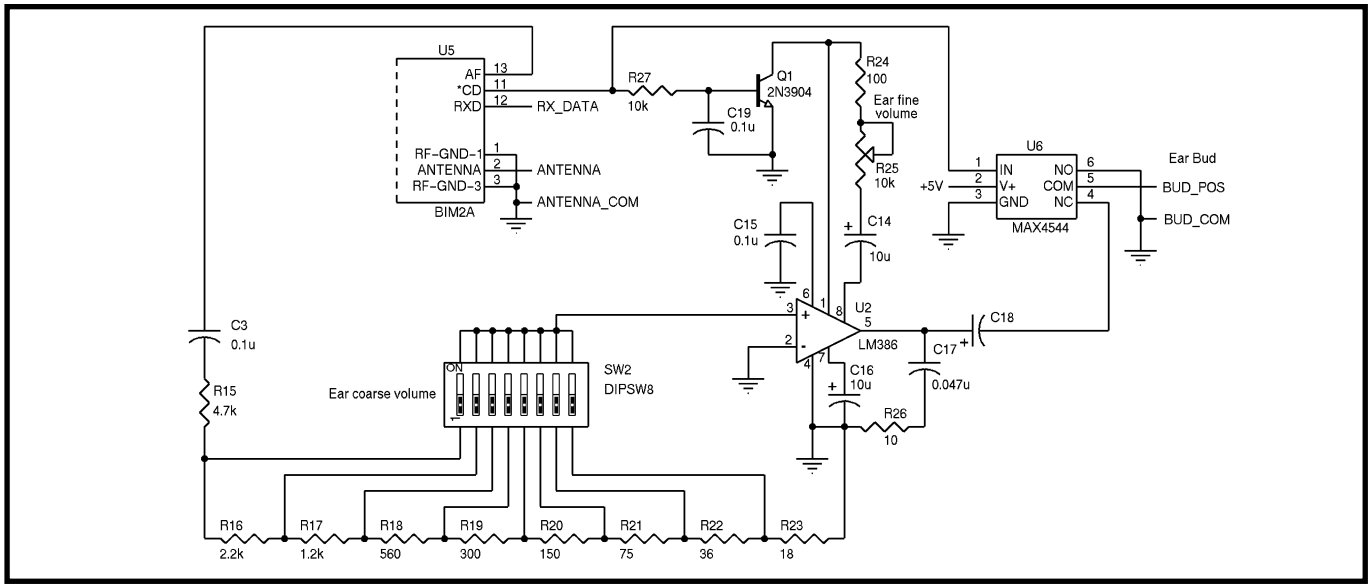


Figure 2—*With the BiM2 *RxSel input tied low, the AF output is always active. The *CD output mutes the LM386 output and connects the earbud to ground to eliminate noise and muting clicks. SW2 sets the overall output attenuation.*

put signal. The average value may be perhaps one third of the peak-to-peak value, so the audio output from the BiM2 will be fairly low.

When the receiver detects an RF signal, the receiver sets the *CARRIER DETECT pin low. A high *CD output should mute the audio output. Photo 2 illustrates why this is a good idea; with no signal, an FM receiver produces nearly full-scale white noise. When you adjust the normal audio to a suitable level, +38-dB noise will be deafening!

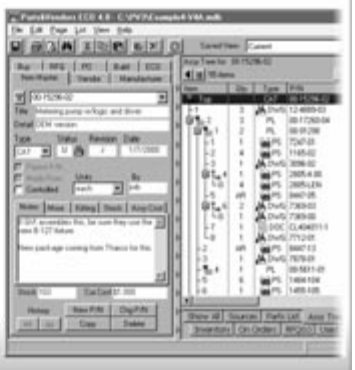
An integral part of every FM receiver is a high-gain RF amplifier that converts the incoming analog signal to a two-level equivalent (either high or low). The next stage, the discriminator, converts the frequency changes into audio voltages.

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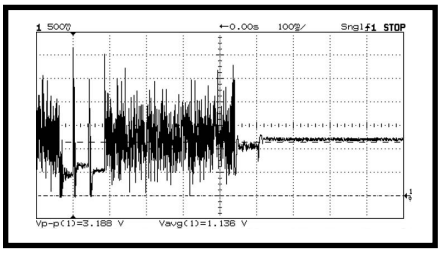


Photo 2—*The AF output is 3 V_{PP} white noise with no received RF. Typical received audio in the right half of the trace is 40 mV_{PP}, nearly 38 dB below the noise. The three blips on the left are interference from the IF oscillator of my scanner radio.*

With no signal present, however, the RF amplifier turns the ever-present, low-level background noise into full-scale hash, which the discriminator interprets as nasty audio with random transitions (white noise).

The left half of Photo 2 shows empty channel noise, and the right half is quiet audio sent from a ham transceiver. The three quiet intervals just after the trace begins are interference from my ancient Bearcat 101 radio scanner; on three successive UHF channels, the LO of the scanner radiates strongly enough to convince the BiM2 it hears something. Unfortunately, the audio during those blips is a piercing whine. So, I had to park the scanner on a VHF channel whenever I was working with the BiM2. This isn't the data radio's fault, because the radio is receiving what it thinks is a perfectly valid UHF signal.

Pulling the *RxSelect input low enables the BiM2 receiver. To save power, you could enable the receiver for a few milliseconds several times each second and check the *Carrier Detect output for activity each time. If *CD is low, then you would enable the receiver constantly until there's no activity for a minute or so.

I simply tied *RxSelect low because I didn't want to get involved with firmware. Besides, with no microcontroller, you have no digital RFI. The total current draw for the entire circuit is about 23 mA in Receive mode, which the 850-mAh battery can supply for nearly 40 h.

The resistor string attached to DIP switch SW2 attenuates the audio output by 6 dB per step. Normally, you'd use an R-2R divider to get perfectly equal steps, but I didn't relish soldering that many resistors (alas, my parts collection lacks any matched R-2R SIPs). Trimpot R25 provides variable gain between the steps, which is why the string need not be particularly accurate.

The LM386 audio amplifier isn't state of the art, but my parts collection did have a few of them. Transistor Q1 mutes the LM386 output when *CD goes high, but with a devastating pop and some residual hiss. As a last resort, I used a MAX4544 DPDT analog switch to force the earbud wire to ground. I suspect a more modern amplifier would work much better.

UNLESS IT STAYS THERE

Inside BiM2 radios, a trio of surface acoustic wave (SAW) filters and oscillators set the overall RF frequency and bandwidth. As you've seen, the DC bias on the TXD pin controls the actual transmit frequency.

Two main factors,voltage and temperature, affect the frequency. I conducted a simple study to see what effect those factors would have on the operating frequency.

NiMH batteries, as with NiCd batteries, have a fairly flat discharge characteristic. Although this makes metering gas gauge capacity essentially impossible, it removes much of the need for regulation in many circuits.

The output voltage of the battery pack I used decreased by about 10% over most of its 34-h life and was well within 5% during the middle 24 h. The radio specs allow operation between 4.5 and 5.5 V, with an absolute maximum of 10 V, so the voltage range is certainly fine.

I popped the radio in the refrigerator over lunch and found that the output frequency increased by about 5 kHz over the next 30 min. That temperature is well within the specified range, and, in any event, I try not to ride my bike on refrigerator-like days.

The effects of power supply and temperature variation would not affect a wide-band data link using the BiM2 radios. If you're communicating with a BiM2 using another transceiver, you may need to retune it every now and again. I don't think this will be a major problem.

CONTACT RELEASE

My next iteration of the circuit will include a voltage regulator to hold the TXD bias more constant, plus a better earphone amplifier. Your first version of the circuit can take advantage of what you've learned here.

When I discussed electret mics in August 2001, I mentioned that I use mini-DIN connectors on the helmet cable ("Mic Check—A Communication System for Cyclists," *Circuit Cellar* 133). Photo 3 shows what happened to one of them after about two years; the plug rammed a socket pin back into the connector body.

Of course it wasn't a surprise that this was an intermittent problem. Whenever the offending pin disconnected and reconnected the power of the electret mic, the mic amplifier drew enough current from the radio's audio line to briefly turn on the transmitter. That was enough to "kerchunk" the repeater without me knowing it.

Fortunately, several people told me I was having audio problems and, after examining everything else, I tore the connector apart. Rule of thumb: It's always the connectors.

Ed is a registered Professional Engineer, electrical engineer, and a ham radio geek (call sign KE4ZNU). You may contact him at ed.nisley@ieee.org.

SOFTWARE

To download the schematic and layout, go to ftp.circuitcellar.com/pub/Circuit_Cellar/2002/139/.

SOURCES

DJ-C5T dual-band HT
Alinco
www.alinco.com/usa.html

ICOM IC-820H base transceiver
Icom America, Inc.
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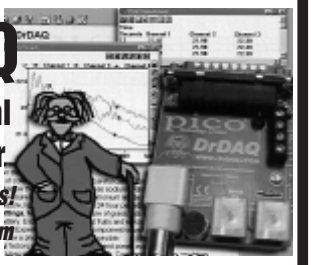
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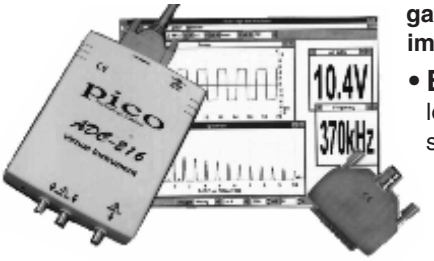
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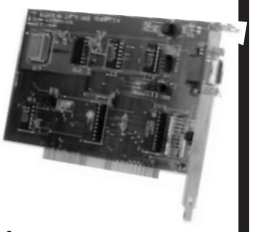
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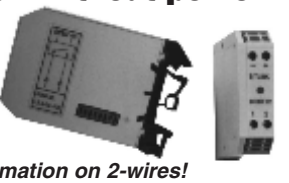
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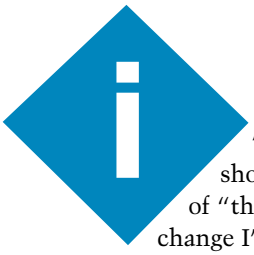
APPLIED PCs

Fred Eady

"The" Embedded Project

Part 2: Into the Hardware and Software

With parts in hand, Fred gets started on his mission to design a better way to program PIC flash memory in the field. Software and hardware setbacks stopped completion of "the" embedded project, so Fred takes us through some of the solutions he found.



'm ready to show you the rest of "the" project. For a change I've done just as much thinking as soldering and coding to make it complete. As my mind was assembling the big picture, I realized that to make this project as efficient as possible, I would need some sub-millisecond precision timing code. Also, after applying common sense coupled with a little bit of logic and a couple transistors, I completely eliminated the need for the step-down simple switcher electronics. You'll also see that I went low-tech on the step-up switcher design.

In the midst of all of this high-level, low-tech thinking and tinkering, I got tired of running jumpers on the phenolic side of Radio Shack's single-sided perfboards and did something about it. I had to employ a technique used by NASA to finalize and legitimize the step-up switcher design. In the process, I created a design tool that may be useful if you need to design step-up switchers with the LM78S40 switching regulator IC.

RIGHT ON TIME

I designed "the" project to afford an easy way to program Microchip flash memory parts with code I use most often using a low-cost SBC and my laptop. Programming OTP and windowed PIC microcontrollers requires specific voltages coupled with fairly precise timing periods. Typically, the minimum pulse width required for programming the OTP and windowed parts is 100 ns. The same holds true for flash memory-based PIC micros. The 100-ns pulse width specification is called out as a minimum width for clock pulses used to read and write data and commands to and from the target microcontroller. Maximum programming pulse widths in the hundreds of microseconds are the norm for standard baseline and mid-range PIC parts whereas flash memory part programming timing delays range into the tens of milliseconds.

For all PIC parts, read/write operation is triggered on the leading edge of the clock pulse for reads and trailing edge triggered for writes. Because read/write operations are performed on the edges of a pulse, this means that the 100-ns minimum clock pulses can be much wider if necessary. The only restriction is that a 1-µs minimum delay must be enforced between the end of a command and the next command. Some programming commands must be followed by data and the 1-µs delay rule applies for the end and beginning of the next datastream, as well.

Because this project is aimed at flash memory microcontrollers, the read/write clock pulses can extend into microseconds and milliseconds if necessary without affecting the data integrity. The programming period for flash memory parts is specified as anywhere between 4 and 10 ms depending on the part. Thus, in terms of this project, the shortest delay that will have to be dealt with is 1 µs. Additionally, the 1-µs inter-command delay is the minimum recommendation, so you can extend it if you need to.

At 20 MHz, a flash memory-based PIC16F877 has a single instruction cycle time of 200 ns. This boils down to a minimum no-overhead timing window of 200 ns, which can be initiated by a simple no operation (NOP) instruction. Depending on clock speed and operating code, a standard PC could possibly generate similar tim-

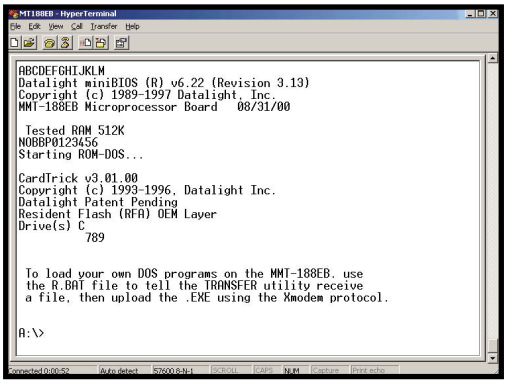


Photo 1—*Datalight reigns on the MMT-188EB. The miniBIOS eliminates the need to cram a full-function BIOS into an SBC that doesn't really need one. The flash memory disk is used to store programs and PIC data is made possible by CardTrick.*

ings. To do this would take custom code designed to reduce or eliminate the effect of overhead processing.

The problem is that if you're not up to writing a custom kernel (I'm not.), you will encounter overhead, because a desktop most likely is running an operating system with dependent applications. Most of today's commercial operating systems don't take kindly to anyone tinkering directly with timing generated by processor cycles or hardware clocks. Stealing too many cycles from these sources will affect the system clock and any process or application that depends on the system clock could be compromised.

There's a similar situation with the MMT-188EB because it's built on the same foundation as the desktop PC and is running a version of Datalight's ROM-DOS. A standard 100% compatible PC runs a hardware system clock with a period of 838.1 ns. A hardware counter counts down from 65535 to zero and issues an interrupt. This software interrupt is commonly known as the hardware timer tick, which occurs every 54.925 ms. To obtain timing periods and delays in the microsecond range, you'll have to somehow tap into the hardware system clock and extract only enough cycles to make specified timing windows shorter than 54.925 ms.

EXACTICKS/DOS

The first law of embedded computing states that nothing is free. The second law reads: When it comes to solving a problem, sometimes it isn't what you know but whom you know. I've used ExacTicks precision timing routines for years in my Visual Basic code; and there's no way I'm going to reinvent the wheel or write sloppy workaround timing code for "the" project as long as Ryle Design is around. So, I headed over to Ryle Design's web site. There, along with my trusted VB timing code, was the newly updated DOS version of ExacTicks, called ExacTicks/DOS, and it was just a credit card number and download away.

The VB version of ExacTicks was painless to install and use; it looks like that philosophy spilled over from PC timer tools (the original ExacTicks DOS timing code that preceded the VB version). ExacTicks/DOS comes with code that enables the ExacTicks/DOS routines for Borland Turbo C and Turbo C++, Borland C++, Microsoft C and C++, Intel 386 C Code Builder, and Zortech C and C++. Basically, all you have to do to install ExacTicks/DOS is execute some self-extracting files that blow up into source code, header code, and batch files to create the desired ExacTicks/DOS environment.

After following the simple steps outlined in the ExacTicks/DOS documentation, I ended up with a set of ExacTicks/DOS libraries that I copied into the LIB directory of my Borland C++ installation. A header file for the libraries was also provided and I stuffed that away in the include directory. As you can imagine, I'm pretty excited now as the next step is to fire up the MMT-188EB and test the ExacTicks/DOS functionality.

I prefer Tera Term Pro as a terminal emulator (it's free and emulates the DEC VT series of terminals), but some of its file transfer functions don't work as designed when running under Win2k. So, Photo 1 is a shot of HyperTerminal containing contents of the MMT-188EB start-up dialog. ExacTicks/DOS comes with sample programs to get you acquainted with the precision timing calls and their structure. I compiled an example program that would allow me to enter a desired delay period and have the program report back the accuracy of my selection.

For this project, I'll be generating delays, so the actions I can perform in Photo 2 are of particular interest. ExacTicks/DOS contains a routine to determine the minimum delay the system it is running on can generate. From the shot shown in Photo 2, you can see that the minimum delay the 20-MHz MMT-188EB running ROM-DOS can do is 3 µs with a resolution of 5.4 µs. Being an experienced user of ExacTicks, the 5.4-µs figure seemed odd. Anyway, I chalked this up to the resolution of the timing influenced by the speed and overhead within the MMT-188EB ROM-DOS-based system.

So, with that seemingly positive feedback, I selected "Microsecond" and entered 10. This didn't go well. The program returned with an error telling me it could not time the 10-µs delay. So, I entered a bigger microsecond delay of 100 µs. I got the same result. What's going on here?

I know the ExacTicks/ DOS software works. So, I need to put the ExacTicks/DOS on a PC loaded with Bill's DOS 6.22 and see what happened. (I keep a DOS-only machine stashed for moments like this.) Sure enough, the ExacTicks/DOS worked to perfection on the PC. Houston, we have a problem.

It was time to regroup and do some supplementary reading. So, my next step was to pull out the Datalight ROM-DOS manual. I found a blurb

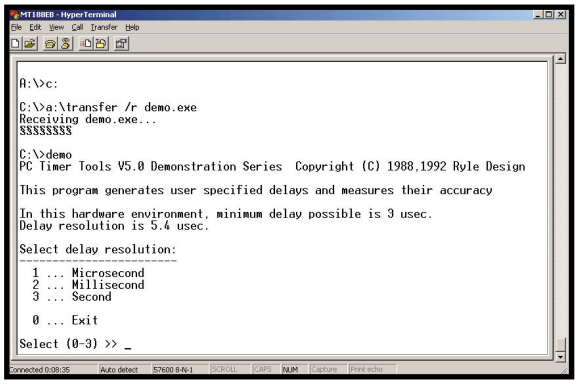


Photo 2—*If you didn't know better you would assume that a desktop PC is behind these operations.* `DEMO.exe` *was transferred from my desktop to the MMT-188EB C drive using XMODEM.*

about turning off the microprocessor real-time clock in favor of an external timekeeping component when generating the miniBIOS. Could this have been done?

I then turned my attention to the 80C188 datasheet. I wanted to know if the timer/counter module in the 80C188 of the MMT-188EB is similar to or identical to the '8253 or '8254 used in 100% compatible desktops since the 8088 days. ExacTicks/DOS depends on this legacy timing system to generate its delays. However, after unsuccessfully trying to find any reference to the original timer parts, my conclusion is no, the 80C188 timer/counter unit is not a true clone as far as ExacTicks/DOS is concerned.

I've never blown smoke at you and I don't intend to start with this article. So, applying the second law of embedded computing, I picked up the phone and called Rick at Midwest Micro-Tek. Rick and I reached an agreement that maybe ROM-DOS was indeed configured to take over the functionality of the old 8253 IC. That was enough for me on the hardware side, but I needed indisputable evidence from the software side as well.

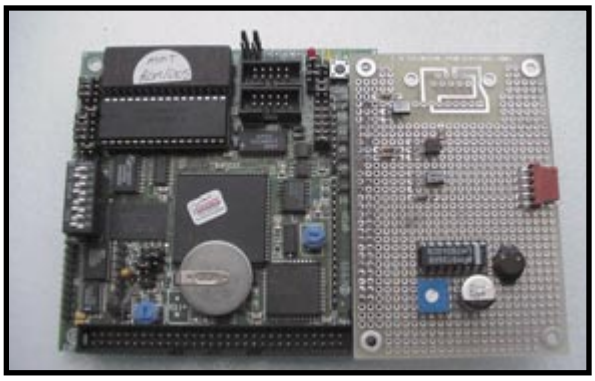


Photo 3—*It seems that every board I rig up needs a DE9 to interface to a serial port. On the Radio Shack boards, I had to dig out a hole to mount the DE9 because the shell connector pins aren't laid out on 0.100″ centers between the rows. So, note the DE9 area on the custom perfboard.*

So, I put the second law into motion again and called Tom at Ryle Design. After describing the behavior of ExacTicks/DOS, Tom and I agreed that either the 80C188 timer module was not set up to be a PC-compatible tick generator or ROM-DOS was having fun at my expense. Tom did mention that ROM-DOS should not affect ExacTicks/DOS, as ROM-DOS is Gates-like and the ExacTicks/DOS code goes after the hardware timer for its timing.

After consultation with the designers of both the MMT-188EB hardware and ExacTicks/DOS software, the final determination is that the MMT-188EB is working as designed and ExacTicks/DOS is OK. I tested the latter on a Gates-controlled PC and ROM-DOS is doing what it's been told to do. The conclusion is that for some unknown reason the 80C188 timer counter unit isn't producing what ExacTicks/DOS is expecting to see when running ROM-DOS.

ExacTicks is a great precision timing package and I'm sure I'll use it again in the future on a '386 or better SBC. Unable to use ExacTicks/DOS in this project, I resorted to using a homebrew timing routine. This will

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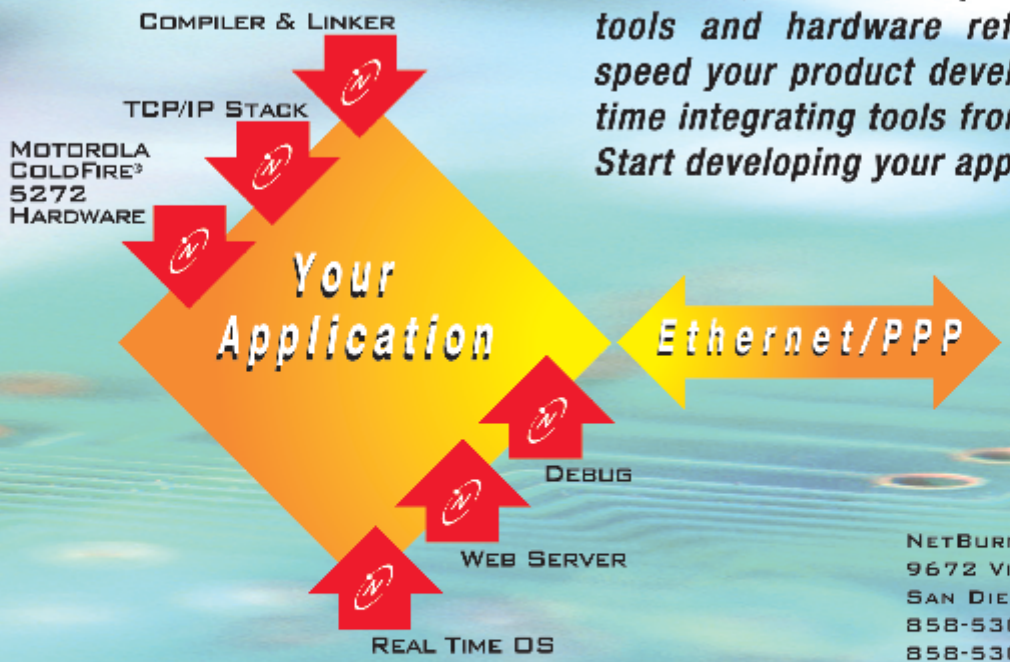
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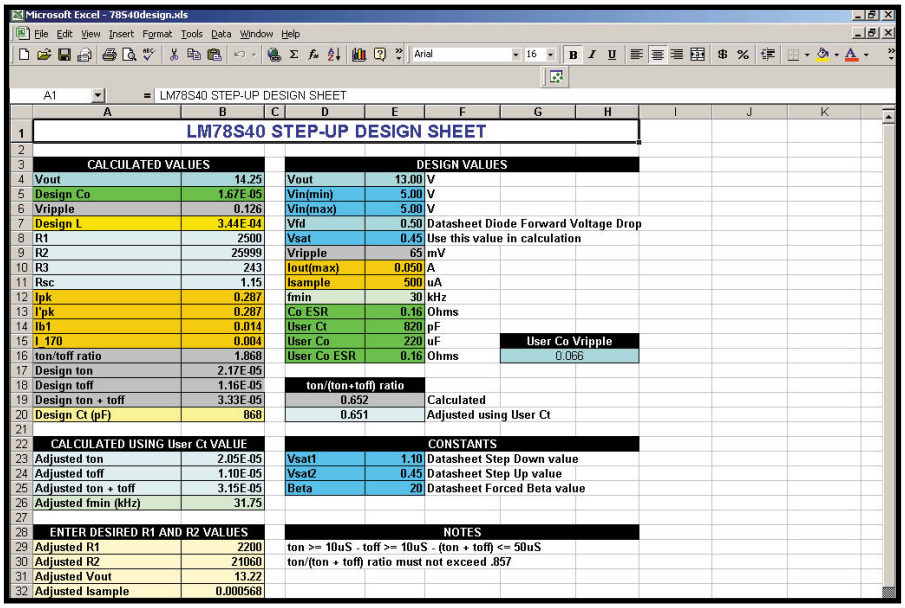
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File Edit View Insert Format Tools Data Window Help

A1 = LM78S40 STEP-UP DESIGN SHEET

LM78S40 STEP-UP DESIGN SHEET

CALCULATED VALUES		DESIGN VALUES			
Vout	14.25	Vout	13.00	V	
Design Co	1.67E-05	Vin(min)	5.00	V	
Vripple	0.126	Vin(max)	5.00	V	
Design L	3.44E-04	Vfd	0.50	Datasheet Diode Forward Voltage Drop	
R1	2500	Vsat	0.45	Use this value in calculation	
R2	25999	Vripple	65	mV	
R3	243	Iout(max)	0.050	A	
Rsc	1.15	Isample	500	uA	
Ipk	0.287	fmin	30	kHz	
I'pk	0.287	Co ESR	0.16	Ohms	
Ib1	0.014	User Ct	820	pF	
I_170	0.004	User Co	220	uF	User Co Vripple
ton/toff ratio	1.868	User Co ESR	0.16	Ohms	0.066
Design ton	2.17E-05				
Design toff	1.16E-05	ton/(ton+toff) ratio			
Design ton + toff	3.33E-05	0.652		Calculated	
Design Ct (pF)	868	0.651		Adjusted using User Ct	
CALCULATED USING User Ct VALUE		CONSTANTS			
Adjusted ton	2.05E-05	Vsat1	1.10	Datasheet Step Down value	
Adjusted toff	1.10E-05	Vsat2	0.45	Datasheet Step Up value	
Adjusted ton + toff	3.15E-05	Beta	20	Datasheet Forced Beta value	
Adjusted fmin (kHz)	31.75				
ENTER DESIRED R1 AND R2 VALUES		NOTES			
Adjusted R1	2200	ton >= 10uS - toff >= 10uS - (ton + toff) <= 50uS			
Adjusted R2	21060	ton/(ton + toff) ratio must not exceed .857			
Adjusted Vout	13.22				
Adjusted Isample	0.000568				

Photo 4—*The Design Values entries are used to compute the component values used in the LM78S40 step-up circuitry. The new Microchip flash memory MCLR pins are level sensors only and don't draw current when the MCLR pin voltage is raised to Vpp (13 VDC). This is because the flash programming voltage is generated internally. I specified a 50-mA load current (Iout(max)) just in case I wanted to power an LED from the 13-V line.*

slow things down a bit, but because I'm targeting flash memory microcontrollers, I can work around this unexpected handicap without affecting the functionality of the project.

STEPPING UP WITH THE 78S40

Because most of my PIC code loads will be performed against in-circuit PIC devices, there's no need to switch the target PIC's supply voltage (5 V or V_{CC}) separately from the project. I won't be inserting or removing the target PIC into or out of a socket. I simply hooked up the unit to the necessary target PIC pins using Microchip's ICSP method: apply power to the target PIC, do the work, remove power, and remove the ICSP (in-circuit serial programming) hook up.

Another reason for abandoning the step-down simple switcher is that I found a regulated 5-VDC power brick rated at 1 A. (In fact, I have about 100 of them leftover from an old project.) In addition to putting the simple switcher out of work, the 5-V power brick also eliminates the need to regulate the voltage needed to power the MMT-188EB. Not having to provide a 7805 regulator makes the power brick-to-MMT-188EB connection remarkably clean.

The MMT-188EB interfaces its 24 8255 I/O pins to the outside world using a 50-pin OPTO22 interface. Pin 49 of the OPTO22 connector provides 5 V and pins 2–50 are grounded. This arrangement allows me to pass the 5-V supply of MMT-188EB, provided by the newfound regulated power brick, through the OPTO22 pin to the step-up circuitry. The step-circuitry is mounted on a custom-designed, plated-through-hole perfboard, which is hanging off the MMT-188EB OPTO22 interface (see Photo 3). Of course, by hanging the perfboard on the OPTO22 connector, the 8255 I/O signals are also easily accessible to the step-up electronics.

The components on the custom perfboard are admittedly low-tech, and I'm proud of that. After all, the third law of embedded computing states that simple is always better. My initial choice for a step-up switcher IC was tiny SOT-23 surface mount parts from Linear Technology. Although those devices are great, after weighing the options, I settled on the LM78S40 because of its high availability, low cost, and ease of implementation.

Two main reasons I redirected to the LM78S40 are because I didn't want to design a special printed circuit board for the Linear switcher and I'm not restricted by space. Also, it's much easier to experiment with standard through-hole parts that can be easily mounted on and removed from standard 0.100″ center pads. Using a

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perfboard with plated-through holes allows me to mount components on both sides of the perfboard and easily make connections between the top and bottom sides of the perfboard. Another plus is that I can mount a passive SMT or standard through-hole component such as a resistor or capacitor on one side of the board and access its physical connections via either side of the board.

Figure 1 illustrates the final layout of the project. With the assistance of an 8255 I/O pin, transistors Q1 and Q2 control the flow of 5-VDC power from the MMT-188EB to the LM78S40 step-up circuit. The collector of Q3 is attached to the target PIC's MCLR pin and is used to reset the target PIC under control of the 8255-based I/O port of the MMT-188EB.

The LM78S40 contains all of the necessary switching regulator subsystems to effect step-up, step-down, and voltage-inversion switching functions. A free-running oscillator and a comparator feed an AND gate, which sets a latch which ultimately drives a pair of switch transistors. The LM78S40 also incorporates a 1.25-V reference, an integrated catch diode, and an independent 741-like operational amplifier. The catch diode and opamp won't be used here.

Designing the circuitry that surrounds the LM78S40 is not as glamorous as it is for the simple switcher and Linear Technology parts, because there are no fancy Java applets to help you select the right parts. I found myself going between the LM78S40 datasheet [1], an LM78S40 application note [2], and a Motorola handbook. [3] The design process became more and more confusing because I couldn't get the resultant formulas to match the datasheet, app note, and handbook. Some of the problem was simply misprinted answers to equations, which I could verify and overcome using my brain and my calculator. Bigger problems presented themselves as misplacements of the formula variables. Houston, do you read?

NASA is known for its penchant for redundancy. I remember someone telling me about how some of the computer arrays on Orbiter decide who's right and who's wrong. It was explained to me that three separate but identical computers synchronously compute data from the same input points. If two of the three computers come up with the same answer, the answer from the third computer is considered bogus and the majority answer is accepted. Well, NASA gets people and equipment back and forth to space this way. So, why not apply the majority computational rule to "the" project, as well.

I ran the numbers from each of my three LM78S40 design sources and threw out the values that didn't match. I also compared the design formula variables and construction of the formulas and nixed the ones that didn't match visually, mathematically, or logically with the others. The result of my formula cleansing is shown in Photo 4.

LM78S40 DESIGN TOOL

The wish list of resulting and known voltages, currents, ripple content, and switching frequency are entered between the V_{OUT} and fmin cells under Design Values. This is enough information to produce the theoretical values based on the datasheet formulas in the cells below Calculated Values.

Most of the time calculated capacitance values are not standard values. Entering user-selected standard capacitance values in the green cells under Design Values will change the original calculated values. I've included some cells to show the results of your changes. For instance, the calculated output capacitor value (Design Co) in Photo 4 is the minimum value computed with the benefit of the output capacitor (Design Co) ESR value contained in the green Co ESR cell. I used a Panasonic FK series 220-µF at 35 WV ESR value for the Co ESR and the User Co capacitance value to eliminate the effect of ESR values that differ on the calculated and user-selected capacitance values.

Consequently, the design Vripple is almost twice my design target value of 65 mV. After entering various standard capacitance values in the User Co cell and using the ESR figures given by the Panasonic FK series capacitor datasheet in the User Co ESR cell, I wound up with a final 220-µF Co value. This

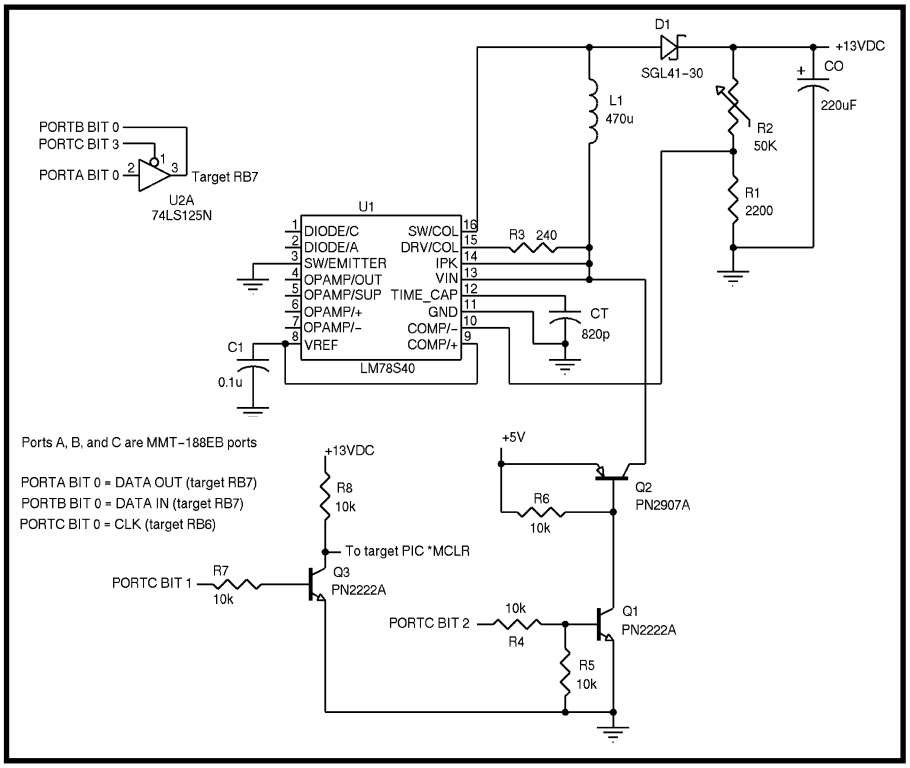


Figure 1—*Law three of embedded computing states that simple is always better. This final schematic is a prime example of that statement's correctness. The 4053 is replaced by three transistors and some resistors. The step-down switcher, 7805, and 9-VDC power supply never made it to the page. The 74LS125 gate isolates PORTA output from PORTB input without having to reset the onboard 8255.*

provided a Vripple figure (User Co Vripple cell) that closely matches my target Vripple figure specified in the Design Values cell.

I substituted the standard value of 820 pF in the User Ct cell because 868 pF is not a standard value (Design Ct). The replacement changed the switching frequency and duty cycle as shown in the cells beneath Calculated Using User Ct Value. One of the Notes fields states that the on versus off pulse width ratio should not exceed 0.857. This is verified by the calculated and adjusted values under the ton/(ton+toff) ratio header.

The same standardization of component values can be performed with the LM78S40 resistor complement. R1 and R2 under Calculated Values will produce the desired results but odds are you won't find either value to be standard. So, under Enter Desired R1 And R2 Values, I input a 2200-Ω baseline for R1 (similar to the 500-µA target of Isample in the datasheet). Then, I entered various R2 values until I obtained the desired adjusted V_{OUT} value.

The ideal Isample current value is 500 µA, so I can live with the new Adjusted value of 568 µA. R3 is close enough to the standard value of 240 Ω, which is what it will become. I opted to not use the Rsc value, because I'm not concerned with current limiting or runaway current consumption. It looks like R2 will be a 50-kΩ potentiometer because I want to be able to tweak the 13-V source.

S.M.O.P.ING UP

The hardware design is wrapped up and all that's left to do is S.M.O.P. (simple matter of programming) up. Code to send an Intel hex file for programming, retrieve the target PIC data in Intel hex format, and erase the target PIC is available on the *Circuit Cellar* ftp site. There's nothing revolutionary about the code, it's modeled after the flowcharts in the Microchip 16F*xxx* programming specifications. The upload and download procedures are already in place as the HyperTerminal/MMT-188EB/ROM-DOS combination performs these operations flawlessly.

I heard that Midwest Micro-Tek will reduce the cost of the MMT-188EB by $100 by the time this article is in your hands. Also, updated precision timing code from Ryle Design should be available by the time you read this.

Again, the laws of embedded computing are preserved. When it comes to solving a problem, sometimes it isn't what you know but whom you know. And, of course, it doesn't have to be complicated to be embedded.

Fred Eady has more than 20 years of experience as a systems engineer. He has worked with computers and communication systems large and small, simple and complex. His forte is embedded-systems design and communications. Fred may be reached at fred@edtp.com.

SOFTWARE

To download the code, go to ftp.circuitcellar.com/pub/Circuit_Cellar/2002/139/.

REFERENCES

[1] National Semiconductor Corp., "LM78S40 Universal Switching Regulator Subsystem," April 1998.

[2] ———, "LM78S40 Switching Voltage Regulator Applications," AN-711, April 1998.

[3] Motorola, "Motorola Linear/Switch Mode Voltage Regulator Handbook, rev. 3, HB206.

SOURCES

ROM-DOS
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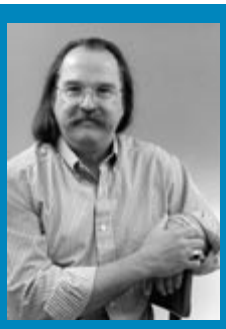


FROM THE BENCH

Jeff Bachiochi

What Good is IrD, Eh?

Part 2: Wireless Communication



Jeff has kicked off a series of articles investigating the lower level of IrDA protocols. This month, he explains what each protocol layer offers in the way of services and opportunities.

Once upon a time, I looked at the layering of protocol stacks as being unnecessarily complicated. Why divide a simple communication task into so many separately defined tasks? Although I don't consider myself to be anymore than an adequate software programmer, I can appreciate dividing a programming task into smaller more manageable routines. Generally it isn't necessary to go back and rewrite a working routine just because another part of the application has been modified (unless it is directly effected by the change). This idea of reusable code can be applied to protocols, as well. It is most easily seen at the bottom level, the physical interface.

Figure 1 should be familiar from last month, when I started discussing using the IrDA standard for infrared data communications. The IrDA stack is built on the firm IrPHY foundation layer. Advances in technology (improved hardware) can be implemented without requiring changes in any of the upper protocol layers. As shown last month, the IrPHY layer defines what constitutes good communication via infrared transmission and reception, but does not define how that is accomplished with any specific hardware.

With the physical layer (IrPHY) previously defined, the link access layer deals directly with the IrPHY layer and handles the bottom level communications tasks. The IrLAP layer provides services to the IrLMP layer. These services include,link start-up/ shutdown, address discovery, address conflict resolution, connection establishment, sniff open, information exchange, connection reset, and disconnection. The IrDA standard defines these service primitives and parameters, but not how the IrLAP must implement them.

The IrLMP layer consists of the link management information access and link management multiplexer. The IAP maintains an information base of IR devices within range and their capabilities. The MUX provides services to both the IAP and the transport entities. An application must deal with one of the transport protocols, such as IrCOMM. This transport layer takes care of defining the emulated connection, which includes how the port handshaking will be implemented along with the data. An intermediate TINY-TP layer is used to break outgoing data and control into chunks, reassemble incoming data and control, and keep track of multiple transports that may be trying to use the IrDA connection simultaneously.

Of the three mandatory IrDA layers, the IrLAP layer may have the most important job. This layer is responsible for taking the requests for and confirming the results of a service from the IrLMP layer. It automatically discovers and establishes connections to those devices within range. Let's look closer.

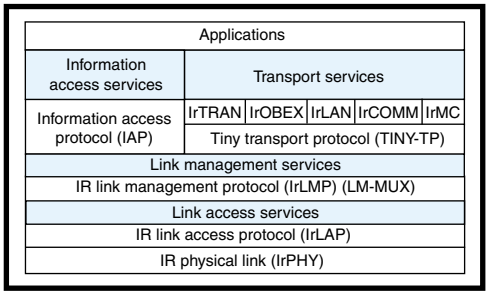


Figure 1—*This is the layer stack between your application and the infrared transceiver components, which make up the IrDA protocol architecture. The service layers define how data is passed between layers.*

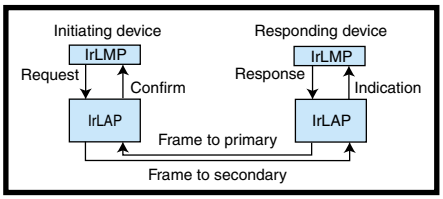


Figure 2—*IrDA service primatives (request, indication, response, and confirm) are illustrated here to show primary and secondary communications.*

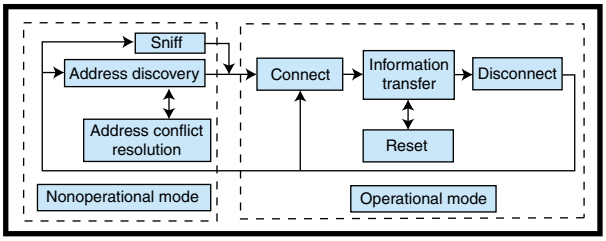


Figure 3—*The IrLAP performs a direct, logical progression through the two modes of its state machine.*

IrLAP/IrLMP SERVICES

Table 1 shows the IrLAP services available to the IrLMP layer. These services have multiple service primitives. The primitives imply direction of data flow as shown in Figure 2.

The IrLAP must translate between these services and one or more frames of data transferred between devices within range via the IrPHY layer. These translations take place as procedures defining the behavior of the IrLAP layer during each phase of the procedure. Figure 3 shows the logical flow of these service procedures.

There are two modes of operation, operational and nonoperational. Nonoperational, or Normal Disconnect mode (NDM), takes place before or after an actual connection is made. All discovery and address conflict resolution is handled in NDM. Normal Response mode (NRM) takes place after a device is connected. Primary and secondary roles must be determined prior to initiation of NRM. The primary station has responsibility for controlling the link, issuing commands, and granting permission to transmit. The secondary station takes orders from the primary and transmits only when given explicit permission to do so.

IrLAP/IrPHY FRAMES

Each phase of an IrLAP/IrLMP service procedure requires one or more IrLAP/IrPHY frames. A frame is a formatted data or control transmission between IrDA devices. The IrLAP assembles/disassembles the frame and the IRPHY sends and receives it via IR. The frame consists of a beginning-of-frame character (BOF), the payload, a frame check sequence (FCS), and a finish-of-frame character (FOF). The payload consists of the address, control, and optional information fields.

The address is a 7-bit (left-justified) address identifying a particular link between two devices. The least significant bit is a command/response bit and is set during a primary (initiator) transmission and clear during a secondary (responder) transmission. (So, odd addresses are from the primary device and even addresses are from the secondary.) The Control field defines the function of the frame. The information field's existence is dependent on the Control field.

WHO AM I/WHO ARE YOU

During link start up, IrLAP enters the nonoperational mode and generates its own 32-bit device address. This address is used in the address discovery procedure and exchanged as identification of each device within range. IrDA devices have two possible modes of operation. Secondary devices respond to IrDA communications and primary devices initiate IrDA communications.

Primary devices can act as primary or secondary devices, whereas secondary devices are only passive. Primary devices initiate the discovery process by polling for devices (within range) by dividing time into slots (see Figure 4). A primary device will make a slot inquiry and then listen during the remainder of the time slot for a device to reply. All devices should randomly choose a time slot to reply to. If the primary device hears a legal reply, it logs the device's address in its device log. The primary device's log of potential connections is continually updated until the upper layer asks for a connection to be established.

After all the time slots have been polled, the primary device sends out an information packet indicating what kind of device it is and its nickname. The information frame is similar to the response of the secondary device (see Figure 4). The polling cycle will then begin again.

If by chance devices come up with the same 32-bit address, an address conflict arises. To solve the problem, those devices can be instructed to choose new 32-bit addresses via bit 2 of the discovery flags.

Service	Type	Description
IrLAP_DISCOVERY	Request	Check for devices within range
	Indication	Unsolicited devices within range
	Confirm	Devices within range
IrLAP_NEW_ADDRESS	Request	Conflicting devices select a new address
	Confirm	Devices within range
IrLAP_UNITDATA	Request	Unreliable data transfer
	Indication	Data received
IrLAP_CONNECT	Request	Establish reliable connection
	Indication	Request reliable connection
	Response	Request reliable connection accepted
	Confirm	Reliable connection established
IrLAP_DATA	Request	Data outbound
	Indication	Data inbound
IrLAP_STATUS	Request	Quality of service
	Indication	Quality of service
	Confirm	Unacknowledged data
IrLAP_RESET	Request	Reset connection
	Indication	Reset request
	Response	Request confirmation status
	Confirm	Reset confirmation status
IrLAP_DISCONNECT	Request	Break reliable connection
	Indication	Break reliable connection request
IrLAP_PRIMARY	Request	Initiate exchange of primary secondary
	Indication	Initiate exchange requested
	Response	Accept/deny exchange
	Confirm	Report request's reply

Table 1—*The IrLAP layer offers these services to the IrLMP layer. Each service incorporates its own set of primatives, which imply the direction of data flow.*

IrCOMM

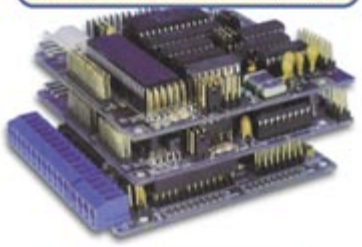
Sitting atop the IrLMP layer are a host of transport services that provide a way for various resources to

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BOF	Payload	FCS	FOF
1 byte	0-n bytes	1 word	1 byte
&HC0	(Information from IrLMP)	&HXXXX	&HC1

Where payload is:

Payload		
Address	Control	Information
1 byte	1 byte	0-n bytes
&HFF	&H3F	(Information from IrLMP)

Where information is:

Information						
Format identifier	Source device address (primary)	Destination device address (secondary) (broadcast)	Discovery flags	Slot number	Version number	Discovery information
1 byte	32 bits	32 bits	1 byte	1 byte	1 byte	≤ 32 bytes
&H01	&HXX &HXX &HXX &HXX	&HFF &HFF &HFF &HFF	x00 = 1 Slot x01 = 6 Slots x10 = 8 Slots x11 = 16 Slots 1xx = Generate new address	&HXX	&HXX	Optional

A secondary reply would be:

BOF	Payload	FCS	FOF
1 byte	0-n bytes	1 word	1 byte
&HC0	(Information from IrLMP)	&HXXXX	&HC1

Where payload is:

Payload		
Address	Control	Information
1 byte	1 byte	0-n bytes
&HFE	&HBF	(Information from IrLMP)

Where information is:

Information						
Format identifier	Source device address (secondary)	Destination device address (primary)	Discovery flags	Slot number	Version number	Discovery information
1 byte	32 bits	32 bits	1 byte	1 byte	1 byte	≤ 32 bytes
&H01	&HXX &HXX &HXX &HXX	&HXX &HXX &HXX &HXX	x00 = 1 Slot x01 = 6 Slots x10 = 8 Slots x11 = 16 Slots 1xx = Generated new address	&HXX	&HXX	Optional

Where discovery information is:

Discovery information		
Up to 32 bytes from IrLMP		
Service hints	Character set	Device nickname
1-n bytes	1 byte	0-(23-n) bytes
First byte	0 = ASCII	i.e., "My PDA"
Bit 0 = PnP-compatible	1 = ISO-8859-1	i.e., "My Computer"
Bit 1 = PDA/Palmtop	2 = ISO-8859-2	
Bit 2 = Computer	3 = ISO-8859-3	
Bit 3 = Printer	4 = ISO-8859-4	
Bit 4 = Modem	5 = ISO-8859-5	
Bit 5 = Fax	6 = ISO-8859-6	
Bit 6 = LAN access	7 = ISO-8859-7	
Bit 7 = Extension bit	8 = ISO-8859-8	
Second byte if needed	9 = ISO-8859-9	
Bit 8 = Telephony	10–254 = Reserved	
Bit 9 = File server	255 = UNICODE	
Bit 10 = IrCOMM		
Bits 11–14 = Reserved		
Bit 15 = Extension bit		

Figure 4—*This figure shows the primary polling and secondary response from an IR device within range. If the blue area is left off, the figure demonstrates the primary's end of the poll frame, which reveals facts about itself.*

make use of the IrDA stack for wireless infrared data communications (e.g., IrCOMM, IrTINYTP, IrLAN, IrOBEX, IrMC, IrTRAN-P, IrWW). Let's look at how IrCOMM uses the IrLMP/IrLAP stack. IrCOMM is the emulation of a serial or parallel connection (legacy). Take HyperTerminal (the PC terminal program) for instance. Sending a file over a serial link would require a null modem cable connected between two computers (or modem pairs connected by a phone line). By choosing a virtual serial port (installed when IrDA hardware is installed), you can fool HyperTerminal into thinking it's hardwired while it is actually using the IrDA port. A HyperTerminal file transfer will use all four IrCOMM services, which are IrCOMM_CONNECT, IrCOMM_CONTROL, IrCOMM_DATA, and IrCOMM_DIS-

CONNECT (see Table 2).

When the IrCOMM requests a connection to some device in the log, the IrLAP generates a request using the 32-bit device address from the log as the destination address. The request assigns a random 7-bit connection address, which will be used as a shortcut to the device, to the connection link. This request also asks for the operating parameters of the secondary device. This will allow the two devices to take advantage of any performance enhancers (e.g., faster data rate). The request to connect is handled using the SNRM frame, as shown in Figure 5.

Any parameter that is not exchanged is implied to be the default. Default parameters should be used while in Normal Disconect mode and prior to any negotiations. The default parameters are 9600 bps, 500-ms maximum turnaround time, 64-byte data size, one buffer window size, and 12 additional BOFs (which exceeds the 10-ms minimum turnaround time.) The secondary device would reply with a UA frame (notice the new address in Figure 6).

Service	Type	Description
IrCOMM_CONNECT	Request	Establish connect
	Indication	Request connect
	Response	Connect response
	Confirm	Connect established
IrCOMM_CONTROL	Request	Request parameters
	Indication	Parameters
IrCOMM_DATA	Request	Data to transfer
	Indication	Data received
IrCOMM_DISCONNECT	Request	Request disconnect
	Indication	Disconnect

Table 2—*Four services are available to applications using the IrCOMM layer.*

At this point, both devices know about the parameters of the other device and have initiated Normal Response mode. With the RR command, the primary device tells the secondary device it's ready (using the enhanced parameters just negotiated), and the secondary device responds. If no data is immediately ready to be sent by the IrLMP layer (from IrCOMM), the link can remain open only if the devices continue talking with one another. This is all handled automatically without direction from above. Unless this continuous banter takes place, the link will close. Figure 7 demonstrates a conversation that keeps the link alive.

When the IrPHY layers have a link among them, the IrCOMM can get its request for a connection handled. An information frame (one with an even control byte) is used to pass IrCOMM data within its Information field of the frame's payload (see Figure 8). IrCOMM data in the Information field of the frame comes in two varieties—data transfer frame and link control frame.

The negotiated parameters thus far dealt strictly with the IrPHY layer. The IrCOMM protocol has its own parameters because it emulates a serial or parallel port. There are four types of emulation, a three-wire raw, three-wire cooked, nine-wire cooked



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BOF	Payload	FCS	FOF
1 byte	0-n bytes	1 word	1 byte
&HC0	(Information from IrLMP)	&HXXXX	&HC1

Where payload is:

Payload		
Address	Control	Information
1 byte	1 byte	0-n bytes
&HFF	&H93	(Optional)

Where information is:

Source device address (primary)	Destination device address (secondary)	Connect address	Negotiation parameters
32 bits	32 bits	1 byte	
&HXX &HXX &HXX &HXX	&HXX &HXX &HXX &HXX	&Bxxxxxxx0 (7-bit Address left justified)	

Figure 5—*Within the SNRM frame, the primary device reveals its optimal parameters to the secondary device.*

serial connection, and a Centronics parallel connection. Three-wire raw emulation has no flow control. The latter three connections support some kind of flow control. Flow control may be hardware (RTS/CTS) or software (XON/XOFF). I'll stop here with this topic because further discussion of flow control is beyond the scope of this article.

IrCOMM parameter exchange is a way for each device to find out what types of emulation are supported by each other and to agree on which one to use. Presumably both devices are now happy with all aspects of the connection, therefore, data can be sent. Exchanging data is uneventful as opposed to the work required to establish a connection. Information frames carry the data and the TINY-TP layer handles the break down of the file into packet-sized chunks. Lower layers autonomously confirm packets and handle resending errors. Finally, an IrCOMM disconnect service breaks the connection after the application is finished with the link.

SHORT STORIES

If you don't have the protocol documentation on each layer printed and spread out all over the desk, it's difficult to follow much of what I just went over. There is so much more that I haven't talked about. As Arlo Guthrie sang in "Alice's Restaurant," "I told you that story, so I can tell you this one…." If you needed to add IrDA to an embedded system, you had a ton of code to write in support of the standard, until now.

Microchip released a preprogrammed micro that handles all of the messy IrDA stuff (see Figure 9). Well, not all protocols, just the IrDA stack and serial emulation via the IrCOMM service. You hang an infrared transceiver onto the MCP2150 and it handles IrLAP, IrLMP, IAS, TINY-TP, and IrCOMM. You interface directly to the RX and TX pins on your micro. Additionally, DSR, CTS, RTS, and CD must be implemented by your micro's hardware or emulated in software with additional I/O bits. These control lines allow you to monitor the status and activity of the link. Notably though, you no longer need to be concerned with the nitty-gritty of the IrDA standard.

If you recall from last month, I touched on some devices that handled formatting the datastream from a UART into IrDA-compatible IR communications. This was accomplished by decoding asynchronous non-idle bits of the UART into IR pulses and decoding IR pulses back into non-idle asynchronous bit times. One of the devices mentioned was the MCP2120 from Microchip. The MCP2150 adds the upper-level software IrDA layers to the physical interfacing abilities of the '2120 to reduce design time to market. Although the MCP2150 does not support multi-point (more than

BOF	Payload	FCS	FOF
1 byte	0-n bytes	1 word	1 byte
&HC0	(Information from IrLMP)	&HXXXX	&HC1

Where payload is:

Payload		
Address	Control	Information
1 byte	1 byte	0-n bytes
&Bxxxxxxx0	&H73	(Optional)

Where information is:

Source device address (secondary)	Destination device address (primary)	Negotiation parameters
32 bits	32 bits	
&HXX &HXX &HXX &HXX	&HXX &HXX &HXX &HXX	

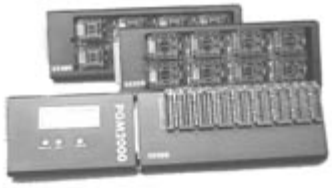
Figure 6—*The UA response of the secondary discloses its own optimum parameters.*

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The primary sends this RR frame:

BOF	Payload	FCS	FOF
1 byte	0-n bytes	1 word	1 byte
&HC0	(Information from IrLMP)	&HXXXX	&HC1

Where payload is:

Payload		
Address	Control	Information
1 byte	1 byte	
&Bxxxxxxx1	&H11	None

The secondary responds with this RR frame:

BOF	Payload	FCS	FOF
1 byte	0-n bytes	1 word	1 byte
&HC0	(Information from IrLMP)	&HXXXX	&HC1

Where payload is:

Payload		
Address	Control	Information
1 byte	1 byte	
&Bxxxxxxx0	&H11	None

Figure 7—*A continuous conversation is necessary to keep an established link open. This is accomplished automatically.*

two devices at a time) applications, the most common applications require only two devices—a primary device sending or receiving communication to or from a secondary device.

On the system side, the MCP2150 communicates with the serial port of the system at one of four fixed data rates (9600 to 115,200 bps). This system communications rate is independent from the IR data rate, which, as discussed earlier, defaults to 9600 bps and is automatically negotiated up to 115,200 bps. The MCP2150 requires an 11.0592-MHz crystal to generate the timing for both the system and IR data rate generation.

You may be asking, "Why are there extra control signals necessary beyond the normal TX and RX?" Well, the input and output buffers of the MCP2150 are limited to 64 bytes and the device can handle communication in one direction at a time. There must be a way of indicating the status of the communications link to the system.

These extra signals are similar to those used by an external modem connected to the system, thus, they are defined to emulate the same functions. The CD output (carrier detect) tells the system when a negotiated link has been established to perform a task. The data set ready (DSR) output indicates that the MCP2150 has initialized itself and is ready to go to work. The clear to send (CTS) output reflects the state of the input buffer, noting when the system can send data through TX.

Additionally, two input signals are

Payload		
Address	Control	Information
1 byte	1 byte	≤ IrLapmax-4
&Bxxxxxxx1	&Bxxxxxxx0	

Data transfer frame:

Information (LM-PDU)		
DLSAP-SEL	SLSAP_SEL	Data
1 byte	1 byte	≤ IrLapmax-6
&B0xxxxxxx	&B0xxxxxxx	&HXX...

Or link control frame:

Information (LM-PDU)			
DLSAP-SEL	SLSAP_SEL	Opcode	Parameters
1 byte	1 byte	1 byte	≤ IrLapmax-7
&B1xxxxxxx	&B0xxxxxxx	&H01 = Connect	&H00 + optional
		&H81 = Connect confirm	&H00 + optional
		&H02 = Disconnect	&H01 = User request + optional
			&H02 = Unexpected disconnect + optional
			&H03 = Failed connection + optional
			&H04 = IrLAP Reset + optional
			&H05 = Disconnect + optional
			&H06 = Disconnected + optional
			&H07 = Nonresponsive + optional
			&H08 = No client + optional
			&H09 = Connection half open + optional
			&H0A = Illegal source address + optional
			&HFF = Unspecified + optional
		&H03 = Access mode	&H00 + (&H00 = Multiplexed or &H01 = exclusive)
		&H83 = Access mode confirm	(&H00 = Success or &H01 = failure or &HFF = unsupported) + (&H00 = multiplexed or &H01 = exclusive)

Figure 8—*IrCOMM data and control information is passed using the IrLAP information frame.*

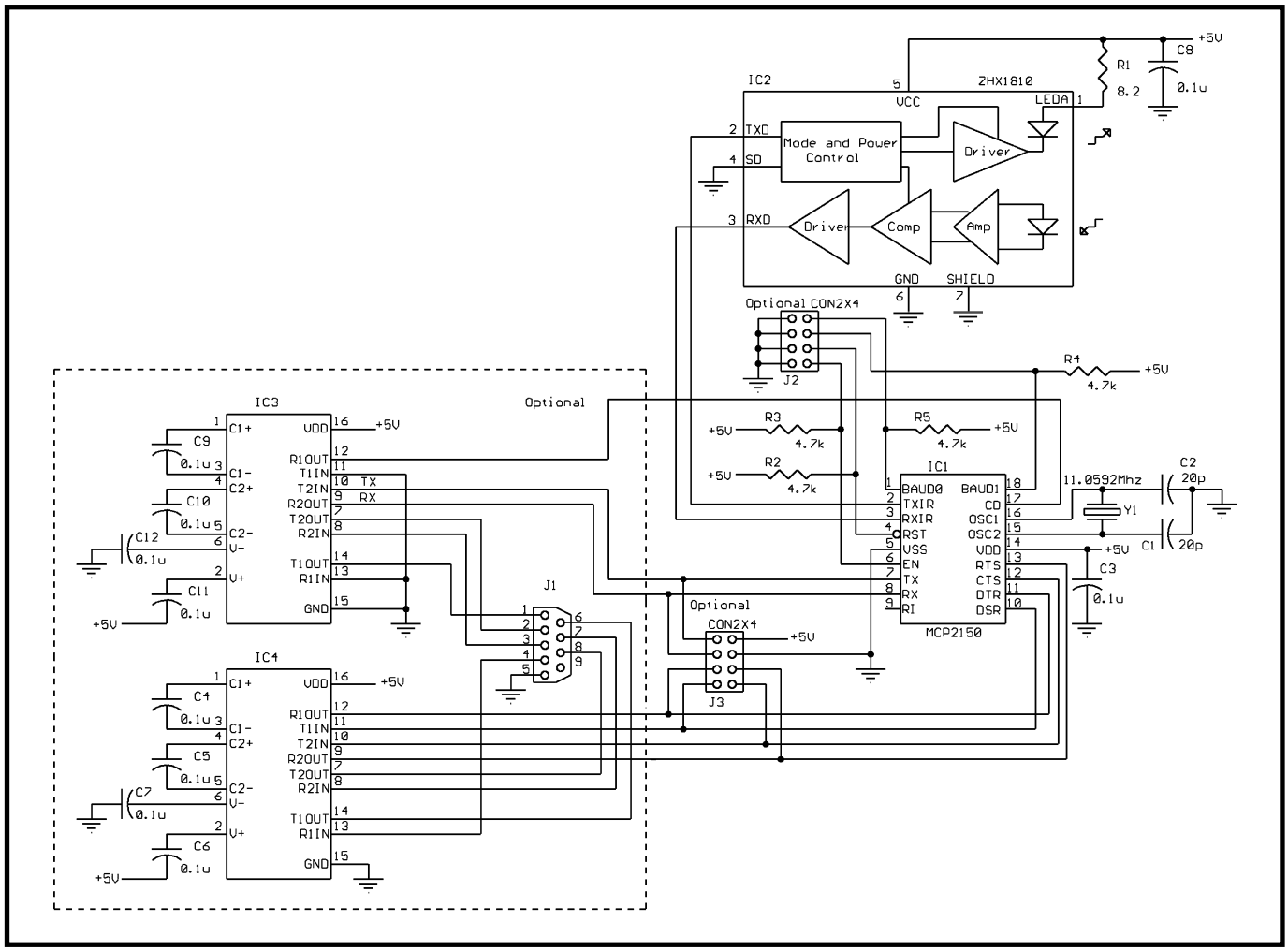


Figure 9—*I used this circuit to experiment with IrDA communications with my laptop. It handles most of the messy IrDA stuff. RS-232-level shifters are not necessary when connecting directly to a microprocessor. These signals are available at J3.*

used. The ready to send (RTS) input lets the MCP2150 know when the system is ready to receive data through RX. Lastly, the data terminal ready (DTR) input can be tied low, disabling Device ID Programming mode. This mode is necessary only if you wish to change the default device name, MCP 9-wire, within the MCP2150 to something more appropriate. For those of you who are highly interested in reducing current consumption to an absolute minimum, the '2150 also provides an enable (EN) input that will reduce device consumption from milliamperes to microamperes.

CONTINUING EDUCATION

Please be aware that column limitations allow me to only brush over some of the more important points of the IrDA standard. I invite you to visit the IrDA web site for access to all of the documentation standards in PDF format. The web site contains a wealth of knowledge far beyond publishing the actual standards. It is this kind of thorough support that often makes the difference when you need to decide which peripherals or protocols to support.

I expect to see a demand for more peripherals of this kind to be developed when more designers become comfortable using this approach to add IrDA communications to their widgets. The MCP2150 is a great example of using today's technology to empower you with the ability to quickly implement IrDA without having to clear the hurdle of complete protocol understanding. It is this kind advancement that directly influences how a standard will be accepted and ultimately used. Beam me up, Scotty.

Jeff Bachiochi (pronounced BAH-key-AH-key) is an electrical engineer on Circuit Cellar*'s engineering staff. His background includes product design and manufacturing. He may be reached at jeff.bachiochi@circuitcellar.com.*

SOURCES

IrDA Specifications
Infrared Data Association
www.irda.org

MCP2150 Infrared communications controller
Microchip Technology Inc.
(480) 792-7200
Fax: (480) 899-9210
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ZHX1810 Slim series SIR transceiver
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SILICON UPDATE

Tom Cantrell

eZ Embedded Web



It's time for another look at the eZ80 offering. This month, Tom looks at how Zilog has enhanced the venerable Z80. With a Web-server Development Kit in hand, getting things up and running didn't take long.

A little more than a year ago, I wrote, "Even though eZ80 silicon actually exists, I'd say it's too soon to pop the bubbly. It could be a long road from a chip that wiggles in the lab to boxes of them sitting in a warehouse, and in this business, let's just say that stuff happens," ("eZ Does It" from *Circuit Cellar* 124). As we've all seen subsequently, stuff happens indeed.

It's a tough time for everyone, including our old pal Captain Zilog. Weak sales, shake up in management, fabrication consolidation, and retrenching on a variety of fronts. Yes indeed, times are tough and it doesn't look like that will change anytime soon.

But so what?. When it comes to Zilog, the last time things weren't tough was, oh let's say, around 1979. Those were the glory days when the little chip that could, the Z80, was giving the big boys a run for their money.

Then, under the misguided tutelage of Exxon, the Z8000 got stomped in the battle for desktop supremacy between Intel and Motorola. Exxon never seemed to figure out that making chips was different than poking holes in the ground.

The first desktop UNIX systems (pioneered by Zilog) hit their twilight years even as the similar Sun boxes were rising. How about those pseudo-static RAMs that were only pseudo-sellable? The mythical Z800 chip had more false starts than transistors and never got much beyond a part number and press releases. All of this culminated in last year's withdrawn IPO, perhaps inevitable for a company that seemingly goes public and private like a yo-yo.

Back in November 2000, I also wrote, "…if and when Zilog delivers a chip that works and a free (or low-cost) high-quality TCP/IP stack, it will definitely be worth a look." So, why don't we do just that, starting with Photo 1.

Yes the old Captain, bless his heart, has taken one licking after another over the years and keeps on ticking. There's a lesson to be learned here, and maybe one more timely than ever.

IN WITH THE OLD AND THE NEW

For those of you who missed my earlier article, let's take a quick and eZ refresher. The challenge posed by the eZ80 was to carry forward the happy days' sentiment for the Z80 while significantly upgrading under the hood. Sounds easy, but it isn't. Nevertheless, I reported in "eZ Does It" that I thought Zilog had done a remarkably good job, at least on paper. See for yourself in Figure 1.

Architecturally, it's always hard to make a chip that is both the same and better than its predecessor. This is especially true when it comes to getting past the 64-KB address space barrier characteristic of practically every popular 8-bit chip. Zilog finessed this well with their dual-mode short (16-bit addresses compatible with Z80) and long (24-bit) addressing scheme.

Under the hood, the eZ80 is hopped up with a pipelined, 50-MHz, 24-bit ALU core. Yes, there are wait states required for off-chip memory to consider, but it's still much faster than its predecessor and most 8-bit chips. There's even a high-performance 32-bit MAC unit that allows the chip to do double-duty as a DSP.

Popularity of the Z80 had as much to do with the add-ons it worked with, the venerable SIO, CTC, PIO chips of

yore. Even by today's higher integration standards, the eZ80 holds its own with fancy serial parts (including asynchronous, I²C and SPI), half a dozen timer/counter channels, a burst and cycle steal DMA controller, a wait chip select state generator,and built-in debug logic.

Although not a single-chip MCU, the 8 KB of on-chip 1-clock code and data-capable SRAM (not to mention the extra 1 KB that comes with the MAC unit) is enough to handle the RAM needs for a lot of embedded applications. Clever designers will put the small portion of their code and data that truly needs top speed there. Combining the eZ80 100-pin QFP with a single external EPROM or flash memory chip makes for a tidy yet powerful two-chip solution.



Photo 1—*Zilog delivers the goods, including a free networking protocol stack, with the eZ80 web server evaluation kit.*

THE WAY OF THE WEB

Internet enabling embedded gadgets is all the rage, as well it should be. Sure there are issues such as cost, performance, reliability, security, and so on. What else is new? The fact is the 'Net offers compelling accessibility and ease-of-use advantages that the embedded world can't ignore. We're a long way from pervasive connections, and the journey from here to there won't be quick or smooth. But progress will march on.

When it comes to getting on the I-way, most of the alternatives seem to fall into one of two camps. At the high end, there's the PC-in-drag approach that relies on 32-bit computer chips running big-ticket operating systems with megs of memory. The good news is that these chips and software already know plenty about the Internet and are comfortable handling that aspect of the job. On the other hand, notwithstanding plenty of eye-candy and whizzy stuff like Java, it does seem like quite a lot of baggage to tote around just to get a few bytes of data from here to there.

Special-purpose, Internet-centric add-ons from the likes of iReady and Connect One or stripped-down mini-me stacks running on conventional 8-bit MCUs represent the other extreme. Although these solutions cut the bill of materials, at the least they sacrifice a measure of functionality and flexibility. Worst case, they raise the chance of ending up with a setup that seems to work fine in the lab but chokes when plugged into a real-world network.

The eZ80 chip itself splits the difference between traditional 8-bit MCUs and desktop-class computer chips. Most of the former handle up to 16-bit addressing (maybe, some are much less) and the latter deal with 32 bits and beyond. That's where the eZ80 fits in with a 24-bit take on the subject.

It's no surprise then that the eZ80 web strategy seems to combine aspects of both the 8- and 32-bit options. It's definitely leaner and meaner (and easier on the pocketbook) than the brute-force 32-bit approach, but more capable and powerful than a mighty-mouse 8-bit solution.

TURN UP THE VOLUME

As I write this, Zilog is running eZ80 web server seminars around the country in conjunction with the chip rollout. Although I wasn't able to attend in person, I did get a copy of the presentation materials and an eZ80 Webserver Developer's Kit for some hands-on evaluation.

If you're interested, keep an eye out for a seminar in your neck of the woods. Besides helping you get up to speed quickly, attendance at the $99 seminar qualifies you for a whopping $400 discount on the kit, effectively cutting the price in half from $799 to $399.

Those of you saying $799 or even $399 is a bit steep for dabbling are preaching to the choir. I think the price is fair, however, if you're seriously considering embedded Internet options.

The board is no toy, outfitted with 1 MB of flash memory, 1 MB of SRAM, dual RS-232 ports, a real-time clock, and an Ethernet interface. But, the kit comes with much more, notably a full-fledged Z-PAK emulator, industrial-strength C compiler (courtesy of Associated Compiler Experts, a.k.a. ACE), and complete TCP/IP stack and RTOS from Metro Link. All of this runs under the fancy ZDS graphical IDE from Zilog.

Before exploring how you get there, let's consider where you might end up with an eZ80-based solution. First, a dedicated design is going to have about half the chips of the developer's board. The CPU, a couple of memory chips, and your 'Net connection of choice (RS-232 or Ethernet) should just about do it. Check out the eZ80-based unit from the German outfit Webolution (see Photo 2) as an example of a typical target design.

Small-quantity deals are well and good, but what about production? I'd say you're looking at less than $20

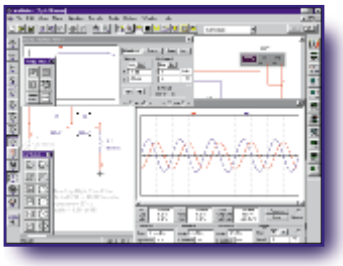


Photo 2—*A typical eZ80-based embedded web design, such as the unit shown here from Webolution, requires merely a few chips.*

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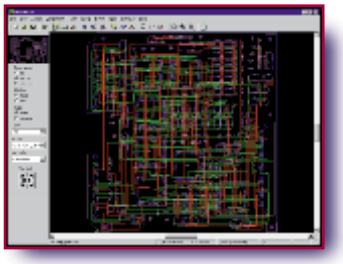
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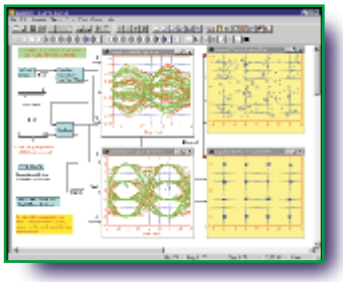
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worth of chips in volume (the eZ80 alone is about $10 for 1000). What about royalties on the TCP/IP stack and RTOS? Good question, with an even better answer: there aren't any! The software is a freebie as part of the XINU project operating system developed by Douglas Comer of Purdue University. [1, 2]

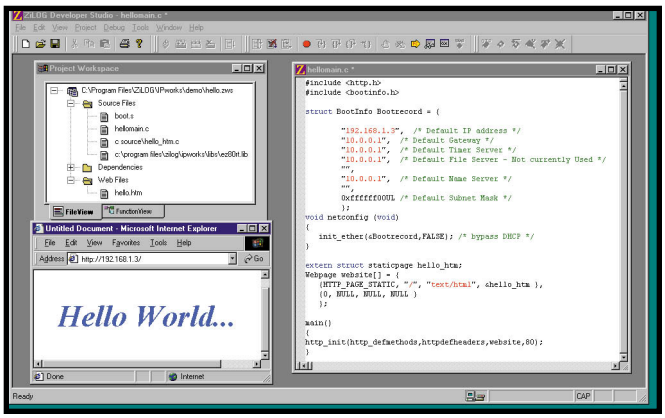


Photo 3—*With high-level network API functions in hand, an embedded web page is only a few lines of C code away.*

PROOF IS IN THE BOOTING

With the board, emulator, development PC, not to mention possible additional 'Net client PCs, and maybe a router, this all makes for quite a lash-up. It's a nice touch that the kit includes all the power supplies and cables (both RS-232 and Ethernet) for immediate gratification.

There were even printed manuals for the board and emulator, which I greatly prefer over electronic ones. How-ever, I did discover there's one important manual that's missing, so I downloaded it from Zilog's web site. [3]

While you're there, make sure you have the latest copy of the eZ80 chip documentation, as well. Remember my earlier comment about breaking out the bubbly prematurely? Check out the eZ80 errata and you'll see that last year's beta chips expectedly had some severe bugs. By contrast, the production rev chips appear more than up to snuff with only two minor bugs noted, so feel free to pop the cork.

All three CDs (ZDS, IAR C compiler, and the Metro Link stack and RTOS) installed without a hiccup, so I was anxious to fire up everything and do some embedded web surfing. The first choice you've got to make is how you want to wire up things (see Figure 2). I advise you to watch out for a few potential stumbling blocks.

The demo in flash memory on the board fires up looking for a dynamic host control protocol (DHCP) server. For those of you, like me, who aren't experts on all this 'Net stuff, the idea is that you can just plug in a client (e.g., eZ80 board) and a web server with DHCP can issue it an IP address. That way you don't have to hardwire an address, which may be problematic in a particular installation, on the board.

According to the Quick Start guide, the eZ80 will look for a DHCP server for a couple of minutes, and then default to a hardwired address (192.168.1.1). Unfortunately, that's the same address as my router. I've learned over the years it's better not to muck around with my main-squeeze work PC. Instead I hauled out my laptop and went with the simplest one-PC setup. It isn't a web server or running DHCP, so I simply went into the networking control panel and hardwired a local IP address of 192.168.1.2.

As you're hooking up everything, a run-in with Murphy's Law will have you juggling regular and crossover Ethernet cables. Fortunately, the board includes LINK/RX/ TX LEDs, so just plug in a cable of any pedigree. If the LEDs light up, you've got it right.

I fired up everything and had a coffee break to while away the couple of minutes. Then, I came back to the laptop, opened up my browser, and typed "http://192.168.1.1". Nothing happened. The browser sat there trying to find the page for awhile, then timed out, just like when my regular ISP is out to lunch.

I've tinkered with a lot of eval gadgets over the years. One thing I've learned is that if something doesn't

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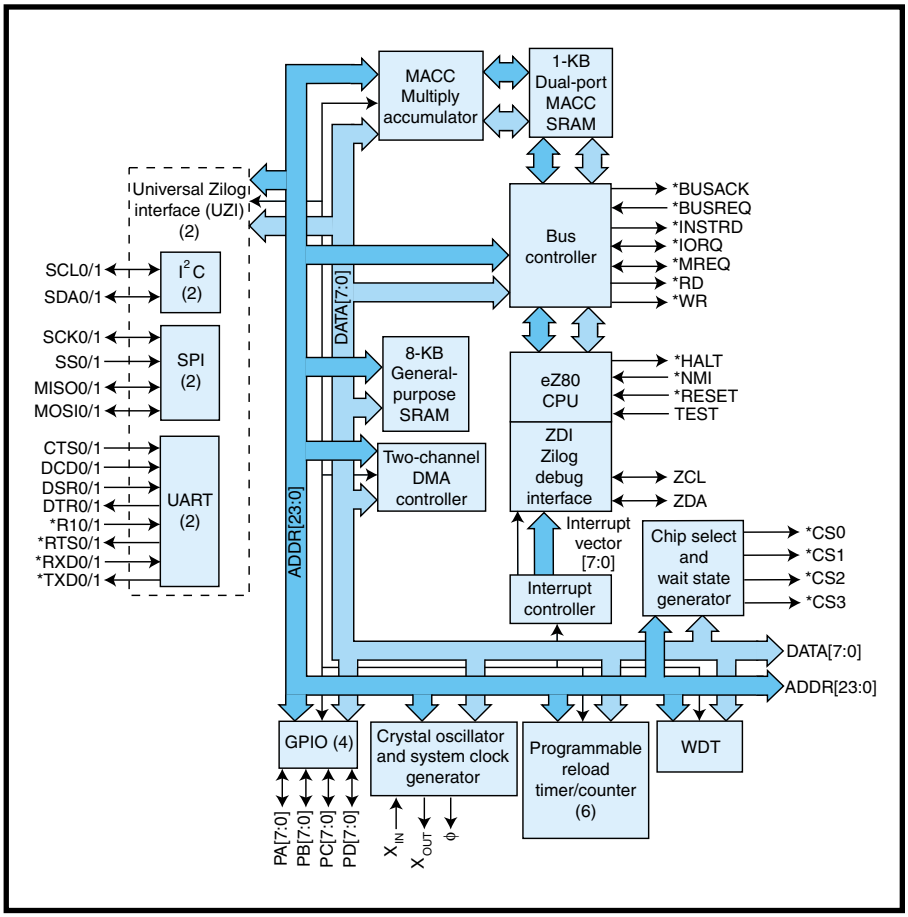


Figure 1—*We're going back to the future. The eZ80 carries the legacy of the Z80 into the 21st century.*

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work, sometimes it's better to just move on and see if you can find something that does work and go from there. So, I proceeded with the next step, which is to compile the same demo ostensibly programmed into flash memory and download it to the SRAM of the board via the emulator. While I was at it, I inserted some code (shown in the documentation) to disable the DHCP time-out stuff and go straightaway with a hardwire address for the board, which I set to 192.168.1.3.

Now, it was time to rebuild the project, connect to the emulator, download, reset, and go. Everything went smoothly, albeit a bit slowly. Despite the speed, I remain impressed with the power and quality of the tools. The only major complaint I have is that the RS-232 connection between the PC and emulator is limited to 57.6 Kbps. That's OK for traditional 64-KB or less 8-bit programs but gets annoying as program size creeps into triple digits.

As an aside, I noticed the ZPAK emulator has a USB port on the back. I strongly encourage Zilog and every other toolmaker to support USB and/or Ethernet connections as an alternative to (rather ungracefully) aging serial and parallel ports.

Anyway, I clicked the ZDS Go button, switched over to the browser, typed in http://192.168.1.3, and that was it. Frenetic blinking by the onboard Ethernet LEDs was shortly followed by the appearance of the Zilog demo page on my laptop. Cool.

I don't know exactly what if anything was put in the flash memory at the factory or why it didn't seem to work. Subsequently, I loaded the rebuilt demonstration program into the flash memory and everything worked as advertised.

I even went back and checked the DHCP function using a two-PC configuration similar to the networked setup shown in Figure 2. Although neither of the PCs is running a web server, it turns out my desktop router

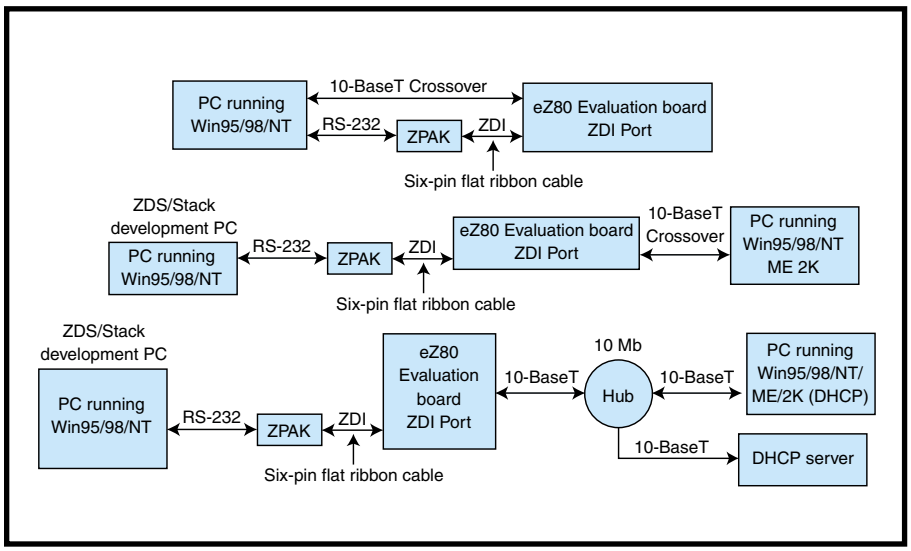


Figure 2—*As with the Internet in general, evaluation board connection options abound. It's best to start using a single PC setup with hardwired IP addresses and move on to multiple PCs and dynamic IP addresses (via DHCP) after everything checks out.*

(taking the place of the hub in Figure 2) does provide DHCP service. Sure enough, the newly flashed eZ80 board happily accepted the IP address offered by my router.

CUT THE FAT

The Zilog demo page, taking full advantage of the spacious memory, shows off many of the advanced capabilities of the board and software: dynamic web pages, CGI, Java, HTML, GET, POST, and so on. The point is that this isn't some emasculated hack of a stack. It will pretty much take anything a top-tier web page design program can throw at it. The only guidelines are to build your web site in a flat directory (all files in one directory) and perhaps use one of the widely available HTML optimizer packages to strip out comments and other unnecessary stuff from the resulting web files.

However, being somewhat of a 'Net newbie, I thought it would be helpful to come up with the simplest possible example. Time for a Hello World program, or in this case, web site (see Photo 3).

As you can see in the photo, the program (`hellomain.c`) is actually quite simple. A web site is simply defined as a collection of HTML pages and objects such as a `.gif` or `.jpeg`. When you add a web file (specifically, `*.html`, `*.gif`, `*.jpeg`, `*.class`, or `*.wav`) to your project, ZDS automatically converts it to a C equivalent and includes it with the rest of your source files.

When all was said and done, my Hello World application ended up consuming about 150 KB versus nearly 500 KB for the Zilog demo page. The difference was the Hello World web site was about 250 KB smaller than the demo page and I also managed to strip out another 100 KB of optional includes such as the operating system console shell.

Even my downsized version didn't go all the way. If you really get into it, you can squeeze even more in the way of unneeded protocols and features out of the stack. You can, but the point is you don't have to. If you want all the bells and whistles and have the memory to spare, feel free to go for the gusto.

BETTER LATE THAN LATER

I find the eZ80 an intriguing alternative in the spectrum of traditional options. Compared to 8-bit chips, it has more ALU and MAC horsepower and a particular advantage of handling 64-KB and beyond addressing in a straightforward manner. At the same time, the high-integration, 8-bit data bus and good-old-days code density make for a lower sticker price and better memory mileage than a 32-bit chip. That's the good news. My only complaint is that Zilog should have introduced the eZ80 to the market about five years ago.

I don't think it's too late for the chip to make waves, but it does mean Zilog can't let up. For instance, I hear there's a version in the works that will integrate a bunch of flash memory and an Ethernet port. That chip is a must, not only to keep up with the pack but also to assure people designing with the eZ80 today that there's a clean upgrade path for tomorrow.

While they're at it, how about a version with a built-in modem? That sounds like a good way to put the MAC unit to work, and Zilog and the Z80 are certainly no strangers to the modem business.

The old Captain has been through tough times before and no doubt will face them again. Life hasn't been eZ, his cape is a little worn and the tights are drooping a bit. But he still packs a decent punch and, above all, never, ever gives up. I like that.

Tom Cantrell has been working on chip, board, and systems design and marketing for several years. You may reach him by e-mail at tom.cantrell@circuitcellar.com.

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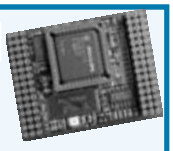
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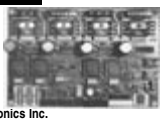
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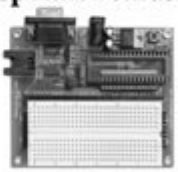
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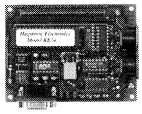
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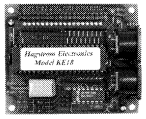


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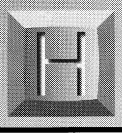
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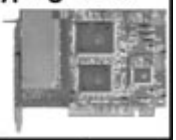
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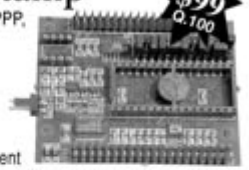


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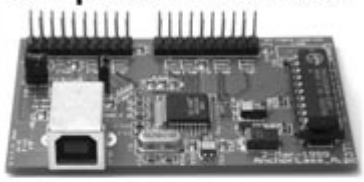


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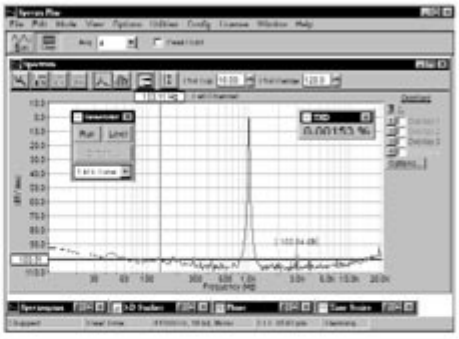
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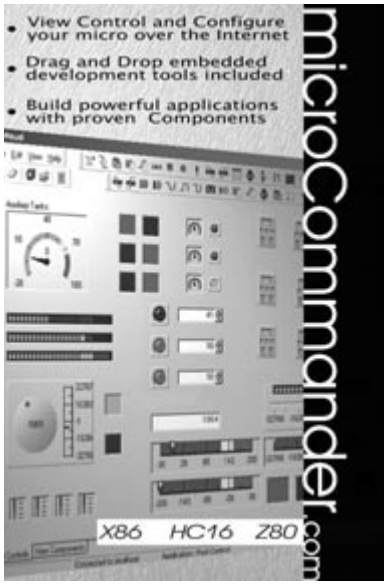
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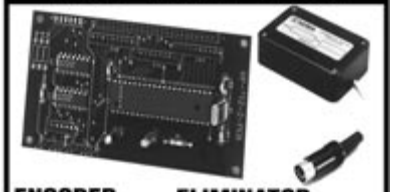
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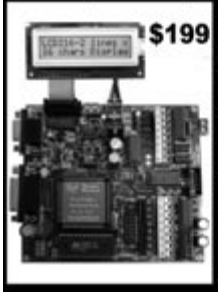
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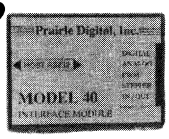
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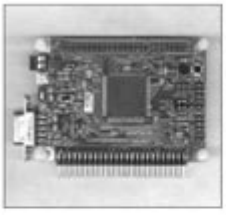
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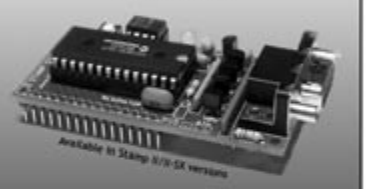
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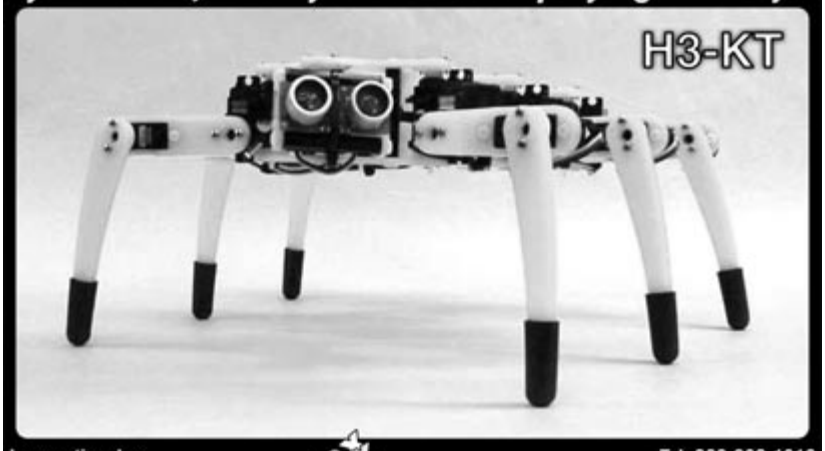
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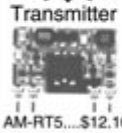


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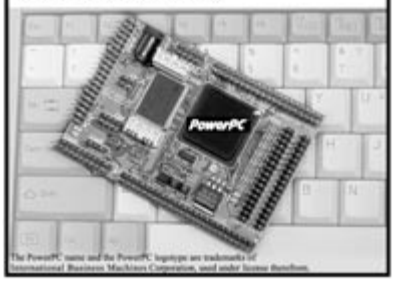
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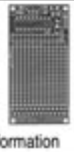
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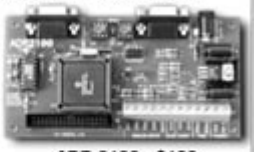
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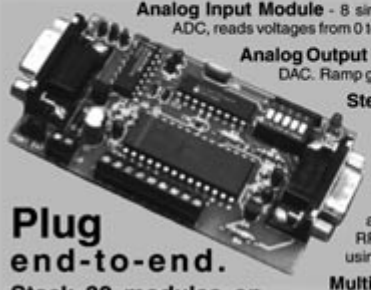
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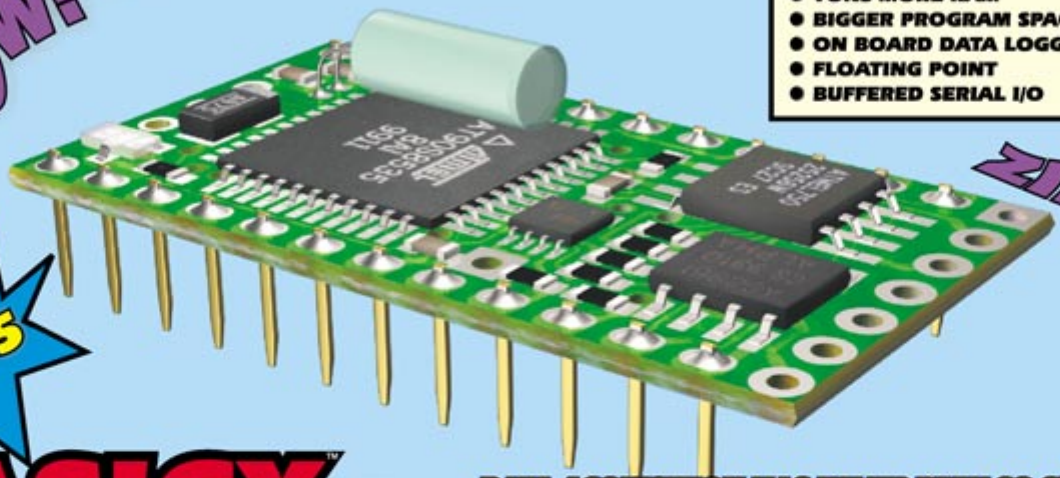
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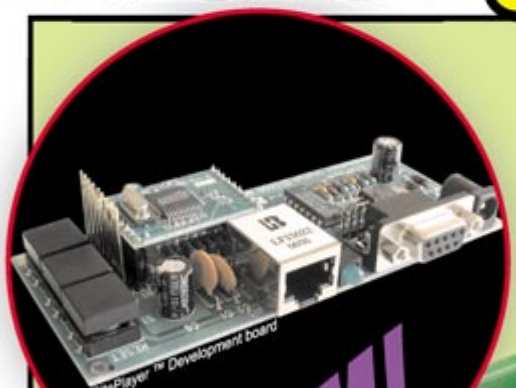
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United We Stand



Every once in a while I like to use this editorial space to discuss what's going on at *Circuit Cellar* and what I'm planning. *Circuit Cellar* is but a small blip on the tech publishing world's radar but I think we have a greater voice than our diminutive stature might indicate. Over the years we've gained a reputation for technical excellence that has become hard to ignore. We've survived and prospered in a climate where other magazines have perished or merged.

I credit a lot of our success to a de facto state of affairs. The technical trade magazines are the closest we have to what I'd call competition. By design or default, they traditionally approach business from the top down. By that, I mean they exist financially and obtain their advertising contracts by dealing directly with the public relations and marketing people within large corporations. I'm not inferring that there's anything wrong with that approach. On the contrary, when business is good, it's efficient one-stop shopping. A couple of power lunches and the deal is done.

I'm certainly not a person who avoids schmoozing and heaven forbid I should pass up a good lunch, but our business approach has been what I call bottom-up rather than top-down. Certainly before we became recognized by the large semiconductor companies, their PR departments would answer "Circuit Cellular?" As a result, our dealings have concentrated primarily on the staff engineers and engineering managers who know what *Circuit Cellar* is all about. Well below the power lunch decision-makers, these people also became our authors and readers and evolved into the strong internal support we enjoy today. Back then, the advertising contracts we got weren't the result of exhaustive negotiations or packaged deals with the marcom department, they were the predictable consequence of *Circuit Cellar* editorial. Publishing an article from inside their own ranks not only helped management discover its own engineering resource, it absolutely demonstrated ours.

Today it is considerably less of a rat race and I haven't heard "Circuit Cellular" in years. Now that *Circuit Cellar* is middle-aged, we get to enjoy our well-earned stature. A lot of it has to do with the fact that many of our readers have advanced, too. Young staff engineers and middle managers who have been with us through the years are now in controlling positions. They know us, and they know our credibility. When marcom people mention our name in meetings these days, there's almost always someone there to reply with the scoop.

Developing with a bottom-up approach to life has imparted a certain amount of humility, however. I'd be the first to tell you that *Circuit Cellar*'s editorial success isn't a result of my personal sweat each month. It comes from the sharp editorial team that edits the technical chronicles of an equally sharp group of hands-on authors. Similarly, our commercial success has nothing to do with power lunches either. It's because we have a message you like to read and together all of you constitute one of the highest powered audiences available. It's hard for advertisers to pass up that kind of audience.

I suppose my first reaction should be simply to accept the applause and run with it. Because we are one of the few magazines that actually grew last year despite the technical sector's meltdown, it is obvious that we have staying power. It should be a golden opportunity to take advantage of timing. Raise the rates and the best show in town simply gets a little more expensive!

Last year was difficult for many companies. There were large layoffs, contracts were canceled, and marketing budgets were slashed. *Circuit Cellar* was fortunate to avoid most of the turmoil because our advertisers stuck with us. On one hand I can say we deserved it, yet on the other hand, I also know how traumatic an economic downturn can be to a business. We're now seeing the light at the end of the tunnel and businesses are starting to recover. It's the next step along the path to recovery that concerns me.

Undoubtedly justified by expenses, trade-publication response to the recovery is to make up last year's shortfall by raising advertising rates up to a whopping 18% (source: SRDS). Unfortunately, the companies most hurt during this recession, and the ones we depend upon most for our technological future, are the ones called upon to face this added obstacle to their recovery.

In light of recent world events, I view this particular round of economic recovery as more important than others. If it is not America's moral integrity that directs the world it has to be our overwhelming economic strength. I could certainly justify higher rates because we have increased costs too, but getting America back on track has to be a higher priority right now. For that reason, *Circuit Cellar* is not raising advertising or subscription rates during 2002. We'll bite the bullet and stay the course to help you recover faster, too. Call the reason anything you want but I think one line in American psyche defines it best, "United we stand. Divided we fall."



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