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THE MAGAZINE FOR COMPUTER APPLICATIONS

#129 APRIL 2001

## EMBEDDED APPLICATIONS

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Looking at Fiber Optic Gyros

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Embedded Reliability



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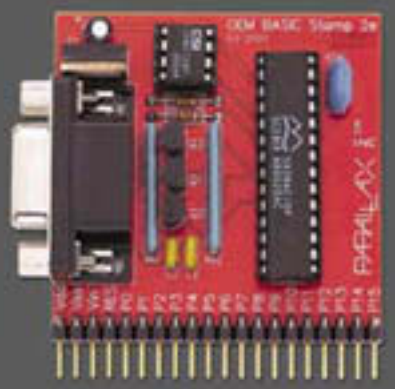
The original BS1 OEM module is available in a handy through-hole format. This module has a 3-pin header for your parallel port. The module plugs into a breadboard where it connects to +5 V, ground, and 8 I/O pins. The OEM Stamp 1 holds about 80 lines of code and executes 2,000 instructions per second.




**BASIC Stamp 2 OEM module $59 (#27290)**

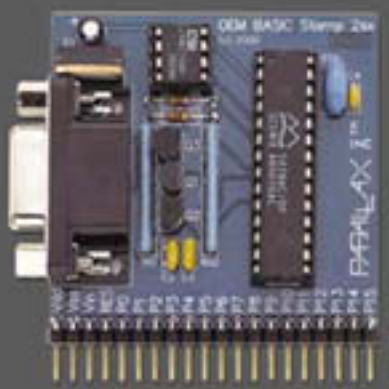
The very popular BS2 OEM module has a DB-9 serial connector built right onto the board. All parts are socketed for easy replacement. Our PBASIC interpreter runs in a PIC16C57 and executes 4,000 instructions per second. Holds about 500 lines of code. Useful commands for serial, DTMF, and sound.

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The OEM BS2sx is 2.5 times faster than the BS2e (left). Ideal solution for BS2 users who have needed additional program execution speed. Executes about 10,000 instructions per second and holds about 4,000 lines of PBASIC code.

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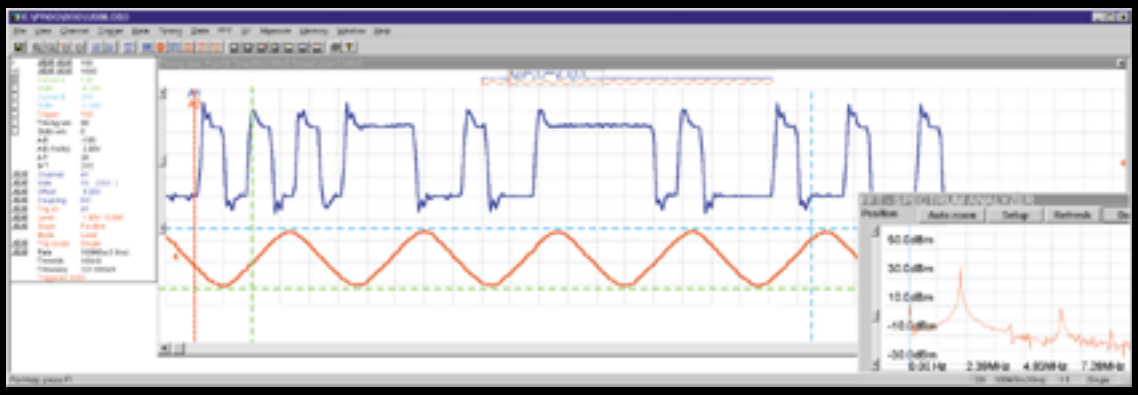
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# Digital Oscilloscopes



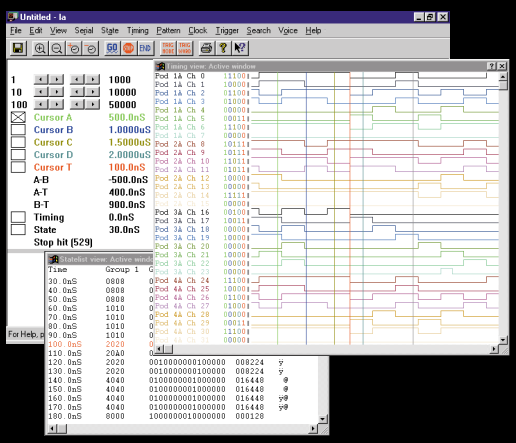
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★★★★★★★★★★
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8 Additional Questions

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## USING PERL IN EMBEDDED SOFTWARE DEVELOPMENT

*by Liu Kai*

The PicoWeb design inspired Liu to use Perl for embedded software development. Because Perl is fully open-source, you can modify the code to your demands. Using Perl may not be a new idea, but why not try using it in embedded software industries? You'll find it useful in almost every session of development. March 2001

GO

## SELECTING THE RIGHT MICROCONTROLLER UNIT

*by Chad Gallun*

It's a personal choice, but there are many factors to consider. This month, Chad takes us through the ins and outs of choosing the right MCU. His chief goal, of course, is to reduce cost while still satisfying the specifications for performance and reliability. The first step is determining your needs, then just follow this guideline for mapping out criteria for the optimal decision. March 2001

GO

## THE POWER FACTOR

*by George Novacek*

Power quality has become increasingly critical for all commercial equipment. The regulations are looming and traditional 400-Hz generators are gradually being replaced by 400-Hz variable frequency generators, delivering power at frequencies between 320 and 780 Hz. Efficiency, weight, and economics dictate in this area of AC electric power distribution. March 2001

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## AN S-7800A/PIC16F877 JOURNEY

**Part 3: Hot-Wiring the System**

*by Fred Eady*

Using a PIC to communicate over the Internet? Fred is just as surprised as you, but nevertheless, that is the task at hand for this month. With in-circuit programmable flash memory and four times the I/O space of the old PIC16C55, he started the ball rolling with SMTP. Once you know how to send e-mail with small embedded devices, you've hit guru status. March 2001

GO

## STRUCTURED DESIGN

**Part 1: An Introduction to Structured Techniques**

Lessons from the Trenches—*by George Martin*

George was betting that he wouldn't be at a loss for words this month, and he was right. Structured programming as it pertains to flowcharts and Nassi-Schneiderman charting holds his interest and ours, as he shows us why we can put the nightmare of debugging spaghetti code on the back burner. All you need is sequence, selection, and iteration and controlled code will follow. March 2001

GO

## ANALOG BIT BOMB

Silicon Update Online—*by Tom Cantrell*

This month, the hardware wizards are defending their spot in what Tom refers to as the "battle of bloat." Even though there is a slowdown in PC sales, older PCs still have the horsepower to get the job done, so why upgrade? Still, we've come a long way, as Tom shows us TI's ADS1216, a complete data acquisition subsystem that deals in precision as opposed to speed. Is relief is just a new chip away? March 2001

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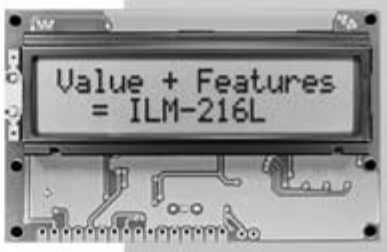
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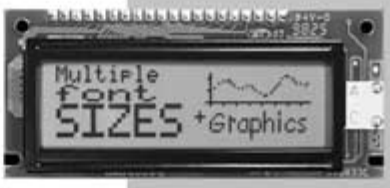
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# TASK MANAGER

## One for The Money…

There are plenty of good reasons for attending a trade show such as the Embedded Systems Conference. There are technical classes and tutorials, industry-expert panel sessions that you can attend, and all kinds of new products being introduced by hundreds of vendors on the show floor. But enough plagiarizing the ESC brochure, besides, as the managing editor, I have my own agenda when it comes to trade shows.

My engineering ability will always take a backseat to my editing ability, so I graciously decline the opportunity to attend any of the technical classes or tutorials. Personally, I've found that the panel sessions are a little more informal and often the best place to get the latest buzz and hear some interesting perspectives. As for the vendor exhibits, there's a reason they call it the show floor—with everything from cheerleaders to racecars, it's entertaining to say the least.

My main purpose at shows like ESC is to stand at the booth and tell long-time *Circuit Cellar* fans when Steve will be back at the booth so they can meet him. (It's April, of course I'm kidding!) Seriously though, I do spend the majority of my time tending the booth, which gives me a great opportunity to talk to engineers who are familiar with the magazine and enjoy the hands-on application articles and solutions that we publish every month.

As I've said in the past, engineers who read *Circuit Cellar* usually make the best *Circuit Cellar* authors. And, asking about their latest projects is like asking about a new baby. I've been shown photos, sketches, and even a completed article manuscript. And that's the real reason I'm there, to find more great projects and authors to publish in *Circuit Cellar* and *Circuit Cellar Online*.

Not everyone who comes by the booth remembers the days of "Ciarcia's Circuit Cellar" in *BYTE*. In the course of each trade show, at least 10 people look at the booth and ask, "Circuit Cellular? What's that?" I'm often tempted to reply, "That's what happens when you don't sound out your letters." However, I've read Dale Carnegie's book, and nowhere does it recommend sounding like a nagging kindergarten teacher in order to win friends and get engineers to write articles.

Rob

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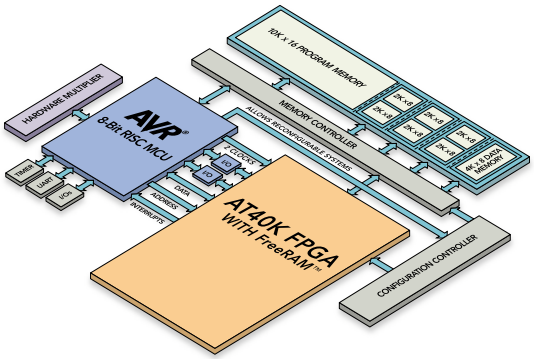


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# Is your entry ready?

# NEW PRODUCT NEWS

Edited by Rick Prescott

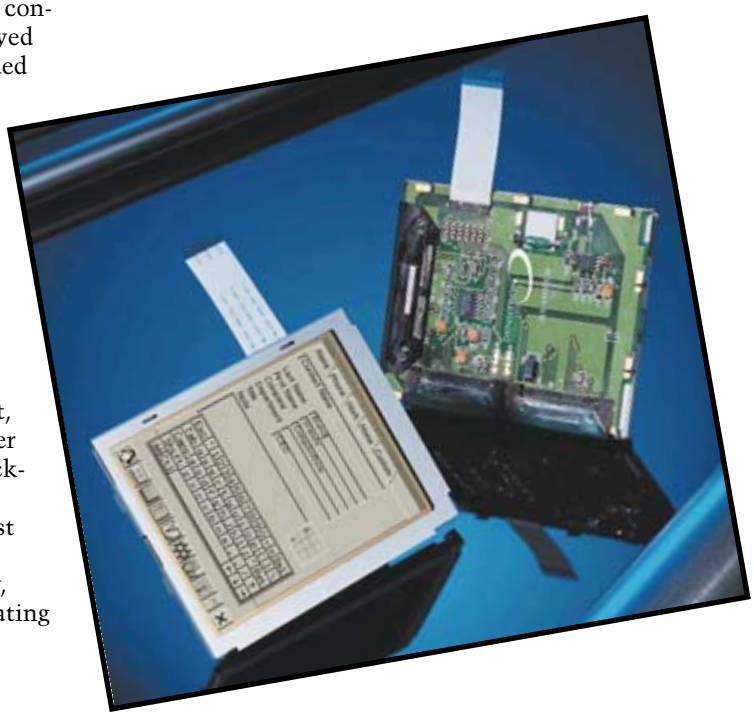
## 1/4-VGA LCD MODULE

By using the latest in Tape Automated Bonding (TAB) packaging technology, an ultra-thin LCD module has been designed that integrates all the necessary drive electronics, electroluminescent (EL) backlight, and EL backlight DC/AC inverter into a single device. The new packaging design has removed the need for elastomers to connect the LC glass to the PCB. The finer pitch employed by TAB packaging allows the driver chips to be bonded directly to the edge of the glass, thereby maximizing the active viewing area and minimizing the inactive area around the display. This technology will enable OEMs to integrate thin, lightweight, and low-power LCD modules into their hand-held and mobile applications at a cost-effective price. Applications include Personal Digital Assistants (PDAs), Global Positioning Systems (GPS), and other hand-held devices.

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Prices start at **$50** for 1,000 pieces.

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The **TSHARC-1OUSBm** and **TSHARC-12USBm** are two new USB analog resistive touchscreen controller lines. TSHARC-1OUSBm controllers support a resolution of 1024 × 1024, making them ideal for most touch input applications. TSHARC-12USBm controllers have a resolution of 4096 × 4096 for drawing, character capture, or other precision-intensive applications.

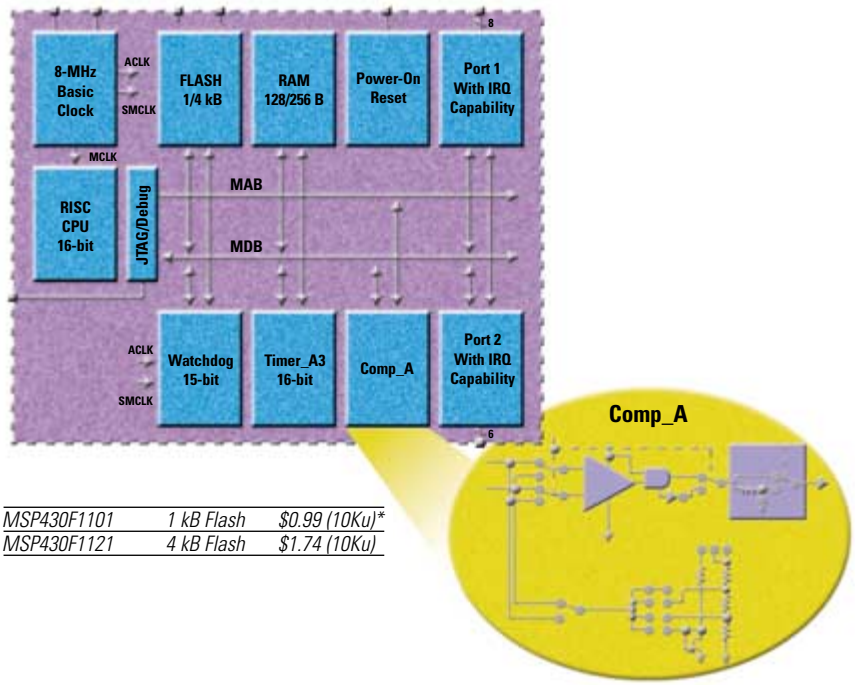


The controllers are HID-compliant to assure smooth integration with OEM applications involving compact LCDs, industrial controls, retail kiosks and medical equipment. They are also compatible with all major touchscreen manufacturers, including MicroTouch, Elo TouchSystems, 3M Dynapro, Transparent Devices, Bergquist, Gunze, Nissha, and others.

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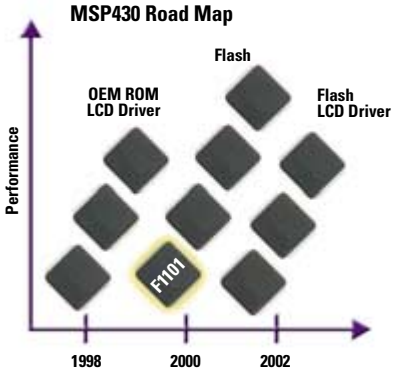
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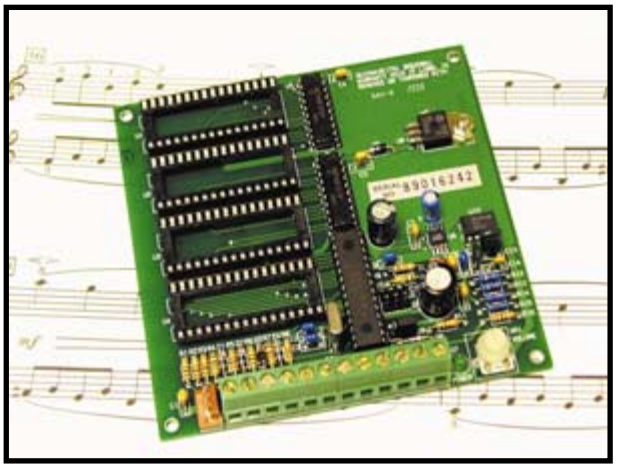
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# NEW PRODUCT NEWS

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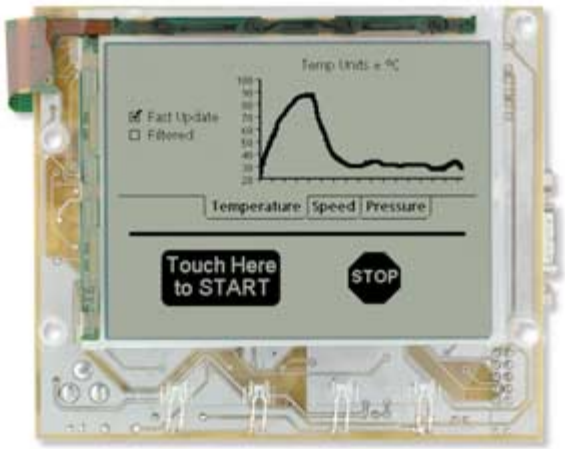


The soundboard's advantage over similar products is that it eliminates the need for signal reprocessing. In the past, sound files in standard formats must be re-digitized or converted into a proprietary format by using special equipment or software. This process usually adds additional noise and distortion to the sound. The board eliminates this extra step and offers sound quality as good as the original sound. Applications include message repeaters, talking displays and exhibits, vending machine and amusement equipment, audio output, security alarms, and more.

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# READER I/O

## BRING THE HEAT

I enjoyed George Novacek's articles relating to high temperature electronics. I have been working as a field maintenance tech in the oil field exploration sector for several years. Working on the repair side I have seen several unique failure modes of various electronic components. Most of the surveying instruments I work on are designed to operate up to 400°F, take severe vibration, and withstand 25,000 psi of pressure. Some of the signals that are measured start in the nano-volt range and must be amplified, digitized, and sent up 30,000' of 7 conductor armored wire cable. The design teams that create these instruments have a tall order in this task. Most of the older instruments used military spec components, but with the shrinking of the military, the selection of higher temp spec'd components has appeared to shrink.

I am curious to see what components you highlight as problematic at temperature, personally I see more problems with capacitors "Tantalum and monolithic, glass caps appear to live forever 10+ years" than analog ICs, resistors rarely fail under normal operating conditions, CMOS and TTL chips also rarely fail. The new generation of instruments that are appearing in the field are using surface mount technology versus through-hole, I have seen a number intermittent failures of SMT solder connections on instruments that are only one or two years old versus instruments using through-hole components 5+ years old that have had few if any solder connection problems. We use HMP solder on nearly all instruments except one that uses lead-free solder. Soldering SMT chips with high-temp solder is a certainly a practice of patience.

Most of the failures I see at temperature clear up when the temperature is lowered. A lot of the failures are from mechanical stress, large components suffer from vibration-induced fatigue. One memorable incidence was an op-amp that was position sensitive when rotated through 360°, and repeatable, the die had come loose in the TO-5 metal case. Small components without stress loops suffer from thermal expansion and contraction forces on their leads. Temperature cycling is another killer of components, the component may survive the initial high-temperature cycle but fail on a subsequent moderate temperature cycle. I also see a lot of oxidation of the solder itself that generates a gray powder that can short out closely spaced exposed traces.

The instruments I work on range from a fairly simple background gamma ray measurement "Geiger counter" to a Magnetic Resonance Imaging tool that has a 32-bit TI DSP down hole, and everything in between (formation density in g/cm$^3$, formation resistively in ohms per meter, porosity, permeability, compressive and shear strengths of the formation, water oil and gas production ratios using a pulse neutron generator and Helium3 filled detectors).

With some insight to designing high-temp circuitry I hope to better understand what can go wrong at elevated temperatures. One of the guys I work with is found of saying "There is only one correct mode of operation, but an infinite number of failure modes." How true.

And a good design will function when on fire, literally, until you use a fire extinguisher!

Alan Hansen

*I truly appreciate your letter. Your experience is right on the button. There isn't anything I disagree with. You will find an answer to your question about where to find high-temp components in the second article (*Circuit Cellar *126). With the demise of MIL, which is limited to 125°C anyway, you're on your own. But you can characterize COTS components yourself and always keep in mind that temperature is reliability killer. With the SMT size components vibrations can be handled gracefully, humidity can be controlled quite well by conformal coating.*

*And since you mentioned SMT, I had a situation where a circular circuit board placed on a rotating propeller shaft had components and solder ooze towards the circumference just after a couple hours operation at room temperature due to the centrifugal force.*

*George Novacek*

## COMING SOON?

I'm a long-time reader of Circuit Cellar Books. (They contain the best articles published in BYTE's supplement). I have some of them, but not all of them so I'm hoping that you'll consider creating a section on the *Circuit Cellar* web site with the contents of all the Ciarcia's Circuit Cellar Books and continually publish them, every year, with the best articles/projects published in *Circuit Cellar Magazine* or *Circuit Cellar Online*.

Juvenal A. Silva Jr.

*I've been thinking about posting the old books. Finding the software for the projects is the problem. People will ask for it and it would be nice to have the complete materials available. In the meantime, stay close to our web site because I'm hoping to post* Take My Computer Please *(I wrote it in '77) by April.*

*Steve Ciarcia*

FEATURE ARTICLE

Design2K Contest

WINNER

Robert Lacoste

# DDS-GEN

## Part 1: A High-Performance DDS Generator

Robert designed his DDS-GEN project with hopes of saving money and still having a way to generate sine and square signals for testing purposes. Not only did the project meet his needs, he turned a profit by winning a grand prize in the Design2K contest!

Like many hardware-addicted guys, I used to read ads presenting new and powerful measurement equipment. But, I knew I couldn't convince my boss nor my wife that I needed this $100,000 stuff! So, I started developing my own test equipment. One of the first pieces I developed was a low-frequency generator (sine, triangle, square, up to 200 kHz or so, with a 100% analog design) with nearly acceptable performance. But now, the progress in digital technology makes designing more precise, powerful, reliable devices, especially with DDS (direct digital synthesis) technology possible.

The DDS-GEN project is a full-featured, DDS-based generator that's able to generate sine and square signals from 0 to 120 MHz with incredible resolution. Moreover, it supports a blazing list of modulation modes (no less than AM, FM, PM, shaped keying, FSK, and PSK), as well as wobulation. In order to support evolution (a project is never finished), I included some daughterboard sockets to implement, for example, a full-featured ARB (arbitrary signal generator), or pulse generator. And last but not least, $400 worth of components is reasonable for such a high-end device (see Photo 1).

DDS-GEN is mainly built around an AD9852 DDS chip from Analog Devices, which is controlled by two low-cost Philips 87LPC764 microcontrollers—one main microcontroller and one microcontroller dedicated to the user interface section.

This project is complex, so you have to wait until next month to have all of the details. This month, I describe the user interface section and highlight the 87LPC764 chip. In Part 2, I'll discuss direct digital synthesis and explain why the AD9852 is really a monster chip and show how it is used in this project.

### I²C-MMI: THE CONCEPT

Developing an embedded system can be fun. Doing it twice is called experience. But, redeveloping the same kind of software again and again consumes money, wastes time, and more important, is boring. DDS-GEN is not my first project with a standard user interface. From project to project, the user interface subsystem specifications are usually stable. However, because each project is usually built around a new microcontroller, you have to rewrite a full set of low-level routines to handle these peripherals, probably copying and pasting some previous code but still debugging everything each time. Moreover, a large number of I/O pins are usually dedicated to the keyboard and LCD, needing a higher cost microcontroller.

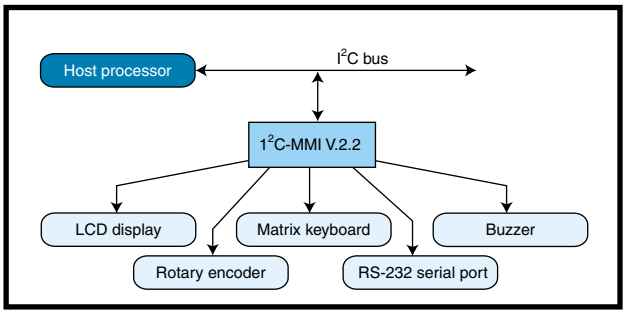



**Figure 1**—*The I²C-MMI dedicated processor chip is a standard user interface driver chip, controlling all the standard peripherals from an I²C bus.*

Of course, serial-driven LCDs are available, but they suffer several disadvantages. Because they are manufactured in smaller quantities, they are far more expensive than a parallel LCD display and are prone to obsolescence or supply shortages. In addition, serial-driven LCDs require a dedicated UART port, a scarce resource on low-cost microcontrollers. Lastly, they are slow (only 9600 bps or so). With that in mind, I started the DDS-GEN project with a "this is the last time I do that" mentality.

The user interface part of this project became a project of its own: the I²C-MMI (see Figure 1). The key idea was to develop a dedicated, low-cost, pre-programmed microcontroller chip that can do many things. It should directly handle the classic user interface, including the LCD, matrix keyboard, buzzer, rotary encoder (useful to modify a numeric value), and an extra remote control UART port. Also, it should be reusable.

The chip should communicate with the host microcontroller through a standardized non-dedicated I²C bus. And, lastly, it should off-load as many functions as possible from the main microcontroller, in particular all binary-to-ASCII formatting stuff.

With the I²C-MMI concept, the total cost of the system is in fact often lower than the cost of a classic design. The extra cost of the I²C-MMI chip is counterbalanced by the main microcontroller's lesser demands in terms of I/O pin count and memory requirements. The development costs, time, and risks are reduced, improving the time to market. And, the I²C-MMI chip can be physically fitted on a front panel PCB, communicating to the main PCB over a simple four-wire I²C and power connection, thus reducing the interconnection costs.

Good ideas are often shared. It should be noted that Jeff Bachiochi wrote about a similar idea last year, that used an I²C-driven LED panel. [1]

## I²C-MMI CHIP FEATURES

Let me list briefly the specifications of this dedicated function processor and its firmware. It's built using a pre-programmed, low-cost 87LPC764 microcontroller in 20-pin, SO20 or DIP20 packages (see Figure 2). The processor operates at 2.7 to 5 V with typically 10-mA power requirements.

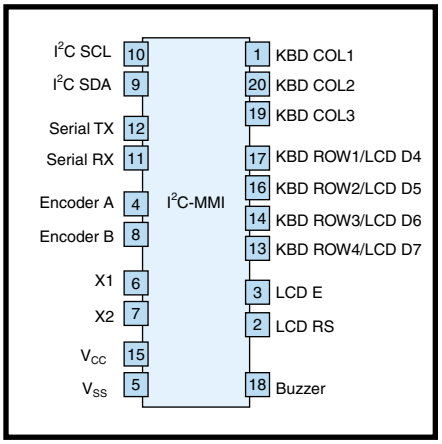



**Figure 2—***Two pins are used to link it to the main processor (I²C bus SCL/SDA) and all the other pins are used for the user interface devices.*

Connection to the host microcontroller is via a standard I²C interface (up to 400 kbps) using a simple ASCII-based protocol (see Figures 3 and 4). The processor drives any parallel LCD display in 4-bit mode. On-chip binary-to-ASCII conversion occurs with formatting. In addition, the processor handles a 4 × 3 phone-type matrix keyboard and debounces on-chip.

Specifications also include driving a piezo buzzer, driving a supplementary 19,200-bps UART port, and handling a rotary encoder for easy data modification.

The host can send a 32-bit number in binary format. The I²C-MMI chip displays it readably according to the specification and handles the local editing via the keyboard and rotary encoder. Then, the chip sends the edited value in binary form back to the host.

**Figure 3—***The I²C-MMI chip is a slave on the I²C bus. The host writes commands to the I²C-MMI I²C bus address ($40 by default) and reads the same address to poll the I²C-MMI chip for events. I²C-MMI returns one byte per read transaction, so several requests are needed for multi-byte answers. These are the possible answers when the host processor polls the I²C-MMI chip.*

| Byte 1 |
|---|
| @ ($40) |

The I²C-MMI is ready and waiting for an order or a user event.

| Byte 1 |
|---|
| ! ($21) |

The I²C-MMI is currently executing an order. No write will be accepted (nack).

| Byte 1 | Byte 2 |
|---|---|
| T ($54) | c |

A character has been received from you (either a keystroke or a character received from the serial port). The character is returned in the second byte (c).

| Byte 1 | Byte 2 |
|---|---|
| R ($52) | v |

The rotary encoder has moved since the last polling. The relative displacement is returned in the second byte (v, signed character binary value).

| Byte 1 | Byte 2 | Byte 3 | Byte 4 | Byte 5 |
|---|---|---|---|---|
| N ($4E) | n | n | n | n |

The editing of a numeric value is finished (after an E command). The new numeric value is returned in bytes 2 to 5 (32-bit unsigned binary value, lowest significant byte first).

| Byte 1 |
|---|
| $ ($24) |

The editing of a numeric value is ongoing. One new command can be written, but this command will not be executed until the end of the numeric edition.

The processor uses pseudo-logarithmic rotary encoder conversion to manage large numbers. A full turn of the rotary encoder doesn't modify a low value by the same amount as with a high value.

The extra UART port can be used as an generic UART port driven by the host processor through I²C bus transactions. But, it also can be configured through I²C orders as an automatic remote control port. In the latter configuration, anything displayed on the LCD by the host is also sent through the UART, and any characters received from the UART are transmitted to the host. It's really easy to implement a remote-control feature without a development cost. Nothing specific has to be developed on the main processor, and the device can be remote controlled via the UART port in a friendly ASCII pseudo-protocol!

## WHY USE AN 87LPC764?

To implement the I²C-MMI chip, I was looking for a microcontroller with the following features: low cost, built-in I²C hardware, supporting slave mode, low power (3.3 and 5 V), small package, one UART, integrated pull-ups to minimize component count, and an integrated watchdog for safe operation.

When the chip is ready (i.e., returns "@" or "$" when polled), the following commands can be sent to the I²C-MMI chip:

| Byte 1 | |
|---|---|
| R ($52) | Frame end |

Clear the LCD display.

| Byte 1 | |
|---|---|
| B ($42) | Frame end |

Beep!

| Byte 1 | |
|---|---|
| E ($45) | Frame end |

Enable the local editing of the last sent numeric value. This must follow an N command.

| Byte 1 | Byte 2 | Byte 3-7 | |
|---|---|---|---|
| P ($50) | c | ... | Frame end |

Send the characters given after P to the LCD at the current cursor position and/or to the serial port. This command accepts one to seven characters to be displayed in a single write.

| Byte 1 | Byte 2 | |
|---|---|---|
| G ($47) | adr | Frame end |

Move the LCD cursor to address adr (unsigned binary character), which is dependent on the LCD specifications. Address 0 is usually the first position on the first line and $40 is the start of the second line.

| Byte 1 | Byte 2 | |
|---|---|---|
| I ($49) | x | Frame end |

Select the input mode:
- x = L— only the local keyboard is activated; the serial port RX is disabled (default)
- x = R— only the serial port is activated; the local keyboard is disabled
- x = B— both the local keyboard and serial port are activated

| Byte 1 | Byte 2 | |
|---|---|---|
| O ($4F) | x | Frame end |

Select the output mode:
- x = L— only the local keyboard is activated; the serial port TX is disabled (default)
- x = R— only the serial port is activated; the local keyboard is disabled
- x = B— both the local keyboard and serial port are activated

| Byte 1 | Byte 2 | Byte 3 | Byte 4 | Byte 5 | Byte 6 | Byte 7 | |
|---|---|---|---|---|---|---|---|
| 'N' ($4E) | n | n | n | n | pre | post | Frame end |

Display the binary number nnnn in readable form on the LCD at the current cursor position and/or send it on the serial port. nnnn is a 32-bit unsigned binary value, lowest significant byte first. "pre" is the required number of significant digits before the decimal point, and "post" is the number of digits after the decimal point. Extra spaces are automatically inserted every three digits before the decimal point.

Here are examples:
- N $01 $00 $00 $00 $02 $00 displays: "_ _1" ($00000001=1)
- N $00 $00 $01 $00 $05 $03 displays: "_ _ _ _ _65,536" ($00010000=65536)
- N $FF $FF $FF $FF $08 $02 displays: "42_949_672,95" ($FFFFFFFF=429467295)

**Figure 4—***These are the different ASCII commands that can be sent to the I²C-MMI chip through the I²C bus. Before sending a new order, you must first poll the device to check if it is ready (answer "@" or "$" to a polling request).*

Some classic PIC devices fit this list, however, the Philips 87LPC76x family has an advantage. Its 8051 compatibility and large ROM code memory (up to 4 Kb) enable the use of good, freely available development tools (in particular, the excellent freeware SDCC optimizing compiler developed under the GNU license by Sandeep Dutta). [2] I don't know of any equivalent for the PICs…yet.

*Circuit Cellar* readers already know about the 87LPC76x family. [3] The Philips chips are the first low pin count versions of the famous 8051 series, fitting an enhanced 8051 core and a bunch of peripherals in a 20-pin package. The core is an accelerated '80C51 CPU running at 20 MHz and provides a turbo mode where all instructions take half the number of cycles of a traditional '80C51. That means an execution time of 300 to 600 ns for 99% of the instructions. Not too bad. An internal RC oscillator option and integrated reset circuitry allows me to use up to 18 I/O pins

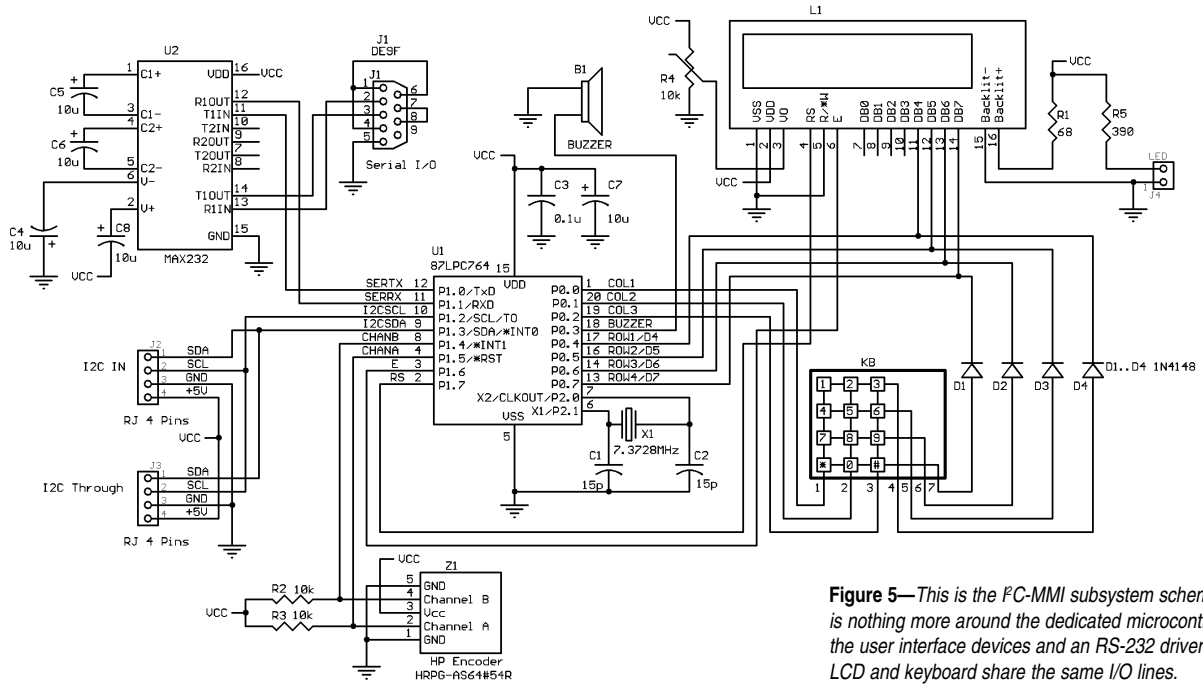



**Figure 5—***This is the I²C-MMI subsystem schematic. There is nothing more around the dedicated microcontroller than the user interface devices and an RS-232 driver chip. The LCD and keyboard share the same I/O lines.*

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**Photo 1**—*Take a look at the DDS-GEN prototype. It's housed in a compact enclosure with a homemade laser-printed front panel. For the user interface, a standard phone keyboard is used along with a rotary encoder and 2 × 16 LCD.*

when a low stability oscillator is enough (a crystal is used because I need an asynchronous UART). Standard Idle and Power Down modes are supported, with current consumption as low as 1 µA.

On the memory side, there are 128 RAM bytes and a 2- or 4-Kb OTP program memory (87LPC762 and 87LPC764, respectively). The peripherals list is complete, with two counters/timers, two analog comparators, a full duplex UART, a versatile bit-level I²C port (master or slave), eight keypad interrupts, an internal watchdog, low-voltage reset, and so on.

The I/O pins have a controlled slew rate, helping to reduce EMC concerns for the system design. All port pins can drive up to 20 mA (enough for an LED), and some provide Schmitt trigger inputs and open drain or push-pull configurations. Read the datasheet for complete information. [4]

## HARDWARE

Figure 5 shows a schematic of the I²C-MMI subsystem. Apart from the 87LPC764 chip, the only components are a MAX-232 serial level shifter, four diodes to multiplex the LCD and keyboard on the same I/O pins, a crystal, and some passive components. Two I²C connectors are included; the first connects the board to the host and the other can be used as a "throw out" connector to easily daisy chain several I²C peripherals. The rotary encoder provides two quadrature signals, which are square signals with a 90° phase shift. On the prototype, I used a Hewlett Packard 64-step encoder, a good compromise between resolution and cost.

All of the components of this user interface section fit on a double-sided PCB, with components on both sides. The user interface components are on the top and all of the other components are on the bottom (see Photos 2 and 3). This board can be directly fitted behind the front panel of the enclosure and provides front access to the LCD, keyboard, rotary encoder, and serial port.

## EMBEDDED SOFTWARE

You have a good chip and hardware around it, now it's time to write firmware. I adapted the main program plus interrupts paradigm. The structure involves a main processing loop in charge of host command decoding and execution, Edit mode processing, and keyboard handling. Also involved is an interrupt routine hooked on a 100-µs timer in charge of generic timer increments, rotary encoder processing, and buzzer signal generation. An I²C bus interrupt routine in charge of command reception and polling processing and an I²C time-out interrupt routine are included. All these routines communicate via a shared RAM (see Figure 6).

Thanks to the interrupt structure of the 87LPC76*x*, the different interrupt sources can be prioritized based on system requirements. Here, the high-



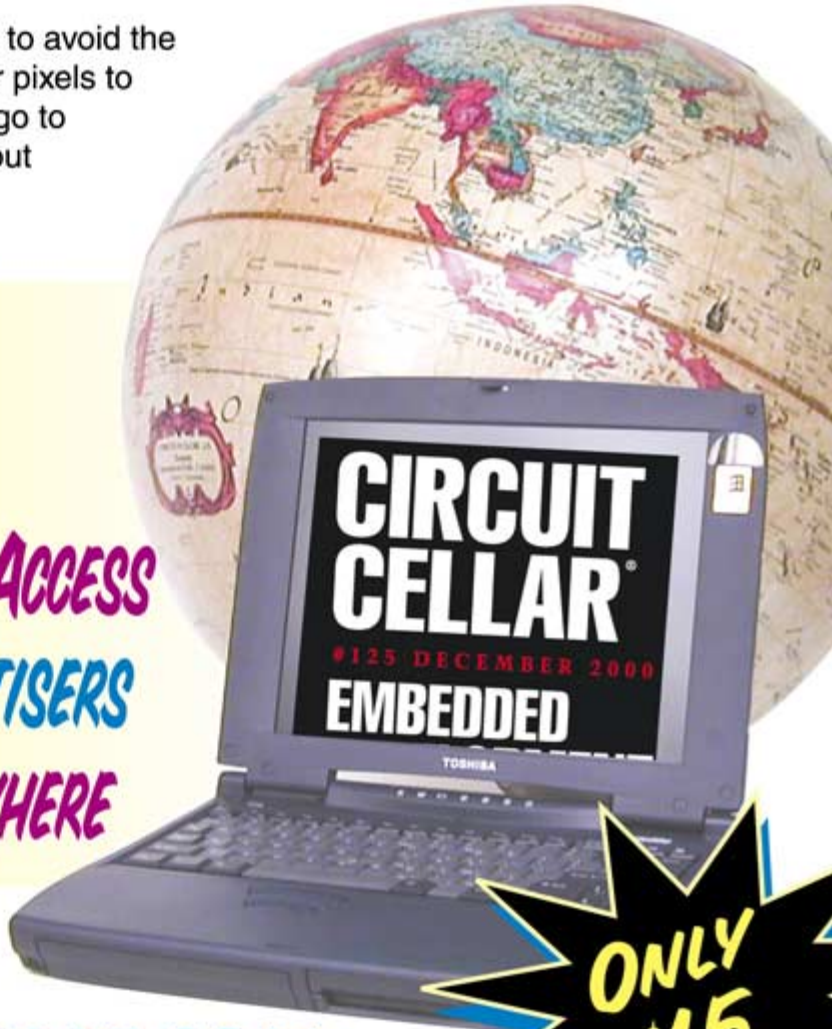
**Photo 2**—*Here is the I²C-MMI assembled PCB. This circuit board fits directly behind the front panel, all the active components (microcontroller, in particular) are on the bottom.*

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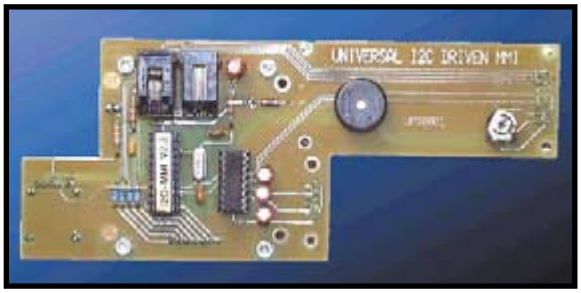



**Photo 3**—*This is the bottom of the user interface PCB. The two I²C connectors are on the top left, just above the microcontroller and MAX232 chips. The buzzer is behind the LCD with the contrast pot.*

est priority is given to the I²C timeout, then the I²C handling, then the 100-µs timer. There is one minor consequence, the beep can temporarily stop when receiving an I²C frame.

Because assembler code should be reserved for critical parts of software, the firmware was developed mainly in C language using SDCC. [2] In fact, only some parts of the interrupt routines are coded in assembler, and 80% of this assembler code comes from Philips' application note. [5]

Using a high-level language has many advantages. For me, the most important is the ability to debug a large part of the code using Microsoft's friendly development tools on a simple PC (more details to follow). And, using a good optimizing compiler like SDCC gives surprisingly good generated code.

As usual, it is better to look twice for existing things before developing from scratch. For the I²C-MMI project, apart from the Philips app note, I also found some good C code routines for handling an LCD display on the Internet for free. Thanks to Thorsten Godau for this useful `TG_4bitLCD.c` file included in SDCC distribution.

The major job of the main program is decoding and executing host orders transmitted through the I²C bus. The different orders recognized by the firmware and the possible answers from the I²C-MMI chip are stated in Figures 3 and 4. The tricky part is the local numeric editing feature. This feature was specially developed to locally handle the manual modification of integer or fixed-point parameters like setpoints in an automated device or output parameters for test equipment.

The flexibility of this feature allows off-loading all "human form" algorithms from the host CPU to the I²C-MMI chip. This is especially useful because these kinds of algorithms (binary-to-ASCII conversion, etc.) are often memory-hungry in terms of RAM and program memory. Basically, the I²C-MMI chip can work in two modes (see Figure 7).

The two modes are Standard and Edit. In the former, all keystroke and encoder rotations are sent to the host directly (with T and R messages). With the latter, keystroke and encoder rotation are locally processed, updating the current number being edited. When a new number is completely entered, it is sent to the host (as an N message).

While in Edit mode, two special keys are managed. When you press "#" or when a "#" is received from the serial port, the current edit is restarted from the first digit. When you press "*" or an "*" is received from the serial port, the Editing mode is aborted, the previous number is displayed again, a "T" message is sent to the host, and the I²C-MMI switches back to Normal mode.

In short, to let you modify a 32-bit numeric value with the keyboard or rotary encoder, the host processor must perform four steps. First, send the previous (default) numeric value with an N command, displaying the value. Second, send an E command (local editing enabled). Third, poll the I²C-MMI chip until an N (new numeric value available and returned) or a T message is received (edit aborted by the user). Fourth, go back to step three if continuous editing is required or to do anything else.

With the current firmware, the 87LPC764 memory is full. In fact, the I²C-MMI code uses all but four of the 128 bytes of RAM, and there are only 20 remaining free bytes out of the 4-Kb EPROM. Of course, this is because I stopped optimizing my code and adding new features immediately when it started fitting exactly in the available space.

When a high-level language is used on a small microcontroller, the tricky part is always the dimensioning and positioning of the stack. In this case, I started the stack just after register bank 0 (the other banks are not used), and the stack can extend up to but excluding the last three bit-addressable registers (see Figure 8). This scheme gives a reasonable stack size of 30 bytes while not using any user RAM for the stack.

The full source code of the I²C-MMI software is available on the *Circuit Cellar* web site. This code is copyrighted but can be used for free as long as it's not included in any commercially sold product. The code is full of comments so it should be easy to read, keeping in mind the global

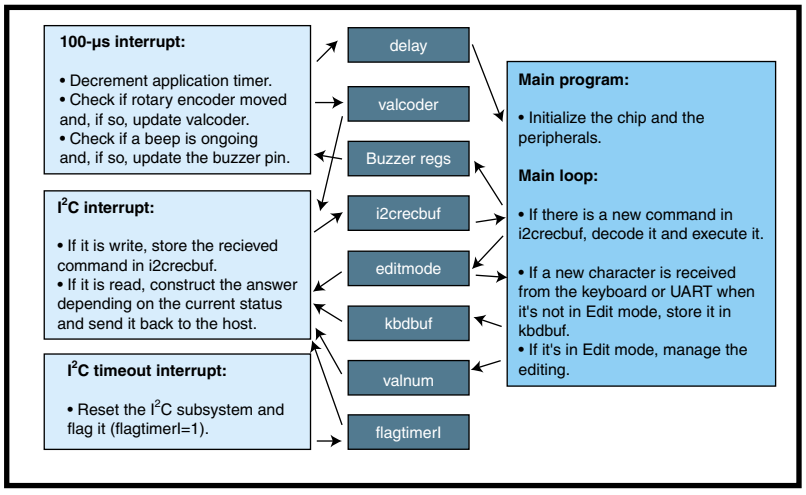



**Figure 6**—*Here is the I²C-MMI firmware structure. A main program loop dialogs with three interrupt handlers through shared variables. This decomposition allows you to manage real-time constraints and minimize software complexity.*

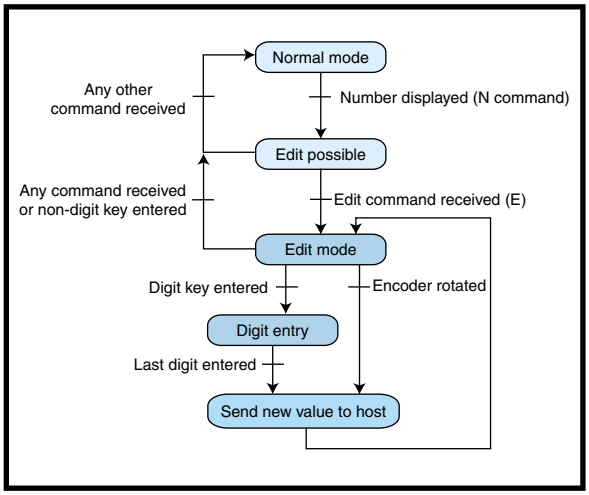



**Figure 7**—*To enter the editing mode, a number must be previously displayed (*N *command) and a specific edition command must be sent (*E*).*

architecture of the firmware.

## DEVELOPMENT PROCESS

I am not a "burn and test" guy, I prefer to spend more time in simulation steps to be sure that the first tested embedded software is not going to hang in the first microseconds. It was especially true for this project, because I didn't have an 87LPC764 in-circuit emulator, and this chip exists only in OTP form. So, burn and test is an expensive option. I would like to share with you the different development steps that I used for this project.

Thanks to the use of C, I first developed the entire message processing software on my PC with Visual C++. Small glue routines simulated the LCD display, keyboard events, and so on. All the number editing features were debugged there. The next step was to replace the classic printf formatting statements by hand-written code, still in C on the PC. This step was needed because I didn't want to exhaust the ROM with full-featured printf code. Compile on the PC, test, and debug still without any 8051 hardware or software.

Next I replaced all the emulation code with embedded stuff: integration of the I²C slave assembler routines, integration of the LCD management routines in C, hand coding of the rotary encoder management routine, and first compilation with the C cross-compiler. Then, I performed a long simulation step on the PC to check the stack allocation, which wasn't large enough at first (as usual). Unfortunately, some specific code was needed to conduct these tests, SDCC simulation software didn't simulate I²C hardware.

To be able to see what the first burned chip will be doing, I added a lot of debug statements in the code. The debug code dumped out flags and memory values through the UART and was displayed on a terminal. And finally, the first chip was burned. Of course, it didn't work. But thanks to the previous steps, I was able to get a debugged chip after only seven burned OTP chips and a couple of nights.

## SEE YOU NEXT MONTH

Now, we have a working generic user interface driven by an I²C bus. Next month, I'll describe what is at the other end of the I²C bus, the master DDS-GEN microcontroller (also an 87LPC764) and the AD9852 DDS generator chip. It will be a good occasion to discuss DDS generators and to have some high frequency headaches. Stay tuned.

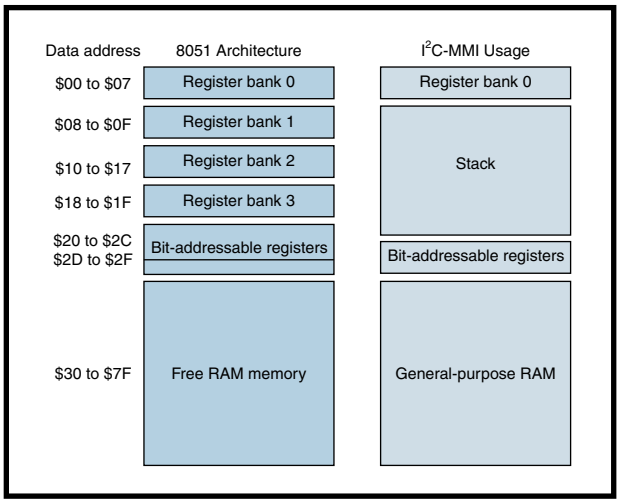



**Figure 8**—*The 87LPC764 memory map for the I²C-MMI firmware is shown here. The stack is in the register's area, leaving only one register bank (which doesn't reduce the contiguous user RAM).*

*Robert Lacoste lives in France. He has 10 years experience in real-time software, embedded system developments, and projects and operations management. He still loves building innovative, microcontroller-based devices after hours. He is currently working for Nortel Networks. You can reach him at robert_lacoste@yahoo.fr.*

## SOFTWARE

The source code is available on the *Circuit Cellar* web site.

## SOURCES

**AD9852 DDS chip**
Analog Devices
(800) 262-5643
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**64-step encoder**
Hewlett-Packard Co.
(800) 752-0900
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**87LPC76*x* family**
Philips Semiconductors
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Fax: (212) 536-0559
www.philips.com

**Visual C++**
Microsoft Corp.
(425) 882-8080
www.microsoft.com

## REFERENCES

[1] J. Bachiochi, "DFPs: Riding the Wave for the Future," *Circuit Cellar* 120, July 2000.

[2] S. Dutta, "A Retargetable ANSI-C Compiler," *Circuit Cellar* 121, August 2000.

[3] T. Cantrell, "LPC—The Little Processor that Could," *Circuit Cellar* 112, November 1999.

[4] Philips Semiconductors, "87LPC764: Low Price, Low Pin Count (20 Pin) Microcontroller with 4 kbyte OTP," January 2001.

[5] ———, "AN433: I²C Slave Routines for the 83C751," rev. June 1993.

David Ward

# PIC This Lock

The days of carrying a separate house key, garage key, breaker box key, and such may be coming to an end. With David's digital combination lock, you can provide an added security feature to your home alarm system. The only hard part is remembering the combination.

After reading several articles about Microchip's PIC16F84 microcontroller and studying its features, it seemed like a great device to design a digital combination lock around. The digital combination lock could be used to operate a garage door opener from outside of the house, arm and disarm an alarm system, or even limit access to an electrical device.

When I began the design process, I wanted specific features. I wanted low power consumption (so it can be battery-powered), either a latched or momentary output to an electromechanical relay, and audio feedback on keystrokes and indication of different modes or conditions. I also wanted LED indicators, a keypad light, and the ability to reprogram the combination from my keypad. The PIC16F84 has the features and capabilities to support all of these things.

## FEATURES

Let's look at some of the PIC16F84's features. The memory map of the PIC16F84 consists of 1 KB of flash memory, 68 bytes of RAM (0Ch to 4Fh), and 64 bytes of EEPROM (0h to 3Fh). It is a true RISC chip in that it only has 35 instructions. The PIC16F84 is designed to operate quickly and efficiently—code is executed in a single cycle. It has 13 individually configurable I/O pins with high-current source (20 mA per pin) and high-current sink (25 mA per pin) capacities. Port A has five pins and Port B has eight pins.

You can wake the PIC16F84 from a low-power Sleep mode several different ways. The digital lock software discussed here uses the change on Port B pins method to wake the chip whenever any key is pressed. Or, a timer module can put the unit back into Sleep mode. And, the digital lock software initiates Sleep mode if no keys are hit within a 3-s time period.

Now, take a look at Figure 1 to see how all of the digital lock features are implemented. The lower four bits of Port B (RB0 to RB3, pins 6 to 9) are configured as outputs in the software and then used to supply 5 VDC to the rows of a matrix keypad. Diodes D1 to D4 prevent problems if more than one key in a column is pressed simultaneously. The upper four bits of Port B (RB4 to RB7, pins 10 to 13) are configured as inputs in the software and are tied to ground via 10-kΩ resistors (R4 to R7) to prevent a floating input condition when no keys are being pressed.

The digital lock software puts the PIC16F84 in Sleep mode, where it spends the majority of its time consuming 1 to 2 µA of current. It wakes when any of the four upper bits in Port B change from 0 to 1. Thus, if the lower four bits of Port B (RB0 to RB3, pins 6 to 9) are set to a "1" condition just before the chip is put into Sleep mode, whenever any key is pressed the chip is interrupted and can begin executing its program.

Any size matrix keypad up to 4 × 4 can be used. I use a 4 × 3 keypad, and as long as the originally programmed combination doesn't use a fourth column key, there is no problem.

The PIC16F84 has several options for its oscillator circuitry, which connects to OSC1 (pin 16) and OSC2 (pin 15). I used a three-lead, 4-MHz, ceramic resonator with built-in capacitors. These resonators are inexpen-

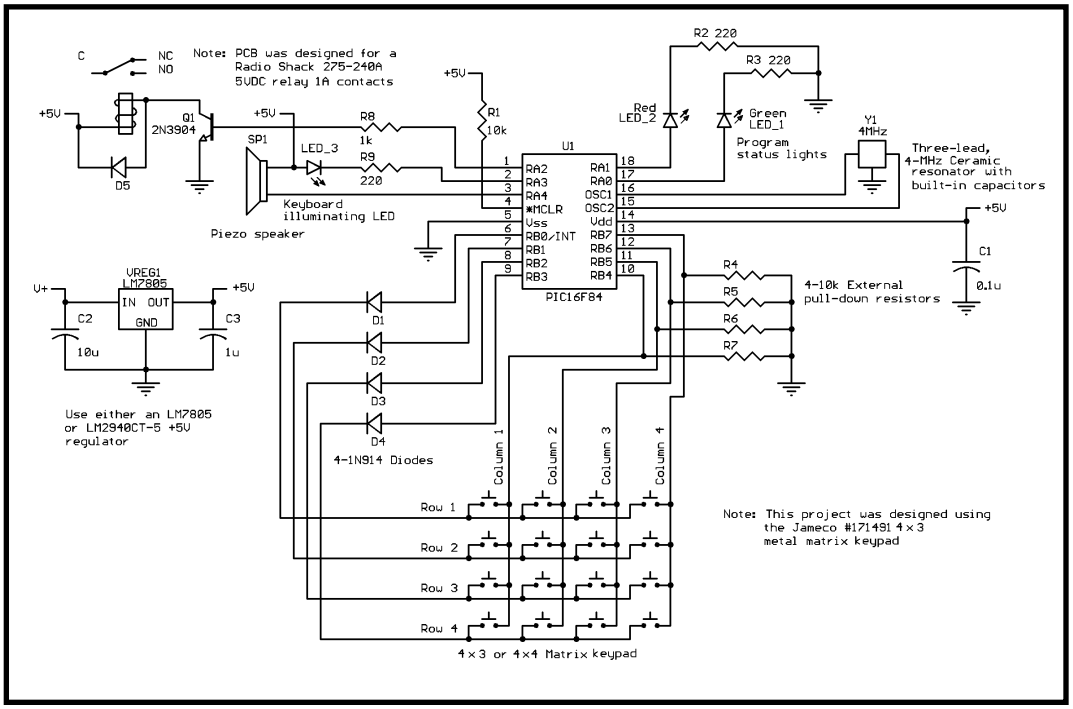



**Figure 1—***The PIC16F84 microcontroller is at the center of the design for the digital combination lock circuit. It scans the rows and reads the columns of up to a 4 x 4 keypad. It outputs to three LEDs, a piezo speaker, and an electro-mechanical relay. This design utilizes all 13 I/O pins available.*

sive, small, and using them assures more consistent system clock speeds than the resistor and capacitor option. The software I included (on the *Circuit Cellar* FTP site) is designed to operate with a 4-MHz oscillator, therefore, using another frequency will affect all of the delay loop timing, tone pitches, and so on.

All five pins on Port A (RA0 to RA4, pins 1 to 3 and 17 to 18) are configured in the software as outputs. RA0 (pin 17) drives LED 1, which is green and normally indicates keystrokes. RA1 (pin 18) drives LED 2, which is red and normally indicates the status of the relay. RA2 (pin 1) drives Q1, which in turn energizes the electromechanical relay. RA3 (pin 2) sinks LED 3, which is a high-output yellow LED used to illuminate the keypad for nighttime operation. RA4 (pin 3) sinks the piezo electric speaker. Because it has an open drain output, it can't be used to source devices connected to it.

## PIC POWER

The PIC16F84 is designed to operate at anywhere from 2 to 6 VDC (see Figure 1). The voltage regulator circuitry works for the PCB layout if you're powering the circuit from a wall power unit rather than batteries. If you desire to minimize current consumption when powering the unit from batteries, eliminate the voltage regulator and its two capacitors because it increases the Sleep mode power consumption from 1 to 2 µA up to approximately 8 to 10 mA.

Another item that can consume power, even though it appears to be turned off, is the piezo electric speaker. The piezo electric speaker connected to RA4 (pin 3) will draw power if its pin is left at a 0 state rather than a 1 condition, therefore RA4 always should be set to 1 before putting the unit into Sleep mode.

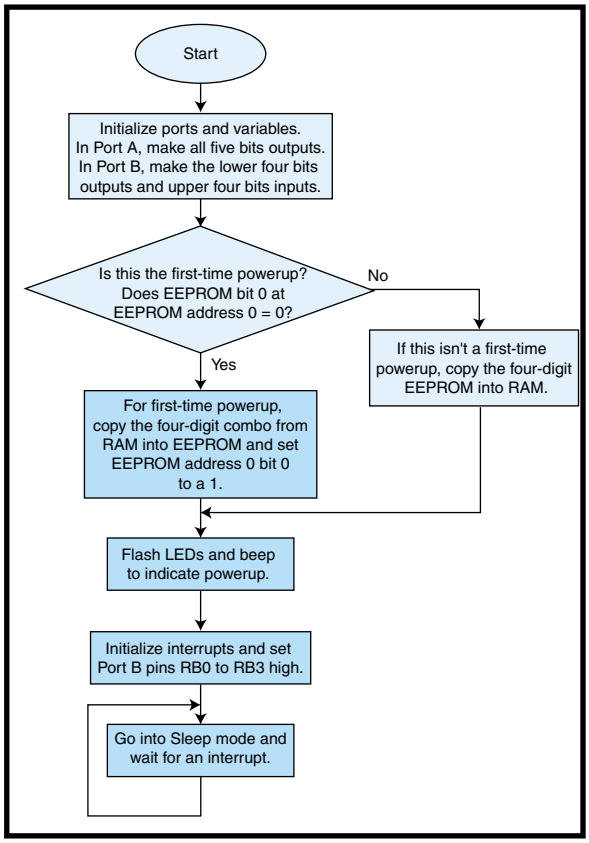



**Figure 2—***This main loop flowchart illustrates how the software functions from powerup. It first determines whether or not this is the first powerup. The first time, the software writes the combination into EEPROM. During all subsequent powerups, it reads the combination out of EEPROM. The unit then immediately goes into power-saving Sleep mode.*

## SOFTWARE

The digital lock software that makes the unit operate is too long to list. Perhaps the best way to see how the software operates is to examine the operating instructions (see "Combination Lock Operating Instructions" sidebar) and the software flowcharts. The main program loop flowchart shows how the software operates from powerup and spends most of its time in Sleep mode waiting for an interrupt (see Figure 2).

Ports A and B are initialized and then the software looks at EEPROM address 0h bit 0. If this bit is clear or 0, this is the first powerup. The program copies the original four-key combination from RAM into EEPROM and sets EEPROM address 0h bit 0 to a 1. During all subsequent powerups, the program will detect a 1 at EEPROM address 0h bit 0 and not overwrite the combination saved in EEPROM. Whenever you program a new combination, this EEPROM bit is also set so that the software will not overwrite any new combinations during subsequent powerups.

The unit then beeps and flashes the LEDs to indicate a powerup condition. The keypad row pins, RB0 to RB3, are then set to a high condition and will remain high even during Sleep mode. The unit then goes into Sleep mode and stays there until interrupted by a key hit. Note that

## COMBINATION LOCK OPERATING INSTRUCTIONS

First, let's examine Normal Operating mode. Upon powerup, the yellow LED that illuminates the keyboard comes on, the red and green indicator LEDs flash alternately, and the speaker plays five tones. The unit will then go into Sleep mode to minimize power consumption.

Pressing any key (doesn't need to be the first key of your combination) brings the unit out of Sleep mode. The yellow LED will come on, and you now have 3 s to enter the first key of your four-key combination. Then, you have 3 s between each subsequent keystroke, or the unit will back into Sleep mode. The unit is programmed with a unique four-key combination that is set by the original programming machine. This original combination doesn't need to be changed unless you desire to change it.

After you enter an incorrect combination, the unit will produce a low audio tone, the red LED will come on, and the unit will go back into Sleep mode after 3 s. You can't reenter another combination until the yellow LED has gone off.

However, if you enter the correct four-key combination, the unit will give three high-pitched beeps and energize the relay and the red LED for 1 s. The yellow LED will then go off and the unit will go back into Sleep mode after 3 s.

## CHANGING THE RELAY OUTPUT MODE

The relay can operate in either a 1-s Momentary mode or Latched mode. The unit automatically comes up in the 1-s Momentary mode after each powerup.

After a four-key combination has been successfully entered, you have 3 s to enter one of three possible mode options before the unit goes back into Sleep mode.

Then, pressing the asterisk ("*") key (row four, column one) four times will put the relay into the 1-s Momentary mode. This is the preferred mode when powering the unit from batteries because it consumes the least amount of power. You will know when the unit has accepted this mode because the yellow LED will flash. Momentary mode would be suitable for operating a garage door opener, for example.

Pressing the pound ("#") key (row four, column three) four times will put the relay into Latched mode. This mode should be used only if the unit is powered from the AC outlet or a large battery source, because the relay draws about 100 mA of current when energized. Again, you'll know when the unit has entered this mode because the yellow LED will flash.

The relay will toggle from off to on or from on to off each time a correct combination is entered. The red LED indicates whether or not the relay is energized—red LED on means yes. Latched mode can be used to activate or deactivate an alarm system.

## CHANGING THE COMBINATION

Pressing the zero key (row four, column two) four times will put the unit into the Combination Programming mode. You'll know when it enters this mode because the red and green LEDs will flash and the five tones produced at powerup will sound. The unit can be reprogrammed to any four keystrokes. However, after the original combination has been changed, it won't work, even if the power is disconnected. If you forget your new combination, there is no way to salvage the unit without reprogramming the PIC with a special PIC programmer.

After you see the LEDs flash and hear the tones play, you have 3 s to enter the first key of your new combination before the unit goes back into Sleep mode. Listen carefully for the proper beeps before entering each key of your new combination:

- after pressing the first key, wait to hear one beep
- after pressing the second, wait to hear two beeps
- after pressing the third, wait to hear three beeps
- after pressing the fourth, wait to hear four beeps

Then, you'll hear three ascending tones indicating that the unit is waiting for verification of the new combination. Enter the new four-key combination again. If it matches, the unit will beep high and low tones and then go back into Sleep mode. The new combination is now saved in the unit's permanent memory and will remain even if the power is disconnected.

During programming of a new combination, if you don't enter a key within 3 s, the unit will go back into Sleep mode and no changes will be made. Likewise, if you don't verify your combination correctly, the unit will give three low beeps and go back into Sleep mode without making changes.



**Photo 1**—*This is a photo of the inside of the digital lock unit. The keypad is mounted to the bottom of a die-cast aluminum project case and the PCB is mounted to the cover.*

the first key pressed cannot be part of the combination, because that keystroke only wakes up the chip and turns on the yellow LED that illuminates the keypad.

Figure 3 shows the interrupt servicing routine, which executes whenever a key is pressed to bring the unit out of Sleep mode. It immediately turns on the yellow LED for 3 s; if no other keys are pressed during this time, the unit will go back into Sleep mode. It will then record the next four keystrokes (unless there is more than 3 s between any keystroke) and compare them to the EEPROM combination. If they don't agree, the unit sounds a low tone and turns on the red LED for 3 s, during which time no keystrokes are accepted. If the combinations agree, then the unit sounds three beeps and energizes the electromechanical relay and red LED.

The unit comes up in the 1-s Momentary mode after all powerups. It stays in this mode until you press the pound ("#") key four times after a successful combination entry to switch to Latched mode. By the way, all keystrokes and combinations are stored as two separate bytes of information in the software, one each for the row and column. So, when referring to certain keys such as the pound key, it may not be the same code for all keypads. On my 4 × 3 keypad, the pound key is in row four, column three, and its row information is saved as 00001000 and its column information is saved as 00000100.

Figure 4 illustrates what occurs if an asterisk ("*"), zero, or pound key is pressed four times within 3 s of a successful combination entry. Pressing any key other than these after a successful combination entry will cause an error condition indicated by a low tone and the red LED being on for 3 s, during which time no keystrokes are accepted. If the asterisk key is pressed four times, the unit clears the variable `relay_flag` bit 0, which makes the unit operate in the 1-s Momentary




**Photo 2**—*By mounting the keypad and LEDs into the bottom of the project case, no bolts, screws,or nuts are exposed, making the lock more secure. However, it also helps to have a friend with a CNC mill to machine the keypad holes.*


Frustration? No, thanks.
Fun? Yes, please.

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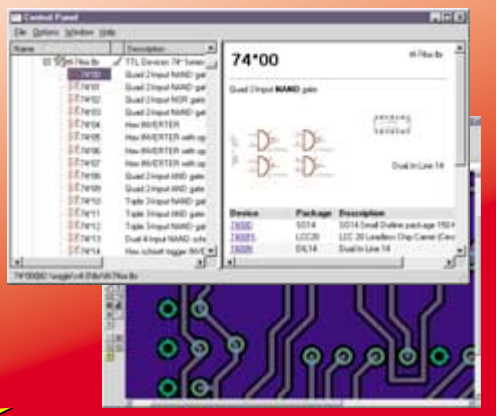
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- New Library Management with Component Browser
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- Design your own commands via User Language
- Unlimited length for component names/values
- Design Rules define pad/via dimensions and shapes
- Net Classes for Autorouter and DRC
- Minimum Autorouter grid: 0.02 mm
- SMD pads can be rounded or round
- Different pad shapes for Top, Bottom, or Inner layers



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mode. Also if the relay was latched on, it will turn it and the red LED off. The unit acknowledges acceptance of this mode by flashing the yellow keypad LED.

If the pound key is pressed four times, it sets the `relay_flag` bit 0, which makes the unit operate in Latched mode. Each time a correct combination is entered, the relay and red LED toggle off if it was on and toggle on if it was off.

Pressing the zero key four times puts the unit into Programming mode so you can teach it a new four-key combination. The unit lets you know it has entered this mode by beeping and flashing the red and green LEDs. You then can enter each new keystroke while waiting to hear one beep after the first keystroke, two beeps after the second, three beeps after the third, and finally four beeps after the fourth keystroke.



**Photo 3—***Look at how all-thread was used to mount the unit through a wall. The only way to open the unit is to undo the nuts from the all-thread from inside the house or garage and then pull the unit out, exposing the screws that hold the project case to the bottom.*

The unit then gives three ascending tones indicating that you should enter the four new keys again to verify the new combination. If a wrong key is pressed during verification, an error signal is given with three low beeps and the unit goes back into Sleep mode, leaving the old combination unchanged.

Like during most operations, you have only 3 s between each keystroke before the unit goes back into Sleep mode. If the verification is successful, the unit will beep several high and low tones and turn on the green LED. The new combination is then saved in EEPROM and will take effect even after another powerup. This poses a problem if you forget the new combination; the only way to recover the unit is to reprogram the PIC using a PIC programmer.

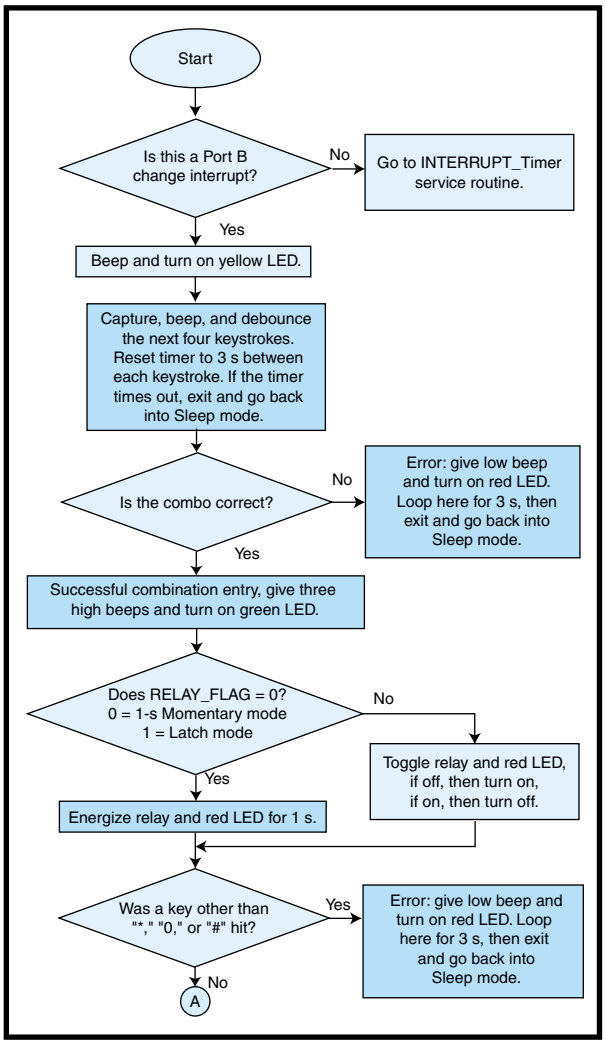



**Figure 3—***The interrupt service routine flowchart illustrates what happens when the unit is awakened from Sleep mode by a keystroke. If a correct four-key combination is entered, the unit then activates the relay. If an incorrect combination is entered, the unit gives a low-pitched tone indicating an error.*

## LAST MINUTE DETAILS

The last item to consider is how to mount the PIC digital combination lock securely. I am using the lock to allow access to my garage through the garage door. We usually leave the door between the garage and house unlocked so our kids can get into the house after school. I mounted my circuitry inside a die-cast aluminum project case that is 4.7″ × 2.4″ × 1.6″. I have access to a CNC mill, so I milled 12 square openings in the bottom of the case for the keypad keys to project through (see Photos 1, 2, and 3).

Then, I mounted two all-thread bolts through the lid and bolted the unit to the garage door frame. Mounting the unit in this manner is preferred because it doesn't expose screws, nuts, or bolts to the outside, which prevents tampering. I power the unit with four series-aiding, AA batteries, which I put just inside the garage because the box is too small for them and the circuitry.

Finally, I made an aluminum deflector that attaches to the top to deflect rain and snow and reflect the yellow keypad LED. The project works well and battery life has been good, because I use only the 1-s Momentary mode to activate my garage door opener. Most openers can operate from a simple N.O. momentary pushbutton switch or doorbell switch. Just connect the C. and N.O. contacts of the combination lock in parallel with the doorbell switch, and the door opener should be activated.

I've learned a great deal about the PIC16F84 microcontroller and nearly every feature that it offers while developing, programming, and building this PIC digital combination lock. Microchip's PIC16F84 has been a great microcontroller to work with, it's cost-effective and has great features, as well.

*Author's Note: I'd like to acknowledge the help of Southern Utah University student Nathan Jones in*

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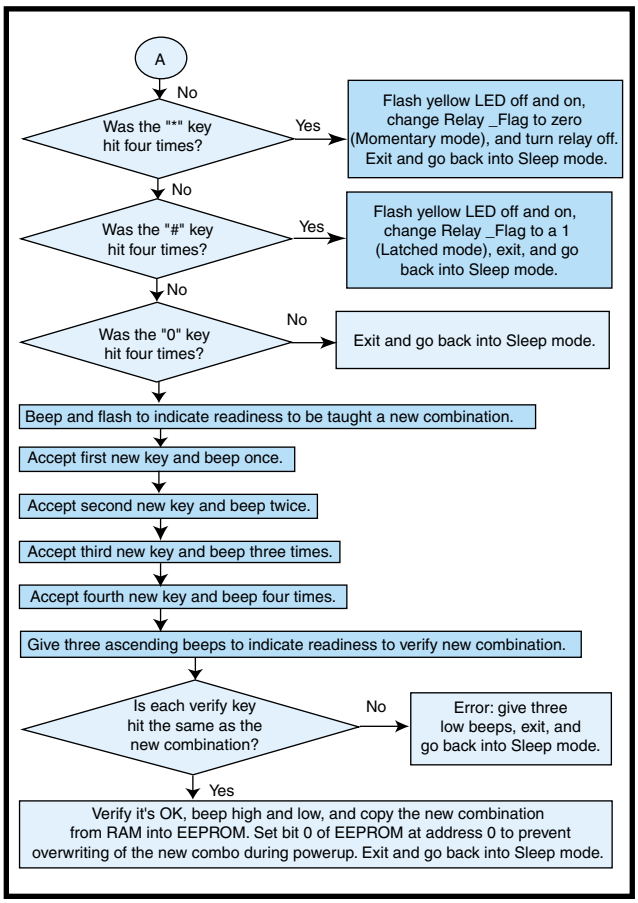



**Figure 4**—*The Programming mode flowchart illustrates what happens if you press the "*", "#", or "0" key four times after the successful entry of a combination.*

*writing the software for this project. I presented him with the features I needed and how I wanted the unit to operate and he made the software work. To order a programmed PIC, send a check or money order for $12 plus $3 shipping and handling to David A. Ward, 2261 W. Skyview Drive, Cedar City, UT 84720.*

*David Ward has been an associate professor of electronics engineering technology at Southern Utah University in Cedar City, Utah since 1985. He holds an M.S. in Industrial Education from Brigham Young University. He can be reached at ward@suu.edu.*

## SOFTWARE

The code for this project is available on the *Circuit Cellar* web site.

## SOURCE

**PIC16F84**
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## RESOURCE

Microchip Technology Inc., "PIC16F84 Rev. A Silicon Errata Sheet," search2.microchip.com/download/lit/suppdoc/errata/er16f84.pdf, 1998.



FEATURE ARTICLE

George Novacek

# A Sure Thing

## Guaranteeing 99.99999% Reliability

If you're a gambler, play the lottery, but if you want to take the gamble out of project design, then listen to what George has to say. Performance guarantees are an important factor in avoiding costly retrofits or redesigns after you've already built the prototype.

One of the challenges you face when designing an electric airplane or, for that matter, any other process control or robotic system, is the performance guarantee. This is something you must face early in the design process. Discovering that the system doesn't meet the performance guarantee after you built a prototype may not be too late to save the project, but will cost a lot of money in rework and late delivery. Investing a little time up front with paper and pencil will pay handsome dividends later. In this article, I will show you how to use reliability tools to your advantage during the concept stage of a new design.

### RELIABILITY DATA

Reliability prediction, fault tree analysis (FTA), and failure modes and effects analysis (FMEA) are powerful design tools, but to use them effectively, you need solid data. Needless to say, your results will be only as good as your data. There are several excellent sources available. The best and most obvious source is your own data or the component manufacturer's records. Any QA (quality assurance) department worth its salt must have a database of product failures during manufacturing, testing, and in the field continuously updated. Often though, component manufacturers do not publish data for competitive reasons and your own records may be insufficient.

"Reliability Prediction of Electronic Equipment" (MIL-HDBK-217) is a military handbook that's a rich source of information. [1] You can download it free from www.dsp.dla.mil. The most recent revision is F, and you also should download Notices 1 and 2.

MIL-HDBK-217's attempts to mathematically model devices by their types. This is a mammoth task, given the variety of uses, environments, and manufacturing processes. It worked well during from the '60s to '80s, but with the explosion of microelectronics in the last decade and the unprecedented strides in their manufacturing process control, the MIL-HDBK-217 could not be updated fast enough. Nevertheless, when used judiciously, it remains an excellent tool.

Another useful and accessible tool is the Reliability Analysis Center (RAC) of the Department of Defense. The center has a web site that includes data books and other information. Unlike the MIL-HDBK-217, the information isn't based on mathematical modeling, but rather on field data obtained from manufacturers and users. You find the component you are interested in and receive a wealth of information not only about its failure rate, but also the types and distribution of failures, origin of the reports, and so on. This is the database your QA manager dreams of developing, if he only had access to all government suppliers' field data.

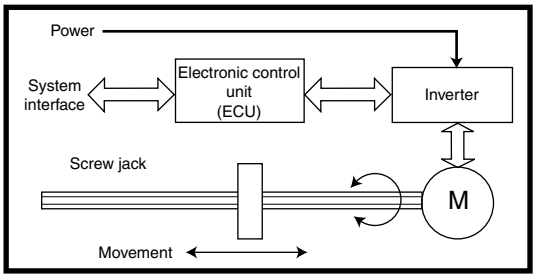



**Figure 1**—*A brushless motor drives a screw jack, which moves a mechanical arm.*

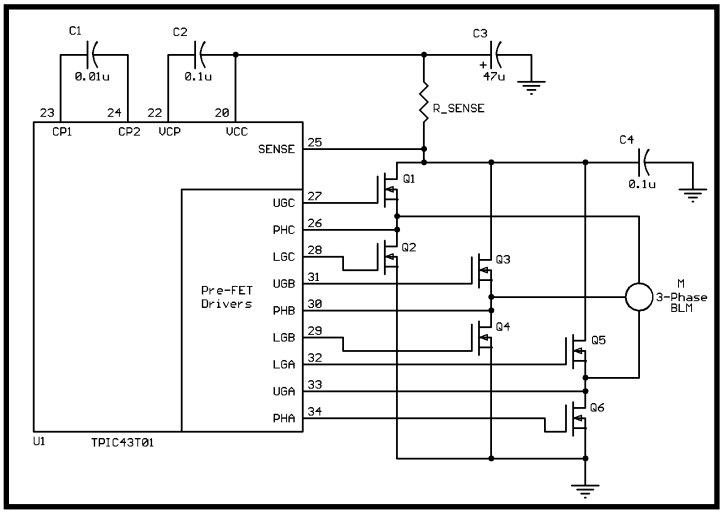



**Figure 2—***A typical inverter can be built with power FETs and a control IC, such as this one from Texas Instruments. Many other ICs are available or you can create your own using an FPGA.*

Unfortunately, this tool is not free. It costs several hundred dollars, but is a bargain for the data it provides.

There is also commercial software available for people who cannot afford not to spend the high asking price for the tool of their trade. One of the better known, widely accepted tools is produced by Relex. You can obtain a database of electrical and mechanical components from the company's web site. And, the software will automatically generate the analyses for you and use different mathematical models, including MIL-HDBK-217.

## 99.99999% GUARANTEE

So, here's the problem: It makes no difference whether you are designing the electric airplane or a robotic system, your task is to design an electrically actuated motion system that moves some mechanical bits and pieces, be it control surfaces, brakes, or whatever. A failure of the system to move the parts won't be catastrophic, but will present enough problems for you to want to minimize the possibility of its occurrence. The customer has done the system hazard analysis and come up with the requirement that the probability of the failure must be less than $10^{-7}$. In other words, the system availability must be better than $1 - 10^{-7}$, that's 99.99999%. Not a laughing matter!

This is where some analysis and simple calculations ahead of time can save you grief later. Figure 1 is a shows the system you are about to design. You will use a DC brushless motor because of its torque/speed characteristics, low maintenance requirements, and low EMI when compared with DC brush commutated motors.

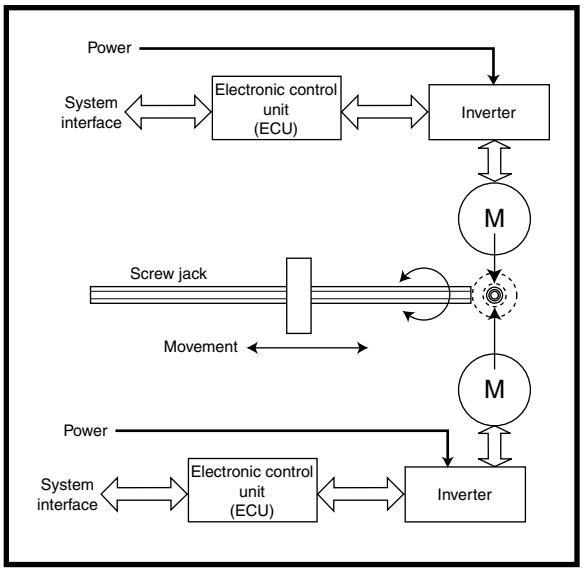



**Figure 4—***Two motors provide a dual redundant drive by coupling through a planetary gear adder. The gear and screw jack remain single-point failures, so it is important that they have low failure rates.*

## COMPONENT RELIABILITY

The first step will be to identify the individual system components and their reliability. The most important one is the motor, so let's start with that. Unlike most electronic components, as a result of wear, motor instantaneous failure rates are not constant but increase with time. Because the MIL-HDBK-217 failure rate model is based on a constant failure rate, you will develop an average failure rate for the motor operating over a time period known as its life cycle (LC). At the end of the life cycle, it is assumed that the motor will be replaced or overhauled. Thus, you can calculate the average failure rate:

$$\lambda_p = \left(\frac{\lambda_1}{A \times \alpha_B} + \frac{\lambda_2}{B \times \alpha_W}\right) \times 10^6 = \frac{\text{failures}}{10^6\ \text{h}} \quad [1]$$

where $\alpha_B$ is the Weibull characteristic life for the bearing and $\alpha_W$ is the Weibull characteristic life for the windings. These parameters depend on the operating temperature. Let's assume that the motor will operate in a room temperature environment from 25°C to 30°C. For this temperature, MIL-HDBK-217 states that $\alpha_B$ = 78,000 h and $\alpha_W = 8.9 \times 10^5$ h.

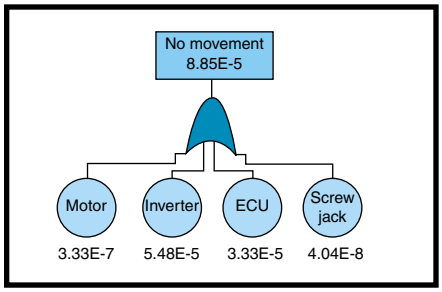



**Figure 3—***The FTA shows you clearly that the system does not satisfy the specification requirement and helps you identify the cause. In this case, note that both the ECU and inverter's failure rates are higher than the required outcome.*

This mathematical model purposely does not take into account failure of commutators (brush or electronic). Brush commutators would have to be inspected and serviced regularly for this failure model to remain valid. As already stated, because this application requires a long life, maximum reliability, and minimum maintenance, you wouldn't consider using a brush commutated DC motor. But I hasten to add that the reliability of modern brush commutators is nothing to sneer at and you shouldn't dismiss this established technology.

For general application electric

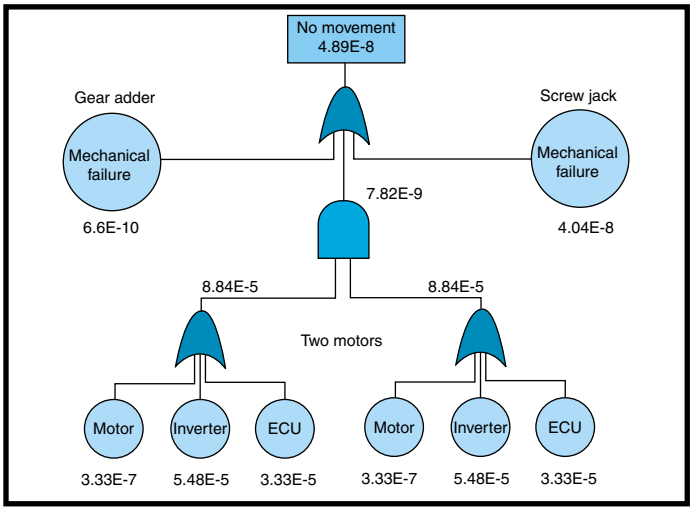



**Figure 5**—*Here's the FTA of the two-motor configuration shown in Figure 4. Notice the importance of the low failure rate of the gear and screw jack.*

motors, MIL-HDBK-217 shows constants A = 1.9 and B = 1.1. $\lambda_1$ and $\lambda_2$ are related to the life cycle (i.e., the expected operating life of the motor). The customer requires that the system last three years without the need for an overhaul. Although the entire system operates 8 h per day, your subsystem requiring 99.99999% availability will not be needed more than one third of this time. Therefore, you can calculate the LC to be 2,920 h, which results in $\lambda_1 = \lambda_2 = 0.13$. And then, plugging these values into Equation 1 results in:

$$\lambda_p = \left(\frac{0.13}{1.9 \times 78{,}000} + \frac{0.13}{1.1 \times 8.9 \times 10^5}\right) \times 10^6 = \frac{\text{failures}}{10^6\ \text{h}} = 1.01 \times 10^{-6} \quad [2]$$

It is worth noting that the bearings have an order of magnitude greater effect on the motor failure rate than the windings, a fact I will revisit later. Because the motor will be required to operate no more than 0.33 of the system operating time, you can apply this duty cycle to its calculated failure rate and assume:

$$\lambda_{pr} = \frac{\lambda_p}{3} = \frac{1.01 \times 10^{-6}}{3} = 3.33 \times 10^{-7} \quad [3]$$

The other electrical components of the system comprise an inverter and an electronic control unit (ECU). The typical inverter is shown in Figure 2. It uses power FETs and a Texas Instruments' integrated circuit, TPIC43T01. Other power semiconductors, such as bipolar or IGBT transistors, can be used in place of the FETs. Similarly, there are numerous control ICs on the market. Or, you can design your own controller using a DSP or FPGA. Based on several different concepts with Hall effect diodes used for position sensing, component level calculation per MIL-HDBK-217 specification will yield an estimated failure rate of $2.01 \times 10^{-4}$ for the inverter. After application of the 33% duty cycle, assuming that the power will be off when the function is not required, the final failure rate will be $5.48 \times 10^{-5}$.

The ECU will be a microprocessor-based embedded controller providing system interfaces, motion control, and most importantly, system diagnostics and failure detection. Similar systems I developed exhibit an MTBF better than 30,000 h in the harsh aerospace environment. For this article's calculation, you convert the MTBF into failure rate by calculating its reciprocal. The result equals $3.33 \times 10^{-5}$. The ECU can't take advantage of the duty cycle, because it will always be powered together with the rest of the system.

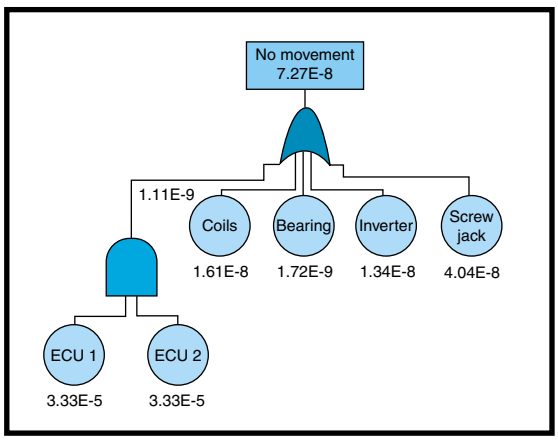



**Figure 6**—*The ECU is dual redundant, as is the inverter. As a result, the single motor system (brushless) satisfies the specification requirement.*

The motor will drive a screw jack as shown in Figure 1; if it fails, the whole function goes down. You do not supply this component. Make sure the customer understands this single-point failure and selects a component with failure rate roughly one order of magnitude better than the function needs. The screw jack selected has a failure rate of $1.22 \times 10^{-7}$. Fortunately, the duty cycle applicable here will bring it down to the acceptable $4.04 \times 10^{-8}$.

## PUTTING IT TOGETHER

It's immediately obvious that the function cannot achieve the required $1 \times 10^{-7}$ failure rate when the inverter alone is more than two orders of magnitude worse than the customer expects (see Figure 3). The system components, which include the motor, ECU, inverter, and mechanical linkage (screw jack), all feed into an OR gate, meaning that any one of these components failing will cause the function to fail. And the failures are additive, making the outcome almost three orders of magnitude worse than required.

What's the solution? The word for it is redundancy. By making the components redundant, both would have to fail for the function to fail. Their individual failures now feed into an AND gate. Mathematically this means that the failure rates multiply.

It is interesting to note that the three solutions proposed here provide similar failure rates. As a result, the best concept selection will not have to be based on the achievable reliability but on other design issues such as economics and practicality.

RABBIT

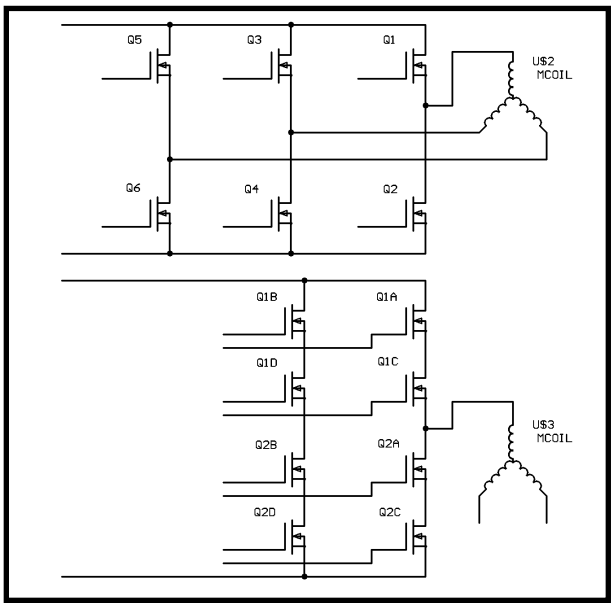



**Figure 7—***Here you can see the business end of the inverter. Six power FETs originally needed to drive the three windings have grown to 24. Also, four independent driver ICs are needed.*

Figure 4 is the most obvious solution, frequently used in the past with brush commutated motors. The brush commutator represents a single-point, high-rate failure, which can't be easily fixed by redundancy. Therefore, two identical motors are coupled through a planetary gear assembly acting as an adder. This is analogous to a car differential drive with the motors attached instead of the wheels.

The FTA of this design is shown in Figure 5. The planetary gear coupler can be obtained with $2 \times 10^{-9}$ failure rate, which is reduced to $6.6 \times 10^{-10}$ by application of the duty cycle. Although simple, this configuration presents several, sometimes insurmountable, problems. First, it needs two motors. Their cost notwithstanding, the increase in size and weight may be prohibitive. The other problem is that the planetary gear is an adder. If one motor fails, the velocity of the screw jack will be cut in half, which may not be acceptable.

## OTHER IDEAS?

The mathematical model for electric motors in MIL-HDBK-217 considers failure of the bearings and the windings. It doesn't take into account the different quality of bearings and windings you can achieve through process control nor does it fully account for different stress levels seen in brushless motors because the windings are stationary. A search through the RAC database reveals that the experienced failure rate of this kind of motor's bearings is $5.2 \times 10^{-9}$ and the windings are $4.87 \times 10^{-8}$. With the application of the 33% duty cycle, these failure rates are reduced to $1.72 \times 10^{-9,}$ and $1.61 \times 10^{-8}$ respectively.

This means that the mechanical, failure-prone motor components, armature, and bearings exhibit failure rates much smaller than the permitted result. Therefore, they can be used in a single point of failure mode. It is the electronics in the ECU and inverter that are the problem and need to be redundant.

The FTA in Figure 6 shows the configuration that will do the job. Notice that two independent ECUs feed through an AND gate, thus achieving a $1.11 \times 10^{-9}$ failure rate. This means that you must be able to determine which ECU is correct if there's a disagreement. This calls for a fail operative controller. The design of such a controller is outside the scope of this article, but I'll address it in the future. Also notice that the inverter's failure rate decreased dramatically, from $5.48 \times 10^{-5}$ (using the 33% duty cycle) to $1.34 \times 10^{-8}$. How is it possible? Consider the simplified schematic diagram in Figure 7.

The failure distribution numbers in the RAC database state that the power FET failures are split roughly 50/50 between short and open circuit. This means that each power semiconductor device has to be replaced with four, such that no single failure can prevent the inverter from continuing to function.

So, while you can achieve the needed failure rate of $1.34 \times 10^{-8}$, the price you pay is the significantly higher component count and a more complex fault detection circuitry. Whether or not this is a practical approach is a matter of economics. For high-power, IGBT (insulated gate bipolar transistor) driven motors, which cost hundreds of dollars, it may be better to add a parallel set of windings to the stator (see Figure 8). The corresponding FTA in Figure 9 shows the result. The driver is now less complex and the winding dual redundancy helps lower the failure rate by about 30%.

## THE NUMBERS GAME

You have seen how powerful and timesaving a simple reliability analysis can be when applied early. Used with common sense, and I must emphasize the common sense, it can save time, money, and frustration that always accompany rework and failures. Do not expect precision! Too many engineers make the mistake of confusing reliability prediction with accounting, not realizing that even accountants are creative.

The predicted failure rate is a number, usually reflecting the worst-case condition, originating from an imperfect mathematical model or statistical analysis that can rarely duplicate or account for all the working conditions your product will encounter. The sta-

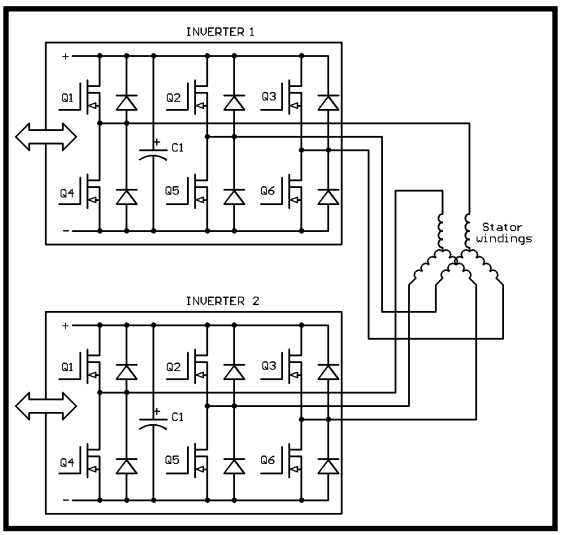



**Figure 8—***This configuration saves 12 power drivers and requires a second set of stator windings.*

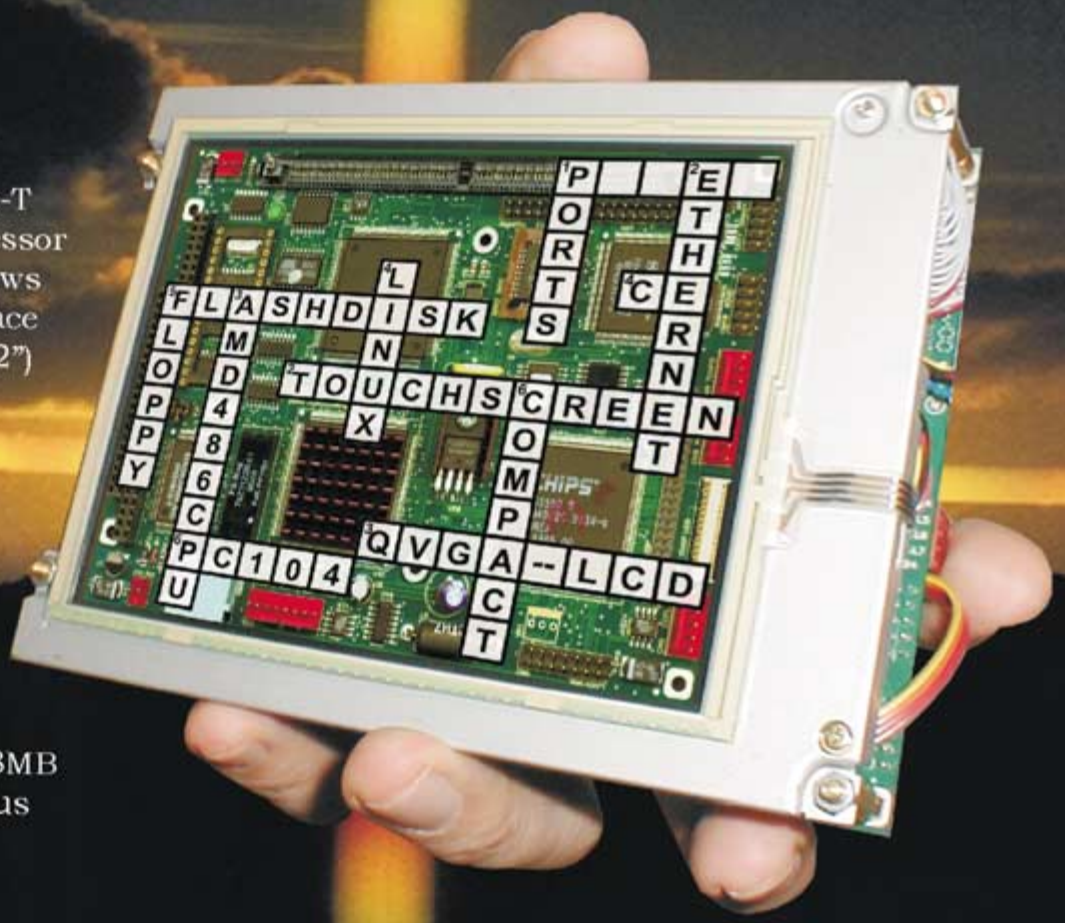
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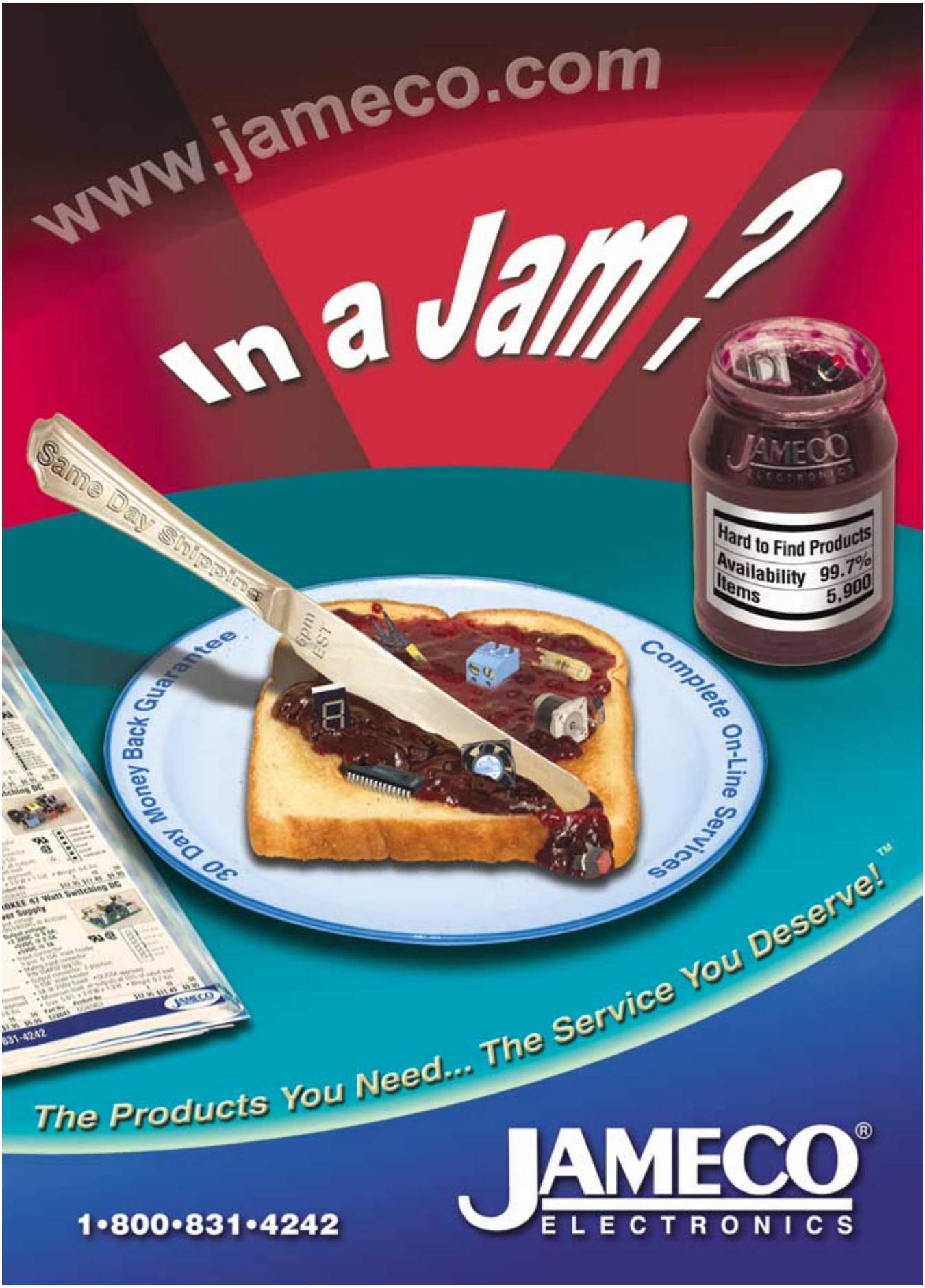
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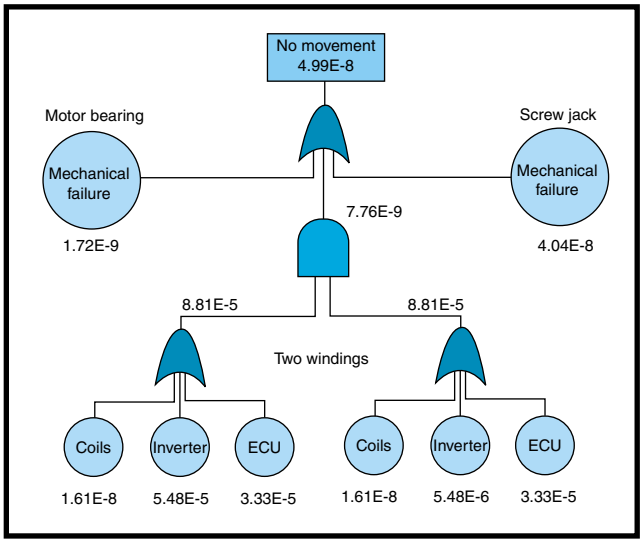



**Figure 9**—*The FTA shows the failure distribution of the two-windings configuration in Figure 8.*

tistical reliability prediction is an excellent tool for identifying potential problems and weaknesses early in the design process and for helping to model the system architecture to meet the intended specification. If I get within the same order of magnitude of the intended performance, I'm happy. I've seen too many (ignorant) customers excited about the analysis result being off by less than 1% and too many (equally ignorant) engineers wasting time by tweaking the numbers to achieve bureaucratic victory and "meeting the spec dead on."

It's a good idea to always keep the concept of the slide rule with its two decimal places of precision in mind. The imperfect world of engineering will rarely require more than that. Remember, the mere presence of 64 decimal places on your calculator display does not mean that the calculation based on your estimate will automatically acquire the same precision. So, make sure you don't lose your perspective by getting immersed in unimportant details.

## WRAPPING IT UP

In the end, it is the performance that counts. No statistical analysis can change that. I have always seen the mature product reliability exceed the calculated value. The reason is not merely the conservative reliability model but the development process, as well.

Having identified weak parts, proper steps can be taken to avoid later problems. It is equally necessary to keep a record of all failures, analyze them, and take corrective action if necessary. In aerospace technology, this has an official name, Failure Reporting and Corrective Action System (FRACAS). Behind the long name is a common sense activity to close the loop between the user and designer.

With critical or large-volume products where the risk of field problems is not tolerable, accelerated testing is done as part of the reliability growth. The system is stressed until its weakest link fails. It is analyzed, corrected, and then stressed again. The purpose is to achieve not only the desired mature reliability quickly but also to have the reliability spread evenly across the product.

There is no point in having a sturdy, expensive design with one weak part causing failures. In fact, if such failures still meet the specification, it may be wise to degrade the rest of the components and reduce the cost.

The one thing I haven't talked about in this article is the power supply. Of course, if the power supply's reliability doesn't support the availability requirement of the function, there is nothing you can do about it. So, from the beginning, assume that the power will be available.

A rule of thumb is that, when it comes to DC motors, voltage gives you speed and current gives you torque. With the increasing power demands you put on DC motors, there is a practical limit for the current, beyond which it is advantageous to increase the voltage and obtain the torque by gearing down the motor's speed. Today, it is not unusual to see DC motors running at 300 VDC and spinning at over 20,000 rpm.

Although automotive systems are moving toward 42 VDC and avionic systems already use 28 VDC to reduce current, this is not enough for the high-power, 50-kW (unbelievably small) motors you encounter in modern servo systems. In a future article, I'll show how the power is generated and talk about some of the peripheral issues such as power quality.

*George Novacek has 30 years of experience in circuit design and embedded controllers. He currently is the general manager of Messier-Dowty Electronics, a division of Messier-Dowty International, the world's largest manufacturer of landing-gear systems. You may reach him at gvovacek@nexicom.net.*

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FEATURE ARTICLE

Tom Napier

# A Single-Chip PN Sequence Generator

Picking up where he left off last November, Tom takes us through the process of constructing a psuedo-random number generator, using only one chip, one crystal, and one selector switch. There are multiple uses for a programmable PN generator, and he'll show you those, too.

In my *Circuit Cellar* article published last November, I described some applications of pseudo-random number (PN) sequences. [1] I explained how to generate them with hardware and alluded to using microcontrollers as PN sequence generators. I'd like to expand on the latter idea this month and introduce a single-chip programmable PN generator.

A single-chip programmable PN generator uses a Microchip PIC16C54 18-pin microcontroller to generate many different PN sequence lengths. You can use this device as a binary test source, audio noise generator, or data encoder. Four of the chip's output pins provide the PN sequence, bit clock, frame synchronization pulse, and byte clock. The latter can load 8-bit random numbers into a DAC with the help of an external shift register. The output bit rate is 0.01 of the clock frequency and can be set by a crystal or an external source. The raw PN generator is shown in Figure 1.

My first draft of the design generated 16 sequences having lengths from 7 to 8,388,607 bits ($2^{23} - 1$), but later that changed. Now you have the option of either a byte clock output or a data modulation input. The maximum sequence length extends to 2,147,483,647 ($2^{31} - 1$) but there is a smaller choice of lengths.

## THE GENERATOR CODE

In my previous article, I gave a fragment of code that generates sequences whose shift registers had fewer than 16 bits. Because this code uses bit test instructions, it generates one predetermined sequence. What I wanted was a chip that can be programmed to provide sequences of several lengths by wiring port pins high or low. How do you do this?

There are two approaches to this type of program that you can use. One uses a single code loop with variable parameters. In this case, these would set the shift register length and the tap positions. The other approach says, hey, I only have a few cases to consider, let's give each one its own dedicated loop.

Which solution you choose depends on whether or not there is program memory space for all the loops and whether or not a single multifunction loop is significantly longer than a dedicated loop. Bear in mind that the multi-loop solution needs room for both the start-up code and the code that reads your input and selects which loop to execute.

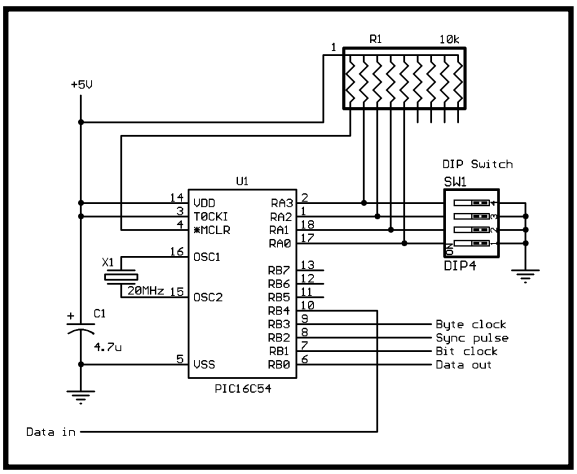



**Figure 1**—*Generating a binary PN sequence takes one chip, a crystal, and a length selector switch.*

So, how many dedicated loops can you shoehorn into the 512 instructions of the '16C54? Well, that depends on how long a loop is going to be. A loop executes once per output bit, thus its length and the processor's clock frequency limit the maximum bit rate. As a general rule, shorter loops are better because they make the output run faster. Within each loop, you have to cycle the shift register, exclusive-OR two bits to get the next bit in the sequence, test for the sync state, and check for a new user input. If you want patterns up to $2^{23} - 1$ bits long, you need to shift three bytes; four bytes allow sequences up to $2^{31} - 1$ bits long.

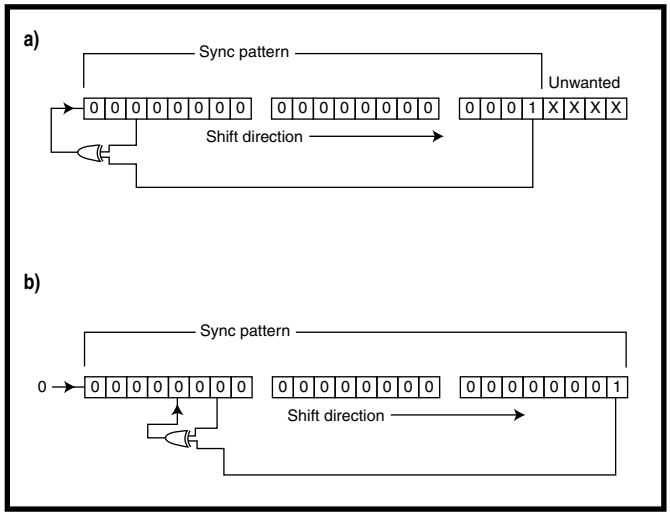



**Figure 2a**—*A conventional PN shift register can be rearranged like* **(b)** *to simplify detecting the synchronization state.*

Not to keep you in suspense, I discovered I can, with some trickery, get down to 23 instructions per loop using fixed parameters. Variable parameters would add a few extra fetch instructions. The jump back to the start of the loop occupies an extra instruction time. Therefore, if you pad the loop to 24 instructions, you get the 100:1 ratio I mentioned between the PIC's clock frequency and output bit rate. (The PIC's instruction rate is 0.25 of the clock frequency.) Numerical convenience thus made a strong case for multiple, fixed-parameter loops.

Some of you may argue that short sequences can be programmed in fewer instructions, which is true, but you don't want the data rate to change when you switch sequence lengths. Hence, all loops have the same length, regardless of the number of shift register bytes they use. Later I traded off sequence length against special functions but kept the loop length the same.

For example, 16 loops that are each 24 instructions long is 384 instructions. This leaves lots of space for the housekeeping routines. Each loop includes a test for any change in the four programming pins. If a change is detected, execution jumps to the housekeeping routine. This reads the user input, resets the shift register to the start condition, and directs execution to a new loop.

Using the PIC16C54's maximum 20-MHz clock, the output bit rate is 200 kbps, a nice round number. Not only can you test data systems running at the popular 64-kbps rate (with a 6.4-MHz crystal), you can also low-pass filter the output to get 10-kHz audio noise. An all-hardware system can easily run a hundred times faster, but if you don't need the speed, this implementation is smaller, cheaper, and more flexible. The '16C54 will run happily with an external hundred-times bit rate clock fed to its OSC1 pin. With a 74HCT4046 VCO/PLL chip, you can lock the output rate to an external bit clock. This can be useful, for example, when PN encoding an existing data source.

## OPTIMIZING THE LOOP

Let's review what the loop has to do. It must exclusive-OR two specified bits, shift a multi-byte register, and then insert the computed bit at one end. It also has to test if the registers contain the frame synchronization state. This occurs once per $2^N - 1$ loops, where $N$ is the number of active shift register bits.

If you want a byte clock, the loop also has to increment a counter. The data bits, frame sync pulse, and byte count must appear at an output port along with a clock that rises and falls once per bit. The last job the loop does is test whether or not you have asked for a new pattern length. If not, the loop repeats.

## SEEKING SYNC

It's the need to detect a unique frame sync pattern in each sequence that drives the firmware design. Suppose you insert new bits into the shift register via the carry bit as you shift from left to right. You have to exclusive-OR a "tap" bit with a "top" bit to create the bit to insert. The tap bit is always in the register's farthest left byte but the top bit can lie in any byte, depending on the sequence length. Messy, but not a major problem.

What makes things cumbersome is that the shift register contains surplus bits downstream from the top bit. These must be masked out when testing for the sync pattern. For example, if you were using 20 shift register bits, the sync pattern could be 19 zeros and one one. Shifting left to right, you would have 00000000 00000000 0001xxxx in the registers. The *xxxx* is whatever bits have been shifted past the end of the 20 active bits. In this case, the bit about to be shifted in at the left is the exclusive-OR of the twentieth and the third bits. The group of unwanted bits to be masked out depends on the sequence length. And, for short sequences, it will extend into several registers.

But, there is a way around this. You can right-justify the active sequence within the multi-byte shift register. Now the lowest bit of the farthest right byte becomes the last active bit. It will be exclusive-ORed with some bit far off to the left and the result ORed into whichever register bit is N bits from the right end of the register. If you shift zeros into the left end of the register, you guarantee that the OR operation will give the correct result and that the unused bits to its left will be zeros.

Now, all sequences will contain the 00000000 00000000 00000001 sync pattern at just one point in their

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**Listing 1**—*This loop, which generates a $2^{23} - 1$ bit sequence, is typical of those using a 3-byte shift register. The 4-byte version omits the byte clock instructions but can modulate an external datastream.*

```
L23:    NOP                         ;Spare instruction
        INCF        COUNT,1         ;Step byte count
        MOVLW       1               ;Identify top bit
        BTFSC       HIGH,3          ;Check tap bit
        XORWF       LOW,1           ;Do ex-OR if it's a one
        BCF         STATUS,0        ;Clear carry
        RRF         HIGH,1          ;Start shifting 24 bits
        RRF         MID,1
        BSF         PORTB,1         ;Raise bit clock
        RRF         LOW,1
        BTFSC       STATUS,0        ;Test carry bit
        BSF         HIGH,6          ;Input to shift register
        DECF        LOW,0           ;Test for 1 state
        IORWF       MID,0           ;Test for 0 state
        IORWF       HIGH,0          ;Test for 0 state
        MOVF        STATUS,0        ;Status word to W
        ANDLW       5               ;Select carry and zero bits
        BTFSC       COUNT,2         ;Test byte clock counter
        IORLW       3               ;Set byte clock output bit
        MOVWF       PORTB           ;Output data, sync and clock
        MOVF        PORTA,0         ;Get user's selection
        XORWF       USER,0          ;Test for change
        BTFSC       STATUS,2        ;Skip if change
        GOTO        L23             ;Repeat loop
        GOTO        NEW             ;Get new user input
```

cycle. The top bit is always the bottom bit of the right-hand register and the tap bit is off to the left somewhere. One bit test instruction can address both the correct byte and bit, so that's not a problem. Figure 2 shows the improved configuration. Note that because you are inserting the new bit after the shift, it goes in one bit farther right than before.

## BUILDING THE LOOP

Because you are going to shift the top bit into oblivion anyway, you can use it as a result bit. The exclusive-OR process then becomes testing the "tap" bit. If it is a one, toggle the "top" bit or do nothing. Now, shift all three registers, remembering to clear the carry to shift in a zero at the farthest left end.

Where did the result bit end up? Not in oblivion, but in the carry bit. There it will remain safely until you need it again. Of course, the first thing you do is insert a one into the proper place in the proper byte to create the correct sequence. That takes two instructions, bit test and bit set.

The sync pattern test comes next. A single instruction fetches the farthest right byte and simultaneously decrements it. If and only if it is 00000001, the result in the W register will be zero. ORing W with the other two bytes leaves a zero result only if they are both zero. Thus, the zero bit in the status register is set only when the sync pattern is present.

The status register now contains two bits that you can use as outputs, the data bit in the bit 0 (carry) position and the sync bit in the bit 2 (zero) position. You can generate both outputs simultaneously by masking the status word and sending it to the output port. Well, it isn't magic, but pretty close.

And there's more. After masking the status byte, test the byte counter's bit 2 and set an output bit accordingly. That gives you a flag that goes high for four bits and low for four bits. It can latch bytes from an external shift register into a DAC. Only one thing is missing, the bit clock. That one's easy. You are already sending four bits to the output port, but one of them is always zero. All you have to do is slip a Set Port Bit instruction into the loop about halfway down. That gives you a bit clock that rises in the middle of an output bit, the perfect place for latch-

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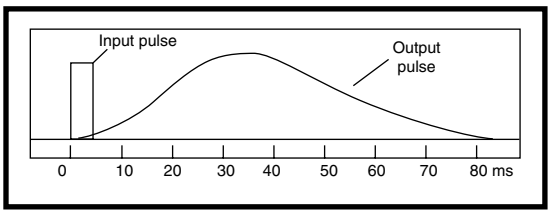



**Figure 3**—*As its response to a 5-µs pulse shows, the low-pass filter stretches each bit over many bit periods. The input pulse is 5-V high and the peak output is 650 mV.*

ing the output. The bit clock falls synchronously with the change in the data bit.

Now, you're one instruction short. Once per loop you must increment the counter register that supplies the byte clock. If you program the chip to select bit 3 of the counter, you will get a word clock and can latch 16-bit random numbers. If you want to be really tricky, you can use the top three bits of the status register as the byte counter and shorten the loop by one instruction!

All that remains is to compare Port A, the current user input, with the register that stores the last user input. If the two are the same, you loop back to the beginning. If they are different, exit to the housekeeping routine. The end result is shown in Listing 1. The frame sync pulse is 1-bit long and occurs once for each repetition of the data pattern. Its main use is to synchronize an oscilloscope to the pattern. Also, the frame sync locks a second generator to the same pattern.

## ADDING MORE GOODIES

At first glance, it looked as if some desirable features would have to be left out unless I accepted a longer loop and lower bit rate. The longer the PN sequence, the better noise spectrum it generates, so an extra shift register byte would be nice. Unfortunately, that takes two extra instructions, one to shift it and another to test it for sync. I also wanted a data input pin to select for a normal or inverted output. This pin also allows binary data to be encoded by the PN sequence, although, because the input data is sampled once per PN bit, its rate has to be the same as or a submultiple of the PN bit clock rate.

In theory, a similarly programmed chip at the receiving end could demodulate the encoded data, but it would need a variable rate clock and what amounts to a phase-locked loop to lock it to the input data. Achieving lock isn't difficult if the frame sync pulse can be transmitted with the data, but is tricky if only the data signal is transmitted. In practice, it may be easier to use the hardware decoder circuit or its firmware equivalent from Figure 2 in my November issue article. [1] Even that requires the clock to be transmitted with the data unless you can lock the receive clock to the incoming data.

In order to add these features, something has to come out. Maybe that byte clock isn't so useful after all (I'll get back to this later). What would you gain if it weren't there? You're using one instruction to increment the counter, one to test it, and one to output it. Plus, you have a spare instruction. You can do a lot with four instructions.

For a start, you can increase the shift register length to 32 bits, which will use two instructions. Then, you can put in that data input I mentioned earlier. One instruction tests the input and one exclusive-ORs the output bit.

My first draft of the firmware used a 4-bit command word to generate one of 16 sequence lengths. I modified this code to give eight lengths having a byte clock and eight lengths having a modulation input. The Byte Clock mode gives cycle lengths of 7, 31, 127, 1023, 32,767, 131,071, 1,048,575, and 8,388,607 bits. The Data Modulation mode drops the 7- and 131,071-bit cycles and adds one of 268,435,455 and another of 2,147,483,647 bits. At full speed, the latter repeats every 3 h.

## PN APPLICATIONS

So, now that you have a pseudo-random serial bitstream, what are you going to do with it? Suppose you take the raw binary data and low-pass filter it. A low-pass filter will take each bit of the output and smear it out over a time roughly the reciprocal of

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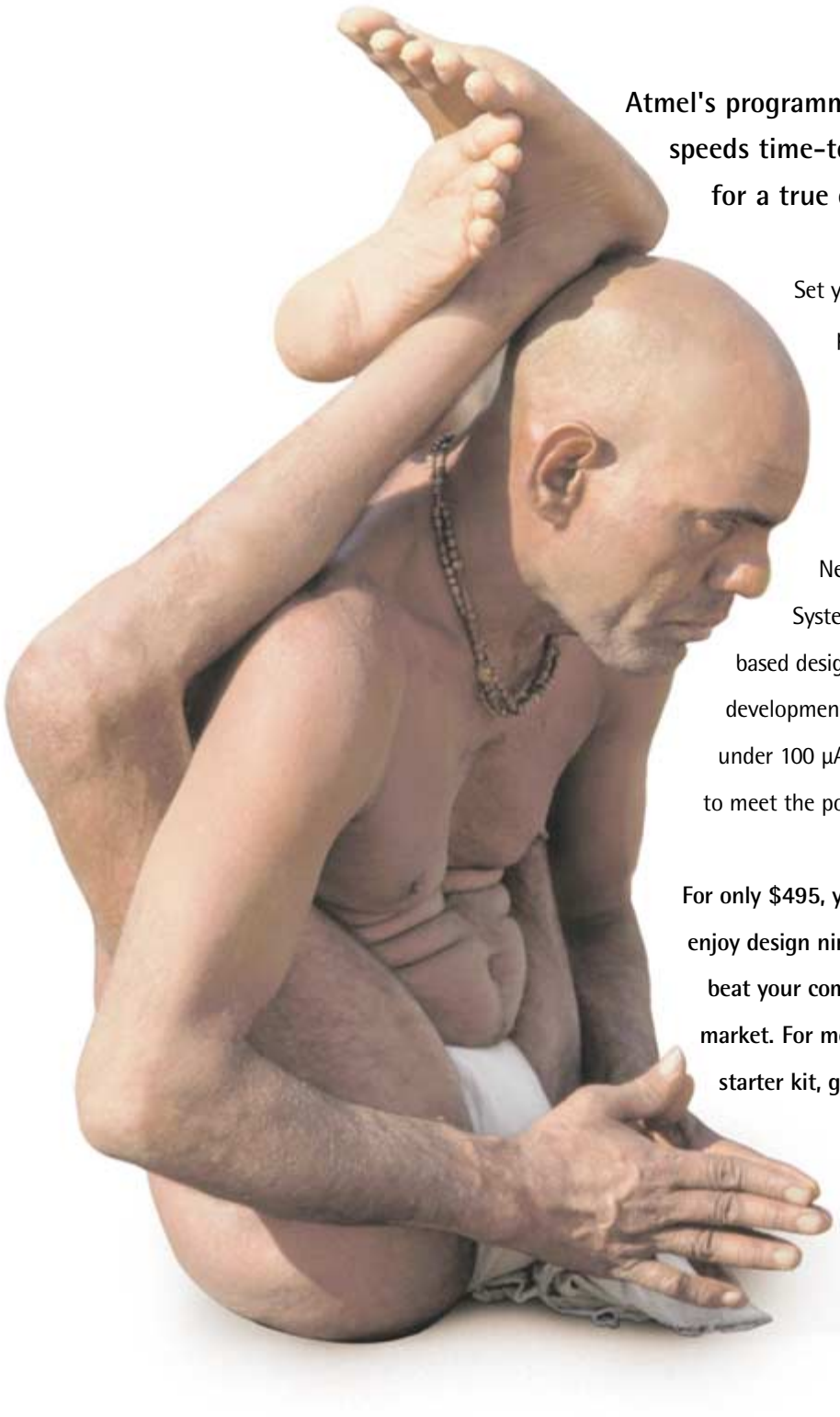
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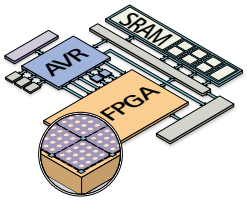
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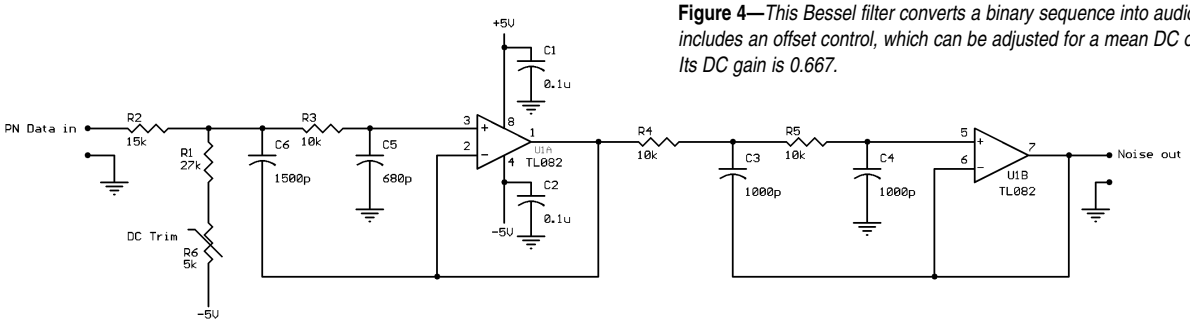



**Figure 4**—*This Bessel filter converts a binary sequence into audio noise. It includes an offset control, which can be adjusted for a mean DC output of zero. Its DC gain is 0.667.*

the filter bandwidth. Figure 3 shows the result, a single 5-µs bit ends up about 80-µs long. Because no energy is lost, the amplitude falls to about 650-mV in this case. The same thing happens to each bit, so the actual voltage at any point will have contributions from about 16 successive bits.

If you sum many random bits (i.e., use a low enough filter bandwidth), the net voltage will have good approximation to a Gaussian distribution. In other words, you will have generated band-limited analog noise from a digital input.

In practice, the filter bandwidth needs to be about 0.05 of the bit rate, so you can't achieve a noise bandwidth above 10 kHz. Ten kilohertz is enough for experimenting with audio signals such as seeing how much noise a voice signal will tolerate before it becomes incomprehensible.

The lower cut-off frequency of the noise is set by the cycle repetition rate. You get a strong beat at this rate so you don't want to use too short a PN sequence for audio testing. A $2^{20} - 1$ sequence is adequate, it repeats about every 5 s. The $2^{31} - 1$ sequence should be random enough for any job. More or less complex ways of creating a higher noise bandwidth from a PN sequence have been determined. [2, 3] The low-pass filter has its limits but is far easier to implement.

## USING THE BYTE CLOCK

There's another way of achieving a similar end. That's why the device has a byte clock output. I thought of providing a byte-wide output from the generator, but that would have required a three-port chip and two or three more instructions in each loop. Instead, you need an external shift register chip to convert the serial bits back to parallel form.

Another possibility is to modify the byte clock timing to drive a serial input DAC. The DAC latch is clocked every eight bits to store the shift register output. Provided the generating shift register is longer than 1 byte, you get a series of 8-bit uncorrelated analog voltage samples at 0.13 of the bit clock rate. If you filter them with a bandwidth equal to half of the byte clock rate, you will get analog noise. There's just one snag, the DAC output takes every possible output equally often, thus, its amplitude distribution is rectangular, not Gaussian.

## THE FILTER

The low-pass filter in Figure 4 is a four-pole, Bessel filter implemented as two Sallen-Key stages. A fast op-amp is needed even though the output is less than 10 kHz. Don't be tempted to use, for example, an LM386 in place of the TL082 or a similar amplifier. A Bessel filter doesn't cut off sharply but it minimizes distortion of the waveform. It's also less fussy about component values than most filters, so readily available parts can be used. A trimmer is included to set the mean output level to zero.

## UNCHANGING NOISE?

The great advantage of this noise generator is that, unlike diode- and amplifier-based noise sources, it always has the same output. The filter input is digital and the amplifiers are simple unity-gain buffers, so the output amplitude doesn't vary with time or temperature (its rms value is about 550 mV). The frequency spectrum is as flat as the filter can make it. And, if the amplitude distribution is not exactly Gaussian, it won't matter for a lot of jobs. (If you want to read more about when it does matter, check out another article I wrote a few years ago. [3]) Besides, every time you reset the PIC, it generates exactly the same random noise. Now there's a paradoxical notion.

*Tom Napier was a principal engineer in the Signal Recovery Group of the Aydin Corporation for eight years. He is now an electronics design consultant and a writer.*

## SOFTWARE

The code is available on the *Circuit Cellar* web site.

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# Flash Gang Programmer for Microcontrollers

With the popularity, and not to mention the practicality, of designing flash memory into projects or using flash memory micros, Noel found a way to program multiple flash memory components at the same time and made using flash memory even easier.

Flash memory microcontrollers and flash memory are popular these days. These devices can be programmed and erased in system and can be erased without the usual UV EPROM eraser. Flash memory devices can be programmed ordinarily like their EPROM counterparts, but there is no need to erase the device using a UV eraser. Erasure is done electrically. Using flash technology eliminates the need for an expensive ceramic package and quartz window. These devices are called flash because part or all of these devices can be erased in a flash.

Second generation flash memory devices do not use an external voltage higher than 5 V for programming and erasing. Programming microcontrollers can be done using a universal device programmer or dedicated programmer. But, to program many devices at once, you need a gang programmer. With this flash memory microcontroller gang programmer you only need to press a switch to program seven microcontrollers at once. Simply insert the master copy and targets. No microcomputer is needed. The circuit is also easy to construct.

## TECHNOLOGY OVERVIEW

Flash memory works by using the principles of Fowler-Nordheim tunneling and hot electron injection. The former is a low-current physical mechanism for erasing, and in some cases, programming a flash memory device. In this mechanism, charge is removed from the floating gate of a memory cell through a thin layer of tunnel oxide. Hot electron injection is a high-current physical mechanism for programming a flash memory or EPROM. In this mechanism, charge is injected from the floating gate of a memory cell through a thin layer of tunnel oxide.

The memory cell of the industry-standard, single-transistor, NOR-type flash memory device is nearly identical in design and processing to the cell on mature UV EPROM products (see Figure 1). There are only two differences. The flash cell uses a graded double diffused on the source and has a thinner tunnel oxide—about 100 angstroms versus 150 angstroms for the EPROM cell. Double diffusion on the source and thinner tunnel oxide help Fowler-Nordheim tunneling during erase.

The first generations of flash memory devices use bulk erase where the entire flash memory array is erased at once. Later generations of flash memory devices have a sector erase archi-

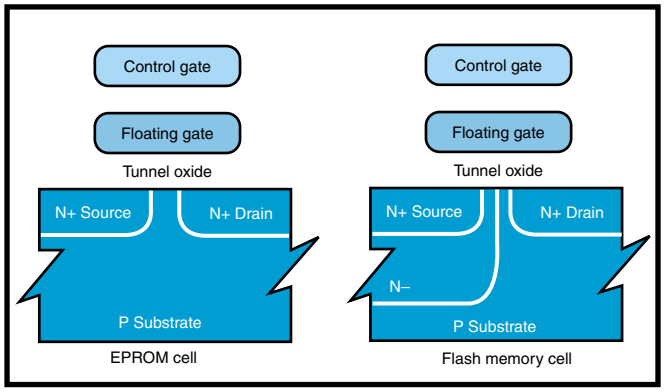



**Figure 1**—*Check out EPROM cell and flash memory cell differences.*

tecture. Sector architecture is the segmenting of a flash memory array into smaller sections for erase operation. Changing logical 1 to logical 0 in the flash memory array is what happens in programming. Programming is accomplished in a flash memory device one byte or word at a time. Erasing is done by changing logical 0 to logical 1 in the flash memory array. Unlike programming, flash devices cannot be erased one byte at a time.

In a single transistor, stacked-gate NOR flash, all bytes must be pre-programmed and erased prior to programming. For flash memory devices that have internal algorithms for programming, the state machine on the flash device will automatically program the byte of data appearing on the data bus. In addition, for flash devices that have an internal erase algorithm, the state machine on the flash memory devices will automatically program the flash array prior to erasure. Internal algorithms automatically time out the programming and erase pulses and ensure the proper cell margin. The system only writes the proper setup command; the device's internal state machine does the rest.

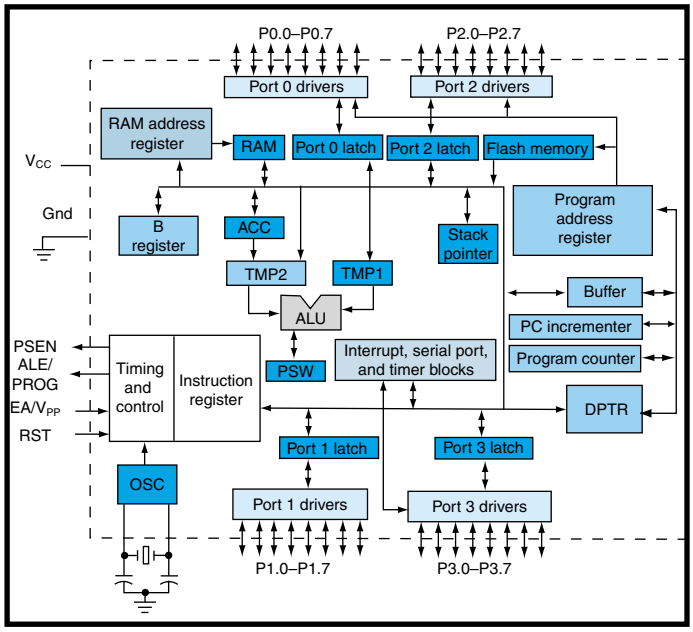



**Figure 2**—*The '89C51 microcontroller contains 4 KB of flash memory, which can be programmed using the gadget featured.*

For single-power supply devices, the programming and setup commands are a JEDEC standard. Flash memory devices also provide hardware methods to indicate the completion of programming or erasure of the flash memory device. These are the busy status pin, data polling on DQ7, and toggle bit on DQ6. If the output status of the busy status pin is high, then the device is ready. If the output status is low, the device is busy.

**Figure 3**—*The seven duplicate microcontrollers are wired in parallel except for their ENABLE signals some signals (pin 28) and $V_{CC}$ pins (pin 40).*

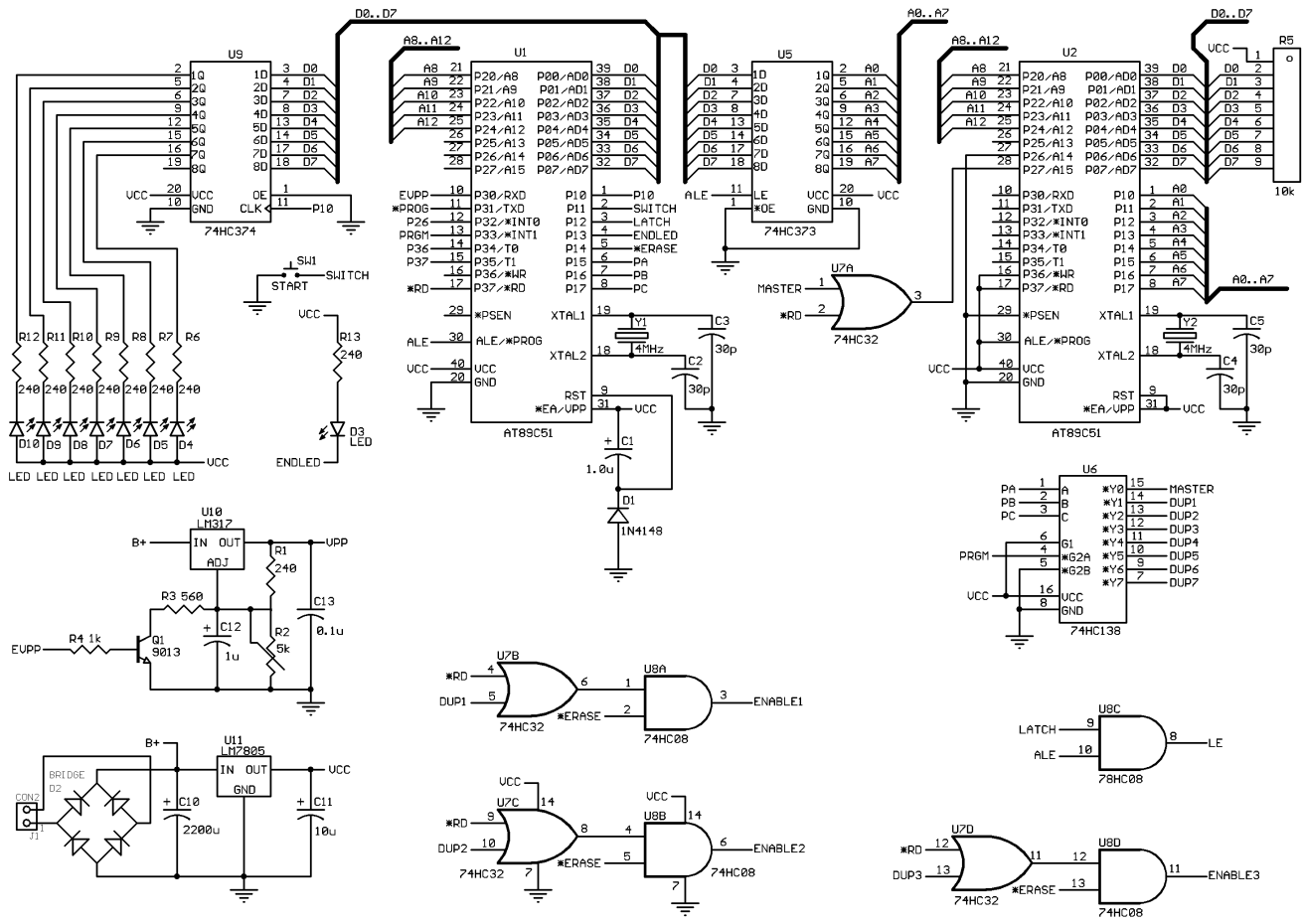
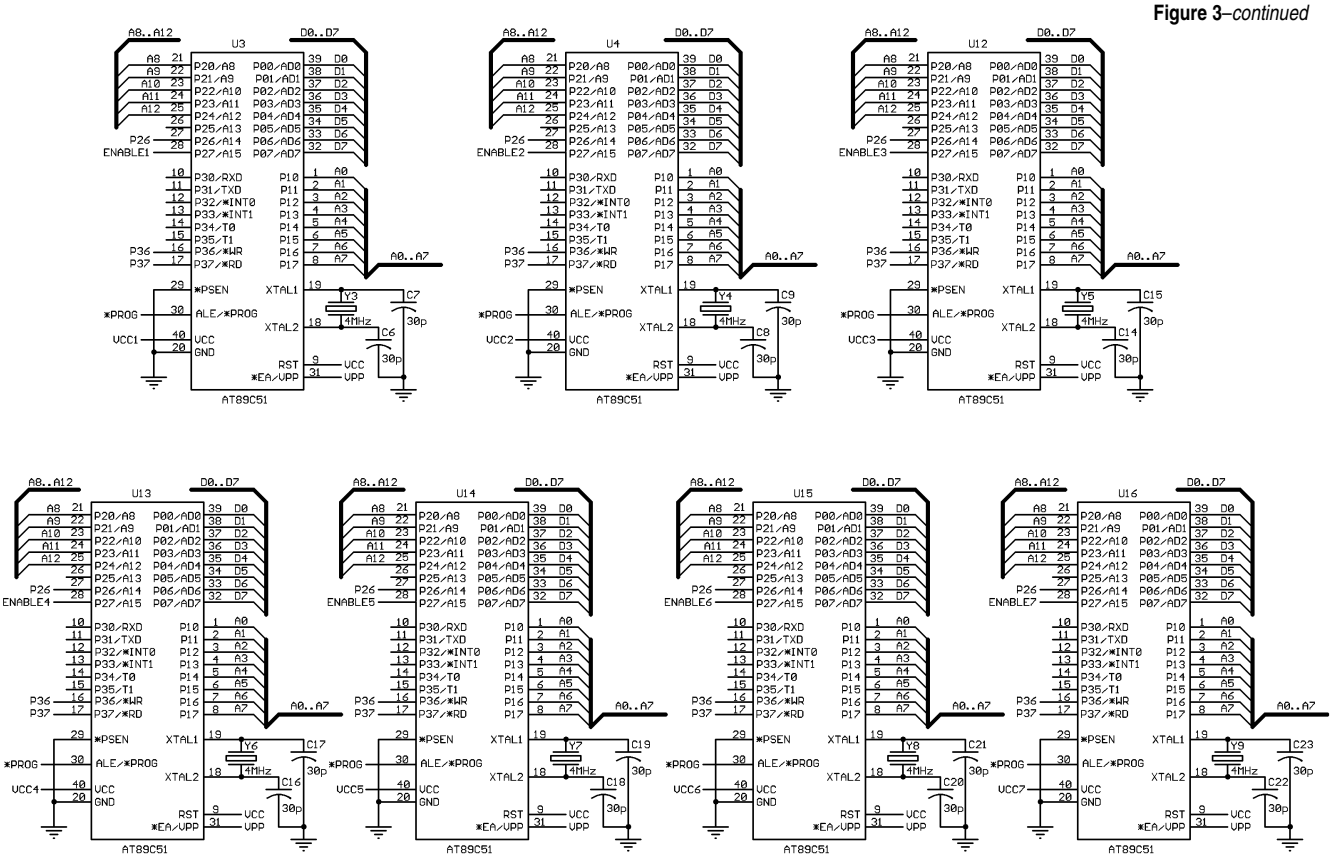


**Figure 3**–*continued*





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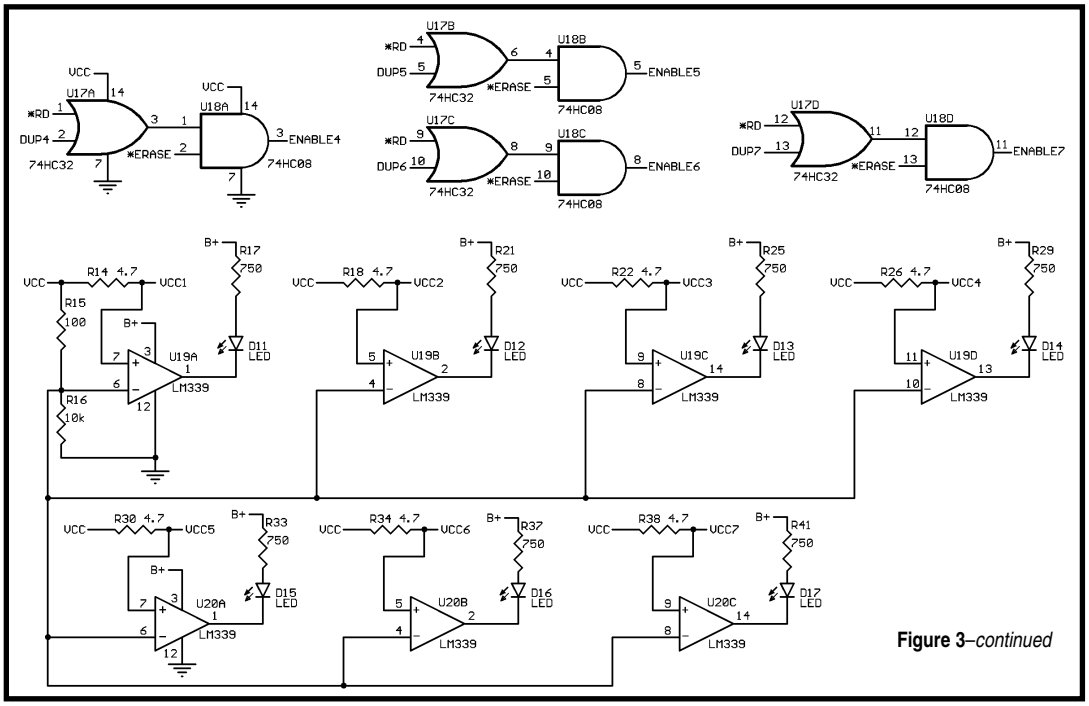



**Figure 3**–*continued*

While a programming operation is in progress, the device outputs the complement of the value programmed to DQ7 for data polling. During an erase operation, data polling produces a 0 on DQ7. When the erase operation is complete, data polling produces a 1 on DQ7. For the toggle bit on DQ6, successive read cycles at any address cause it to toggle. DQ6 stops toggling when the operation is complete. While erasing, successive read cycles at any address cause DQ6 to toggle. DQ6 stops toggling when the erase operation is complete.

Like their EEPROM counterparts, flash memory devices have a limited number of write/erase cycles they can withstand without failure. The reason for this is charge trapping in the tunnel oxide. This introduces a term called endurance. Endurance is a measure of the number of programming/erase cycles that a flash memory array can achieve while retaining data integrity.

Today, the industry standard is a minimum guaranteed of 100,000 endurance cycles. In many cases, you


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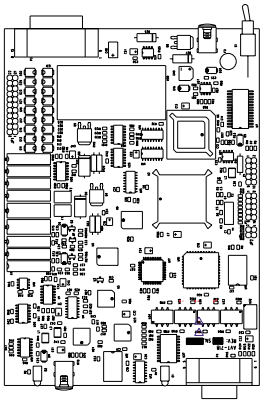
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will not need high endurance for applications such as PC BIOS and other designs that require infrequent code changes. However, it can be used as a measure for device reliability. Two failure modes are typically associated with flash memories, hard failures and soft failures. Hard failures are complete and unrecoverable, and their root cause lies in the manufacturing process. Flash memory endurance is typically limited by soft failures. Soft failures occur when random bits erase too quickly.



**Photo 1—***Zero insertion force sockets (ZIF) are highly recommended for the master copy and duplicate flash memory microcontrollers for ease of inserting and removing ICs.*

Flash memories are erased in blocks, and because not all bits exhibit identical erase characteristics, a fast erasing bit must be exposed to the erase voltage until the slowest bit is erased. As a result, the fast bits can be erased too much, forcing the transistor cells into Depletion mode. This condition is called over-erase.

An over-erased bit produces leakage current that causes an entire column to malfunction. The result is a system failure. Soft failures occur as a result of incorrect implementation of manual program and erase algorithms. These incorrect implementations occur in flash memory devices that do not have embedded algorithms on chip. Embedded algorithms monitor internally the successful erasure and programming of all bytes. Equally important with embedded algorithms is the fact that device level code generation is minimized, reducing overall system-level code development and debug time.

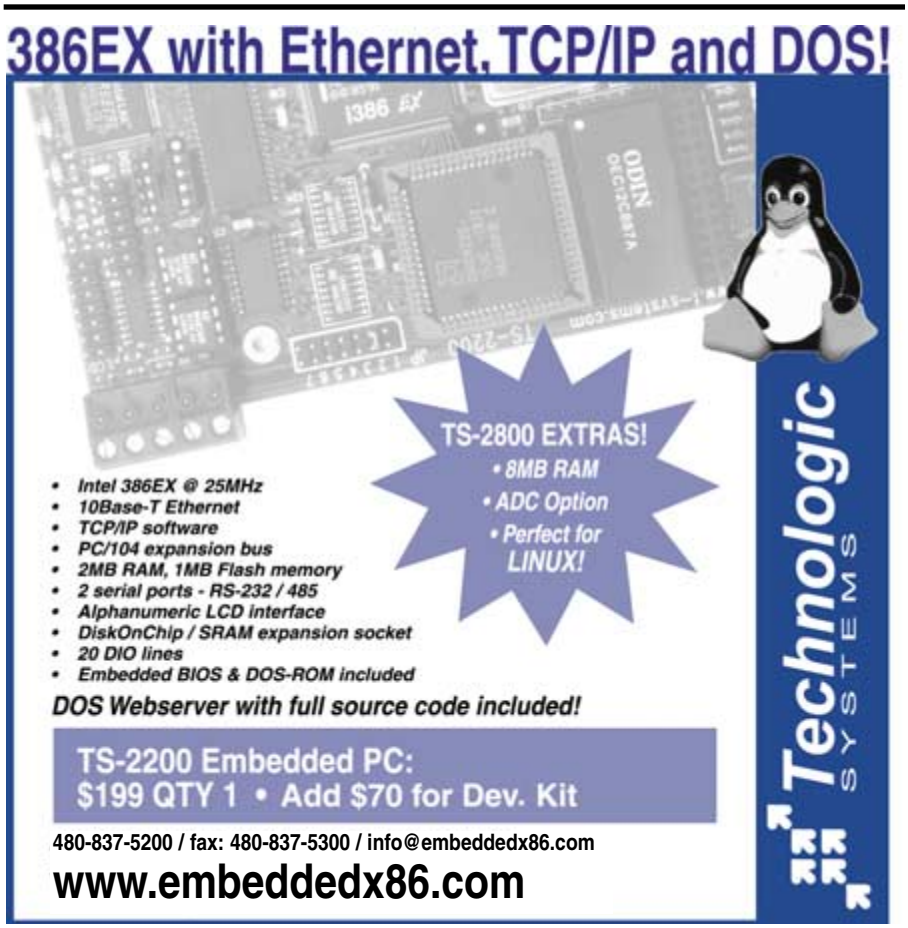
## CIRCUIT DESCRIPTION

The circuit relies on the power of the AT89C51 to act as a microprocessor when accessing external memory and as a microcontroller when memory expansion lines become I/O ports. The heart of the circuit is an '89C51 4-KB flash memory microcontroller (see Figure 2). It is in charge of erasing, programming, verifying, and lighting the corresponding LEDs if the whole process is successful. The '89C51 generates the proper timing and sets the correct flash programming modes using its I/O ports. It also controls the super voltage or programming voltage and the address decoder to read the eight microcontrollers. Table 1 describes the flash memory programming modes used to program the duplicate microcontrollers.

The table describes how the master pins and the duplicates are wired and port lines control other pins of the duplicates. Looking at RESET and /PSEN, these two are hardwired to $V_{CC}$ and ground, respectively, because these pins do not change state for all the programming modes.

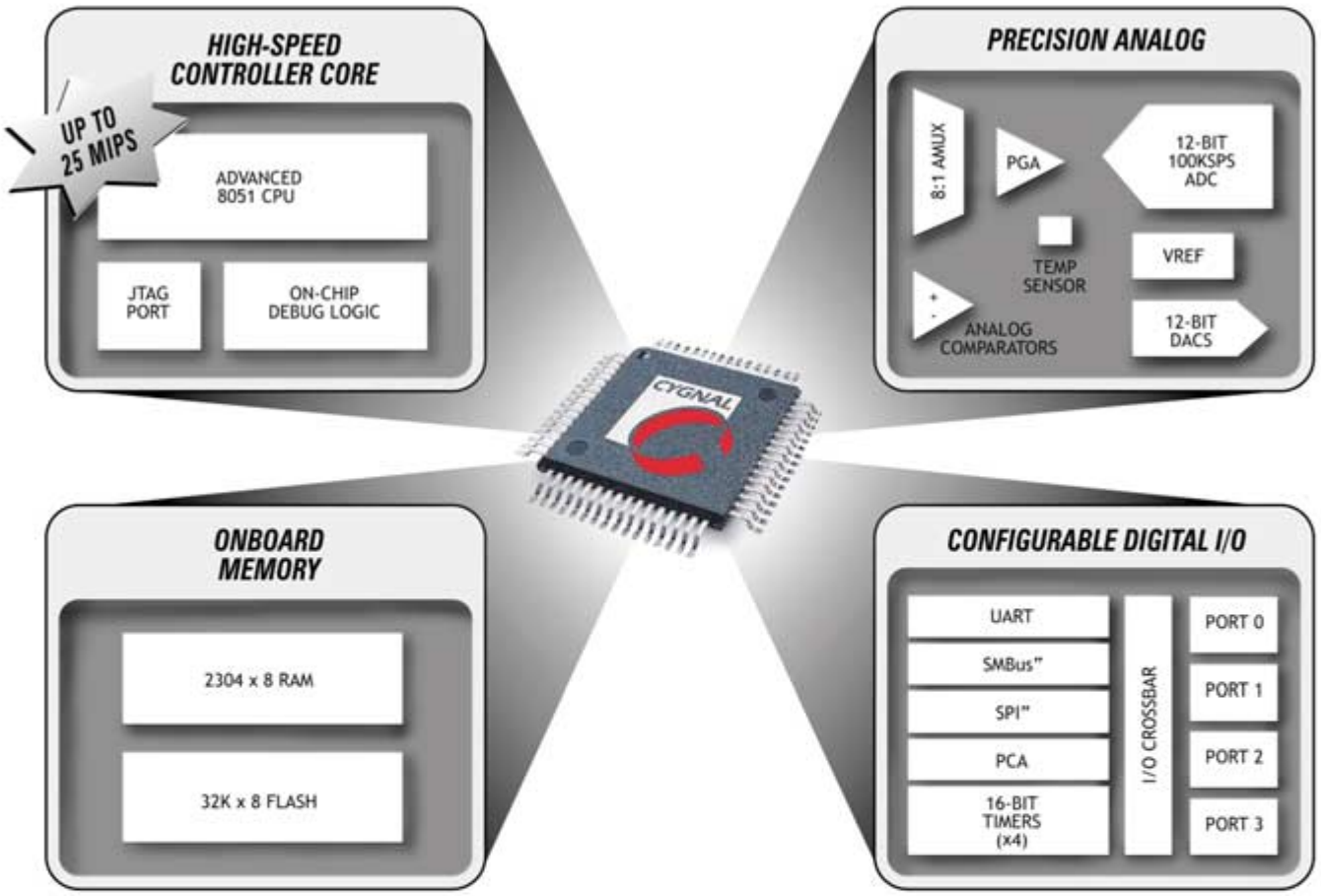
Other lines vary so they are connected to the I/O pins of the main controller U1. One I/O line controls the $V_{PP}$ circuitry composed of U1, Q1, R1, R2, R3, R4, C12, and C13. U10 is an adjustable linear regulator whose voltage is dictated by two resistors. In this case, it is R1 and R3 or R2. During Read mode, 5 V is needed at the $V_{PP}$ pin. So, controller U1 turns on transistor Q1, and R3 is in parallel with R2.

The combination produces a lower resistance, so 5 V is the result of the resistor combination. During Write mode, 12 V is needed to program the chip so that controller U1 turns off Q1. In effect, R1 and R2 are a two-resistor combination, so the result is 12 V. R2 is a resistor trimmer that lets you adjust the voltage to 12 V. C12 filters the voltage appearing across R2 to minimize ripple.

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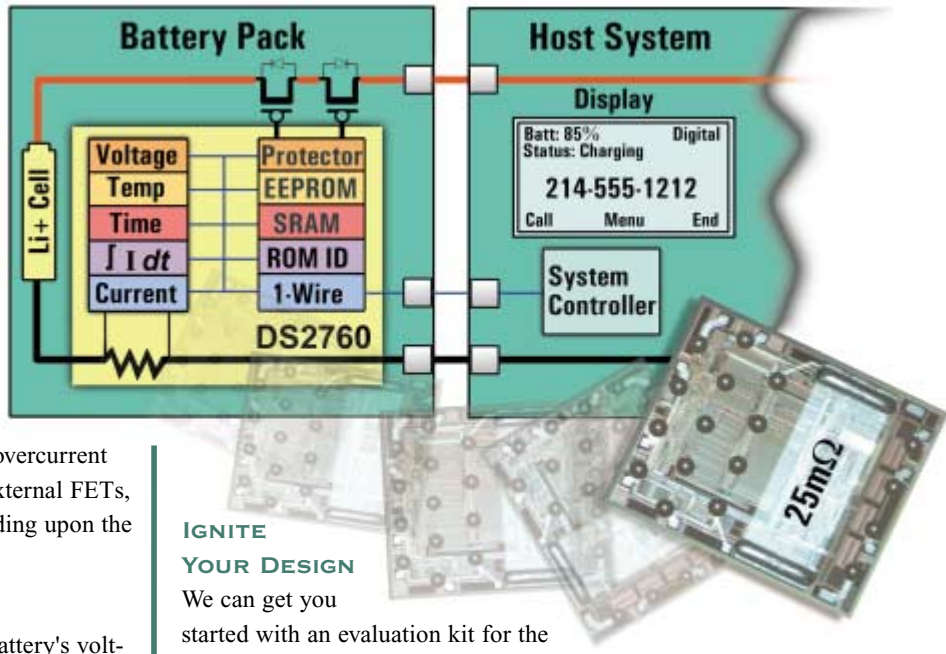
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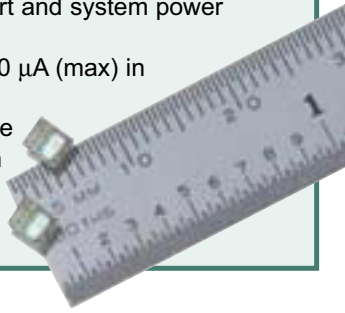
All DS2760 data is transferred between the battery pack and host via a single wire, multi-node, digital communication interface. The 1-Wire interface minimizes battery contacts, reducing overall pack cost. The DS2760 is also the first Li-Ion protector that allows the host processor to electronically monitor/override the on-state of the safety FETs. You can even use this feature to cycle power of the portable product or to swap between packs in multi-pack applications.

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C13 also acts as a filter and absorbs some transient that may appear at the output of the regulator. U11 is a voltage regulator that gives a 5-V output. D2 is a bridge rectifier that converts AC to DC. With a bridge rectifier, you can use an AC or DC adapter and not be concerned with the polarity of the input (with a DC adapter).

C10 is a filter capacitor that smoothes the ripple of the voltage. C11 is also a filter needed by the 5-V regulator as indicated in the datasheets. U9 is an octal D flip-flop, which is used to latch the outputs of P0. The IC has enough output current on each pin to drive the LEDs to an acceptable level. Resistors R6 to R12 limit the current so that U9 will not be damaged. And, U5 is an octal transparent latch, 74HC373, which captures the lower address A0 to A7 when the signal ALE (address latch enable) is present.

From this moment, I will refer to the microcontrollers to be written to as duplicate microcontrollers. This is used to access the duplicate flash memory microcontrollers as external memory to the main controller U1. Memory read access is done using the MOVX instruction.

With this method, the read access is automatic, and there's no need to set up ports for the address. Because the write memory cycle cannot be used to write to the duplicate microcontrollers, an AND gate, 74HC08 (U8C), is used to latch the address to U5 without using the MOVX instruction. A simple write to Port P0 is used, and then Port P1.2 (labeled "latch") applies a signal to latch the address appearing at Port P0.

U7 and U17, 74HC32 are an OR gate that is used to enable the duplicate microcontroller at the proper time when it's accessed via the MOVX instruction. To access a certain microcontroller as a memory element two things are needed. One is a signal from the address decoder, another is the *RD signal generated by the MOVX signal. U6, 74HC138, is a decoder used to enable the duplicate microcontrollers one at a time. Take note that the address lines are not decoded to enable the duplicate microcontrollers, because a write memory cycle cannot be used to program the microcontroller.

Ports are used to access the microcontrollers one at a time for reading and writing the data to the microcontrollers. The reason for this is that the signals at the ports do not change for the duration of a write cycle. In addition, writing one byte to one microcontroller takes as much as 2 ms. Also take note that a MOVX is not used for writing to the microcontroller. The address is manually latched and data is written to port P0. A SIP resistor connected to the data bus as indicated in the datasheet for programming the flash memory microcontrollers.

A 4-MHz crystal is used for the clock oscillator. The clock must be running because the device is executing internal address and program data transfers while programming. Quad comparators U19 and U20 detect the current for each microcontroller. R15 and R16 set the reference voltage for the threshold of the current detector. A voltage drop is produced when current passes through R14 (the same for other current detectors) and when the voltage drop is lower than the threshold. This causes the LED to light, indicating misinsertion.

## CONSTRUCTION AND ASSEMBLY

The prototype was constructed using point-to-point wiring. Use different colors of wrapping wire so that you can trace the connections. Ordinary IC sockets were used, but if you desire, you can use wire-wrapping sockets. Lay out the ICs such that ICs connected together are near each other. For example, place U5, 74HC373, close to U1, AT89C51.

After wiring the circuit, check the connections among the ICs according to Figure 3 using a multimeter. Notice that the duplicate microcontrollers are wired in parallel except from some signals. Check that their connections are parallel. Place the crystals and load capacitors (e.g., C2 and C3) close to the microcontrollers. It is recommended to use ZIF sockets for the master copy and duplicates if










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| Mode | RST | /PSEN | ALE/PROG | EA/$V_{PP}$ | P2.6 | P2.7 | P3.6 | P3.7 |
|---|---|---|---|---|---|---|---|---|
| Write code data | H | L | Pulse | 12 V | L | H | H | H |
| Read code data | H | L | H | H | L | L | H | H |
| Chip erase | H | L | Pulse | 12 V | H | L | L | L |

**Table 1—***These are the flash programming modes and required pin statuses for proper erase, read, and write to the flash memory.*

you have them (see Photo 1). Before inserting the ICs, check for the presence of 5 V on the $V_{CC}$ pin of each IC. Also check that the ground pin of each IC is connected to the ground of the power supply.

## CHECKOUT AND USE

The first thing that you must do is calibrate the programming voltage appearing on pin 31 (*EA $V_{PP}$) on the duplicate microcontrollers. Pull controller U1 from its socket so that the programming voltage appears on the $V_{PP}$ pin. Then, slowly adjust the voltage to 12 V. Note that failure to adjust the programming voltage may result in electrical overstress on the $V_{PP}$ pin of the microcontrollers. This will result in defective microcontrollers. The duplicate microcontrollers may also fail to program in cases of under voltage. Equally important, check if 5 V is present on $V_{CC}$ pin 40 of all microcontrollers.

To use the programmer, insert the master copy and the duplicate microcontrollers to the corresponding sockets. Then, turn on the device. Make sure to press the Start button at powerup to indicate if you're going to program an '89C51 (4-KB flash memory). Otherwise, it defaults to programming an '89C52. The green LEDs will blink once if it is set to program an '89C51 and twice if it will program an '89C52. After that the LED will blink to indicate the start of the programming process.

Wait for the "program end" LED to light up and indicate it is finished. The datasheet states that the timed write for one byte takes no more than 2 ms. However, the write timing for one byte is adjusted in the firmware to 2.5 ms for allowance. The green LED will light up for each corresponding microcontroller to show if the programming process was successful. If it does not light, you must check the microcontroller to see if it is correctly seated in the socket. The DC adapter used must have a potential of 14 V or greater to overcome the drop-out voltage of the LM317 U10.

## TROUBLESHOOTING GUIDE

There are several possibilities if the device does not work. For example, there may not be power on some ICs. Or, there may be a wrong or poor connection of the control signals (P2.6, P2.7, P3.6, and P3.7) among the duplicates and controller U1.

If $V_{PP}$ (pin 31) is missing or at a high potential all the time, check the wiring of LM317 U10's pins. Also, check Q1 for proper operation. Another possible problem is a missing enable pulse on the master copy that contains code. This would cause all of the duplicate microcontrollers to verify correctly even if they are in an erased state.

Incorrect wiring of the data and address buses can be a problem, too. Using a logic probe, check if the controller U1 is active by monitoring its pins. If it isn't functioning, check the reset circuit C1 and D1 and the connection of the crystal. Also check pin 31 (*EA) of U1 to see if it's wired to $V_{CC}$ (5 V).

## LIMITATION

The device essentially performs replication, so it can't check if the duplicate microcontroller is defective or not. However, there is an indicator you can see. If one of the duplicate microcontrollers is defective, the LED will not blink at powerup.

To determine the defective IC, remove the duplicate microcontrollers one by one until the LED blinks at powerup. Because it does not connect to a PC, you can't load code from a file and burn it to the duplicate microcontrollers. You need a device programmer for this. The main use of

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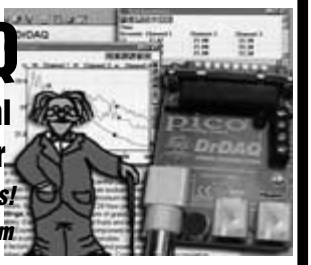
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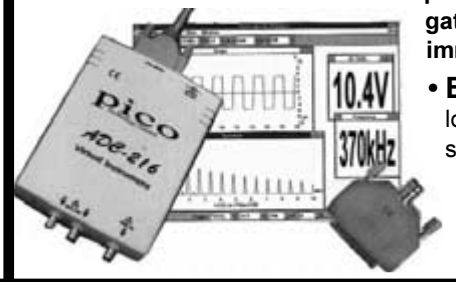
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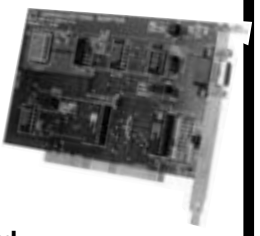
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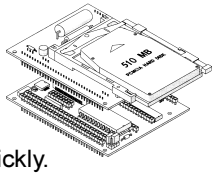
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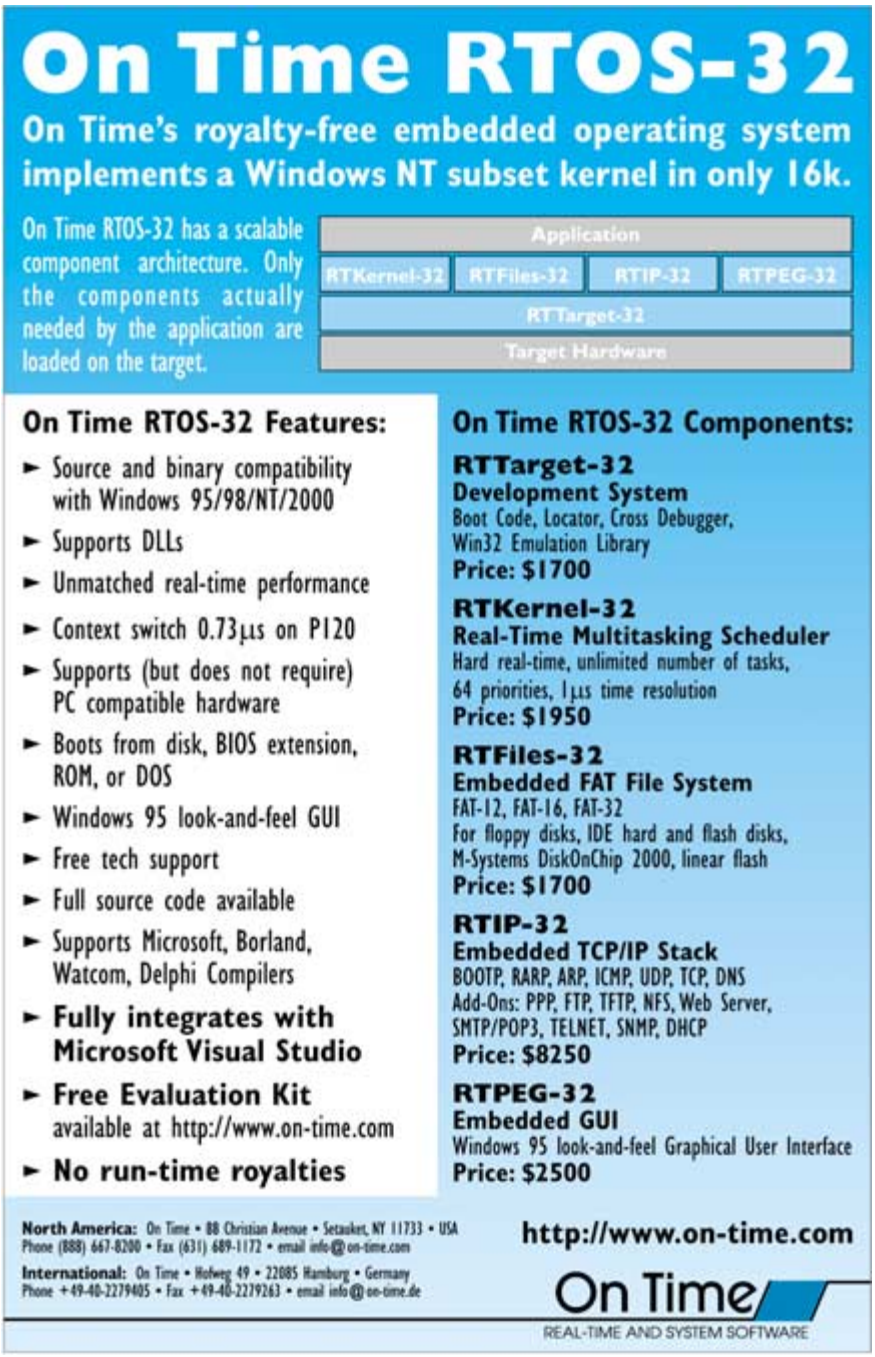
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the device is to replicate up to seven microcontrollers simultaneously from a master device.

## CONCLUSION

The flash memory microcontroller gang programmer can program up to seven flash microcontrollers at once. It has been tested with Atmel's AT89C51 and AT89C52s with good results. And, the circuit can be modified to accommodate microcontrollers from different manufacturers. But, it is important to note that AT89C51 and AT89C52 contain embedded algorithms, which simplified the programmer's firmware. So, if you're going to modify the circuit, you may need to modify the firmware.

*Noel Rios is an electronics and communications engineer. He has worked with semiconductor and electronics companies like Microcircuits, IMI, Allegro, and ASTEC. His interests include computers, embedded control, power conversion, test & measurement, and GPIB control. He can be reached at narios@philonline.com or nar@edsamail.com.ph.*




## SOFTWARE

The code and a parts list are available on the *Circuit Cellar* web site.

## SOURCES

**AT89C51, AT89C52 flash microcontrollers**
Atmel Corp.
(408) 436-4270
Fax: (408) 436-4314
www.atmel.com

**Command standards**
JEDEC Solid State Technology Association
(703) 907-7534
Fax: (703) 907-7583
www.jedec.org

**LM317**
National Semiconductor Corp.
(408) 721-5000
www.national.com/pf/LM/LM317.html

**74HC373, 74HC08, 74HC32, 74HC138**
Philips Semiconductor
(212) 536-0500
Fax: (212) 536-0559
www.philipslogic.com/products/hc

## RESOURCES

Atmel Corp., "8-bit Microcontroller with 4K bytes Flash," rev., 80C31, February 2000.

———, "8-bit Microcontroller with 4K bytes Flash," rev., 80C32, February 2000.

———, "Microcontroller Databook," Atmel Corp., October 1995, CD-ROM.

Advance Micro Devices, Inc., "AMD Flash Memory Quick Reference Guide—Succeed with Flash Technology Leadership from AMD," rev. 2000.

———, "Flash Memory Products Databook/Handbook," Advance Micro Devices, Inc., 1996.

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# NOUVEAU PC

Edited by Rick Prescott

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The carbon monoxide logger is suitable for monitoring CO levels in areas such as garages, loading docks, terminals, furnace rooms, basements, and office buildings. The resulting data can be used to identify problems with furnaces, vehicles, gas appliances, ventilation, air supplies, and flues.

The logger's sampling rate is user-selectable from 0.5 s to 9 h. The logger measures 5.7″ × 2.6″ × 1.6″. The optional pocket-sized HOBO shuttle uses a single button to off-load, test, and restart the loggers where they are deployed. The reusable shuttle is then brought back to a PC where the data is off-loaded, analyzed, and stored. Capacity is 468K measurements, which is enough for 13 full carbon monoxide loggers.

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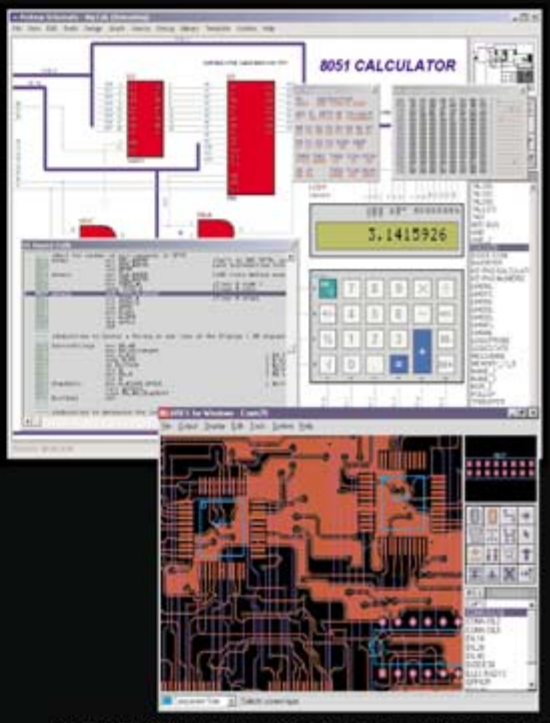
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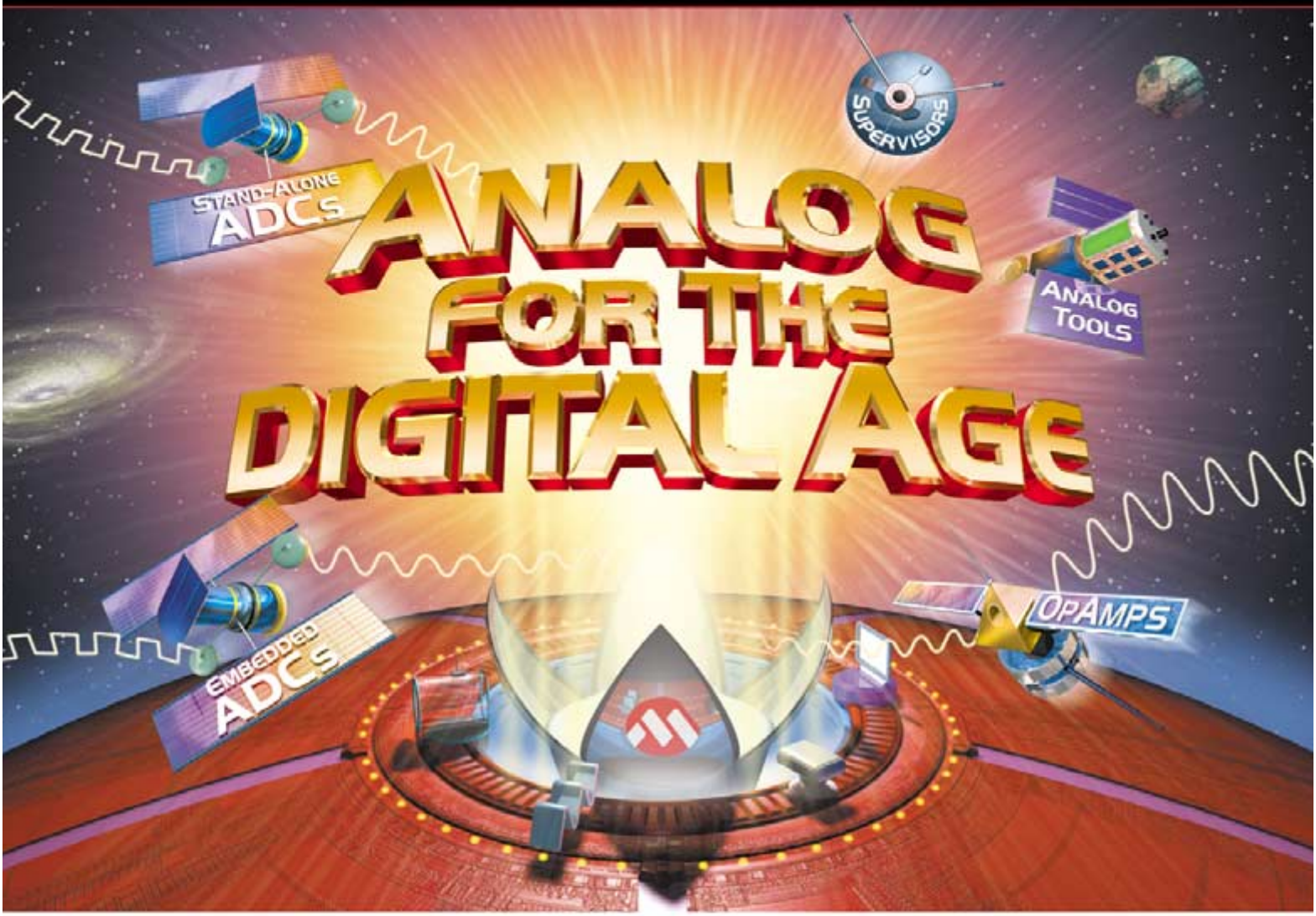

*E.g. PROTEUS VSM can simulate an 8051 clocked at 12MHz on a 300MHz Pentium II.

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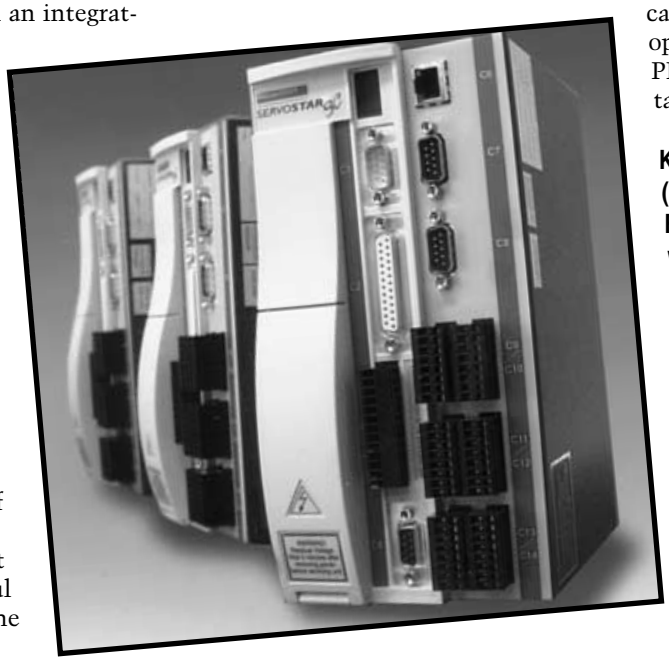
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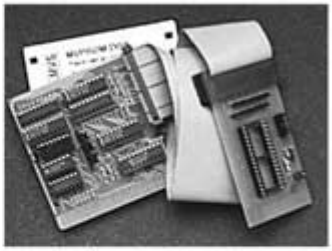
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Fred Eady

# Just Like in the Movies

## Working with SBC-386EX-S

Taking a tip from a reputable source, Fred decided to go behind the scenes to find out if Arcom's SBC-386EX-S was going to be the box-office blockbuster that it looked like. With a great supporting cast of features and documentation, there's serious star potential here.

You saw it in *Circuit Cellar*'s Nouveau PC section. It was touted as the most direct way to get an embedded product to market with minimum cost and effort. Everything an embedded PC could offer in a single, inexpensive, highly integrated package was there, and then some. In effect, this was the working embedded engineer's single-board computer. At the time, it seemed so simple and yet so powerful, and it was cheap. I wanted to know more about it and I figured you would, too. So, here's the skinny on that unassuming workingman's board you see in Photo 1, the Arcom SBC-386EX-S.

### HIGH EXPLOSIVE SBC

Ever see the war stories in movies where the underground agent puts what seems to be just a little bit of plastic explosive on a bridge support? Did you ever question why the whole bridge goes up in splinters when he or she triggers the explosive play dough? Well, if you discount the fact that it was done in Hollywood, that little bit of C4 on the bridge support is powerful stuff! A little goes a long way, just as it does with Arcom's new SBC-386EX-S.

I really didn't know how much built-in compute and network power I had here until I started reading about the SBC-386EX-S SDK that arrived at the Florida-room stoop. In addition to the standard cadre of embedded PC peripherals, the SBC-386EX-S comes out of the box loaded with a custom-fit RTOS and a sidekick TCP/IP stack. And, it costs less than $200 in OEM quantities.

Here's how the SBC-386EX-S that comes with the SDK is configured. The processor is an Intel '386EX running at 25 MHz. Supporting the '386EX is 2 MB of DRAM, 1 MB of flash memory, and 512 KB of battery-backed SRAM. The "S" denotes the battery-backed SRAM variant of the SBC-386EX that comes with the SDK.

Everyone knows that, to me, Ethernet is the heavyweight of networking, and I'm sure the designers of the SBC-386EX-S have been tuned into my embedded articles, because the SBC-386EX-S includes onboard Ethernet in the form of Realtek's RTL8019AS Ethernet engine. If the '8019 is not immediately familiar to you, check out an earlier article I wrote as part of my Rabbit series, "The Wonderful World of TCP/IP" (*Circuit Cellar* 125). The presence of the RTL8019 makes the SBC-386EX-S NE2000-compatible. The SBC-386EX-S's Ethernet support is configured for

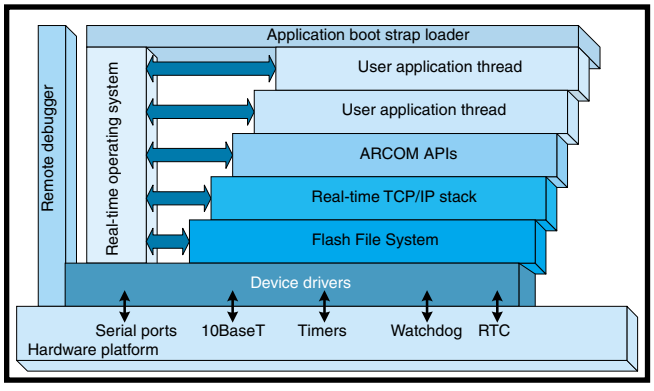



**Figure 1**—*This "stack" comes pre-loaded on the SBC-386EX-S.*

10BaseT operation, as the RJ-45 female jack implies. Three serial ports, two implemented as integrated 16C450 UARTS and one with a 16C550 UART, are standard equipment on the SBC-386EX-S. Of course, the serial ports support RS-232/422/485.

To round out the system, Dallas Semiconductor was kind enough to provide an RTC in its onboard DS1302 RTC IC. And to keep the SBC-386EX-S personal, a Dallas Semiconductor unique ID tag is also riding on the SBC-386EX-S fiberglass. There are plenty of other toys on the SBC-386EX-S, including Arcom's SVIF source view interface software debugging port, a user-controlled LED, and three integrated timers. If animals are your thing, there's a (watch) dog in the yard too, and he can bite you at –20°C.

That's a quick rundown of what the SBC-386EX-S is made of. The explosive materials that make up the SBC-386EX-S are shown in Photo 1. The hardware collection is impressive, but the real power of the SBC-386EX-S lies in its software and firmware support package.

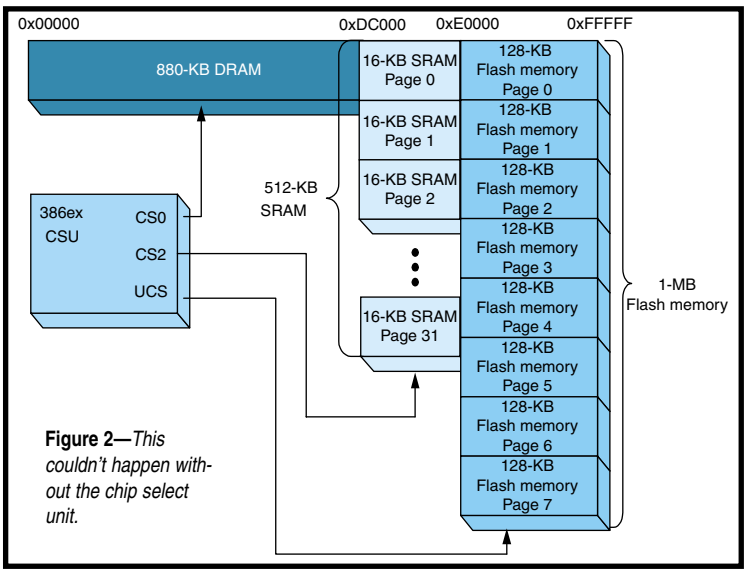



**Figure 2**—*This couldn't happen without the chip select unit.*

## C4 ON CD

US Software's SuperTask! RTOS was adapted to run on the SBC-386EX-S supported by the Arcom software library. A complete set of software drivers for all of the hardware components is included with the SDK (see Figure 1). Translation: You don't have to write your own drivers! A full-function, interrupt-driven, serial communications library is there to back up the three serial ports. The Dallas RTC has its own library of routines, and Treck provides the TCP/IP stack for use by the Ethernet hardware module. There's no guesswork when it comes to using the Treck TCP/IP stack because it's fully integrated into the SuperTask! RTOS. You name it, the Treck stack does it, including PPP, SLIP, ARP, Proxy ARP, IP, ICMP, UDP, and, of course, TCP. If some of these terms are foreign to you, an Acrobat PDF file describing them all along with the theory and operation of the Treck TCP/IP stack is included in the manual area of the SDK CD-ROM. I also visited the Treck web site and found a complete PDF user manual for the Treck low-level and application-level Internet protocols. Try saying that 10 times fast. Networking is covered as far as the SBC-386EX-S is concerned.

The SBC-386EX-S Flash File System is treated just like any other file system component. Using the Flash File System component in conjunction with the Arcom boot loader allows the Flash File System to be heavily involved with managing the flow of executable code, configuration files, and application data storage within the SBC-386EX-S's hardware, software, and firmware hierarchy.

Going back to our Hollywood war movie, the secret agent who attached the explosive to the bridge had to detonate the lethal package from a remote location or be blown to bits along with the bridge. The same holds true for the SBC-386EX-S, but in a different context. The SBC-386EX-S can be remotely debugged using a Paradigm debugger. The blasting cap in this remote debugging effort is supplied by hardware from Zilog and Maxim in the form of an SVIF board, which is included with the SDK. The SVIF board in Photo 2 is based on Zilog's Z85C30 CMOS serial communication controller. Basically, the Z85C30 provides a UART interface with interrupts to the SBC-386EX-S. Maxim provides the RS-232 conversion in the form of a pair of omnipresent MAX232 ICs. This hardware and firmware SVIF arrangement allows the final debug session to be the final production session as well. Debugging the SBC-386EX-S is a non-intrusive process. After debugging is complete, the SVIF board can be disconnected and everything flows just as it did when the debugger board was connected. The compiler make files that are part of the development environment create files that are compatible with the Paradigm Remote Debugger package.

Speaking of compilers, the SBC-386EX-S SDK is supported by compiler tools from Borland and Datalight. The SBC-386EX-S development system includes a complete Borland 5.02 C compiler with the TASM *x*86 assembler and TLINK linker. Hooking up the Borland compiler and the Paradigm debugger qualifies the software development side of the SBC-386EX-S SDK as flight-tested. Paradigm's Link/Locate is also in the

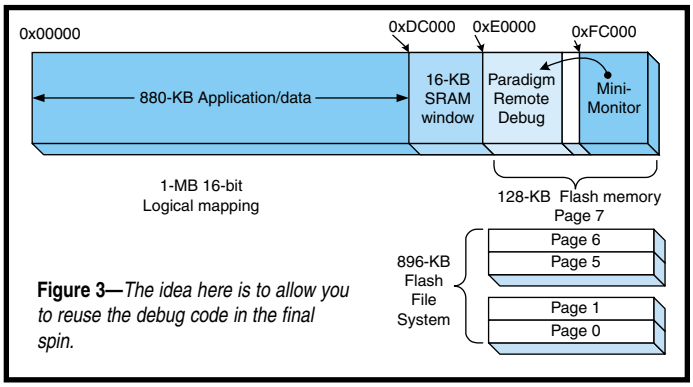



**Figure 3**—*The idea here is to allow you to reuse the debug code in the final spin.*

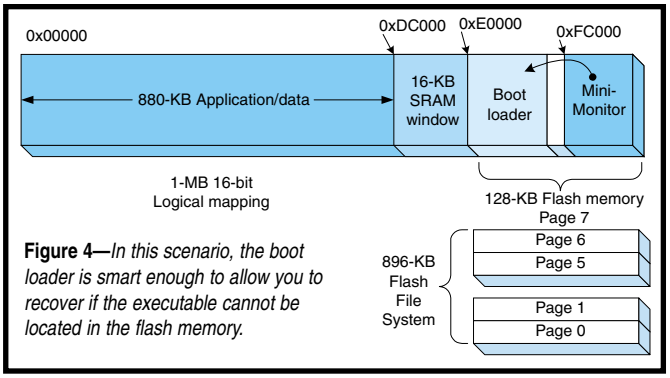



**Figure 4—***In this scenario, the boot loader is smart enough to allow you to recover if the executable cannot be located in the flash memory.*

mix, seamlessly integrated into the inner workings of the SDK. Translation: You don't have to worry about it. The Borland C compiler and the Datalight Software Development Kit are contained on the Datalight CD-ROM that comes with the SDK.

The Paradigm Remote Debugger allows you to examine and debug code that is running on the remote SBC-386EX-S, just as if it were running native on the debugging platform. Source code can be viewed as either assembler or C source. The SVIF debug module not only provides a window into the '386EX, it has a finger on the NMI interrupt as well. This means that breakpoints can be set anywhere, including within the interrupt routines themselves.

What gives the Paradigm debugger these attributes? A remote serial debug application running on the SBC-386EX-S is talking to a host debugging application running on the host PC. The SBC-386EX-S part of this equation is loaded and ready to roll in the flash memory. Installation of the Paradigm toolset on the host PC enables your view of the debugging process. The SVIF puts the Zilog and Maxim hardware to work, providing a 115-Kbps pipe between the SBC-386EX-S and the host PC.

Don't plan on keeping a machine with an active web browser handy while you're working with the SBC-386EX-S SDK, because everything from operation manuals to IC datasheets is included with the SDK CD-ROM. The main idea behind the SBC-386EX-S and companion SDK is to get your project up and running with minimal time and effort. If it has something to do with the SBC-386EX-S hardware, software, or firmware, it's on CD-ROM.

## MORE NITRO

Shifting from WWII movies to Hollywood westerns, you see lots of explosive "experts" wearing spurs and carefully handling clear vials of nitro. Better yet, in the heat of a fierce gun battle, the good guys shoot into a wagon full of dynamite. You know the outcome of each scenario.

Well, my little bundle of dynamite consists of two more CDs that are included with the SDK. One of the CD-ROMs is the Borland 5.02 C compiler and Datalight tools. The other CD loads the Paradigm Remote Debugger. After careful reading, I got the serial numbers to match with the correct products, and Borland 5.02 and the Paradigm debugger became residents in the data hotel.

Now that all of your software and firmware explosives are in place, it's time to run the wires and push the plunger on the detonator. During the Paradigm install process, I told the debugger to use COM1. COM1 connects directly to the SVIF on the MAX232 side at 19,200 bps. The Zilog Z85C30 uses a 20-strand ribbon cable to pass the serial data to the PL1 port on the SBC-386EX-S. Of course, a suitable power brick is included with the SDK and, upon proper connection of all of the ribbon cables and power sources, Photo 3 results. Boom!

## THE LOGICAL SBC-386EX-S

The hardware works and the software seems to be installed correctly at this point. The SBC-386EX-S is memory-rich and, because memory is a major factor in an embedded system that doesn't rely on external physical storage, let's take a closer look at how the SBC-386EX-S uses its stash of memory cells.

The SBC-386EX-S can support both Real and Protected modes of operation. The software suite on the SBC-386EX-S is tuned for Real mode operation. Every piece of code that comes with the SDK was built using a large memory model for *x*86 CPUs running in 16-bit mode. A logical Real mode memory map of the SBC-386EX-S is depicted in Figure 2. The memory is physically different and the chip select unit (CSU) on the CPU allows physical memory to appear at differing logical addresses in Real mode. In this mode of operation, when using the large memory model, the top of memory is 1 MB, or 0xFFFFF.

When the SBC-386EX-S powers up, the CPU jumps to code that is residing in the flash memory area at physical address 0xFFFF0. Referencing Figure 2 again, the UCS line is the only active select line at this point in time. The Arcom Mini-Monitor code you see in Photo 3 resides at this vector. In addition to displaying the banner, the Mini-Monitor initializes the rest of the system. In the initialization process, the CSU on the SBC-386EX-S CPU is programmed to give CS2 an operational address of 0xDC000 to 0xE0000, which establishes a 16-KB SRAM page area. The UCS line is reprogrammed to provide coverage of the memory area between 0xE0000 and the top of the memory area at 0xFFFFF. This provides a 128-KB chuck for flash memory access. The UCS and CS2 signals have a higher priority than the CS0 signal.

So, all that's left to do is define the DRAM using CS0. In the case of the SBC-386EX-S, the DRAM is logically everything that is not used by the flash memory and SRAM. Therefore, that leaves the area from 0x00000 to 0xDBFFF, or 880 KB.

The pages of SRAM and flash memory are enabled using a bank control register. SRAM is cut up into 32 pages of 16 KB, and flash memory is chopped into eight pages of 128 KB. The Arcom Flash File System handles paging the flash memory area if you choose to use it, and Arcom supplies APIs to get at both the SRAM and flash memory areas if you decide to go your own way. The SRAM is always available, as it does not depend on the Flash File System for operation. That pretty much covers

all of the necessary words behind the concept of the cool graphic shown in Figure 2.

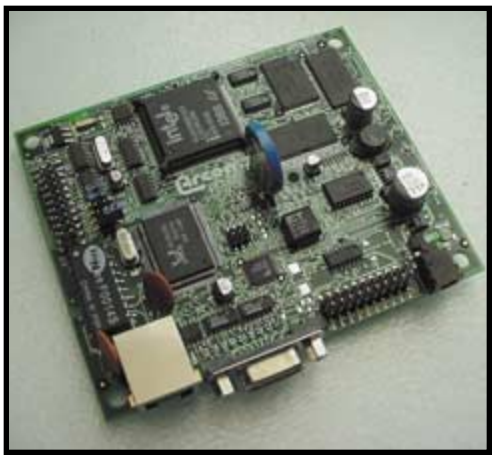


**Photo 1**—*This has a lot of bang for your buck.*

## BLOWING UP BUGS

Because I'm on this blow-it-to-bits kick, remember the movies that used black powder poured from a barrel on the ground as a fuse? Or better yet, think back to those scenes where the bad guy foolishly strikes a match in the powder room to see where he is and has to hit the deck. Such scenes came to mind when I began this article, because now all of those explosive SBC-386EX-S components I've been describing (software APIs, the Borland C compiler, Datalight toolset, SVIF, and the SBC-386EX-S itself) are coming together and you can see what's in the "barrel." You shouldn't be striking matches in the dark, so let's take a look at what the SBC-386EX-S does after the Mini-Monitor checks a shorting link on the SBC-386EX-S board.

That link is marked "MM." If this link is missing, the Mini-Monitor jumps to location 0xE0000, which is a flash memory location. If this is a debugging session, the Paradigm debug will be waiting at the 0xE0000 location. The Paradigm Remote Debugger will then prompt bits on the SVIF to initialize the Z85C30's UART and, thus, establish a debug communications session between the Paradigm host debugger session and its counterpart code running on the SBC-386EX-S. When the debugging session is complete and you wish to place the final code in flash memory, the Arcom Bootloader program takes its position at location 0xE0000, replacing the Paradigm debug code. Figure 3 shows what the debug memory configuration looks like before the boot loader code is introduced. If all goes well in the debugging phase, you can FTP the debugged `.exe` file into the Flash File System while still in Debug mode.

Referencing Figure 4, the only difference you see is the boot loader code where the Paradigm code used to be. There's a bit more that goes along with the boot loader residing in this position of memory.

Again, at powerup the SBC-386EX-S checks the "MM" link. If the link is missing, the Mini-Monitor again jumps to location 0xE0000. This time the boot loader code is given the go-ahead for execution. The boot loader initializes the Flash File System and then begins a search for a file with an `.exe` extension. This `.exe` extension file should be the same file that was debugged and FTPed to the Flash File System earlier.

The first encounter with a file with that extension alerts the boot loader to load the `.exe` file into DRAM at location 0x01000 and jump there to allow the `.exe` file to execute. If a valid `.exe` file is not found, the boot loader opens a serial interface so the flash memory can be repaired or another `.exe` file can be downloaded.

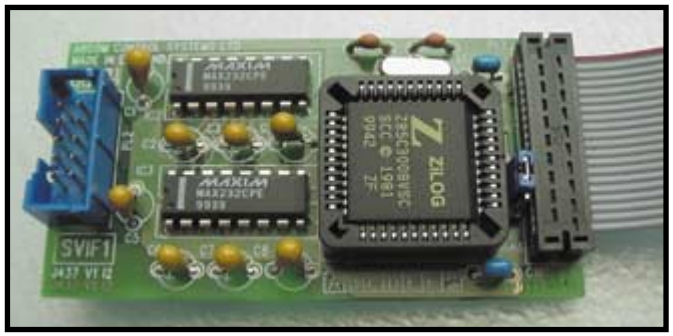



**Photo 2**—*Plug it in and debug. Unplug it and run.*






**Photo 3—***I pressed "H" to bring up the command summary.*

## GET READY TO LIGHT THE FUSE

There's only one more step remaining to get the SBC-386EX-S online and ready to develop and debug a project: set up the environment. In an effort to leave no stones unturned, Arcom has provided a batch file for that purpose, `SetPaths.bat`. Because this whole SDK is running under Win98, DOS is and it isn't as far as environment is concerned. Every time the DOS window is closed, out go the environment settings for that window. So, to be sure that the directory environment is set up correctly each time you start the SDK suite, you'll use a shortcut configured to run the `SetPaths.bat` file and set up the DOS memory environment variables.

The first step is to create a standard MSDOS shortcut and place it on the desktop. We'll call it SBC386. Next, open the properties window of SBC386 and choose the Program tab. You need only establish the working directory and the batch file to execute, as shown in Photo 4. Because DOS is involved, memory management comes into play. Selecting the Memory tab, max out the conventional memory environment allocation and make sure HMA is checked. This all may be trivial, but if it isn't done correctly, nothing will work. I can't tell you the hours I've wasted because I missed what seemed to be an insignificant step in the process. Ultimately, you want to see the DOS window portion of Photo 4 when you click on the shortcut.

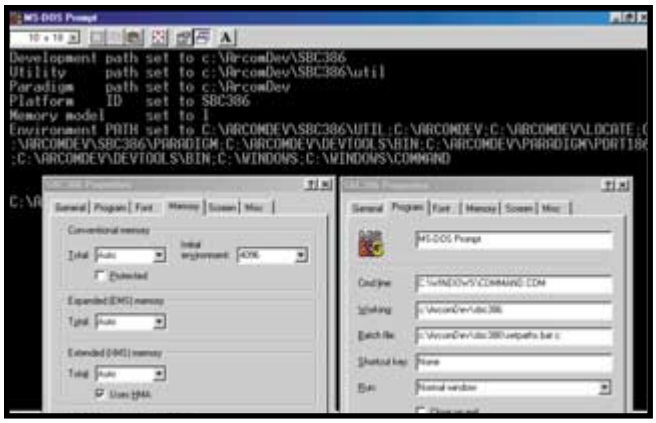
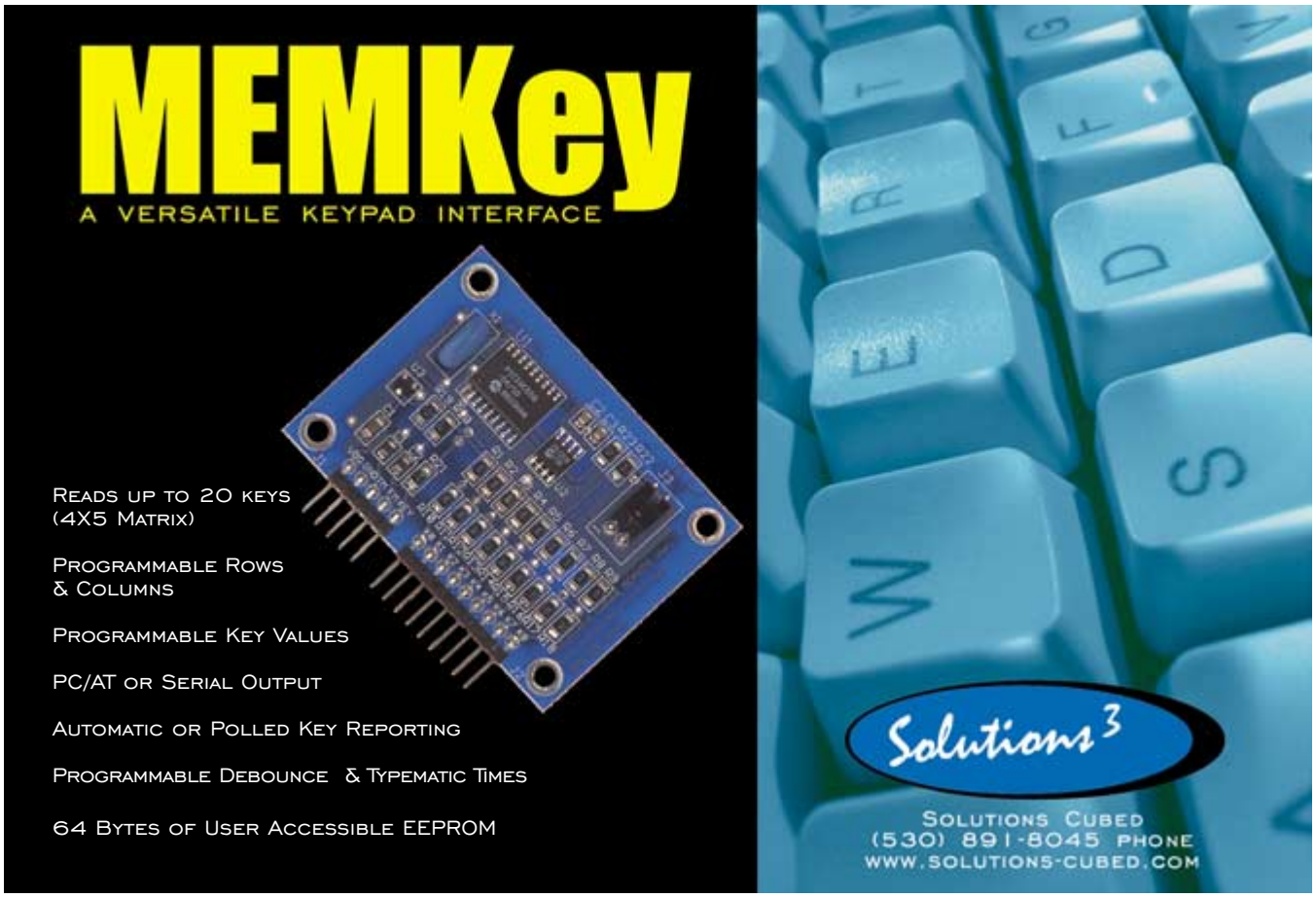


**Photo 4—***Sometimes it's the purely simple things that matter.*

What you have now is a totally complete embedded development environment. There is still quite a bit I want to show you about the SBC-

386EX-S. I've covered the basics in this installment, and next time I'll show you the inner workings of the Paradigm Remote Debugger SVIF combination. In addition, I will whip up some Borland C statements and make the SBC-386EX-S perform some internetworking.

As you can see, the engineers at Arcom have gone to great lengths to provide a ready-to-roll embedded development environment. I guess they feel as I do, that it doesn't have to be complicated to be embedded.

*Fred Eady has more than 20 years of experience as a systems engineer. He has worked with computers and communication systems large and small, simple and complex. His forte is embedded-systems design and communications. Fred may be reached at fred@edtp.com.*

## SOURCES

**SBC-386EX-S board**
Arcom Control Systems
(408) 586-5300
Fax: (408) 586-5306
www.arcomcontrols.com

**5.02 C compiler**
Borland Software Corp.
(831) 431-1000
www.inprise.com

**DS1302 RTC IC**
Dallas Semiconductor Corp.
(972) 371-4000
Fax: (972) 371-3715
www.dalsemi.com

**'386EX**
Intel Corp.
(408) 765-8080
Fax: (408) 765-9904
www.intel.com

**Software Development Kit**
Datalight Inc.
(425) 951-8086
Fax: (425) 951-8095
www.datalight.com

**SVIF board**
Maxim Integrated Products
(408) 737-7600
Fax: (408) 737-7194
www.maxim-ic.com

**RTL8019AS**
Realtek Semiconductors Corp.
886-3-578-0211
Fax: 886-3-577-6047
www.realtek.com

**TCP/IP stack**
Treck, Inc.
(800) 340-6648
Fax: (513) 688-0993
www.treck.com

**SuperTask! RTOS**
United States Software Corp.
(503) 844-6614
Fax: (503) 844-6480
www.ussw.com

**Z85C30 CMOS**
Zilog, Inc.
(408) 558-8500
Fax: (408) 558-8300
www.zilog.com

## RESOURCE

**Paradigm C++ Debugger Interface**
Paradigm Systems
www.devtools.com/pcpp/debugger.htm.

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Connect a controller card, printer, weighing scale, or any device with a serial port to the Ethernet. The MSS-C is a universal thin server with TCP/IP protocol stack and Ethernet interface. Use the MSS-C for industrial control, monitoring, lighting, heating/wentilation systems, and process reporting.

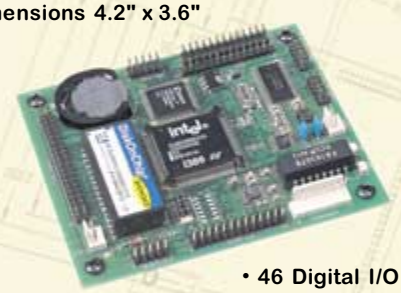
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Ed Nisley

# Have You Seen the Light?

Anyone who spends a good amount of time on a bicycle knows that keeping yourself visible is an important part of keeping you (and your bicycle) in one piece. This month, Ed takes a look at high-intensity LEDs and how to construct a simple blinking safety device.

Recumbent bicycle riders divide neatly into two groups when the subject of blinking taillights comes up. Some folks say that bents are so conspicuous that lights add nothing, and others contend that every little bit helps. Although I've ridden a non-blinking bent for six years with only a few close encounters of the fender kind, I've decided now it's time to see how the other fraction lives.

Now, if you're going to have a blinking light, you want a blinking light that's really bright. Years ago, my daily commuter bike sported a red-filtered xenon strobe powered by three 90-V batteries. I should have used a DC/DC converter instead of batteries, but relaxation oscillators are dead simple, and I was less experienced.

But, that was then. This is now.

## AND THEN THERE WAS...

High-intensity LEDs have become bright enough to be easily visible in daylight, particularly when equipped with directional lenses. Even better, those highway message boards sporting red, green, and yellow LEDs are now so common that you can find their component LED clusters at many surplus sources.

Photo 1 shows the 52-mm Sharp LT6750 LED cluster lamp I picked. The case has a hood over the top half that enhances contrast and an O-ring seal on the back to keep water out. Figure 1 details the internal connections: 14 red LEDs in two parallel strings and 27 green LEDs in three parallel strings.

At 40 mA, the red string drops 14 V and produces 5.6 cd. The green string draws 80 mA at 20.5 V and shines at 5.3 cd. Asymmetric lenses produce a 70° beamwidth in the horizontal plane and about half that vertically.

The LT6750 is dazzling when you're in the same room and nearly blinding at the bench. Mounted on a bike, it will serve as a fine marker lamp.

However, there's an obvious mismatch between those LED forward voltages and the output levels of common batteries. Although I could wire two 12-V batteries in series, this seemed like a perfect opportunity for a DC/DC converter. What used to be a rather touchy design problem for my old bike transmutes into a single chip with a few external components, all of which appear on the circuit board in the left of Photo 1.

The main component, a MAX629 boost converter, is the small-outline, 8-pin DIP near the top. Three LM317 linear regulators in TO-92 plastic cases set the supply voltage and LED currents. The board is shaped like a boot heel for a good reason: it mounts

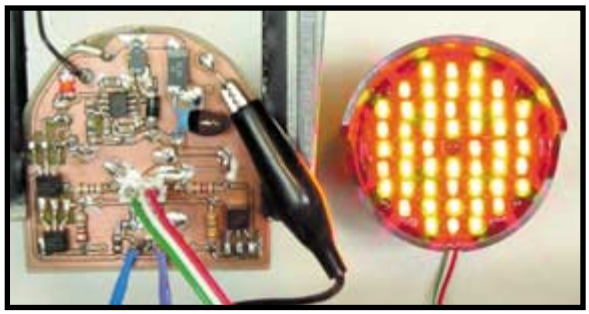


**Photo 1—***A MAX629 DC/DC converter powers the LT6750 LED array from a 12-V battery. Three LM317 linear regulators set voltage and current levels. A signal generator supplies pulses to this prototype unit.*

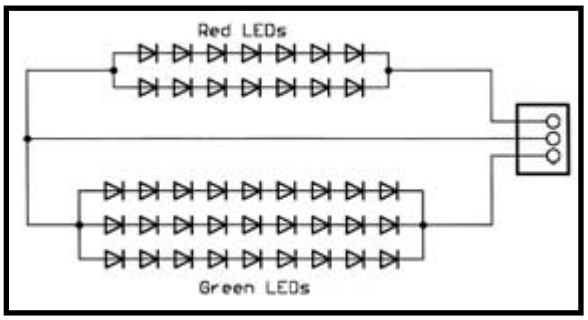



**Figure 1—***The Sharp LT6750 LED cluster uses series and parallel diode connections to improve reliability and reduce drive current. Unfortunately, that makes the terminal voltages higher than common batteries.*

directly behind the LED cluster in a machined housing, with the flat edge clamped to the bike frame.

But, as is usually the case with analog circuitry, it seems you need a handful of parts to get anything done, so let's see what all those parts do.

## SLAM-BANG SWITCHING

Quick survey: Raise your hand if you've ever fried a transistor relay driver before you found out about resistor capacitor snubbers and clamp diodes. Hah! Thought so. And ever since then, you've regarded inductive kick as a really bad thing, right?

Boost mode DC/DC converters harness inductive current to a good cause. The MAX629 stores energy as current in an inductor, then routes that current into a capacitor to create a higher voltage. It's the same principle as the relay coil frying your transistor but done deliberately.

The key components in Figure 2 are L1, a 47-µH inductor (the small black circle at the top of the circuit board in Photo 1); C2, a 10-µF tantalum capacitor; and D2, a Schottky diode.

The circuitry behind the MAX629's LX pin includes a high-current, open-drain FET with a current monitor in the source. With that transistor off, C2 charges quickly through D2, and with the voltages equalized to about 12 V from the battery, the current through L1 drops to zero. When the transistor turns on, the LX pin sinks current from L1. D2 prevents current flow from C2, so the capacitor maintains its charge and voltage.

The current through L1 builds up from zero with a time constant determined by the parasitic resistance of the inductor plus the internal resistance behind the LX pin. According to the datasheets, the total resistance is about 1.5 Ω, giving an L/R time constant of 30 µs.

The MAX629 monitors the LX current and shuts off the FET at 500 mA (or 250 mA, depending on the ISET input pin). Figure 3 shows the voltage at LX, which starts at 12 V, drops to zero (actually, about 200 mV) when the FET goes on, then rises to 24 V when it turns off.

Where did the 24 V come from? You'll recall that the current through an inductor cannot change instantaneously. When the FET turns off, no current flows into LX and the diode is still reverse biased. That's the point when your relay driver transistor fried itself, but things are different here.

The voltage at LX rises rapidly, until D2 becomes forward biased and routes that half amp to C2. The inductor current then drops as the voltage on C2 rises. Over the course of several hundred cycles, the MAX629 pumps the initial 12 V on C2 up to 24 V, which is why we call the MAX629 a "boost converter."

The upper trace in Figure 3 shows the voltage across C2, AC-coupled at 200 mV per division. When the LED turns on at the second division from the left, the output voltage on C2 ramps down as the MAX629 is charging the inductor. The sudden 340-mV jump occurs as the inductor stuffs half an amp into the capacitor.

Perhaps this is the first time you've seen equivalent series resistance (ESR) in action. Only 0.7 Ω of ESR in C2 will account for that bump. This is why boost converters don't often power sensitive analog circuitry, at least not without a post regulator to smooth things out.

The combined effects of declining inductor current and LED load reduce the voltage on C2. The MAX629 begins another cycle when the voltage falls below the minimum setpoint. The cycle repeats at about 330 kHz.

Because the L/R time constant for L1 is greater than the cycle time, the inductor current rises predictably. It also falls predictably as the capacitor absorbs the charge.

I picked 24 V because it was high enough to run the LEDs with just enough headroom for current regulation. The MAX629 is a mature device and you'll find similar products from many vendors. One of them will produce the voltage you need, although some require an external switching FET to deliver higher power.

OK, pop quiz time. What happens when (not if) you accidentally short the positive terminal of C2 to the ground plane around it? Answer: Poof! L1 emits magic smoke!

That 30-µs L/R time constant may be large with respect to normal operation, but it's small compared to human reaction times. The current through L1 rises past the inductor's

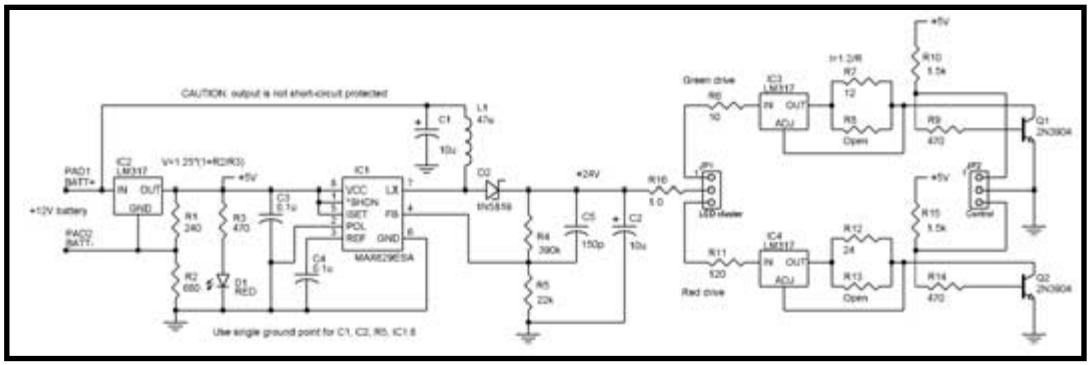



**Figure 2—***As is typically the case with analog circuitry, you need a remarkable number of parts to get anything done. The LED cluster connects to JP1, and timing controls enter through JP2. Good PCB layout can minimize RFI caused by the abrupt, high-current pulses generated by the MAX629.*

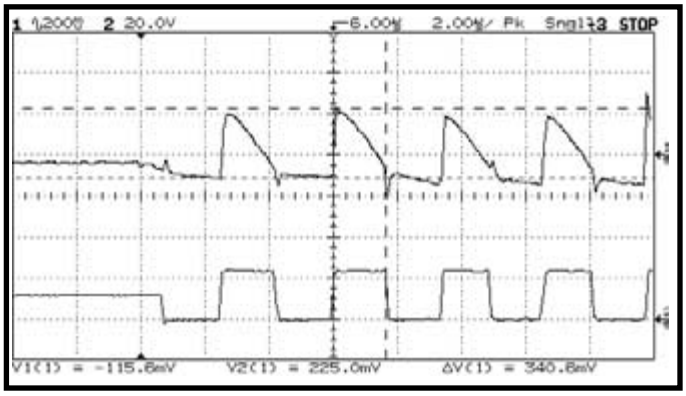



**Figure 3—***The AC-coupled top trace shows the output voltage across C2 and the bottom trace shows the voltage at the MAX629 LX pin. When the LEDs turn on at the trigger point, two divisions from the left, the output current jumps from 0 to 150 mA.*

500-mA maximum rating toward the 12-V/0.6-Ω DC limit. However, the AWG 37 wire in the inductor burns out long before the current stabilizes at 20 A. Consider yourself warned.

## CURRENT DRIVE

LEDs are, first and foremost, diodes, with their exponential current-versus-voltage characteristic. In general, you must regulate the current through an LED and let the LED set its terminal voltage. Imposing a constant terminal voltage) is a recipe for disaster.

As you see in Figure 1, the LT6750 connects the anode ends of the diode strings to a common (as in shared, not ground) terminal that connects to a positive supply voltage. The green LED strings require about 20 V to turn on and the red LED threshold is 13 V. You must supply enough voltage to not only turn on the LEDs, but also account for drops across the switches and current limiters. Because the two LED strings have different current ratings, you must use two limiters, not one in the common lead.

You probably used resistors to set LED currents in your circuits. Subtract the LED forward drop from the supply voltage, divide by the desired LED current, and you get the limiting resistor in ohms.

The LT6750 spec sheet shows typical and maximum voltages for each string. Those voltages differ by 1.5 V, and the datasheet mentions neither the minimum LED voltage nor its temperature coefficient. Suppose you pick 80 mA for the green LEDs with a 24-V supply voltage and the maximum LED voltage of 20.5 V. The resistor sees 3.5 V, so 80 mA means 44 Ω.

The reason your resistors worked so well is that the LED forward drop is usually much lower than the supply voltage, making typical variations small compared with the nominal voltage across the resistor. In this case, I don't want to produce 40 V just to drop half of it across a resistor!

The solution requires a resistor that adapts to changing voltage while maintaining a constant current. The familiar LM317 can serve as a current limiter, although most folks don't think of it in that role. IC3 and IC4 in Figure 2 show how it's done.

A single resistor sets the current limit according to the formula:

$$I = \frac{1.2}{R}$$

So, to get 100 mA, you'd use a 12-Ω resistor. The LM317 regulates the current within about 1% and protects itself against output shorts.

The current-setting resistor, however, must carry the entire output current across a voltage drop of 1.2 V. At the 100 mA I chose for the green LEDs, that amounts to 120 mW, uncomfortably close to the 125-mW rating for 0805 (0.08″ × 0.05″) surface-mount resistors.

I laid out the circuit board with two parallel, 0.25-W, through-hole resistors for each LM317. Carbon film resistors have a higher power limit, they're easier to install and replace, and you can hand-select two cheap 5% resistors to precisely set the current. I used one 12-Ω resistor to get 100 mA and a 24-Ω resistor for 50 mA, with no trimming required.

The series resistor ahead of each LM317 drops 1 or 2 V, reducing the regulator's dissipation. R16 is a small resistor that's handy for measuring the total output current, but I replaced it with a jumper after I saw that the LM317 regulators work exactly as expected.

You should maintain at least 3 V across the LM317, however, to ensure that it regulates correctly. The green string runs under that limit; it seems my LM317s have a lower drop. You can use a low-dropout regulator if your minimum supply voltage gets closer to the maximum drive voltage.

With a MAX629 supplying voltage and LM317s setting the current, all that's left is some on/off control to make the LEDs blink. I used a pair of NPN switches driven by an external pulse generator to make things simple. The bias resistors hold them on with no external input, just to make for easy setup and testing.

Blinking those LEDs at 10 Hz with a 30% duty cycle gets my attention. I wonder how it works on the road.

## RING THAT BELL!

The MAX629 datasheet recommends single-point grounding for several components and encourages good circuit board layout. Figure 4 shows you how important layout can be.

The square waves leading up to the middle of Figure 4 show the MAX629 pulling LX to ground and letting the inductor snap it back to 24 V. The LEDs switch off at the middle division, where L1 is still charging C2. The MAX629 briefly yanks LX low, then shuts it off again. Where does the current flowing through L1 go with D2 biased off and LX turned off?

Answer: You've just (re)discovered the fact that analog schematics don't tell the complete story. Obviously, current through L1 must flow through either LX or D2. It has nowhere else to go, right? Well, sorta kinda.

At RF frequencies, parasitic effects become just as important as the components you solder to the circuit board. In this case, current flows through several parasitic capacitors, across the ground plane, and back to the inductor.

The resonant frequency of an LC (inductor-capacitor) tank circuit is, at first approximation:

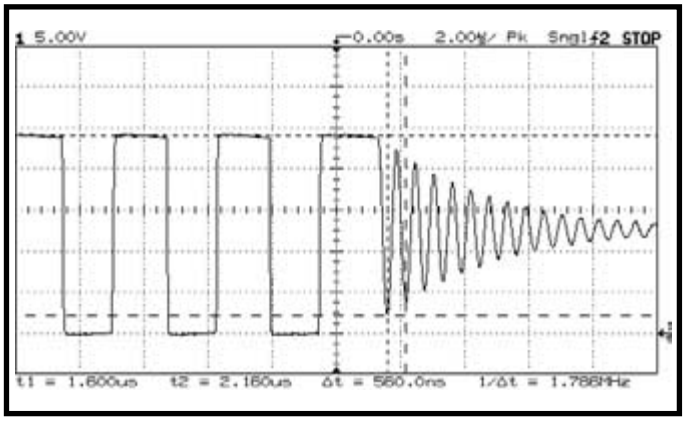



**Figure 4**—*The voltage at LX rings like a bell when the load disappears and the MAX629 shuts off the current. A good ground layout keeps the oscillating current within the circuit board, not broadcast through space.*

$$f = \frac{1}{2\pi\sqrt{LC}}$$

With the circuit ringing at about 1.8 MHz and L = 47 µH, the capacitance is 170 pF. But where's the capacitor? For extra credit try to figure out the effective Q of the LC circuit from the waveform in Figure 4. Hint: Q is the ratio of stored-to-dissipated energy per cycle. Bonus: Find the circuit's effective series resistance and compare it with L1's rated DC resistance.

The largest parasitic capacitance isn't through the circuit board to the ground plane. I measured 275 pF of capacitance on a 16"² circuit board, so the foil on that node is 1 or 2 pF. The inductor's parasitic capacitance isn't more than a few picofarads either.

The 1N5819 datasheet specifies a reverse biased junction capacitance of 50 to 80 pF. The MAX629 datasheet doesn't specify the LX pin's capacitance, but discrete FETs rated at 1 A run about 100 pF.

There you have it. Most of the parasitic capacitance hides inside the active devices. In a sense, the current does flow through the LX pin and D2, but not in the way you expect from the schematic, which illustrates normal circuit operations. This is why attention to proper grounding and component layout are important; that current must go somewhere. Use ugly construction when appropriate, but don't let ease of construction outweigh good design.

Once again, you have been warned.

## CONTACT RELEASE

Yes, the switching transistors cry out for a little 8-pin microcontroller. I'll leave that to your imagination.

Longtime *Circuit Cellar* readers know generating pulses is a simple matter of firmware.

You can download the schematic and board layout, both in EAGLE format, from the *Circuit Cellar* web site. I used Press-n-Peel blue image transfer film to mask the circuit board.

With any luck, just about the time you are reading this, I will have discovered whether being more conspicuous is a good or bad thing. See you on the road!

*Ed Nisley is an electrical engineer. In addition, he is a ham radio hobbyist (call sign KE4ZNU). You may reach him at ed.nisley@ieee.org.*

## SOFTWARE

The schematic and board layout are available on the *Circuit Cellar* web site. The EAGLE and PCB layout programs can be downloaded from www.cadsoftusa.com or www.cadsoft.de.

## SOURCES

**LT6750 LED lamp cluster**
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FROM THE BENCH

Jeff Bachiochi

# See Through the FOG Using Fixed-Point Calculations

## Fiber Optic Gyros



Yet another column from Jeff that starts with "I got this toy...." Read along this month and you'll see (again) how simple observations can lead to a better understanding of technology.

Most of you have probably received a toy gyroscope as a gift at some point. I can't guess how many times I've wound up and pulled the string on one of those things. Sometimes when pulled too hard, the heavy wheel would dislodge from its bearing pins, hop out of the frame, land on the floor, and continue to spin for what seemed like forever. This misuse encouraged me to experiment with other toys such as tops and yo-yos. All of these use a rotating mass to sustain often illogical positions. Little did I realize at that time that there was a practical use for the gyroscopic effect.

The balanced rotating mass resists movement of the axis on which it spins. It seems that any attempt to tilt the mass' axis applies a force to the mass, which is counteracted by an (almost) equal and opposite force when the mass is rotated 180°. There is a tendency for the mass to transfer the tilting force to a vector, 90° to the original force (and the axis of rotation). This force can be counteracted by gimbaling the gyro (allowing a second axis of rotation) around the original vector. So, a single rotating gyro will attempt to prevent motion in two (2-D x, y) of the three possible dimensions (3-D x, y, z), with the z dimension being the axis of rotation.

To create a platform that attempts to prevent rotation in all three dimensions, a second gyro can be added at right angles to the first. Now movement in all three dimensions is counteracted. In this configuration, a force in one of the dimensions is actually resisted by both gyros. By isolating the platform with at least three sets of gimbals, the inner gyro platform will remain stationary, independent of the motion of the outer gimbaled ring. This part is usually attached to the ship, plane, missile, or other vehicle that is in need of position reference. Note that the position is relative to the gyro platform and not an absolute position (i.e., GPS).

Today mechanical spinning gyroscopes are being replaced by two new classes of technology, optical and silicon etched. Although advances in micro machining have come a long way, optical gyroscopes are more reliable and less expensive than their mechanical counterparts. KVH Industries uses optical techniques (optical fiber) to measure angular movement. This is done by splitting a polarized and modulated laser beam such that the two beams travel through a coil of fiber optic cable in opposite directions. When the beams have completed their journeys, they recombine to produce an interference pattern. Because both travel the same distance, they cancel exactly. But, if the coil is rotated in one direction, one of the beams will have to travel a

| Value | Meaning in bits | Meaning in degrees |
|---|---|---|
| 7FFF | 32767 bits change counterclockwise | 2.9981805° maximum in 100 ms |
| 0001 | 1 bit changes counterclockwise | 0.0000915° |
| 0000 | No change | No change |
| FFFF | 1 bit changes clockwise | –0.0000915° |
| 8000 | 32768 bits change clockwise | –2.998272° maximum in 100 ms |

**Table 1**—*This is how the rate value corresponds to an angle in degrees.*

| Character number | Character data | Where |
|---|---|---|
| 1 | '1' X7 X6 X5 X4 X3 X2 X1 | X7–X0 is a byte of checksum data |
| 2 | '0' X0 B15 B14 B13 B12 B11 B10 | B15–B0 is a word of built-in test data |
| 3 | '0' B9 B8 B7 B6 B5 B4 B3 | |
| 4 | '0' B2 B1 B0 C7 C6 C5 C4 | C7–C0 is a byte of odometer data |
| 5 | '0' C3 C2 C1 C0 T7 T6 T5 | T7–T0 is a byte of temperature data |
| 6 | '0' T4 T3 T2 T1 T0 R15 R14 | R15–R0 is a word of rate data |
| 7 | '0' R13 R12 R11 R10 R9 R8 R7 | |
| 8 | '0' R6 R5 R4 R3 R2 R1 R0 | |

**Table 2—***This is KVH Gyro's digital output format.*

longer distance. So, the beams won't cancel, and the output of the detector will be proportional to the rotation rate. The phase modulation allows the direction of rotation to be distinguished. The KVH E-Core 2000 Fiber Optic Gyro is available with either analog or digital output.

## NOT THE RESTAURANT

In the song "Alice's Restaurant," Arlo Guthrie sings, "I didn't come here to tell you about Alice. I came to talk about the draft." In this case it's not the draft or gyroscopes, it's number handling. To make use of this gyro's output, you need demanding digit dexterity. This project requires taking in the rate of change data from the KVH Gyro, computing the position in degrees, and displaying it on a small LCD. I believed this project could be done using microEngineering Lab's PicBasic. A visit to their web site revealed an application note on how to incorporate Microchip's floating-point routines into PicBasic. But the more I thought about it, the more I convinced myself that I wouldn't need floating point. Here are the facts.

The gyro's digital output is a block of eight characters at 9600 bps, 10 times per second. Nine-thousand six-hundred bps is ~104 µs/bit, so eight characters of 10 bits each will take ~8.3 ms. These blocks come every 100 ms, so that leaves ~90 ms to do something with the blocks of data.

For now, let's skip directly to part of that data. One of the pieces of data transmitted is a 16-bit word, which indicates a change in position (rate) since the last block of data 100 ms before. Each bit of rate data is equal to 0.0000915°. The rate is a signed word because the position can either be clockwise or counterclockwise, as is shown in Table 1.

If this rate is converted to degrees and the maximum number is 360 (or 359.99), you'll need to total an integer of 360 with a resolution of 0.0000915. If you multiply everything by 10,000,000, you can rid yourself of the decimal. This shifts the maximum integer to 3,599,999,999 (D693A3FF), requiring a double word, or 32 bits, of storage for this accumulation. To display the degrees on an LCD, divide this number by 100,000 to a maximum of 35,999. This fits into a single word and can be easily formatted by outputting a decimal point before the last two characters (i.e., 359.99°).

The evaluation of the numbers involved in an application is essential for choosing a programming direction. A quick look at floating point shows that the mantissa's 32 bits (resolution portion of the number) of a single precision floating-point number has a maximum of 2,147,483,647. Your maximum number won't fit into one floating-point number and retain all the precision you need, so it's necessary to use double precision for storing this value. My gut feeling is that the conversion to floating point isn't worth the execution speed penalty for that level of number crunching. So, here's how I attacked the application.

## BLOCK CONVERSION

The KVH Gyro outputs eight characters of data in a block (see Table 2). Notice that the first byte always has the MSB set, and the remaining bytes have their MSB cleared. This allows you to identify the beginning of the block. You may choose to grab just the data bytes that hold the information you are interested in. It's just as easy to grab them all. When all the data has been received, there is 90 ms to finish the rest of the work before the next data is available. All of this code runs in line (i.e., no interrupt or background routines are necessary).

Converting the raw data into variable data is straightforward, with a few exceptions. Temperature data must be built from receiving two consecutive blocks (see Tables 3 and 4). The built-in test data also requires multiple blocks. Because none of that data is used for this application, I'll spare you some of the boring stuff. A checksum byte is part of every block's data. This byte, as with most checksums, allows all the derived data bytes of a block to be added to modulo-256 to determine if there has been an error in transmission. You can log this fact, however, there isn't anything you can do to get it resent.

## RATE ADJUSTMENT

The raw data block has now been converted to individual data variables, and the rate data must be adjusted before it is summed. The rate must be multiplied by the angle/bit constant 915 (915/10 billionths of a °/bit). Because the rate is a signed number and the math routines in PicBasic are unsigned integers only, you need to do more work with the negative numbers than with the positive numbers.

Let's look at the number factors first. Both the multiplicand (rate), and multiplier (angle/bit) are words, so the product can be a double word. PicBasic can do 16-bit multiplication and present the result in two 16-bit words. When the gyro is rotated near its maximum allowable rotational rate of ~30°/s, the product can be large. The application design must take into account the largest possible numbers for the application to work correctly under extreme conditions.

A positive rate will have a value <8000h. Positive values go directly through the multiplication process. Negative values must be changed into

| Temperature data format | Where |
|---|---|
| '1' CT6 CT5 CT4 CT3 CT2 CT1 CT0<br>'0' '0' '0' CT11 CT10 CT9 CT8 CT7 | CT11–CT0 is a 12-bit signed value of Celsius temperature |

**Table 3—***The Celsius temperature value is sent via two consecutive blocks.*




**Photo 1—***The 2 x 16 character LCD displays 000.0–359.9° relative rotation of the Fiber Optic Gyro with optional temperature output on the second line.*

their absolute values, multiplied, and then changed back into the negative equivalent. This is done using 2's complement method:

Rate = (Rate XOR FFFFh) + 1

After the multiplication, the reverse is done to make the product negative:

Lowwordofproduct =
Lowwordofproduct + 1
Highwordofproduct =
Highwordofproduct + C (if any)
Lowwordofproduct =
Lowwordofproduct XOR FFFFh
Highwordofproduct =
Highwordofproduct XOR FFFFh

At the maximum turning rate, the Highwordofproduct Lowwordofproduct double word actually can approach ±30 million/10 millionths of a degree or be as little as zero if the gyro is stationary. This input has a large dynamic range.

## SUM RATE

A running total of the adjusted rates indicates where the gyro is in relation to its beginning position. The total continuously changes as a result of continuous 100-ms updates via the adjusted rate. Again, the adjusted rate is a double word. The total can also be a double word. How is this possible, because the total can be increased by 30,000,000 every 100 ms? Indeed, if the maximum rotation continues for over 14 s, the double-word total will overflow. But, at the maximum rate, the gyro rotates 360° in 12 s. You need to adjust the total so that if it attempts to exceed 3,599,999,999, it will be adjusted (rolled over) to zero. And, the total must be adjusted if it falls below zero.

So, the first part of this routine adds the adjusted rate to the total. At this point, the adjusted rate is checked for a positive or negative value. The routine's execution branches are based on the adjusted rate's sign test. If the adjusted rate is negative, you look for an underflow condition of the total, where the total is >3,599,999,999. If this is the case, the total is reduced by 694,967,296 (the difference between FFFFFFFFh and 3,599,999,999).

If the adjusted rate is positive, then you look for an overflow condition of the total, again >3,599,999,999. If this is the case, then the total is increased by 694,967,296, which rolls over to the proper low positive number.

## ADJUST PIXEL POLARIZATION

To prevent too much flicker, the LCD is updated every 0.5 s. So, four out of five times through this loop, you're done. Every fifth time there is an additional calculation. If the total is divided by 100,000, you would reduce it to a single-word variable (35,999 max). PicBasic is capable of 16-bit divides. Neither the total nor the constant 100,000 are 16-bit values, so this throws a monkey wrench into the works. If you break down 100,000 into pieces, one possible solution is 16 × 250 × 25 = 100,000. I like the 16 because you can shift by a nibble to accomplish that. Both 250 and 25 are byte constants, so the division is manageable. The only routine that needs to be written is a 32-/8-bit routine using multiple 16-bit divisions on the 32-bit total.

If you look at maximums again, the original total D693A3FFh is divided by 16 by shifting a nibble to the right. This gives a new maximum of D693A3Fh. After going through the 32-/8-bit routine, where the 8-bit value is the constant 250, the maximum value is DBB9Fh. Going through the routine one more time, with the constant 25, the maximum value is 8C9Fh (35,999). One of PicBasic's nice features is having the remainder available. This comes in handy when I want to separate this word (holding the angle in hundredths of a degree) into two parts, the integer and the decimal portion. A divide by 100 gives the angle in degrees in one variable and the fractional part of a degree in a second variable.

The variables are simply printed to the LCD with a "." between them. The DFh character is a degree symbol, which can be printed instead of using the word "degrees" if you prefer. And that is that, or so it seems.

## GET MY DRIFT?

It seems as though these gyros aren't perfect. First, there's the random noise component called angle random walk, which averages zero and is the smallest of the errors. Temperature, on the other hand, has a direct effect because of the gyro's internal DC amplifiers. The drift is directly related to the temperature and changes linearly with it. After the temperature has stabilized and the gyro remains stationary, the drift factor stays constant so it can be compensated for in a number of ways. The simplest way is to



**Photo 2—***The LCD, gyro, VCR battery, and circuitry are mounted in a wooden box (shown here with the cover removed). Connectors on the right side are for the battery charger and serial output to a PC.*

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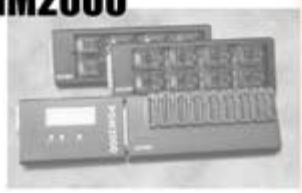
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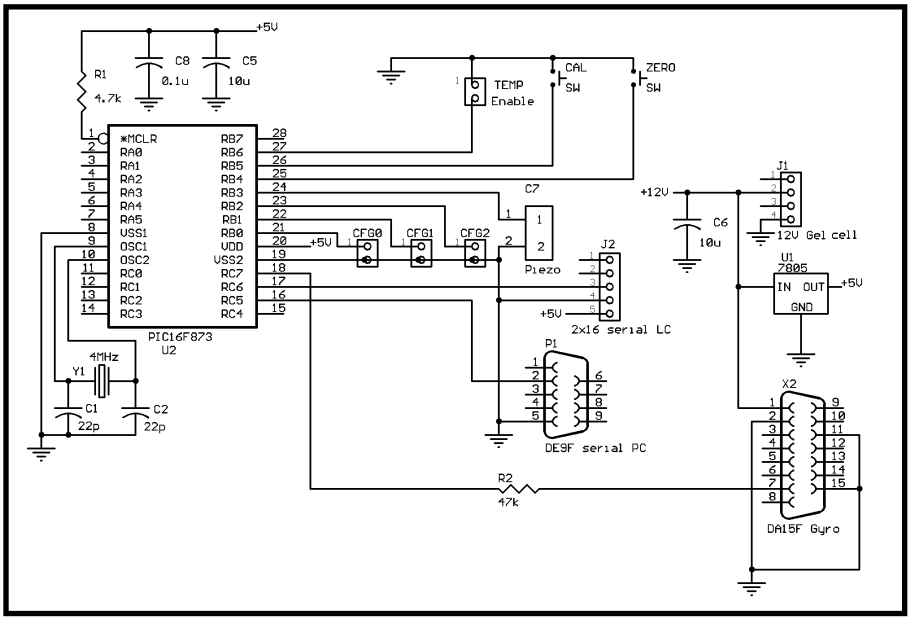



**Figure 1**—*This schematic shows the circuitry and connectors needed to interface with the other parts of the system. The gyro requires 12 VDC and outputs a serial block of 8 data bytes every 100 ms. One of the advantages of writing in PicBasic is the configuration flexibility of the bit-banged serial I/O. PB allows the serial to be I/O as true or inverted. This can get rid of extra RS-232 level shifters.*

take a sampling over a short period of time to determine the drift and use this as a correction factor. A more complex algorithm may sample at two different temperatures and determine how to adjust the drift dynamically based on change in temperature.

I added a calibration routine to do a simple average over the 256 sample. As you might have guessed, 256 was chosen because it is easily implemented. When the gyro is stationary, the rate output of 256 consecutive data blocks is totaled. The grand total is shifted eight times to the right, dividing the total by 256. This provides an average drift and is stored as the variable drift. Now each time through the main loop when the rate is adjusted and added to the total (angle), the average drift is also subtracted from the total (angle). Please note that when computing the average drift, the rate being sampled can be either positive or negative. It is therefore necessary for the averaging routine to be able to handle overflow, underflow, and adjust properly for negative 16-bit values.

## MAGNETIC ERRORS

A magnetic compass will show absolute direction. That is, it always knows where north is. When a magnetic compass is used in an area that has a high metal content, the earth's magnetic lines of flux won't reach the compass needle without being pulled slightly off course by the metal. This means that the magnetic compass needle will not be accurate throughout its rotation because it doesn't know that the magnetic flux lines have been shifted. The magnetic compass' error can be corrected if the relationship between the compass and the metal remains constant.

One way to calibrate the magnetic compass is to use a gyro, which is not affected by metal. The gyroscope doesn't replace the compass because the gyro doesn't know which way north is; it just knows relative position. However, if the two devices are rotated together, the gyro's position output can be used to calculate an error correction for the magnetic compass.

## STANDALONE

The LCD is shown in Photo 1, and Photo 2 shows the elements of the gyro project. A 12-V 2.2 Ahr camcorder battery supplies plenty of operating time for the gyro. The largest current draw is from the gyro. Total draw is about 300 mA, with only about 1/10 needed for the interface circuitry, including the serial LCD.

| Value of Celsius temperature | Meaning of value | Actual temperature |
|---|---|---|
| 07FF | 127 × 0.05 | 102.35°C |
| 0001 | 1 × 0.05 | 0.005°C |
| 0000 | 0 × 0.05 | 0°C |
| 0FFF | –1 × 0.05 | –0.005°C |
| 0800 | –128 × 0.05 | –102.4°C |

**Table 4**—*The potential span exceeds the –40°C to 75°C maximum operating temperature.*

Drift after an initial warm-up period is measured at >200°/h (3.6°/min.). After the calibration routine is run, the drift is reduced to 4.4°/h, which is ±1 bit (1 bit × 0.0000915°/bit × 10 samples/s × 60 s/min. × 60 min./h).

As an added feature, I used the second LCD line to report temperature. This is the temperature of the gyro, not necessarily room temperature. In fact, it runs close to body temperature. An extra input bit allows this output to be optional by tying the input low to enable the second line.

As you can see in Figure 1, in addition to the serial LCD output (J2), there is a DB-9F serial output to a PC. This output is used for debugging purposes. Configuration jumpers CFG0–2 can be tied low to enable additional serial output. These jumpers allow different variables in the application (within various routines) to be displayed as verification that computations are being handled correctly.

You may not have a specific need to interface with a gyro. That's OK. This application serves as a perfect example of how to use what you have to get what you want. All it takes is a clear understanding of what the data parameters are, how you need to massage them, and what the limitations of the tools are.

At first glance, it looked as though floating point would be necessary to get reasonable results. Not only can the task be accomplished with integer-only arithmetic, but this task requires double-precision floating point to achieve the necessary accuracy (i.e., significant decimal places).

*Jeff Bachiochi (pronounced BAH-key-AH-key) is an electrical engineer on* Circuit Cellar*'s engineering staff. His background includes product design and manufacturing. He may be reached at jeff.bachiochi@circuitcellar.com.*

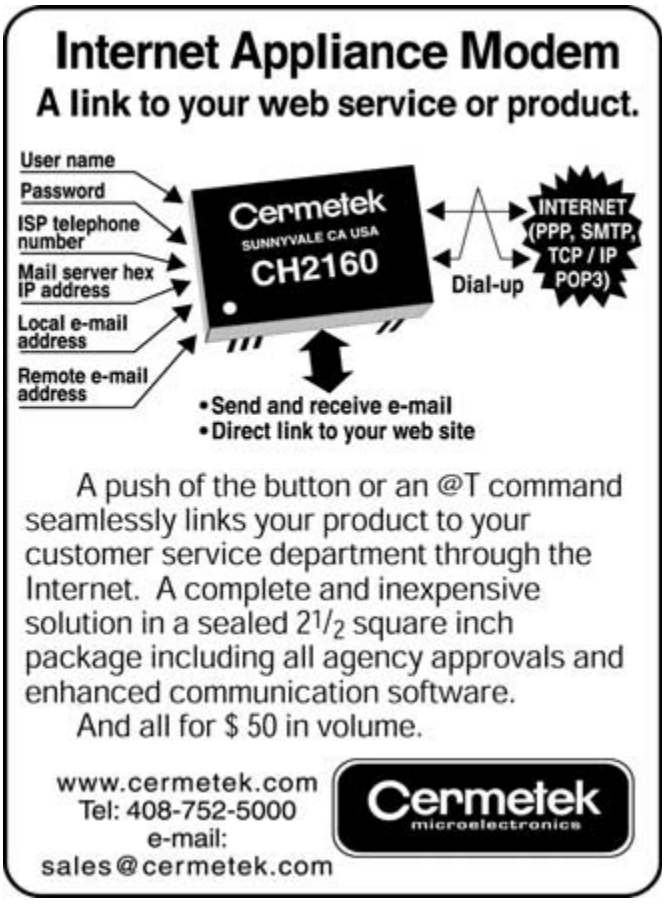
## SOURCES

**E-Core 2000 Fiber Optic Gyro**
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# SILICON UPDATE

**Tom Cantrell**

# Motor City MCU



As the importance of processing power extends beyond the world of the PC, the automotive industry is paying close attention to the shiny new racers rolling off the Silicon Valley production lines.

Detroit isn't the new hotbed of microchip design, yet in a sense it is, given the prodigious automotive appetite for silicon. It's only a matter of time before the mine's-bigger-than-yours bragging rights include MIPS along with horsepower and torque. Brains, not just brawn, will distinguish the luxury class from the slow-lane sitters.

As I said in "On the Road Again" (Circuit Cellar 118 and 119), networking is just as hot under the hood as it is on the desktop, maybe hotter because automotive networking (or multiplexing) is just hitting its stride.

It's not hard for computer types to understand the evolution of automotive electronics. As with computers, the first step was a centralized mainframe approach in which a single, expensive chip was put in charge of the most critical functions (e.g., engine control). Then, à la the minicomputers of yore, lower-cost chips became available, enabling department (e.g., brakes and transmission) level processing.

Today, thanks especially to highly capable, low-cost MCUs, cars have entered the equivalent of the PC age when practically every corner of the vehicle, like every desktop, is home to some silicon.

Now many desktops also sport networking gear like the Ethernet router and USB hub blinking happily on mine. It's not hard to guess where automotive electronics is headed.

## GETAWAY GATEWAY

The latest mobile MCU from Motorola hints at the shape of things to come. The MC9S12D lineup (see Figure 1) combines the latest 'HC12 CPU core with a rack's worth of networking (up to five CAN 2.0 ports and a J1850 port), a bunch of memory, and an everything-but-the-kitchen-sink collection of I/O.

Clearly the '9S12 is a natural for automotive apps. However, it also seems like a match for the broad-based applications that interest many designers. In particular, there are versions available with only a single CAN port and four different permutations of memory sizes (see Table 1).

Furthermore, CAN itself is also finding favor in industrial field bus applications, which share the real-time and reliability concerns of their road-going brethren.

Many of you can take advantage of the robustness demanded of automotive apps, extended temperature range (–40 to 125° C), full-on 5-V analog and digital I/O (an on-chip voltage regulator delivers the 2.5-V supply for the CPU core), and low power and noise (EMC). All the more impressive that the '9S12 takes a licking in low-cost plastic packages including 80- and 112-pin QFP initially (others between 44- and 144-pin to follow).

Or, if CAN or J1850 aren't your cup of tea, there are plenty of other bit-banging options on-chip including UART (two channels), SPI (up to three channels), and I²C.

Besides communication, on the control side of the equation the '9S12 is no slouch. Parts come with either one or two 10-bit, 100-kHz successive approximation ADCs, each fronted with eight channels via a multiplexer. The ADC includes internal or external triggering, signed or unsigned results, left- or right-justified results, and programmable multi-channel conversion sequences (or multiple conversions of a single channel).

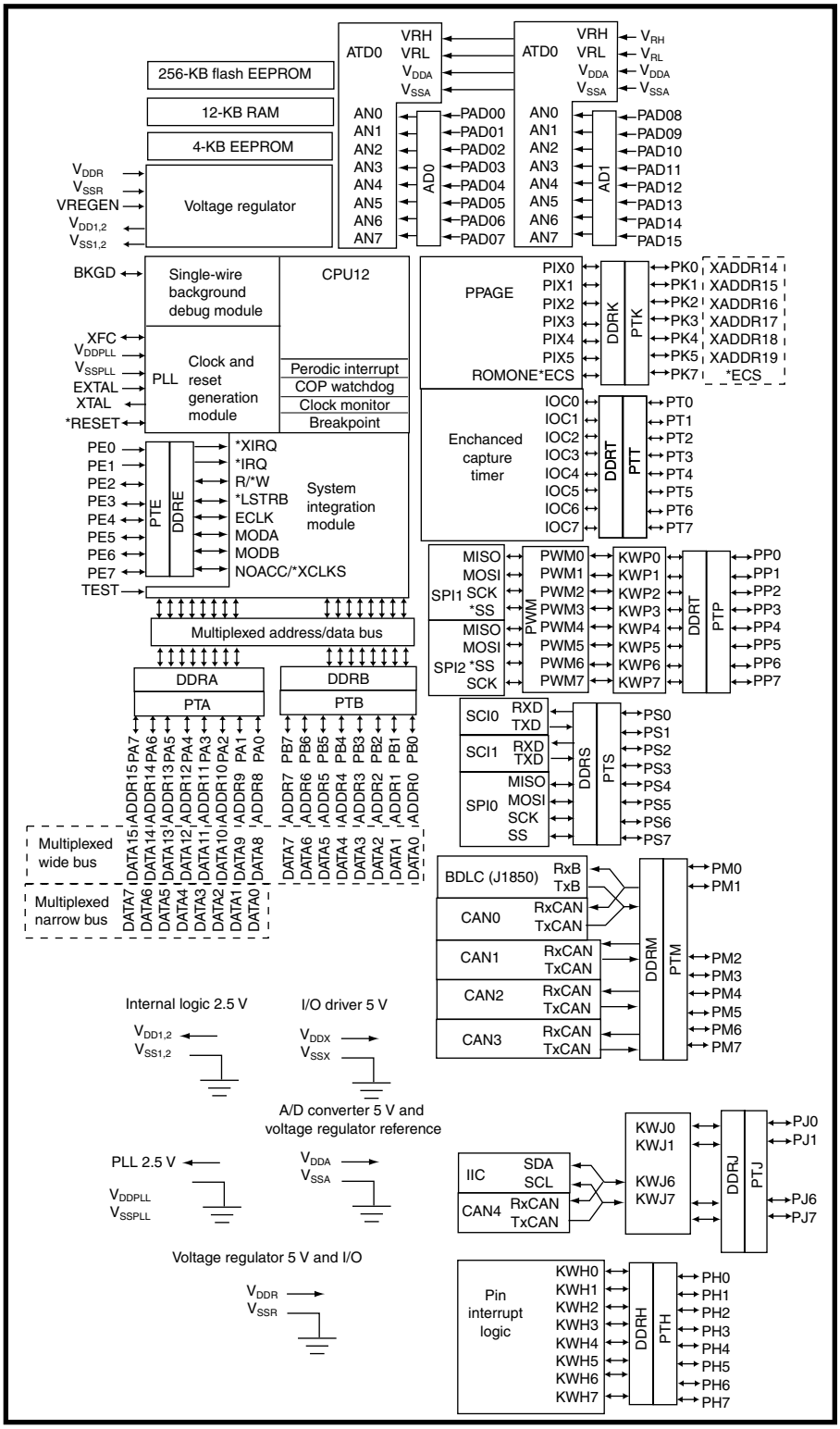



**Figure 1—***Although the '9S12 traces its roots back to Motorola's first micro, the circa 1970s '6800, it sure ain't your father's MCU.*

There are up to eight channels of PWM with 8-bit resolution that can alternatively be configured as four channels with 16-bit resolution. Double buffering solves the nuisance of PWM waveform glitches when the parameters are reprogrammed (i.e., changes are held off until the current cycle completes).

Finally, there's an enhanced capture timer (ECT) that, with 64 control registers and a 50-plus page datasheet, could easily consume an entire article by itself. It starts with a 16-bit counter and 7-bit prescaler, followed by eight programmable input capture or output compare channels and two 16-bit (alternately, four 8-bit) pulse accumulators. The input capture section features buffering for up to three captures, reducing the chance of overrun and offering the luxury of leisurely interrupt response.

With a 16-bit chip, you can access all the 16-bit counters in a single cycle without the freeze gyrations required of an 8-bit chip that can only read half at a time.

## 16-BITS OR BUST

The new STAR12 incarnation of the 'HC12 CPU is a full-fledged 16-bit core (actually a 20-bit ALU) that boasts high-speed (50 MHz yielding a 25-MHz bus cycle) and extended math (e.g., 16 × 16 bit multiply with 32-bit result). Yet it remains source code upward-compatible with the popular 8-bit 'HC11 predecessor that harkens back to the original '6800 of yore.

That's no mean feat, given that the opcode map has been reworked and many instructions and addressing modes have been added. For example, the 'HC11 treated index registers X and Y differently, imposing a one-cycle penalty on the latter. That penalty has been eliminated on the 'HC12. Going further, the 'HC12 allows the use of the SP and PC as index registers, offers accumulator (A, B, and D) and 5-, 9-, and 16-bit constant offsets, and adds pre- or post-increment or decrement by any value between –8 and 8. New LEA (load effective address) instructions for SP, X, and Y allow math operations directly on these index registers rather than having to move them into an accumulator.

Some of the trickiest challenges for an architecture upgrade revolve around the details of status flag and stack usage. For instance, the aforementioned LEA instruction is used to emulate the 'HC11's stack pointer increment and decrement instructions (i.e., 'HC11 DES becomes LEAS –1, S on the 'HC12). That's OK because neither instruction affects the flags. However, the similar increment and decrement instructions for X and Y

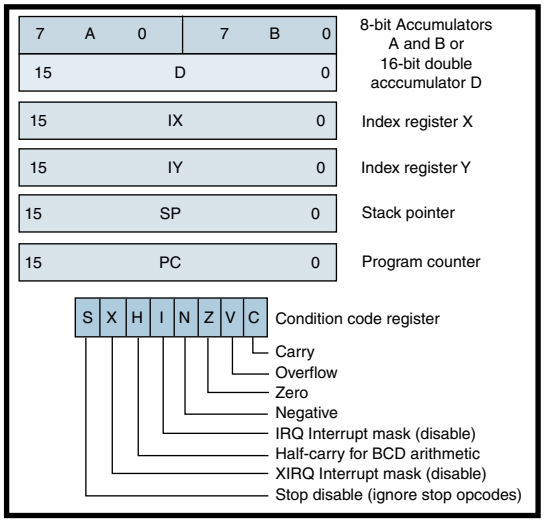



**Figure 2—***The programmer's model hasn't changed much (exactly the same as the 'HC11), but under the hood it's a different story.*

(INX, DEX, INY, DEY) on the 'HC11 do affect the status register (Z flag), so they are retained on the 'HC12 rather than emulated with LEA.

The 'HC12 programmer's model (see Figure 2) is the same as the 'HC11, including the nitty-gritty details, such as the way stuff gets stacked in response to an interrupt. One caveat, the 'HC11 stack pointer points to the next available location and the 'HC12 points to the last one used. That means for a given value in SP, the stack contents for the 'HC12 are located in memory one byte lower than the 'HC11. This would be an issue only for the rare (and generally discouraged) practice of accessing the stack via absolute addressing.

Another stack issue is alignment. As a 16-bit machine with nine bytes to stack and un-stack, there's no way to guarantee a particular alignment. This could cause the execution time of a 16-bit push or pull instruction to vary. Biting the bullet, Motorola designed the on-chip RAM to be able to deliver a 16-bit quantity in a single cycle regardless of the alignment, eliminating concern (as long as the stack is located on-chip).

Similarly, as long as programs are stored on-chip, instruction alignment of the variable length opcodes isn't a concern. Built-in queue logic includes a multiplexer that automatically prefetches and presents the next three instruction bytes to the CPU, independent of alignment.

## GONE IN 40 NS

One of the most noteworthy points about the new chip is performance. Motorola was competitive in the good old 1-MIPS days, but fell behind over the years as challengers introduced faster chips like the Scenix (recently re-christened as Ubicom) SX and Dallas Semiconductor's hyper '51s. For more information, take a look at two of my earlier articles, "Socket Rocket" (*Circuit Cellar* 100) and "'51 Soldiers On" (*Circuit Cellar* 127).

It's the usual recipe; reduce the number of clocks per instruction and speed up the clock rate. The STAR12 incarnation cuts the cycle count of many instructions by one or even two cycles, compared to the existing 'HC12 implementation. Again, in Single-Chip mode (i.e., on-chip access only), the clock runs up to 50 MHz, which translates to a 25-MHz bus speed for a 40-ns minimum instruction cycle. Not to worry, an on-chip PLL (see Figure 3) allows the use of a low-frequency (low-cost) crystal.

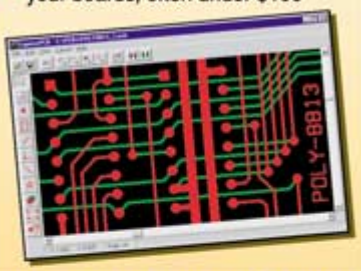
That doesn't mean the '9S12 is a 25-MIPS machine. Many of the simplest ALU and register ops execute in one cycle, but generally instructions take one to six cycles depending on their length (1 to 6 bytes) and the complexity of the addressing mode (i.e., number of memory accesses required). Branches, always a concern because of their high frequency, are three clocks if taken, one clock if not taken. The throughput for meat-and-potatoes code approaches 10 MIPs, which is quite competitive.

Remember, the 'HC12 is about as CISCy as they come, what with all kinds of fuzzy logic instructions, table

| Flash Memory | RAM | EEPROM | Package | Device | CAN | J1850 | SCI | SPI | IIC | A/D | PWM | I/O |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 256 KB | 12 KB | 4 KB | 112LQFP | DP256 | 5 | 0 | 2 | 3 | 1 | 2/16 | 8 | 39 |
| | | | | DQ256 | 4 | 0 | 2 | 3 | 1 | 2/16 | 8 | 41 |
| | | | | DT256 | 3 | 0 | 2 | 3 | 1 | 2/16 | 8 | 43 |
| | | | | DJ256 | 2 | 1 | 2 | 3 | 1 | 2/16 | 8 | 45 |
| | | | | DG256 | 2 | 0 | 2 | 3 | 1 | 2/16 | 8 | 45 |
| | | | 80QFP | DQ256 | 4 | 0 | 2 | 2 | 1 | 1/8 | 7 | 22 |
| | | | | DT256 | 3 | 0 | 2 | 2 | 1 | 1/8 | 7 | 24 |
| | | | | DJ256 | 2 | 1 | 2 | 2 | 1 | 1/8 | 7 | 26 |
| | | | | DG256 | 2 | 0 | 2 | 2 | 1 | 1/8 | 7 | 26 |
| 128 KB | 8 KB | 2 KB | 112LQFP | DT128 | 3 | 0 | 2 | 2 | 1 | 2/16 | 8 | 43 |
| | | | | DJ128 | 2 | 1 | 2 | 2 | 1 | 2/16 | 8 | 45 |
| | | | | DG128 | 2 | 0 | 2 | 2 | 1 | 2/16 | 8 | 45 |
| | | | 80QFP | DT128 | 3 | 0 | 2 | 2 | 1 | 1/8 | 7 | 24 |
| | | | | DJ128 | 2 | 1 | 2 | 2 | 1 | 1/8 | 7 | 26 |
| | | | | DG128 | 2 | 0 | 2 | 2 | 1 | 1/8 | 7 | 26 |
| 64 KB | 4 KB | 1 KB | 112LQFP | DJ64 | 1 | 1 | 2 | 1 | 1 | 2/16 | 8 | 45 |
| | | | | D64 | 1 | 0 | 2 | 1 | 1 | 2/16 | 8 | 47 |
| | | | 80QFP | DJ64 | 1 | 1 | 2 | 1 | 1 | 1/8 | 7 | 26 |
| | | | | D64 | 1 | 0 | 2 | 1 | 1 | 1/8 | 7 | 28 |
| 32 KB | 2 KB | 1 KB | 80QFP | D32 | 1 | 0 | 2 | 1 | 1 | 1/8 | 7 | 28 |

**Table 1—***A mix and match package, peripherals and memory yield quite a few permutations and, according to Motorola, that's only the start.*

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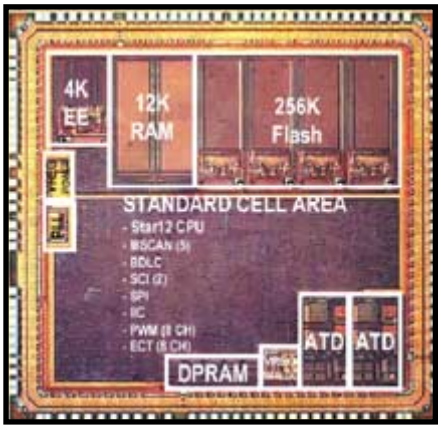



**Photo 1**—*Synthesis gets real and the '9S12 comes to life. One of the benefits is fabrication portability, as witnessed by the fact that initial production is coming from TSMC.*

interpolation, and so on. These instructions will boost apparent performance accordingly.

One place where the chip shines is in math class. As shown in Table 2, I'm talking about a real Poindexter here. Check out the multi-MIPS multiply and divide performance, an advantage over 8- and 16-bit MCUs.

## MORE FLASH, LESS CASH

When it comes to adopting the latest technology, automotive designers are held in check by strict reliability concerns and glacial production lead times. This makes the fact that the '9S12 is a flash memory-only part all the more striking. I'm not known for making understatements, so I'll simply say that the adoption of flash memory for workhorse automotive apps means that the party is officially over for ROM and OTP.

Like performance, flash memory was another area where the folks at Motorola fell behind. They had to scramble to make technology deals and ended up being late to market.

It's really no surprise that they didn't have an especially smooth start. For instance, the flash memory on the 'HC908 (see "Flash Forward," *Circuit Cellar* 104) was remarkably difficult to program. Software was sentenced to hard labor, tunneling the electrons shovel-by-shovel with excruciatingly precise timing, or else. Furthermore, thanks to all the bit-by-bit machinations, programming was slow. That's OK in the lab, but definitely a problem on the production line.

By contrast, for '9S12 programming, the main flash memory and secondary EEPROM (which are essentially the same except for erase granularity) is a simple three-step, address-data-command sequence. All the critical voltage control and timing is handled through built-in logic. Furthermore, programming is pretty speedy at only about 10 s for a 256-KB part.

Similarly, at $10 in volume for the high-end, 256-KB part, and with $3 projections for the lesser models, the price premium for flash memory over OTP is negligible now, and will continue to shrink.

The temptation to go beyond 64 KB for 16-bit chips is fraught with danger, especially when compatibility is a constraint. Indeed, I suspect it's the fact that Motorola's own 68HC16 designers got a little too fancy, straining compatibility with the 'HC11, which led to the popularity of the 'HC12 emergence as a 16-bit solution.

People had mixed feelings about "kludgy" segment register schemes 20 years ago, and the concept surely hasn't aged well. Instead, the '9S12 uses a simple paging approach in which a 16-KB portion of the address space acts as a fixed window into the larger flash memory array. If that doesn't cut it

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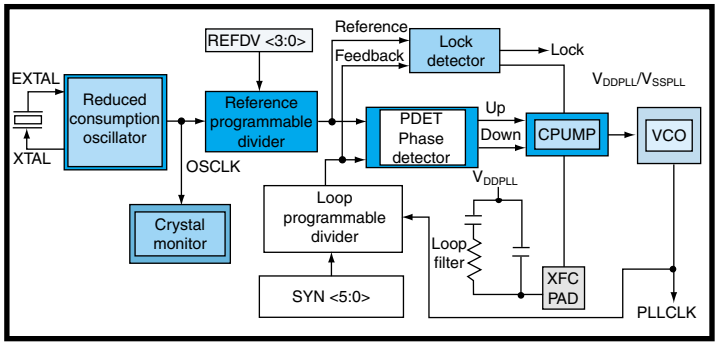



**Figure 3**—*Motorola was one of the first companies to incorporate PLLs in MCUs to address the need to extract more megahertz from low-cost, reliable crystals. The '9S12 keeps up with the latest trend with an on-chip oscillator to back up the external clock source.*

| Instruction mnemonic | Math operation | M68HC11 1 cycle = 250 ns | STAR12 1 cycle = 40 ns |
|---|---|---|---|
| MUL | 8 × 8 = 16 (signed) | 10 cycles | 1 cycle |
| EMUL | 16 × 16 = 32 (unsigned) | | 3 cycles |
| EMULS | 16 × 16 = 32 (signed) | | 3 cycles |
| IDIV | 16 ÷ 16 = 16 (unsigned) | 41 cycles | 12 cycles |
| FDIV | 16 ÷ 16 = 16 (fractional) | 41 cycles | 12 cycles |
| EDIV | 32 ÷ 16 = 16 (unsigned) | | 11 cycles |
| EDIVS | 32 ÷ 16 = 16 (signed) | | 12 cycles |
| IDIVS | 16 ÷ 16 = 16 (signed) | | 12 cycles |
| EMACS | 16 × 16 = 32 (signed MAC) | | 12 cycles per iteration |

**Table 2—***Ironically, the '9S12 is a true 25-MIPS machine when it comes to doing multiplications that are as fast as NOPs!*

for you, the answer is simple; quit messing around and go with a full-fledged 32-bit chip.

## REVERSE ENGINEERING

Just for kicks, I downloaded Motorola's application note, "Mask Set Errata 1: PC9S12DP256 Microcontroller Unit," which is applicable to mask OK36N. Whew, got all that? It's always a good idea to check this stuff out if you're working on the bleeding edge. Of course, a bug list is mandatory. There's no feeling worse than chasing after an unknown bug, only to find it wasn't unknown; kind of like making it to the North Pole "first" to glimpse someone else's flag flapping in the breeze when you finally get there.

Even if you're not in the development phase, a bug list allows you to get an idea of how real the part is. Are the bugs showstoppers or easy to work around? Are they related to features you do, don't, or may plan to use? Do they call for minor logic fixes or could things get really ugly?

Ironically, a bug list can also prompt thinking about interesting application tricks. By their very nature, many bugs relate to rarely used or less understood aspects of the device operation. That knowledge can yield valuable insights when it comes to milking all the functionality a chip has to offer or coming up with a clever design hack.

Anyway, returning to mask OK36N, I was taken aback by the quantity (more than 40) and severity of the bugs. Yes, a lot of them were simple gotchas (i.e., Port A and B have pull-down rather than pull-up resistors. Oops!), and most have a workaround of some sort. Others such as A/D accuracy out of spec indicate that they need more practice to get the recipe right. But, there were also some fundamental flaws, such as less-than-vigilant memory protection and security, that likely rule out this mask for production use.

I can understand such an extensive list for a newbie startup's first silicon, or a baroque 64-bit super-duper chip. But, Motorola is certainly no newcomer to MCUs, and even though the '9S12 has a lot of stuff, it's hardly rocket science.


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Technologic SYSTEMS

Following up on my curiosity, it turns out that the '9S12 may come with extra labor pain. It's Motorola's first MCU fully designed under a modern synthesis development regime. As Photo 1 shows, although the analog and memory portions are hard macros, every bit of the 1s and 0s stuff is implemented in HDL.

It's not hard to imagine why taking that first big step to synthesis could be shaky. It's one thing if you're starting with a clean slate, but the '9S12 didn't have that luxury because of the dictates of 'HC12 compatibility. In essence, Motorola's designers had to go through a reverse engineering process to translate the circuit-level design of earlier parts to functionally equivalent HDL.

As an analogy, I'd like to see someone try to convert a hex code listing to C and not end up with a lot of bugs! It's the same old story of a program (HDL) doing what you told it to do, only you didn't tell it quite right.

The good news is, after Motorola engineers get it straightened out, they'll be able to rationalize and build on an efficient IP-based design methodology. Instead of reinventing the wheel each time, Motorola will be able to cut and paste chips on a whim with less worry about top-to-bottom testing and new bugs every time.

## ROAD WARRIOR

The '9S12 was designed for automotive applications, but it won't hit the road for a couple of model years at least. Despite its roots, the chip will find a home in commercial and industrial applications long before that.

The biggest winner? That's the lucky designers who have access to parts that have progressed well in the relatively short era of silicon. Thanks to hot rod chips like the '9S12, the only limit is our imagination, which means there are no limits. Don't you just love this business?

*Tom Cantrell has been working on chip, board, and systems design and marketing for several years. You may reach him by e-mail at tom.cantrell@circuitcellar.com.*

## REFERENCE

[1] Motorola, Inc., "Mask Set Errata 1: PC9S12DP256 Microcontroller Unit," rev. 5, 0K36N, November 21, 2000.

## SOURCE

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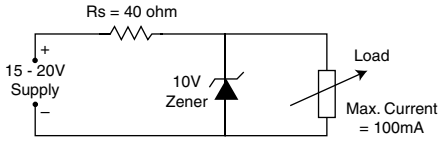
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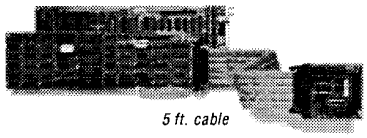
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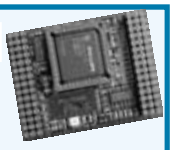
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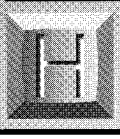
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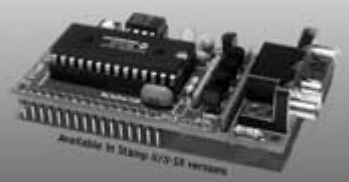
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   printf("press any key to begin\n\r");
   getc();
   printf("1 khz signal activated\n\r");
   while (TRUE) {
     output_high (pin_B0);
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     }
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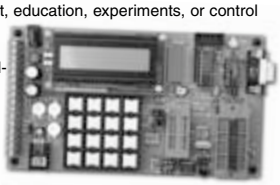
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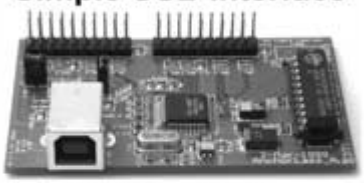
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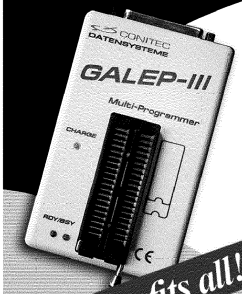


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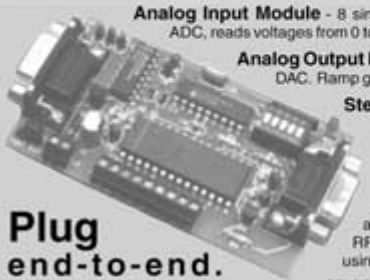
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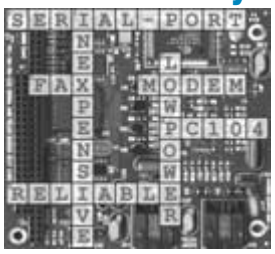



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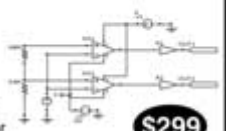
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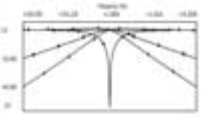
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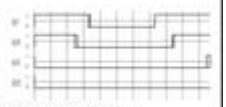


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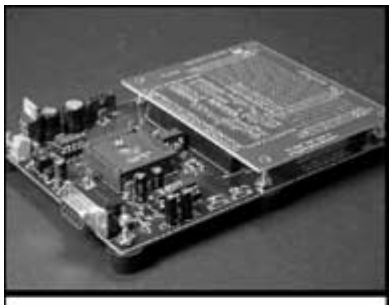
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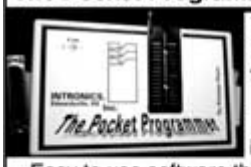
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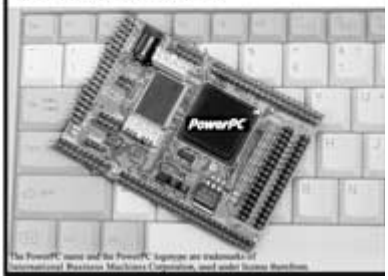
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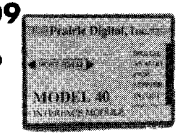


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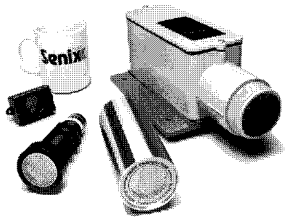
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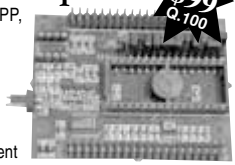

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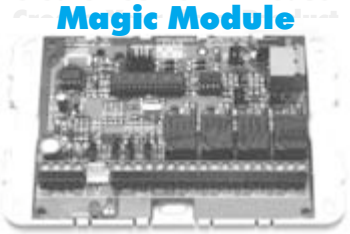
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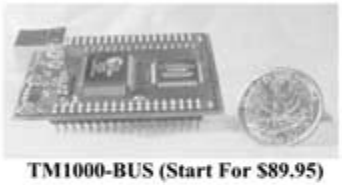
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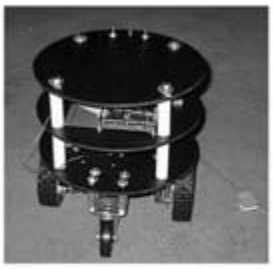
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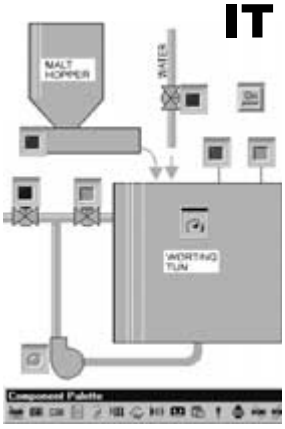
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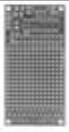
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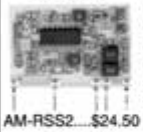



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The PC revolution is over. Well, not quite over, just on an indefinite vacation. P4s and PowerPC chips sit on shelves and the economy is headed for the toilet because we're just not buying as many PCs anymore. At least that's what you are led to believe if you pick up a newspaper these days. With the collapse of semiconductor company stock prices, increased layoffs, and all the dot-com bombs, what other conclusion can there be in our PC-centric culture?

Of course, in my experience reporters have never been particularly deep thinkers. They're entirely missing the fact that PCs are merely one facet, albeit significant, in our electronic evolution. Fifteen years of feverishly buying and upgrading PCs has left them with the perception (or should I say misperception?) that the business-justified growth of desktop PCs was an infinite market that has suddenly crashed. In my opinion, when you sell enough of any product to fill the customer demand, there is a natural decline in continuing sales growth. We're all just taking a little longer before upgrading these days and now there is more competition for how we use a PC. Today, we think about buying an e-book, MP3 player, or Internet message pad rather than trying to do everything through a desktop. Basically, these days we're thinking about distributing electronic requisites rather than concentrating them.

The real future growth for semiconductor companies is consumer electronics and embedded processing, not PCs. As much as Microsoft and Intel want the world to espouse their brand of electronic religion, sales of a hundred million cell phones and video games have more significance to bottom-line watchdogs.

Some companies have gotten the message. For example, IBM has evolved into a custom chip maker, designing custom ASICs for the likes of Ericsson and Cisco. More importantly, the PowerPC may get more market respect from being the brains in Nintendo's new GAMECUBE than it ever could hanging around Apple. Certainly it will be an adjustment in culture adapting to high volumes and lower profits in the consumer marketplace, but IBM has the right idea and the right direction.

Making the change might be a little harder for Intel. Approximately 80% of its revenue is derived from PC-oriented sales, so it's little wonder that their present attitude is to promote all these new electronic toys such as digital cameras, e-books, and the like as peripherals that still ultimately need a PC host. I beg to differ.

Over the years, we've had articles on wearable computers and discussed ubiquitous computing. Embarrassingly, I must admit that I held my nose during some of it because, at the time, I considered it to be fringe reality. Today, I have to say that I was too conservative and simply did not think far enough ahead. Ideas like having a bracelet that constantly transmits a child's GPS location or a front door video camera that automatically recognizes the home owner are not only conceptual, they are realizable.

If there is an understanding about our present predicament, it's that our PC mania has at least created a manufacturing infrastructure that easily adapts to and facilitates new applications. Combine this with the new wireless communication technology and you have the prime ingredients for a future of embedded-everything.

Computing in the future will not revolve around bigger processors and more centralized control. Forty million transistor P4s will still have their place of course, but the winners will be the companies who design new materials and computers so small and inexpensive that they can be incorporated into virtually anything. Concentrating on specific applications rather than generic processing capability will seem alien to old-line semiconductor houses, but they'll adapt. As for *Circuit Cellar*, we'll still be in the thick of things as usual. Our focus has always been embedded control by any name. Now at least I have the satisfaction that much more of the world agrees with me.



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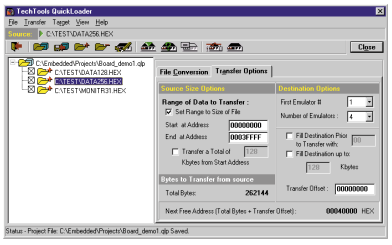



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