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THE COMPUTER APPLICATIONS JOURNAL

DATA ACQUISITION

Data Collection with the HP-48SX

Theory and Practice of CVSD Digital Speech

Embeddable RISC

The Firmware Development Board Begins to Take Shape

April 1993 — Issue #33



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EDITOR'S INK

Take Up a Collection

Living in what the "experts" call the Information Age, someone is always collecting data on something. Packed in that new toaster is a little postcard you're supposed to fill out and mail back to "register your warranty." What the number of people living in your house or the brand of underwear you prefer has to do with toaster warranties, I'll never know.

The tax man wants to know how much you earned last year. The credit card companies want to know how much your mortgage payment is while the mortgage company wants to know how much is on your credit card. The federal government wants to know how many people live in your house (for the census) and the local government wants to know how many rooms live in your house (for property assessments).

Just when you thought you could escape data collection by withdrawing into your own home, along comes version 2 of the HCS II and its data logging capabilities. Now you can even keep track of how long you spend in the bathroom!

On a somewhat smaller scale is our first project this month. Using the infrared communications capabilities of the popular HP-48SX calculator, the ADCM-48 I/O interface provides a very portable means of doing data acquisition and control in even the most inaccessible areas. John Wettroth gives a full accounting of his design process, so you can decide for yourself if he's met his goals.

Next, we look at data collection of a different sort: digitized speech. While most people are familiar with the more popular methods of speech storage and playback (such as PCM, ADPCM, or LPC), many haven't yet heard of CVSD. Let Jeff Schmoyer be your guide into the inner workings of CVSD, while Jim Hubert presents some practical hardware.

Our final feature is a continuation of William Von Novak's computer-controlled light dimming system from last month. This time, he discusses some of the more common dimmer circuits and describes the hardware and software of a complete, working system.

Kicking off our columns, Ed explores the timing of the ISA bus in detail and begins to piece together his Firmware Development board. For all you RISC junkies who haven't been able to use your favorite processor in your latest embedded project, Tom has some good news for you. The new AMD29205 looks to have a promising future in those embedded designs where 8 bits just won't do.

Jeff and John both build sample applications based around the displays they presented last month (LEDs for Jeff and vacuum fluorescent for John). Finally, Russ looks at several patent abstracts that look nearly identical, and among the inventions he highlights is a "device for transmitting sonic vibrations, such as music, to a fetus [through]...an abdominal belt...worn by the mother." Not to be missed!

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Cover Illustration by Bob Schuchman

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READER'S INK

OMISSION?

In reading your article "Temperature Monitoring" in the February 1993 issue, I noticed an omission which many readers may want to be aware of. I have used the LM34 for many jobs, however the output is not unconditionally stable when driving a capacitive load, such as a shielded twisted pair cable. This type of cable is often used to allow the LM34 to be placed far from receiving electronics. The capacitance of these cables can be up to 100 pF/ft between conductors.

Under this sort of load, the LM34 output begins to "lope" or "motorboat," usually manifested as a triangle wave added to the normal DC offset. It's hard to detect except as "noise" in the data or strange, cyclic variations of temperature at some frequency related to the sampling interval of the monitoring system.

The cure is to place a 1-5 kΩ resistor in series with the LM34 output as shown in the National Semiconductor application notes. This decouples the LM34 output from the load capacitance. For example, using a 2.2-kΩ, 5% resistor, I have been able to use a 25-foot cable without oscillations. The only caveat is that there will be a voltage-divider formed by the decoupling resistor and the input impedance of the monitoring system. Depending on the input impedance and bit resolution of the monitoring system, the effect may be negligible.

Thanks for another fine issue. I've been reading Circuit Cellar articles now for over ten years; each one's been a treat! Keep up the good work.

H. Ward Silver
Vashon Island, WA

We don't presume that Circuit Cellar readers take everything they read verbatim and jump off cliffs. Before applying a new *technology* or using a new *device,* we *expect that successful application includes consulting a data book for additional facts.*

Editorial policy aside, the cables on all of the LM34 probes I used were under 6 feet long and the outputs did not exhibit "motorboating," so *I overlooked the potential eccentricity in alternative operation, The facts you point out are better defined as professional experience. We try to include as much wisdom as possible in our presentations. Thanks for adding more.-Steve*

SAMPLE GAME

I recently read your editorial "The Sample Game" from issue #3 1. To paraphrase a punch line from one of our southern jokes, maybe you need to be dealing with a better class of folks. While I can empathize with some of your frustration, I can also make some recommendations.

My company is basically a one-man show. While I have some very good subcontractors, most of the real work that gets done falls on me. While involved on a project recently, I had to reengineer about 10 hours of work my so-called "engineer" had already done. Lacking both knowledge and information of some particular parts, I started making calls.

The first was to Digi-Key, and they were invaluable in helping me locate parts that would run at the speeds needed. Next, they were honest in that some of the questions were beyond the realm of what they could handle, but they gave me phone numbers of some manufacturers that might be able to help.

I called manufacturers "H," "T," and "S," all to no avail. Then I called National Semiconductor. When you are a multibillion dollar, multinational firm, it's reasonable to expect companies to be ecstatic when you condescend to call them. When you are "Micro Ventures" you usually are not treated the same. This concept holds true at National Semiconductor. They treat you better. I needed one of their reference books that five different vendors told me was out of print. The lady with whom I spoke assured me they were not, and I could get one free of charge in about a week from their California office. When I told her that time was of the essence, she Fed-Ex'd a copy she had on her desk that very day, telling me she fully understood that sometimes you just can't wait. Since then I have been trying to find her name so that I could write the president of National with my compliments.

As if that wasn't enough, once I had the reference book and solved one problem, another arose. I called National's tech support and was given more help and information than I could use. While I was still in a daze about the high level of service that had been afforded, the engineer in tech support actually followed up with a phone call to see how things were going. I told him that his parts were working fine, but I had an interface problem. Although the specific problem did not involve anything that National made, he had me describe the circuit and the problem. The next day he phoned me again and gave me not one, but two solutions, both of which he had checked on his circuit design/emulation software! If I were Bill Gates or Ross Perot, I wouldn't expect this level of help and dedication, but to be MGC Data Services, a "Micro Ventures" type firm, is beyond belief.

Since then, I have called Digi-Key numerous times and not once been asked how much I was spending

whenever I have needed their support department. Also, National Semiconductor has shipped numerous reference books from their literature department and I didn't have to pay freight. A commitment to customer relations at these two firms is not dead. It does not need to sink in at the top, but rather seems to emanate from there. Guess who's parts I will be buying and from where, whenever possible regardless of price?

Gerald J. **Nagy**
West Columbia, SC

IN THE EYE OF THE BEHOLDER

I am writing in response to the letter in the March 1993 issue of the ***Computer Applications Journal*** from Ronald Brown. I think many of us toy with the idea of mixing art with controller technology to form some kind of fantastic kinetic art object.

It occurs to me that this type of design experience becomes an exercise in packaging. I am not certain what Mr. Brown had in mind, but using a controller to move motors, blink lights, or even talk is pretty much a commonplace thing for controllers to do.

The trick is to decide what to move with these motors (for instance, do you motorize a mannequin?], how to use computer-controlled lights for theatric or artistic effects, or even using controller-based sensors so the artwork can sense when it is being viewed?

It seems that merging technology and art could create some very dynamic and enjoyable objects. These objects, should they become accepted, could certainly enhance the public and private spaces on our world. But I think the question really becomes one for the critics to decide: what applications of controller technology can be called art and which ones cannot be called art? I have seen many objects-de-engineering that gave me an impression that the engineer and the artist are one, but that is just my opinion. Still, I would urge Mr. Brown to follow his inspiration and mix these two worlds together. Only after the critics have something physical to talk about can they begin to argue the artistic merits of it.

Name and address
withheld on request

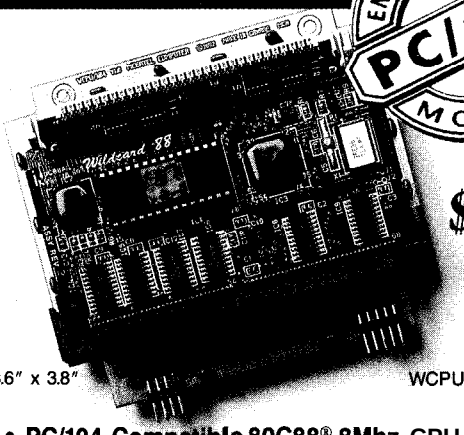
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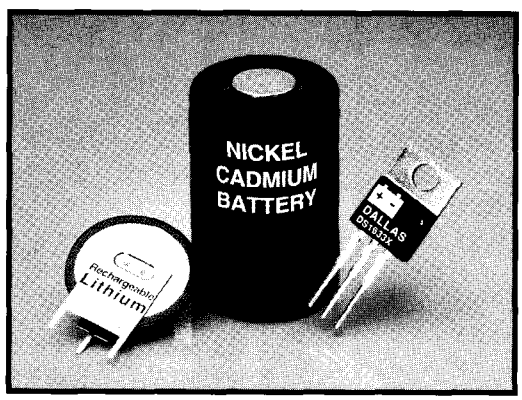
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NEW PRODUCT NEWS

Edited by Harv Weiner

SINGLE-CHIP BATTERY CHARGER

The DS1633 Battery Charger handles a variety of charging requirements without the need for external configuration components. Applications include cellular phones, portable computing systems, and portable instrumentation.



The DS1633 can be configured to charge a one- to three-cell NiCd battery pack or a single rechargeable 3-V lithium cell at a maximum current of 100 mA. Unlike existing battery chargers, the DS 1633 is "smart." It charges quickly but does not shorten battery life by overcharging. Upon power-up, the DS1633 charges the battery at maximum current until the specified cutoff voltage or charging time exceeds a preset limit.

The DS 1633 is programmable with three pins, and must be configured before use. Through the use of a one-wire serial interface, the DS 1633 requires only three connections: Vcc to its power supply, Vbat for the battery to be charged, and a ground connection. The battery pin is used as an output to the battery during charging and also serves as a connection that brings information into the chip during configuration.

Designers can use the DS1633 to meet the specifications of a particular battery pack by simply drawing a load line using a PC mouse and a software design tool supplied by Dallas Semiconductor. This software tool converts the load line to specifications for the charger and transfers them to the chip. Users can simulate the chargers first on the PC and then program the chip at a rate of 10 seconds per chip.

The DS1633 is programmed with a template of the kind of battery it is expected to charge. Characteristics such as maximum charging current, level of charging current with respect to battery voltage, maximum charging time, and level and frequency of trickle charge are all stored in an on-board EPROM. A time base that can be used to terminate standard charge at a user-defined length of time is also included on the chip. The chip also provides the ability to pulse trickle charge after the standard charge is complete.

The **DS1633K** Battery Charger Kit contains all the hardware and software needed to integrate the DS1633 into an application. The kit includes a programming module that connects to the serial port of a PC and does the level conversion and wave shaping necessary to program the device. Also included is an AC-DC adapter, cable, and connectors, four DS 1633s, software, and an instruction manual.

The DS1633 sells for $2.90 in quantities of 5000. The DS1633K sells for $100. Preprogrammed DS1633 chips are also available.

Dallas Semiconductor
4401 South Beltwood Pkwy.. Dallas, TX 75244
(214) 450-0448 . Fax: (214) 450-0470 **#500**

HIGH-SPEED MICROCONTROLLERS

The industry's highest speed 8-bit **80C5x** microcontrollers, operating to a clock rate of 42 MHz, are being offered by Matra MHS. Internally, these 8-bit CMOS microcontrollers are a fully static design, operating from DC to a maximum clock rate of 42 MHz over the full commercial temperature range.

The 80C32µ-42(ROMless)/80C52µ-42(8K ROM), and the 80C154µ-42(ROMless)/83C154µ-42(16K ROM) are both derivatives and upgrades to the 80C51. They are pin-for-pin replacements and fully hardware and software compatible with previous members of the family. The chips are available in 40-pin DIP, 44-pin PLCC, 44-pin PQFP, and the new, thin 44-pin SQFP package for PCMCIA applications.

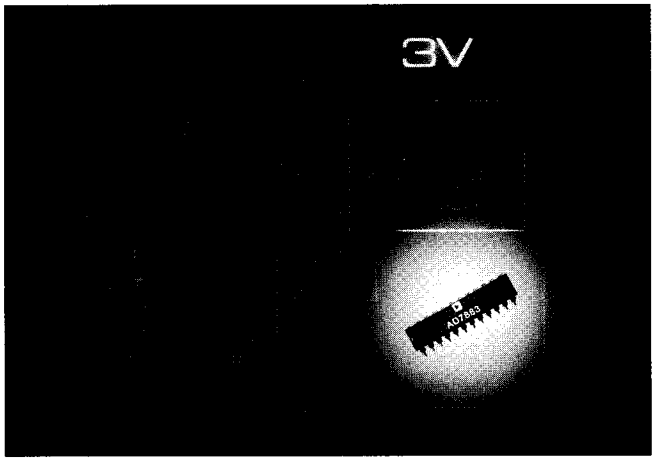
Both families of chips feature power control modes, 256 bytes of RAM, ROM as applicable, 32 programmable I/O lines, 64K of program memory space, and 64K of data memory space. They also feature a boolean processor, six interrupt sources, and a programmable serial port.

Typical applications for these high-speed microcontrollers are fast disk drives, printers, and high-speed modems.

The 80C32µ-42 and 80C52µ-42 microcontrollers sell for $9.25 and the 80C154µ-42 and 83C154µ-42 sell for $10.50 in OEM quantities.

Matra MHS Electronics Corp.
2201 Laurelwood Rd., MS #53 . Santa Clara, CA 95056-0951 • (408) 748-9362 . Fax: (408) 748-0439 **#501**

NEW PRODUCT NEWS



12-BIT SAMPLING A/D CONVERTER

Designed specifically for battery-operated, low-power applications, Analog Devices' **AD7883 12-bit sampling A/D converter** operates from a single supply between 3 V and 3.6 V, and consumes only 8 mW during normal operation. In addition, the AD7883 features a unique Power Save Mode, which reduces power consumption to only 1 mW. With a sampling frequency of 50 kHz and guaranteed AC and DC specifications, the AD7883 is an excellent match for laptop computers, telecommunications, industrial controls, sonar, and digital signal processing.

The AD7883 consists of a 5-µs track-and-hold amplifier, a 15-µs successive approximation A/D converter, interface logic, Power Save Mode circuitry, and a multiple input range circuit. When the reference voltage is derived from the power supply, the AD7883 becomes a complete 12-bit data acquisition system, with no external components required for operation. AC specifications include 69-dB minimum signal-to-noise ratio and –80-dB typical total harmonic distortion. DC specifications include ±2 LSB maximum integral nonlinearity and guaranteed no missing codes. An easy-to-use parallel digital output is compatible with most microprocessors and digital signal processors.

The AD7883 12-bit, 3-V, sampling A/D converter is available specified over the extended industrial (–400 to +85°C) temperature range and packaged in a 24-pin plastic DIP or SOIC. Pricing begins at **$14.00**.

Analog Devices, Inc.
181 Ballardvale St.
Wilmington, MA 01887
(617) 937-1428
Fax: (617) 821-4273

#502

DATA ACQUISITION BOARD FEATURES THERMOCOUPLE INTERFACE

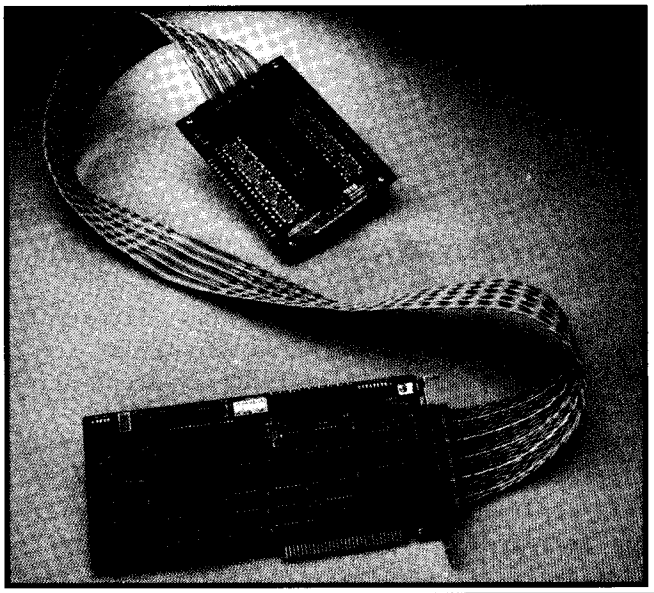
Real Time Devices Inc. has released two products to facilitate collection of thermal data: the **ADA520 PC bus analog I/O board** and the **TS16 16-channel thermocouple interface**. The ADA520 features 13-bit (12-bit plus sign) A/D conversion; 8 differential/16 single-ended high-impedance analog inputs; programmable gains of 1, 10, 100, and 1000; two 12-bit analog outputs; three timer/counters; and 32 buffered digital I/O lines. Using a dual-slope integrating ADC, the ADA520 converts signals at 30 samples per second to ensure rejection of 60-Hz noise.

The ADA520 is designed for use in applications requiring the measurement of low-level signals in noisy environments as well as in chromatography, industrial and laboratory automation, sensor interfacing, and temperature measurement. The ADA520 can be operated in either polled or interrupt A/D conversion modes. The base I/O address and interrupts are jumper selectable.

The TS16 thermocouple signal conditioner connects directly to the ADA520. It conditions and multiplexes 16 thermocouples into a single analog input channel, and provides low-pass filtering, amplification, and cold-junction compensation for J- and K-type thermocouples. The TS16 uses the Analog Devices AD594/595 thermocouple chip for amplification and cold-junction compensation supporting the temperature range of –200 to 1000°C. Input return grounding for each thermocouple is jumper selectable.

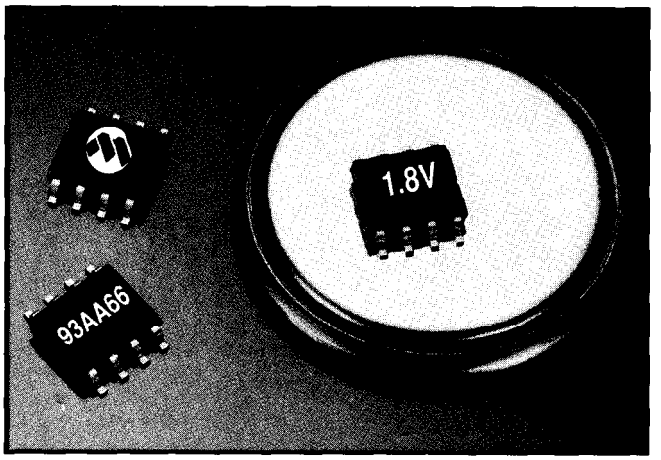
The ADA520 sells for **$395** and the TS16 for **$298**.

Real Time Devices, Inc.
820 North University Dr. • State College, PA 16804-0906
(814) 234-8087 • Fax: (814) 234-5218 **#503**



NEW PRODUCT NEWS

1 .&VOLT SERIAL EEPROMS

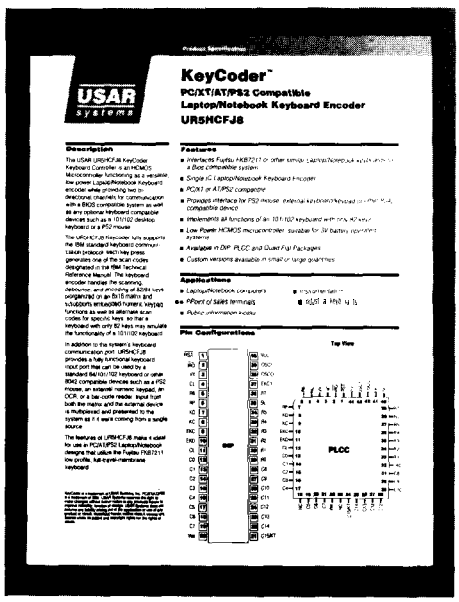


Three members of a family of 1.8-V serial EEPROMs have been announced by Microchip Technology. The **93AA46, 93AA56, and 93AA66** can be used through the entire operating life of two AA batteries, and will be a valuable resource for many portable and hand-held battery-powered embedded control applications as well as for remote battery-operated devices.

The new Serial EEPROMs can operate (both read and write) down to the cutoff voltage of two batteries, so the user gets the most life out of the batteries. This enables more devices to be attached to the batteries, more user features, longer product life, and reduced battery power (thus reducing system cost, size, and weight).

All of the new devices will meet an endurance and retention standard of 1 million erase/write cycles typical, and 40 years data retention. The chips are offered in SOIC and DIP packaging. One-hundred-piece pricing for the units is as follows: 93AA46 $1.35, 93AA56 $1.95, and 93AA66 $2.78.

Microchip Technology, Inc.
2355 West Chandler Blvd. . Chandler, AZ 85224-6199 • (602) 786-7200 • Fax: (602) 899-9210 **#504**



KEYBOARD ENCODER TECHNICAL BROCHURE

A new, comprehensive 16-page technical brochure entitled **"Keycoder Laptop/ Notebook Keyboard Encoders"** is available from USAR Systems Inc. The brochure provides descriptions and specifications for USAR's UR5HCFJ8 series of keyboard controllers in an easy-to-read format for design engineers and others seeking to interface Fujitsu FKB7211 or similar Laptop/ Notebook keyboards to a BIOS-compatible system.

The USAR UR5HCFJ8 Keycoder keyboard controller is an HCMOS microcontroller functioning as a versatile low-power keyboard encoder while providing two bidirectional channels for communications with a BIOS-compatible system, as well as a 101-/102-key desktop keyboard or PS/2 mouse.

Complete pin descriptions are provided for the three basic packages. A functional diagram shows interconnections and functions, and other topics, such as Mode Control, PC Communications, and 8042 Emulation Control, are carefully described.

To demonstrate how the keyboard encoder implements various keyboard layouts, four different arrangements are presented in an easy-to-understand graphic format. Also provided is a comprehensive list of the scan codes associated with each key, as well as complete electrical specifications.

The brochure is appropriate for design engineers and others seeking keyboard controllers for various applications including laptop/ notebook computers, point-of-sale terminals, public information kiosks, instrumentation, industrial keyboards, and others.

The 16-page keyboard encoder brochure is free.

USAR Systems, Inc.
Customer Support
568 Broadway, Ste. 405
New York, NY 10012
(212) 226-2042
Fax: (212) 226-3215

#505

NEW PRODUCT NEWS

DIGITAL DATA RADIO TRANSCEIVER

A complete two-way radio that can be used for short-distance wireless transmission of digital data has been announced by Kiefer Electronic Development. The TR-1 can transmit up to 50 feet indoors or 200 feet outdoors at data rates from DC to 2400 bps.

The TR-1 is a UHF transceiver operating in the 902–92%MHz band. Its power consumption is only 25 mA at 5 V and is just 1.8" x 2.2" x 0.7" in size. An 8-cm monopole antenna is supplied. The transceiver provides simplex operation, and several transceivers may listen to one unit sending in a broadcast mode. For example, several B-type units might simultaneously listen to data sent from one A-type unit.

In a typical application, the transceiver is connected to an RS-232 interface chip, or data is supplied directly from the port of a microprocessor. Digital data of any duty cycle may be transmitted, and the received data is of the same polarity as the transmitted data. Applications include remote data acquisition systems, process control monitoring, low-power security systems, wireless mouse, and computer-to-computer communications.

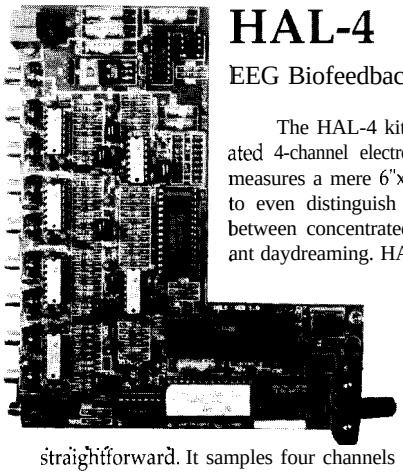
The TR-1 is FCC part 15 certifiable and easy to incorporate into a design. The small printed circuit board has a very low profile with surface mount components on one side and through-hole components on the other. Interface connections are through a 10-pin ribbon cable connector.

The TR-1 sells for $160 in single quantities.

Kiefer Electronic Development
1727 Hawthorn Pl.
Boulder, CO 80304
(303) 444-2535
Fax: (303) 444-7709

#506

CIRCUIT CELLAR KITS



HAL-4

EEG Biofeedback Brainwave Analyzer

The HAL-4 kit is a complete battery-operated 4-channel electroencephalograph (EEG) which measures a mere 6"x7". HAL is sensitive enough to even distinguish different conscious states—between concentrated mental activity and pleasant daydreaming. HAL gathers all relevent alpha, beta, and theta brainwave signals within the range of 4-20 Hz and presents it in a serial digitized format that can be easily recorded or analyzed.

HAL's operation is straightforward. It samples four channels of analog brainwave data 64 times per second and transmits this digitized data serially to a PC at 4800 bps. There, using a Fast Fourier Transform to determine frequency, amplitude, and phase components, the results are graphically displayed in real time for each side of the brain.

HAL-4 kit.. .....**$179.00** plus shipping

• The Circuit Cellar Hemispheric Activation Level detector is presented as an engineering example of the design techniques used in acquiring brainwave signals. This Hemispheric Activation Level detector is not a medically approved device, no medical claims are made for this device, and ii should not be used for medical diagnostic purposes Furthermore, safe use requires that HAL be battery operated only!

Sonar Ranging Experimenter's Kit
Targeting ◆ Ranging ◆ Machine Vision

The Circuit Cellar TI01 Ultrasonic Sonar Ranger is based on the sonar ranging circuitry from the Polaroid SX-70 camera system. The TI01 and the original SX-70 have similar performance but the TI01 Sonar Ranger requires far less support circuitry and interface hardware.

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#104

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The **PCI-20377W-1 data acquisition board** includes 16 single-ended or 8 differential analog input channels with 12-bit resolution; 45-kHz throughput rate; programmable gains of 1, 10, 100, and 200; and 16 protected digital I/O channels. The board also includes a rate generator, two 16-bit counters, DMA support, a sequential channel scanner, and separate digital and analog connectors for low noise.

User-selectable configuration features such as gain, signal range, and single-ended / differential modes are software controlled. Users can select one of eight different signal ranges from O-10 V to ±0.025 V full scale.

Master Link Software Libraries for both the DOS and Windows environments are included at no extra charge. These libraries support QuickBASIC, C, Turbo Pascal, and nearly all of the PCI products. A SYSCHECK system assurance utility is also included.

To simplify the selection of termination panels and cables for the board, a 3U-size **Euro-Style Termination Panel Starter Kit,** PCI20377T-1 **is also offered.** The Starter Kit includes an analog and digital termination panel, and an analog and digital cable.

The PCI-20377W-1 Low-Power Multifunction Board sells for $495. The Starter Kit sells for $249.

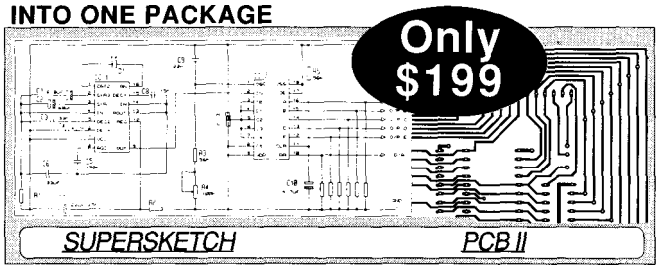
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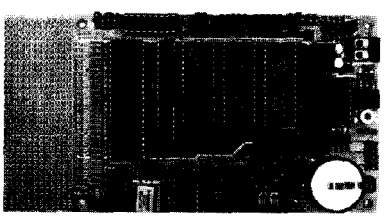
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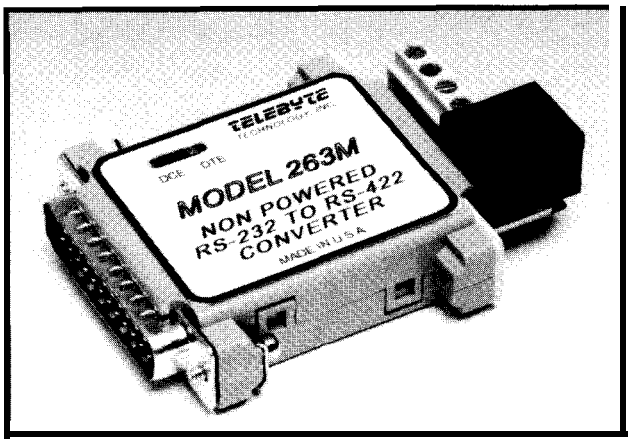
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The Model 263 can be used in DTE or DCE configurations by using the DTE/DCE switch, which reverses pins 2 and 3 of the RS-232 connector. The Transmit Data input to the Model 263 is used as the source of power. Special circuitry develops the operating voltages required by the unit from the applied Transmit Data signal.

The Model 263 operates over a temperature range of 0 to 50°C and has a calculated MTBF of 360,000 hours. The unit is packaged in a small plastic case measuring 2" x 2.75" x 0.75".



The Model 263 Interface Converter sells for $89.

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#108

FEATURES

14 Data Acquisition and Control with the HP-48SX

20 What Makes CVSD Tick?

24 Generate Digital Speech Using CVSD

32 Computer-controlled Light Dimmers: Part 2

Data Acquisition and Control with the H P-48SX

Hewlett Packard's HP-48SX calculator is not only a powerful mathematical computation device, but it makes an excellent platform for portable data acqusition when used with John's ADCM-48 interface.

FEATURE ARTICLE

John **Wettroth**

Hewlett Packard's newest high-end calculator, the HP-48SX, is a device that I've found to have great functionality as well as excellent mathematical computation and graphics abilities. It is fully programmable in a language that lies somewhere between Forth, LISP, and assembly. The HP-48SX's hardware capabilities are extremely flexible considering its size. It includes an RS-232 serial link with built-in Kermit protocol, a real-time clock capable of waking the unit up to run a program unassisted, 32K of RAM that is expandable to 256K, and a bidirectional infrared link.

An HP-48SX and a suitable interface device to get data into the calculator would make building prototype data acquisition systems or simple automated controllers possible without having to build a controller from scratch every time. You would simply prototype your front-end and possibly back-end hardware, hook it up to the interface, write a bit of code on your calculator, and-voila-a portable prototype that you can get some information out of before you build a hard prototype.

The following describes the specification and design of a commercial data acquisition and digital I/O module for the HP-48 called the ADCM-48.

HOW IT ALL STARTED

The idea for the controller came from a digital compass that used a flux-gate sensor, which I was working on as a Circuit Cellar Design Contest entry. After a bit of amplifying and

rectifying, a flux-gate sensor produces two quadrature signals. One represents the sine of the direction the compass is pointing and the other represents the cosine. Signal amplitude varies with strength of the earth's magnetic field, so the arctangent of the ratio is generally the most reliable measure.

My experimentation consisted of two digital voltmeters and my new HP-48 with a program I had written to crunch the trig and display the results. This arrangement was tedious to say the least, considering a dime store compass reads out in real time. What I had created was a compass that might fit in my kids' wagon that took an engineering degree to operate!

The next step in my development was to make it portable for field testing. I connected the two quadrature signals to a little 8052 BASIC board I had built a few years back, programmed it to do the trig, and then passed the values to the calculator over its RS-232 link for display and logging. I now had a relatively portable system that was fairly solid. Around this time, I realized that my BASIC board was acting as a little data acquisition front end for the calculator, ending my compass experimentation. All hopes of defending my title in the cost-effective category of the design contest disappeared.

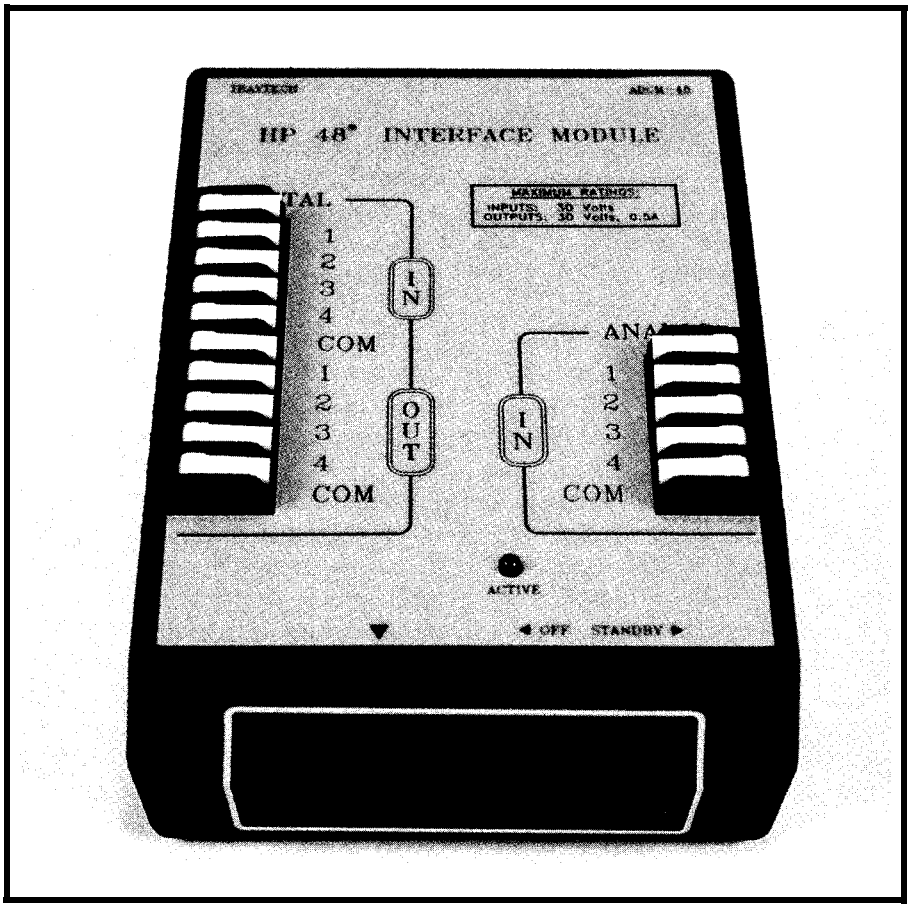


Photo I--The *ADCM-48* is a simple *but rugged* **portable** data acquisition *interface for the HP-48SX.*

THE "ADCM-48" INTERFACE IDEA TAKES OVER!

The first couple steps made when developing a product is figuring out what the widget needs to do and how much it should cost. I set a design-to-cost goal of $200 retail, estimating a bill-of-materials cost of less than $50. The next step was to determine what the calculator should be capable of doing. My method of attack was to figure out which application problems I would like to apply it to and what capabilities they would require.

The applications that made sense were slow- to medium-speed tasks with some degree of computation and a bit of control. A short list of applications includes:

- The Computing Voltmeter: essentially the flux-gate compass system. It should take in one or more voltages and then scale, massage, display, and store them if possible.

•The Data Logger: take in one or more analog, digital, or both kinds of inputs at regular intervals and store them for later analysis or graphing. The clock in the calculator could even be used to make a data logger that sleeps for hours or days between data points if the interface includes a sleep mode as well.

•The Bang Bang Controller: controls one or more high-current digital outputs to sequence relays or drive stepper motors. This capability also leads to inductive-load-protected outputs and an isolated communication link with the HP-48.

*Events Counter: count pulses on a digital input. The calculator would start, stop, and reset this counter.

THE CAPABILITIES LIST

These applications led to a list of capabilities that I felt the interface needed to provide. I compiled them through a process of refinement, redesign, and value engineering. During this iterative process, the capabilities list would grow, then shrink when I tried to figure out how to realize them in cost-effective hardware. A reasonable list of capabilities emerged after a few cycles of cost-limited brainstorming, such as:

*Communication with the calculator over the IR link for convenience and isolation

- IOO-hour battery life with a 9-volt battery and on/off control from the calculator

*Four 0- to 5-volt high-impedance analog inputs that would be converted to 8-bit accuracy

*Four TTL-/CMOS-compatible digital inputs with internal pull-ups

*Four OS-amp high-current digital outputs

•One counter input capable of 100-kHz rate and 24-bit total counts

•One 8-bit pulse-width modulator

PROBLEMS AND CHALLENGES IN THE DESIGN

This design gave me my share of headaches. The one design constraint

that proved to be the most challenging was the cost goal. The cost entered into every single decision made for the system. The system had to do a job but it would be useless if it cost more than people were willing to pay. The result is shown in Figure 1.

Processor Selection

The system needed some sort of processor in order to take commands from the calculator over the IR link, decode these commands, and return responses. I wanted a processor with lots of on-chip resources, especially an ADC to keep costs low and parts count down. I looked at the Motorola 68HC11, and several from Signetics, before I finally settled on a Signetics 8051 derivative packaged in a 28-pin DIP called the 87C752. It includes an on-board five-channel ADC, a pulse-width modulator, counter, and 2K of EPROM for less than $20. Four of the five ADC channels are used for external inputs, with the fifth used for internal battery condition monitoring. The two limitations to this part are a 2K nonexpandable code limitation and no on-board UART. These limitations both proved to be minimal.

The IR Transceiver Circuit and Power Circuits

The HP-48 infrared calculator-to-calculator protocol is a short-range link (2 inches) with a fixed speed of 2400 bps with no parity. It is similar to a normal UART output except that zeros are sent as very brief (52-µs) pulses to conserve power.

One design issue for the receiver was very low standby current because the calculator had to have the capability of turning the interface on over the link. Another issue was controlling ambient light swamping of the receiver in sunlight. I solved these problems with a low-cost infrared filtered photodiode and a single-transistor amplifier followed by a Schmitt trigger. I handle ambient light swamping by keeping the DC gain low and applying gain only to the AC signal. A set-reset flip-flop handles the power on and off by driving a PNP high-side switch as shown in the schematic. The transmitter was nearly trivial due to the limited range, and consisted of just an IR LED, resistor, and drive transistor.

Analog Inputs

The analog inputs have some special problems associated with them. The ADC does not have a particularly high input impedance, and the need for input protection led to op-amp followers on the inputs. The inputs also need to go to ground to measure the O-S-volt range. In my effort to keep costs low, I didn't want to add the parts and complexities associated with generating a negative supply. As a result, I then needed an op-amp follower with an output voltage swing and input common mode range that includes ground. My favorite general-purpose op-amp, the LM324, can't swing all the way to ground on its outputs. After a lot of searching, the Texas Instruments TLC27M4 arose as the perfect candidate. It's a quad part with good offset

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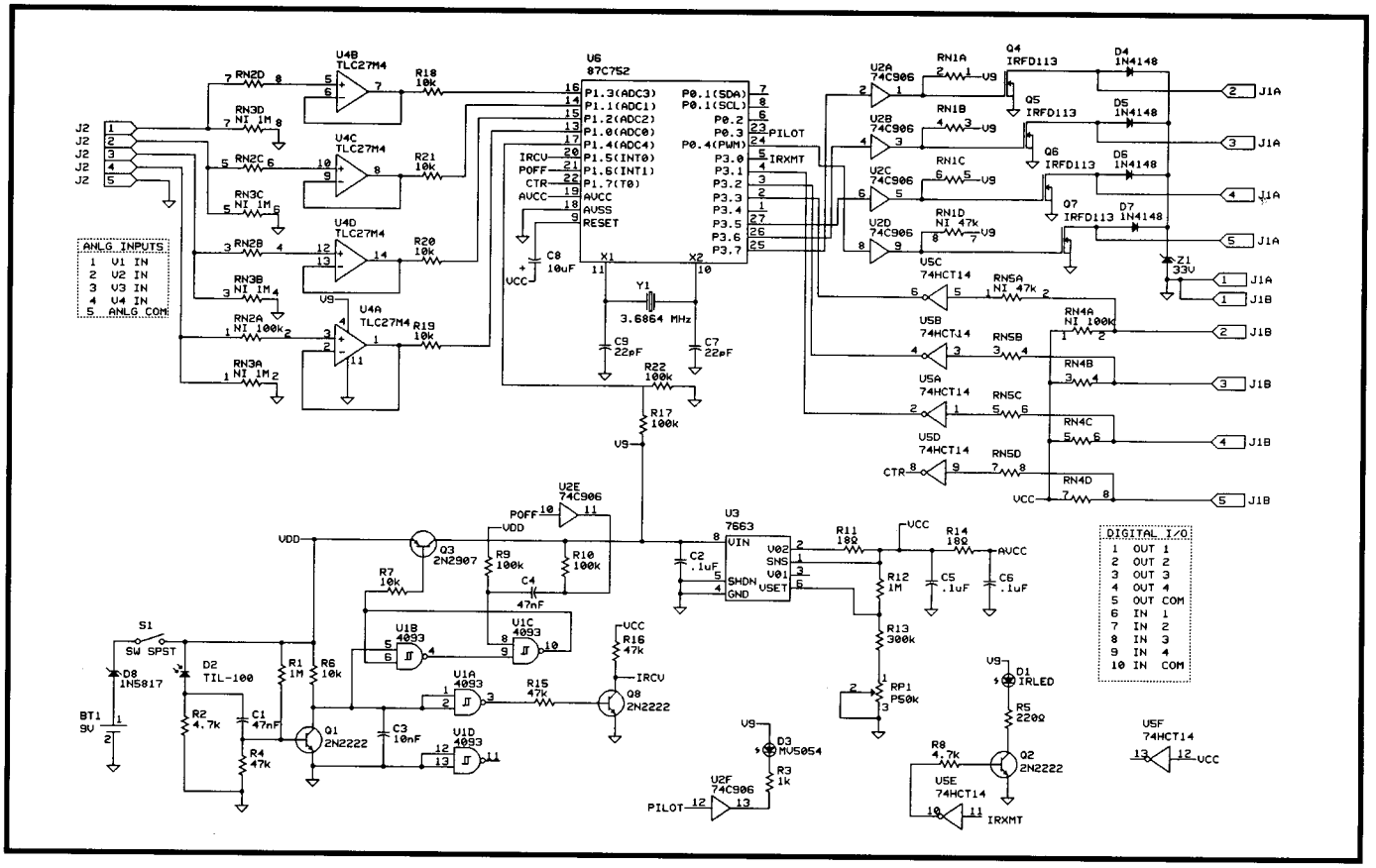


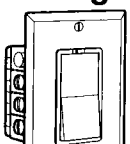
Figure 1—*Based on the 87C752 with built-in A/D converter, the ADCM-48 communicates with the HP-48SX using the calculator's two-way infrared interface.*

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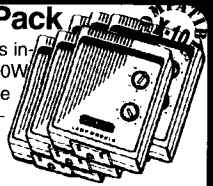


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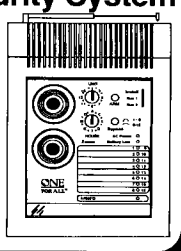


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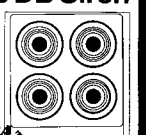
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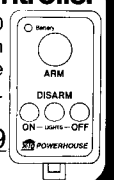
Powerhorn Remote 110 DB Siren



For use with Supervised Security System (left). Can also trigerred by the PowerFlash module (below left) or any X-10 "On-Off-On" sequence. Off-white. By Schlage. HCC-508X

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HOME CONTROL CONCEPTS

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and drift performance and is fairly cheap. As you can see in the schematic, the positive supply is the switched 9-volt battery and the negative supply is ground. The input protection network protects the inputs against fault to 30 volts conservatively and provides an input impedance of 1 megohm. This input impedance could be extended to 10 megohms with only a resistor change. The only tradeoff would be increased noise pickup on unused analog inputs.

Digital Inputs

The digital inputs were relatively simple. Protect the processor from voltage faults, provide pull-ups for the simple interfacing of switches, and provide Schmitt triggers for slow-rising signals. I met these criteria with a simple 74HC14 Schmitt trigger and a handful of resistors.

Digital Outputs

The digital outputs had to provide high current and avoid drawing large amounts of power from the interface. These requirements led to a open-collector-type configuration with inductive load protection. Darlington transistors appeared reasonable at first, but proved unworkable due to their V,. saturation voltage of about 1 volt. This value would limit the outputs to sources over one volt. Packaged driver chips were also unacceptable because of their high quiescent current demands and even higher "on" currents. The final output design uses low-cost n-channel power MOSFETs driven with battery voltage by open-collector drivers for a hard turn-on. The outputs also include an unusual clamp circuit that clamps the outputs against a 33-volt zener. This configuration is necessary because the upper supply rail is not available as is usually the case. The final circuit draws almost no current and can drive large inductive loads, including stepper motors.

Packaging

The packaging was a formidable problem. Probably because I'm an electrical engineer but also because packaging is something very sensitive to the quantity of products produced. The final packaging is simple and rugged. An off-the-shelf enclosure with a Y-volt battery compartment is the basic packaging. An inverted PC board inside carries all the components, with the connectors mounted on its back side. A tough, polycarbonate overlay provides front-panel legends and hides board-mounting hardware, and an off-the-shelf bezel makes a front window for the IR link.

CONCLUSION

The HP-48SX is an excellent platform for portable data acquisition, control, and portable equipment application prototyping. The ADCM-48 is a well-engineered, portable interface that brings low-cost interfacing capabilities to this machine. With an ADCM-48 and HP-48SX, you can control the world!

John Wettroth ***is the Chief Engineer of Science Applications Military Products Division in San Diego,*** *Calif.* ***He also owns Travtech, a sole proprietorship involved in electronic instrumentation development and HP-48 calculator data acquisition.***

SOURCE

The ADCM-48 is available fully assembled and tested with a manual, disk of HP-48 programs, and a 90-day warranty for $250. It is also available as a partial kit, which includes a professional-quality PC board, special switches and connectors, a preprogrammed 87C752 controller, a complete bound manual, and a disk of HP-48 programs for $150 (packaging not included) from

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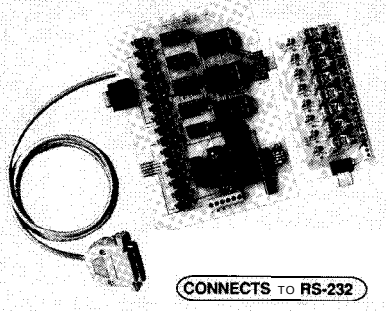
(Firmware is available from the same source on request to those who build the ADCM-48 from scratch.)

I R S

401 Very Useful
402 Moderately Useful
403 Not Useful

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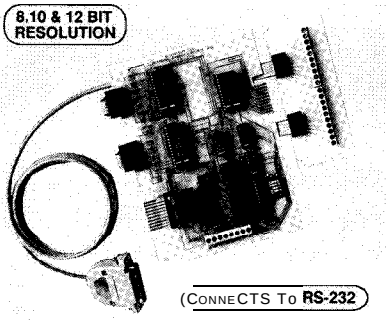


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#112

What Makes CVSD Tick?

FEATURE ARTICLE

Jeff Schmoyer

The quest for a better mousetrap is never ending. Just as you become comfortable with PCM, ADPCM, and LPC, along comes a new method for storing digitized speech. Find out what makes CVSD different.

Digital sound is going great guns these days. Applications entailing various sample rates, data resolution, and compression schemes abound. Most of you are probably familiar with PCM (pulse code modulation) and ADPCM (adaptive PCM) techniques for storing digital sound since these are the most popular, being used by most PC sound cards, Windows .WAV files, Macintosh sound files, and even CD players. A more novel method with some interesting advantages is known as CVSD modulation.

CVSD stands for Continuously Variable Slope Delta modulation, a mouthful to say and just as hard to remember. 1'11 first contrast some of the numerical differences between PCM and CVSD, then I'll look at what makes CVSD worthwhile.

Most PCM schemes use 8 to **16** bits of storage per sample clock. ADPCM compresses those required storage bits to varying degrees. CVSD uses one bit of storage per sample clock. PCM generally uses a sample rate between 8 and 44.1 kHz. CVSD commonly uses 32 kHz and above for sample rates.

The amount of storage required to record a PCM sample at an 8-kHz sample rate and 8-bit resolution is 64 kilobits for each second of the sample. Sixteen-bit PCM samples at 44.1 kHz jump to roughly 705 kilobits per second (multiply that by two if you want stereo sound). On the other hand, each second of 32-kHz CVSD sampled sound uses 32 kilobits of storage.

You can see the first benefit: CVSD uses less storage space to record the same data. However, doesn't this "compression" affect the sound quality of the sample? Not necessarily. You'll see why in a moment.

Eight-bit PCM uses its 256 bit pattern possibilities to represent 256 different analog output voltages, half of which are positive and half negative. These values are centered around 128, which usually represents an output voltage of zero. There is a specific output voltage for each PCM value. To get sound, you simply vary each consecutive PCM value-and thereby the output voltage-in a sinusoidal pattern to create the desired frequency.

CVSD doesn't use its bits to represent actual output voltages. Since each sample consists of only one bit, there would only be two output voltages available. Sounds a little like the PC speaker, doesn't it? Instead, its single bit specifies whether the output voltage should be increased or decreased. If a CVSD bit is a one, the output voltage will be increased by a fixed amount. Conversely, if it is a zero, the output voltage will be decreased by this same amount. By varying the number of one bits in a row, followed by a number of zero bits, any frequency up to **16** kHz (for a 32-kHz sample rate) at almost any amplitude may be synthesized.

You can now see that CVSD output voltage is always going either up or down, hence the name continuously variable slope delta modulation. Of course, this also means that CVSD has no way to create a steady-state voltage, something that is necessary to create silence, for example. To get a roughly steady output voltage, each consecutive CVSD bit needs to be of alternate states (i.e., 10101010...). This creates a continuous low-amplitude 16-kHz signal that can be easily filtered out.

FILTERING

One of the biggest advantages of the CVSD method of storing digitized sound data is the simplicity of the necessary output filter. All that is needed is a low-pass filter with its roll-off complete at 16 kHz, or half the sample rate. This fairly high cutoff frequency does not infringe very much

on the audible range of most humans. Filtering for lower-sample-rate PCM audio necessarily affects the frequency response and quality of the final output.

The filter itself may also be smaller. It does not need to store as much energy for a CVSD transmission since the rate of change of voltage per sample time is always constant using the CVSD technique. A PCM transmission may entail much larger voltage shifts per step, requiring a larger, more sophisticated antialiasing filter to smooth its stair-stepping (see Figure 1).

EFFECTIVE RESOLUTION

While CVSD modulation does allow the digitization of sound data all the way up to 16 kHz—or half the sample rate-there is a price to pay: the higher the frequency, the higher the amplitude attenuation of the signal. Since the CVSD technique incorporates a constant voltage step per sample clock, there is insufficient time for the output voltage to make large swings at high frequencies.

As examples, a 40-Hz signal allows 400 units of amplitude; more resolution than S-bit PCM. However, as the frequency goes up, the effective resolution drops. A 400-Hz signal has 40 units of amplitude available, while a 4-kHz signal has only four (see Figure 2). This amplitude normally equates to audio volume. Therefore, the higher the frequency, the lower the output volume that is available.

Everyday speech consists of fairly low frequencies. CVSD modulation provides a good match with a reasonable resolution at normal voice and most music frequencies.

CONVERSION SOFTWARE

Sometimes you need to convert from one sound format to another. PCM Mac or PC sound files could be converted to CVSD and used in a stand-alone application with a playback unit like the one described by J. Conrad Hubert elsewhere in this issue, for example.

Converting from one type of digitized sound format to another is fairly easy. Most difficulties occur

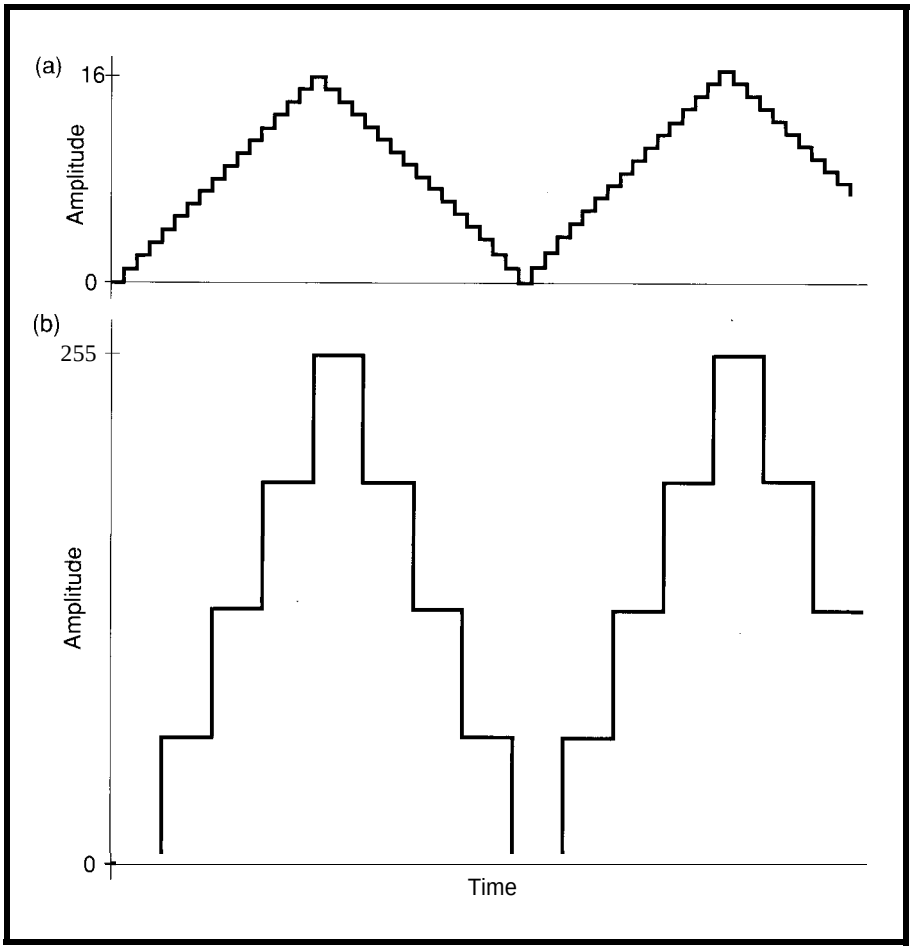


Figure I--When *comparing* **a** *1-kHz* **signal** *sampled at* **32** *kHz using CVSD (a) and a 1-kHz signal sampled at 8 kHz using PCM (b), you'll note that a much higher amplitude can be generated using PCM, though the aliasing is much more severe.*

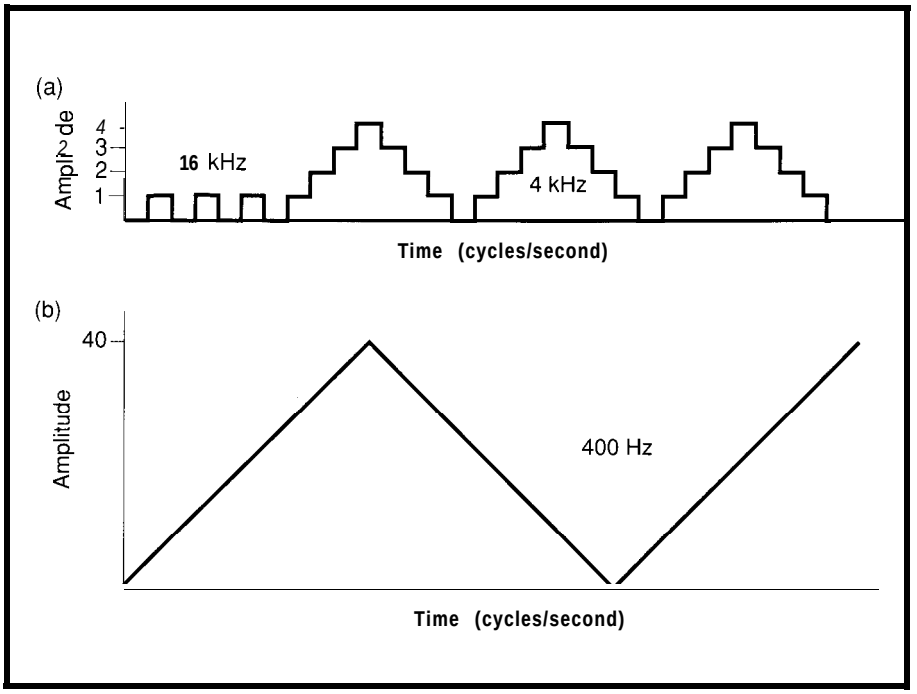


Figure 2—*The maximum amplitude of a CVSD signal depends on the frequency of the signal and the sampling rate. (a) Using a sampling rate of 32 kHz, you'll on/y get one unit of amplitude when generating a 16-kHz signal, buf you can get four unifs when generating a 4-kHz signal. (b) When the generated signal's frequency is much lower-400 Hz- if's possible to get 40 unifs of amplitude.*

Listing 1-A *short C algorithm to convert each 8-bit PCM chunk to 4 bits of CVSD allows the resultant audio to be played back at the original speed.*

```
int i, j;
int pcm, cvsd;
int delta = 1;
int running_cvsd = 128:

while  (!eof(infile)){                  /* do it 'til there's no more input data */

    for (i = 1; i <= 2; i++){           /* pack two bytes PCM into each byte of CVSD */

        pcm = getc(infile);             /* get a PCM byte */

        for (j = 1; j <= 4; j++){       /* convert to 4 bits of CVSD to maintain data rate */
            cvsd >>= 1;                 /* shift output data down one bit position */

            if ((running_cvsd) >= pcm)
                running_cvsd -= delta;
            else {
                running_cvsd += delta;
                cvsd += 128;            /* put a one bit up top */
            }
        }
    }

    putc(outfile, cvsd);                /* write the new CVSD data */

}
```


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when you need a different sample rate in the result. I'll look at a relatively simple sample rate conversion from 8-bit, 8-kHz PCM data to 32-kHz CVSD.

Since we want the playback speed of the resultant audio to be the same as the original, each 8-bit PCM chunk will be converted to 4 bits of CVSD data. This conversion will yield an effective data compression of 2 to 1 in the process. Listing 1 shows a short C algorithm which can be used to do this conversion.

Some notes about the program listing are in order. The short integer `pcm` is used to contain each byte of PCM input data. The short integer `cvsd` has the resultant CVSD bits shifted into it from the left.

Two other variables, `running_cvsd` and `delta`, demand explanation. The algorithm keeps track of what the actual analog output might look like as a result of the CVSD data that it is constructing in `running_cvsd`. It compares this information to the current PCM value to see if it is above or below the desired curve. If it is above, it shifts a 0 into the output byte to reduce the output voltage. If below, it shifts in a 1 to catch up. This technique works very much the way CVSD input hardware does. It compares the previous voltage level to what the microphone is currently sending and determines if it needs more or less amplitude for the current sample. Very simple.

I use `delta` to make the best match of input to output amplitude. If the input data is of low amplitude or frequency, a `delta` value of 1 preserves as much of the input information as possible. For data that has very large amplitude swings or very high frequencies, a `delta` value of 4 or greater smooths out the sound of the resulting CVSD data. You can experiment with different `delta` values on the same input data to see what value gives the best results. The PCM data could also be prescanned to determine its mean amplitude and predict the best delta value.

This algorithm creates four CVSD output samples for each PCM input sample, which works out nice and even for our example. If you are starting with, for example, a 22.05-kHz PCM sample, it is not as simple to derive the CVSD data. Actually, all you need to do is interpolate the data to the higher sample rate. Interpolation looks at several input values around the output sample time to give an average value for that sample. This technique could even be implemented in the algorithm in Listing 1 to yield a potentially more accurate 8-kHz conversion. However, I had to leave something to your imagination.

Jeff ***Schmoyer develops microcontroller-based*** hardware ***and software*** at *microEngineering* ***Labs,*** *P.O.* ***Box 7532, Colorado Springs, CO 80933,*** (719) *520-5323.*

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#114

Generate Digital Speech Using CVSD

FEATURE ARTICLE

J. Conrad Hubert

After Jeff Schmoyer's introduction to the CVSD method of digitizing speech (see page 20), it's time to build some hardware. A chip from Texas Instruments and a PIC processor make embedding speech simple.

A few days before Christmas in 1990, I was given a consulting referral by Scott Specker, a technical salesperson from Texas Instruments' semiconductor group. He had received an inquiry about TI's speech technology from a manufacturer of trade-show display booths. Scott realized the inquiry wouldn't lead to a huge design win for TI, but felt it was a good application for their Continuously Variable Slope Delta-modulation (CVSD) voice recorder. Scott put me in contact with a manager from the display-booth company, sent samples of their TMS3477 voice recorder, and wished me luck.

What the manager needed was a device that spoke one of six messages based on the state of some contact closures. Since the demo would be actuated hundreds of times each day, he was disinclined to use audio tape. Several aspects of this project intrigued me and on Christmas day I immediately plunged in and built a prototype. As it turned out, the display-booth company lost their customer, and I didn't get the consulting work. Nevertheless, I was impressed enough with the TMS3477 that I thought it would form an excellent basis for a product. It was easy to use, required few additional parts, reproduced high-fidelity speech, and costs only $2.67 in 100-piece quantities.

One of the chief advantages of CVSD over the brute-force Nyquist-frequency, A-to-D-to-A technique is that the playback filter requirement is eased considerably. The brute-force technique (typified by first-generation CD players) requires a high-order (9- to 13-pole) filter. But because CVSD data is inherently oversampled, reconstructed speech sounds great with a simple third-order filter.

Unfortunately, since the TMS3477 was developed by TI Japan, there is little technical information available about it. What I did receive was a bad photocopy of a data sheet written in broken English. Much of what I know about this chip was learned through experimentation, and I hope to pass some of that knowledge along to you. If you work with the chip, you'll find it is not particularly amenable to rapid prototyping. The only package in which it's available is a 400-mil-wide plastic DIP with a 2-mm pin-pitch. I ended up hot-melt gluing the chip to a 28-pin machine-tooled socket, and hand soldering wire-wrap wire from each IC pin to its corresponding socket pin. The end result was a standard 600-mil-wide, 100-mil-pin-pitch device.

EVOLUTION

It was obvious from the data sheet that the TMS3477 was designed for "semivolatile" applications like the outgoing message of a telephone answering machine. As such, its bit-serial data I/O is intended to mate with up to 2 MB of DRAM. (A slightly more costly version of the chip, the TMS3478, accepts up to 4 MB of DRAM.) Although the chip itself generates the refresh signals needed to nonvolatilize the DRAM, the current required to do so in a battery-powered system is prohibitively high. The other drawback to this type of system is that once you're satisfied with a given message, there is no easy way to replicate it into other DRAMs. In contrast, I thought an EPROM-based system would make replication trivial and standby power consumption negligible. The biggest problem is converting the parallel-word generated by an EPROM into the serial bit-stream expected by the TMS3477.

To overcome this problem, I developed a design based on an 87C51 which plays messages stored on EPROM via the TMS3477. This board became the playback portion for SoundByte-a two-part system which

provides multilingual stand-alone speech capability for product enhancement. (The recording part of the system uses a PC platform.) The product generated enough interest that Steve Ciarcia requested the system for review. I soon learned from talking with Steve that he felt there was a market for a much simpler device which would intelligibly speak a message at the push of a button. But it had to be cheap!

THE $29.95 CHALLENGE

The gauntlet was down, and the remainder of this article is my best effort at meeting the challenge. The device is a stand-alone system that plays a single message of high-quality speech from an EPROM. Of course, the obvious question is, "How do you get a message into the EPROM in the first place?" Well, if you have a Covox or similar speech board, you might want to look at Jeff Schmoyer's article in this issue (see page 20). Jeff provides an algorithm for converting PCM data into CVSD data. Otherwise, I have already uploaded 19 generic messages to the Circuit Cellar BBS. If you have an idea for a message you'd like, leave me a note on the BBS (addressed to "Jim Hubert"). If I get enough similar requests, I'll create an EPROM image of that message. **[Editor's Note:** Due to ***the size of the digitized messages, only a few are included on "Software on Disk" for this issue.]***

EXECUTIVE SUMMARY

I'll discuss the schematic in more detail shortly, but first a brief overview. Momentarily pressing the play button resets the PIC, waking it from its sleep state. Power is then applied to the rest of the circuitry via Q 1. This commences a power-up reset which zeros the address generator, and initializes the TMS3477. Next, 5 12K bits of data from the EPROM are spoon-fed to the CVSD chip as they are needed. This permits about 15 seconds of speech. When the EPROM data has been completely played, all circuitry except the PIC is again powered down. Finally, the PIC puts itself back to sleep and waits for someone to press the play button.

TMS3477

The heart of the system is the CVSD voice recorder IC. It is permanently held in "play" mode by tying the "play" pin low. Whatever bit-stream is presented at the "data" pin is transformed into a discontinuous analog output via the internal CVSD algorithm.

Notice that the TMS3477 has two V_{dd} pins, one for the analog section and one for the digital section. Power must be applied to the digital section for at least one millisecond (while holding the part in reset) prior to powering up the analog section. This delay is necessary to correct a design defect in the TMS3477 and is achieved with R3 and C4. The chip will eventually fail catastrophically if this power-up sequence is not observed. It is, however, to TI's credit that Applications Support here in the U.S. notified users about the flaw. It also shows how important it is to maintain good communication with field applications engineers. In any case, don't try to "simplify" the design by eliminating R3 or C4.

R4 and C2 form an RC oscillator which clocks the TMS3477 at a nominal frequency of 320 kHz and this results in a 32k-bits-per-second sample rate. Resistor R4 allows you to affect the playback speed by altering the TMS3477's oscillator frequency. Increasing the RC time constant will lower the oscillator frequency, whereas decreasing the time constant increases the frequency. Playing EPROM data with a lower oscillator frequency than that at which it was recorded sounds like the "Jolly Green Giant." Conversely, playing the data at a higher frequency results in a "Mickey Mouse" speech quality. Since all of the speech files on the BBS were recorded at the same rate, about 35 kbps, a fixed resistor is used for R4. However, the printed circuit board is drilled to also accommodate a 50k15-turn potentiometer. This allows you to take advantage of the infinitely variable bit rate, whereby you can trade speech quality for a longer message, or vice versa. (Just be sure to start with the potentiometer set at midpoint, otherwise the frequency may be so far off that you'll only get silence.) Finally, because the oscillator frequency is somewhat dependent on

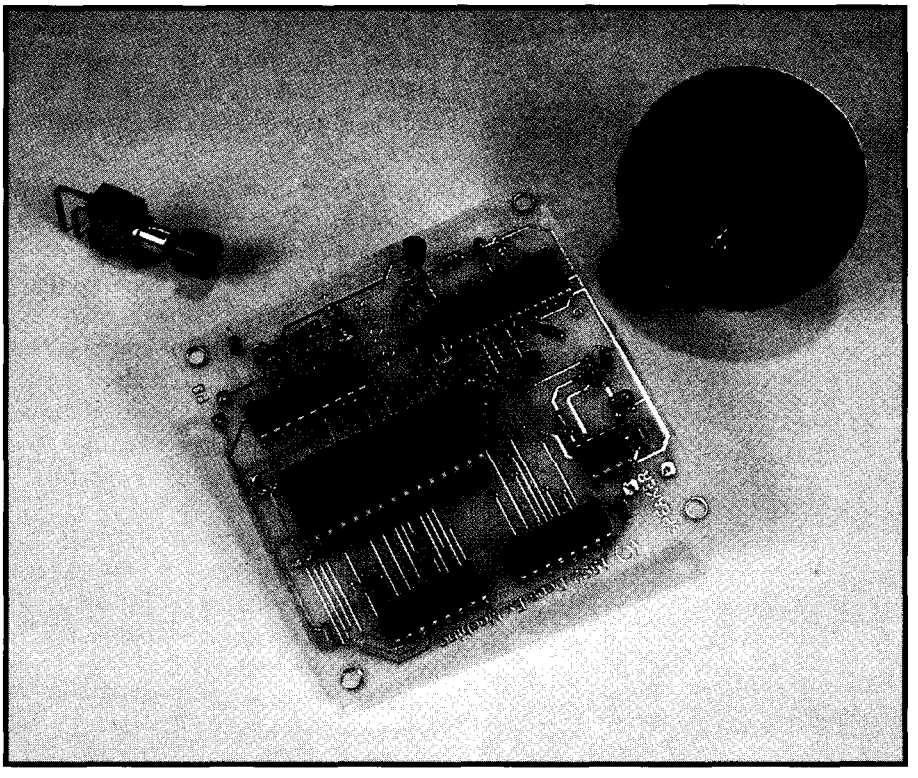


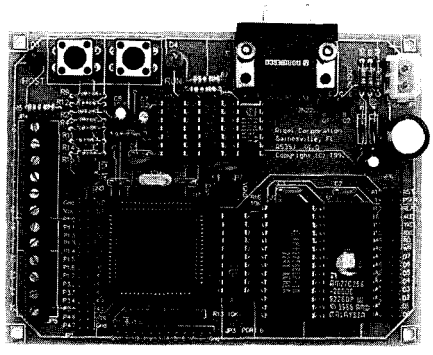
Photo 1—*SoundByte Jr. is a neat, little 3" square board that can be* embedded in applications *that* require voice annunciation. A push *button or TTL signal may be used to trigger the message. The on-board amplifier directly drives a speaker.*

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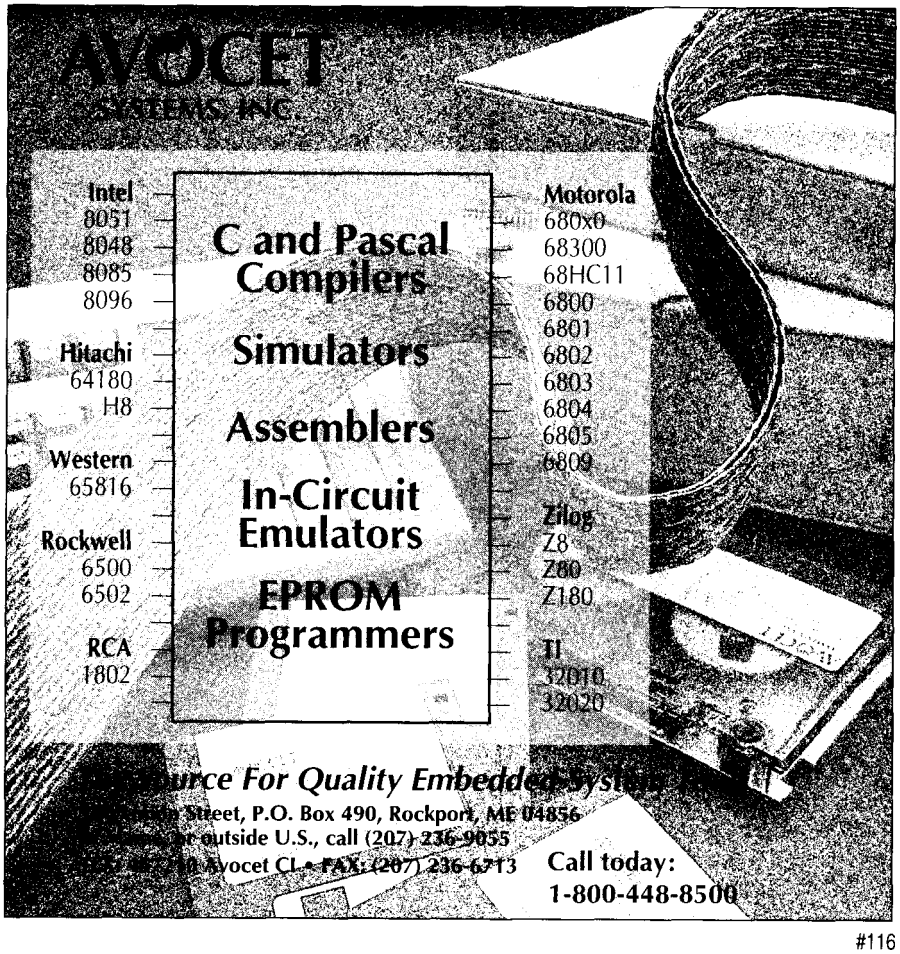
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the power supply, **R4** may need to be trimmed if you use something other than a 4.5 volt battery.

R6 and C8 generate an active-low power-up reset. Configuration programming parameters are sensed during reset. This permits designers to configure the TMS3477's various operating parameters via the pins marked AD0 through AD9. During normal operation, these pins are address lines for the DRAM. However, in reset, the lines are inspected to determine which of them are pulled low via resistors. Resistor R9 configures the only necessary parameter. A complete summary of all programming parameters is given below. Although most of these parameters aren't germane to this application, they are explained in case you want to tinker with the TMS3477.

APO and AP1 select the particular size of DRAM used. If both APO and AP1 are left open, addresses are generated for 256K-bit parts. When only APO is pulled low, addresses are generated for 64K-bit parts. Conversely, when only AP1 is pulled low, addresses are generated for 1M-bit parts. The condition when both APO and AP1 are pulled low is reserved.

AP2 left open implies that speech data will be contained in a single DRAM. Tying this pin low permits double the speech data using two DRAMs.

AP3 left open implies a variable phrase size. Tying this pin low selects a fixed phrase size, which uses the entire DRAM. When a variable phrase size is selected, the "stop" signal would mark the stopping address. The TMS3477 would then not play "dead air" at the end of a short phrase. Note that R9 is the only programming resistor needed for the device in this article.

AP4 left open causes the TMS3477 to stop recording when the DRAM is full, whereas the data is cyclically overwritten if this line is pulled low.

AP5 selects either the "host interface" or "keypad interface." In host interface mode, the TMS3477 expects the play, pause, record, and stop keys to be encoded by a microprocessor rather than coming directly

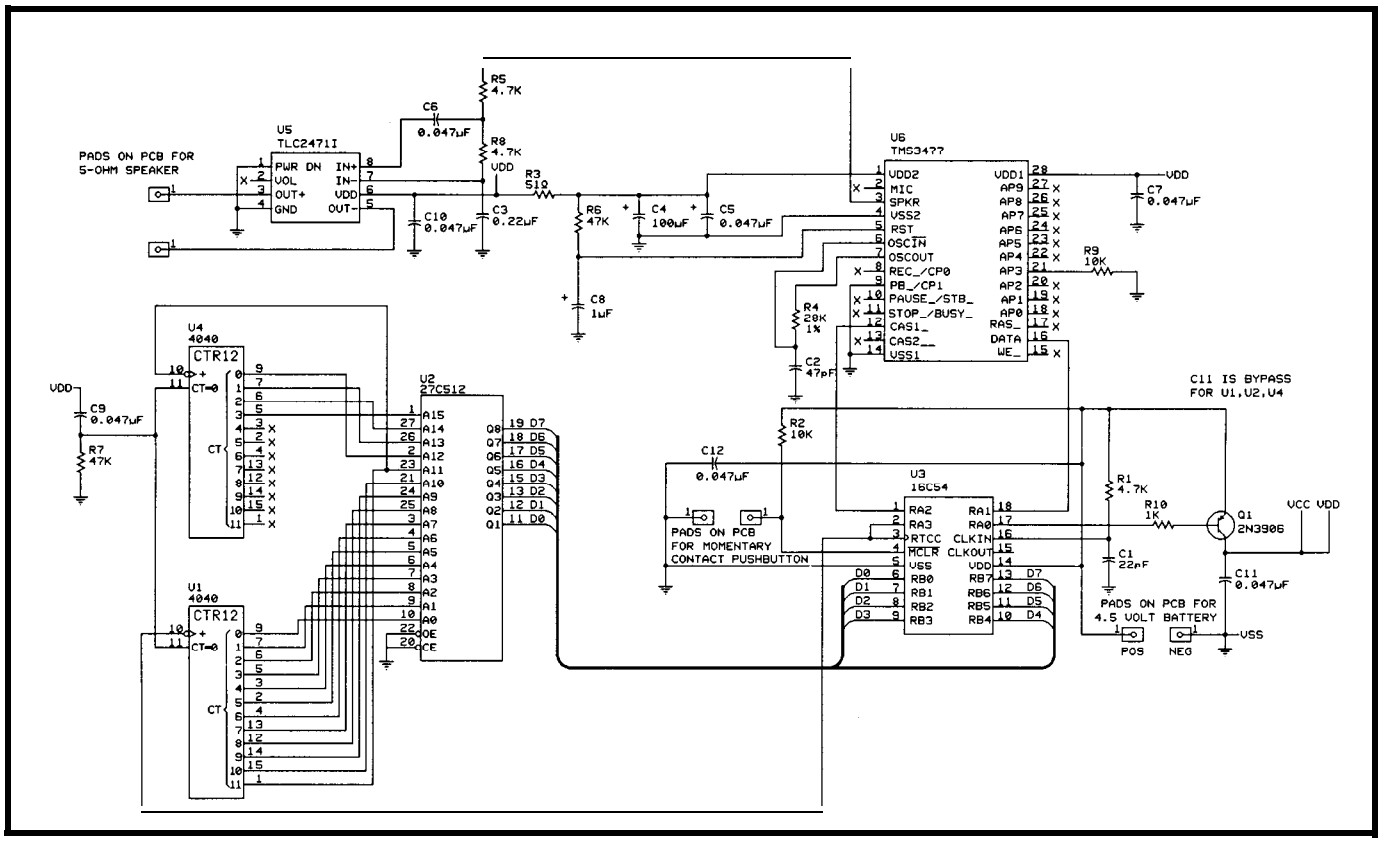
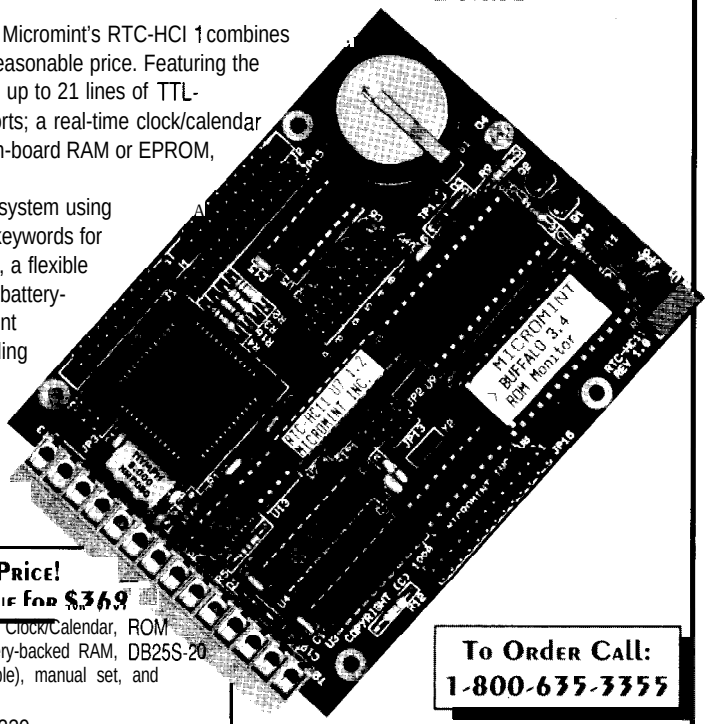


Figure I--The *TMS3477 CVSD* voice *recorder/playback chip is the heart of the circuit. A PIC processor is used to usher data out of a 27C512 EPROM to the TMS3477 as it requests data. A TLC24711 amplifies the final output and can drive an d-ohm speaker.*

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from discrete keys. When AP5 is left open, a keypad interface is selected.

AP6 and AP7 select the base sampling frequency. When both are open, the nominal rate is selected (32 kHz when driven by a 320-kHz clock). When only AP6 is pulled low, one-half the nominal rate is selected. When only AP7 is pulled low, twice the nominal rate is selected. The condition when both AP6 and AP7 are pulled low is reserved.

AP8 left open implies no data compression. Data compression (Tl's terminology) is a misnomer-it is really data expansion. The purpose is to boost the output level of weak signals during playback. This is accomplished by left-shifting the data two bits. (Incidentally, the digital data has 10 bits of resolution.) Pulling this line low activates data expansion.

AP9 left open implies no recording monitor. Recording monitor is a condition in which the analog input is "passed through" to the analog output. Pulling this line low activates the recording monitor.

16C54

U3 is a Microchip PIC microcontroller. I selected this processor because of its low cost, high performance, and minuscule power consumption in sleep mode. At $2.34 each in 1000s, the 16C54 is an excellent value. In case you're interested, here's a useful "rule of thumb" the next time you're contemplating high-volume production: For semiconductors, the highest-volume price is generally one-half of the 1000-piece price.

Together with internal circuitry, R1 and Cl form an RC oscillator which clocks the microcontroller. RC oscillators are appealing because they are much cheaper than a crystal or a ceramic resonator. However, when clocking the PIC with such an oscillator, you must be able to tolerate wide (±25%) frequency variations (higher-precision resistors and capacitors may be used to reduce such variations). Therefore, it is important to test real-time code for proper operation at the lowest clock frequency.

Operating at a clock frequency of 4 MHz, the PIC executes instructions (other than jumps) in 1 microsecond. By comparison, an 805 l-family microcontroller must operate at 12 MHz in order to execute similar instructions in 1 microsecond. The PIC's high performance was an important design consideration. Originally, I wanted the microcontroller to operate at a clock frequency of less than 1.705 MHz. This would have exempted the device from radiated emissions testing under FCC regulations. Furthermore, if the device were run only from batteries, it would be exempted from conducted emissions testing as well. Unfortunately, the PIC is not as efficient at the required bit manipulations as is the venerable 805 1, and I couldn't achieve satisfactory performance at 1.705 MHz. This means if you use this design in certain types of products-whether alone or in conjunction with other circuitry-the entire product must undergo FCC compliance testing.

TLC2471 I

U5 is a filtered audio amplifier. It implements a 3-pole switched-capacitor low-pass filter with a 3.5-kHz corner frequency. (A similar part, the TLC2470I, has a 5.0-kHz corner.) The power amplifier section differentially generates ±2 volts across an 8-ohm speaker, to produce 0.5watt peaks from a 5-volt supply.

If either input is left open or AC-coupled, that input is held at one-half V_{dd} by an internal high-impedance voltage divider. This is to permit an automatic power-down feature. If a 3-µF capacitor is connected from pin 1 of U5 to ground, the amplifier will automatically power up or down in the presence or absence of an input signal. Because power is switched via Q1, pin 1 is tied to ground thus defeating this automatic control. However, because of this high-impedance divider, C3 is required to give a low AC impedance path to ground, and C6 provides AC coupling for the input signal. Volume control is achieved with R5 and R8 which, together, form a resistor divider. You may want to tailor their values to your application, or use a potentiometer instead.

CD4040B

U1 and U4 are 12-bit binary ripple counters. These ICs form a 24-bit address generator. Although a 512K EPROM only requires 16 address lines, the PCB is designed to accept up to a 4M-bit EPROM, which requires 19 address lines. As you may know, ripple counters' outputs are inherently asynchronous. However, this fault is overcome by latching data from the EPROM just prior to incrementing the address generator. By the time data is again latched, the counter's outputs will have settled. R7 and C9 provide a power-up reset that clears the address generator's outputs to all zeros. (The 4040 requires an active-high reset signal.)

27C512

U2 contains the speech data. It is important to use a CMOS part here since the power consumed by an older-technology EPROM will put too great a load on Q1.

2N3906

Q1 is a PNP transistor that is used as a high-side switch. It controls the power distribution to all chips except the microcontroller, which is always under power. Since beta is such an unreliable transistor parameter, I selected R10 to give plenty of excess base current to saturate Q1.

POWER SOURCE

This design will work with a variety of power supplies. A regulated source of 5 volts is ideal, however the unit can also be powered from a battery. The quiescent current consumption is under 3 µA, and when tht unit is playing a message, the current draw is less than 50 mA. This means that three or four 1.5-V AA cells in series will work perfectly. Three cells produce over 4.5 volts when they are fresh, and the unit still works when their output capacity has diminished to less than 4 volts. Also, the unit fail: gracefully by playing the message more and more slowly as the batteries wear down. In some applications, it may be desirable to provide reverse-polarity protection in the event the batteries are inadvertently installed backwards. In this case, use a 6-volt battery and connect a diode (like a 1N4001) in series with either supply lead.

Although the PIC is specified to run from a 6-volt supply, the other TTL chips would like to see no more than 5.5 volts at their inputs. This is okay since these chips won't be powered up until the unit is actually playing a message. If you use AA cells, their output will sag enough to limit the voltage to an acceptable level (assuming there are a few tenths of a volt dropped across the diode).

AUTHOR'S NOTE

Just before this article was to go to press, the author discovered the design has a sensitivity to ESD (electrostatic discharge).

It is possible for the microcontroller to latch up if its MCLR pin is subjected to ESD. This is likely to happen if, as the article suggests, a mechanical push button is used to trigger the board.

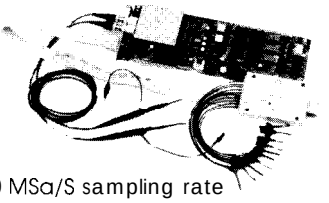
The problem stems from the input structure of the MCLR pin coupled with the somewhat unconventional manner in which that pin is being used. The MCLR pin (and RTCC pin as well) lacks an internal clamp diode to Vdd because this pin must see a voltage greater than Vdd during programming.

To protect MCLR in a manner similar to that of the other I/O pins, connect a Schottky diode (IN.58 17) with the cathode to Vdd and the anode to MCLR. However, an even more robust (and cheaper) solution is to connect an NPN transistor (2N2222) with emitter to ground and collector to MCLR. The push button should then apply Vdd to the base of the transistor via a Ik resistor. Of course, the base should also be held weakly to ground via a 47k resistor to avoid inadvertent turn on.

Note that this additional circuitry is unnecessary if MCLR is being toggled via a TTL-level signal rather than a "real-world" mechanical push button.

#1

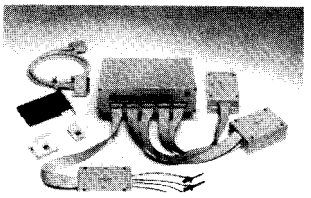
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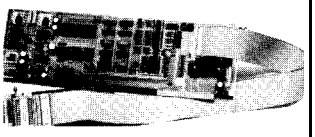


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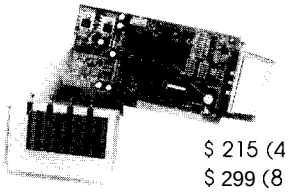
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CONSTRUCTION TIPS

The circuitry shown in Figure 1 is fabricated on a rectangular PCB which measures 3.05 inches on a side. In order to hit Steve's target price, we had to omit the silkscreen, however all necessary nomenclature is etched in copper on the board. Capacitor polarity is marked, and square pads indicate pin 1 of all ICs. To save space, resistors are populated "standing up" as they might be in an old transistor radio.

The only area that might cause confusion relates to the EPROM. Although the schematic shows a 28-pin EPROM, the board is drilled to also accept larger-capacity 32-pin JEDEC devices. When installing a 27C512, it must be "bottom-justified," as is done with EPROM programmers. This will locate pin 28 directly opposite one of the pads for JP 1. JP 1 is a jumper that must be installed in order to provide V_{dd} to a 28-pin EPROM. Because pin 28 (V_{dd}) on a 28-pin EPROM is pin 30 (A17) on a 32-pin EPROM, the connection to the address generator (U4, pin 2) must be cut. This is best accomplished by drilling out the via found on that trace. Note that the PCB comes with this via removed in order to circumvent damage to U4.

To hear the fruits of your labor, connect an 8-ohm speaker between the pads marked "SPEAKER." A momentary-contact push button goes between the pads near the "PB" marking. Finally, wire a 4.5-volt battery to the "DC POWER" pads (positive terminal is nearest the edge of the board). ❑

*J. **Conrad Hubert is a principal in Deus Ex** Machina **Engineering Inc. where he is involved with the** development of **hardware and** software for **embedded systems, data acquisition, and digital signal processing.***

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#120

Computer-controlled Light Dimmers

Part 2: Filters, Snubbers, and Design Issues

FEATURE ARTICLE

William Von Novak

Following up on last month's introduction and theory, William dives into the hardware end of dimmer design with some sample circuits, design tips, and a complete application.

Last month, I talked about the history and purpose of dimmers, and started on some design issues. This month, I'll finish the general issues and describe the dimmer project itself.

The simplest possible phase-control dimmer is shown in Figure 1. In fact, this design appears often in those $5.99 dimmers found in hardware stores. This circuit uses a diac trigger fed by a variable RC delay circuit. A diac exhibits high resistance until its threshold voltage is exceeded, then "snaps" to a lower resistance. This allows current to flow from the capacitor, through the diac, and into the triac trigger terminal. Since both the triac and diac are bidirectional, this circuit works on both sides of the AC cycle.

The above circuit will work, but there are some problems. When the diac snaps on, the triac will fire and go to full conduction instantly. The result is a very fast current and voltage rise time (high di/dt and dv/dt, respectively) into a resistive load such as an operating light bulb. The sharp waveform edge generates a great deal of acoustic and electromagnetic noise, which translates into buzzing lights and lousy TV reception.

To combat these problems, dimmer designers use inductors to reduce di/dt. The inductor smooths out the waveform seen at the output of the dimmer, thereby reducing noise and EMI. Filter chokes for this purpose are available commercially in a wide range of inductances.

Adding an inductor to the circuit of Figure 1 unfortunately causes a new set of problems. The mostly resistive load provided by the bulb has now become an inductive load. When the current through the triac reaches zero, the device will shut off. The voltage, which is no longer in sync with the current due to the new inductance, can shoot up rapidly. If the rate of rise of the voltage (dv/dt) exceeds the limits for the device, it may turn back on (see Figure 2). Although this action won't damage the device, it makes the dimmer extremely erratic. It can also cause problems for the trigger triac if a triac optocoupler is used, since the trigger triac sees the same dv/dt as the main device.

Figure 3 shows an optocoupled dimmer circuit with an inductor. I also added snubbers to reduce dv/dt. The first snubber, made up of the 22-ohm resistor and the 0.22-µF cap, protects the terminals of the main triac from a large dv/dt. The second snubber, composed of the 180-ohm resistor, the 1.2k resistor, and the 0.1-µF cap, protects the smaller trigger triac. In an ideal world, one could calculate values for the components of the snubbers to minimize heating in the resistors and

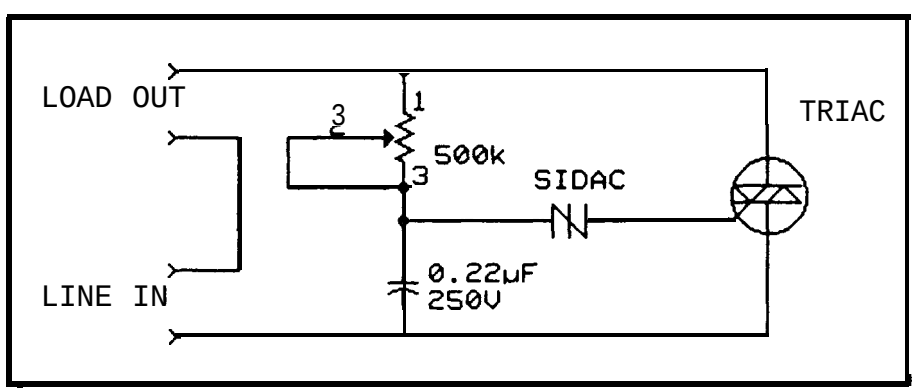


Figure 1—*The simplest possible phase-control dimmer uses a triac to switch the load and a variable RC delay to control how long after zero corssing the triac is fumed on.*

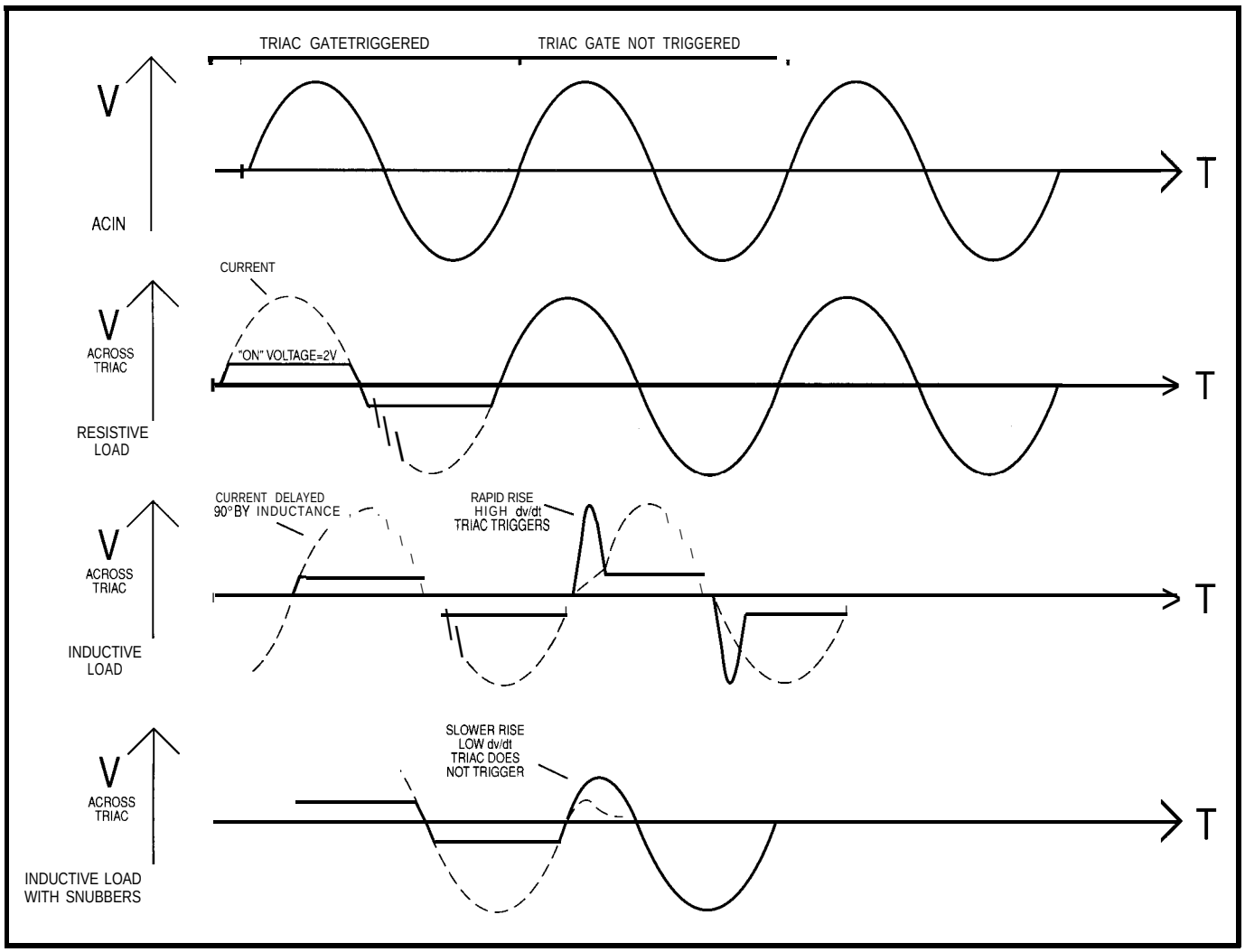


Figure **2**—*To correct the effects that result from a sharp rise in voltage and current, an* inductor is *introduced info the circuit of Figure 1. As a result, voltage and current are no longer synchronous. Now concern is put on whether the voltage rise rate exceeds the limits of the device, which can cause the device to be turned back on, making it erratic.*

maximize damping. Since no one ever uses dimmers in an ideal world, selection of the values are largely empirical. I've used suggestions from Motorola's thyristor data book as a guide for my design, but you should feel free to experiment.

The final consideration in dimmer design is the control circuit. The idea here is to detect the zero-crossing of the AC power line, start a timer, and trigger the device when the timer expires. No delay gives full on, and a delay of 8.33 milliseconds (a half cycle) gives full off. Most dimmers still use analog timers for this purpose, but some have begun using digital timers. Digital timers, besides being more accurate and less susceptible to drift, are easier to interface to DMX-512.

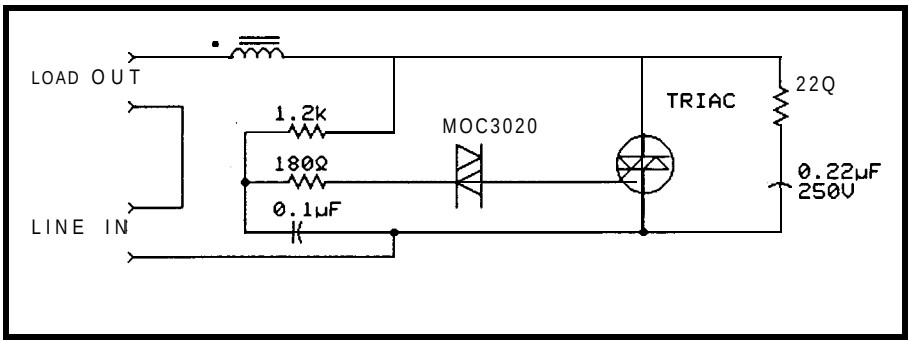


Figure *I--Adding a triac optocoupler (MOC3020), inductor, and snubber to the original circuit improves circuit reliability.*

The problems I mentioned earlier regarding the nonlinear response by both the eye and the lamp are compounded by a third problem: nonlinearity between firing angle and power output. When the firing angle of the dimmer is 90°, it's half on. At 0" and 180°, the power levels are 100% and 0%, respectively. So far so good. At 45°, however, the power sent to the lamp is NOT 25 %. Power is roughly proportional to the area under the voltage waveform. Since AC power is a sine wave, the power is proportional to the integral of the square of the sine of the firing angle (see Figure 4).

When all three factors (perception, power, and sine-wave area correction) are taken into account, the equation describing perceived brightness for a given firing angle is given by Figure 5. These equations are usually used to make a table (desired brightness in,

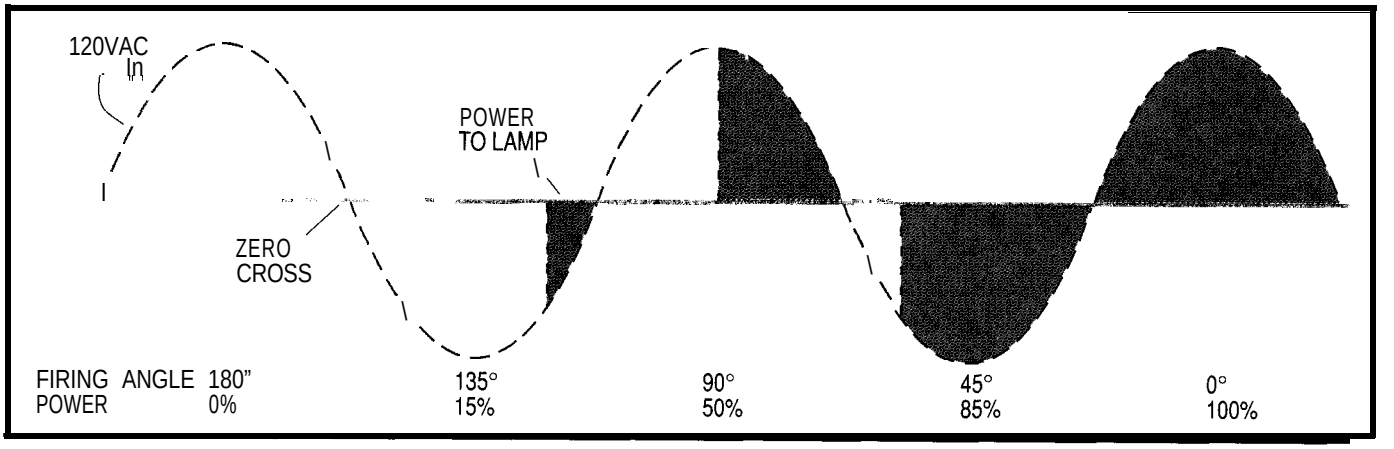


Figure 4—Power is proportional to the area under the sine wave, however it is not proportional to the firing angle. To determine the correct firing angle for a given intensity, the integral of the sine of the firing angle must be used.

firing angle out) and then discarded. Feel free to use this table for your experiments, but bear in mind that the equation given for light output versus power in is approximate at best.

The primary control over firing angle always comes from the console. The desired 0–100% is converted via the table to a firing angle and used to set the zero-crossing timer. Many modern dimmers further correct the angle for line regulation, load regulation, prewarm, and speed-up filtering.

OTHER TRICKS

Power in theaters is usually flaky to begin with. Most older theaters weren't designed with today's high-tech power-hungry productions in mind, and wire gauges are often undersized for the currents they carry. Such undersized wiring causes quite perceptible dips in light output when new instruments are turned on. Line regulation helps by sensing the input voltage and correcting the firing angle to prevent a visible dip. Load regulation carries this a step further by sensing total power output and adjusting the firing angle to maintain desired power-output levels. The final cost is a reduction in maximum intensity; the dimmer must reduce intensity at 120 volts to have enough margin to correct for a dip to 90 volts.

To reduce response time, filaments are sometimes prewarmed, which can be done three ways. In a manual system, the LD simply nudges the sliders up on all the instruments he'll be using to about 5%. This isn't enough to cause significant light

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#121

output, but it keeps the filament warm and responsive. Some systems have a built-in prewarm circuit that does the same thing. Newer computerized systems can predict which lights will be used next and preheat only those instruments a few seconds before they're needed. This last approach saves energy and reduces wear and tear on the filaments.

To further reduce response time, some dimmers sum a high-pass filter output with the desired output. If an alternating high/low power waveform were fed to an incandescent lamp, the resulting intensity would resemble a low-pass-filtered square wave (see Figure 6). By summing a high-pass-filtered version of the control signal with itself, response time can be somewhat improved.

$$\text{Power} = \int_0^{180^\circ} \sin^2 x\,dx = \frac{x - \frac{1}{2}\sin 2x}{\pi}\Bigg|_0^{180^\circ}$$

$$\text{Intensity} = \text{Power}^2$$

$$\text{Perception} = (1 - e^{-2\,(\text{Intensity})}) \times 1.16$$

$$= 1.16\left(1 - e^{-2\left(\frac{x - \frac{1}{2}\sin 2\Phi}{\pi}\right)^2}\right)$$

Φ = Firing Angle
Power = Power to Lamp
Intensity = Lamp Intensity
Perception = Perception of Intensity

Figure 5—*Due to the complexity of the math, the equation that relates perception to firing angle is usually only used to make a table, and is then discarded.*

PROJECT DESCRIPTION

The dimmer system I developed (see Figure 7) was part of a larger project involving the use of a power-line modem lighting control system. I've left out the modem part (it can be controlled via an RS-232 line) and I've only described two of the eight dimmer channels. It's a good starting point for any digital phase-control dimmer system.

The input power is fused and switched where it enters the case. D1, a metal oxide varistor (MOV), protects the dimmer from power line spikes and surges. A four-pole filter made up of L3–L6, C6, and C7 preserves power quality in both directions: it prevents false triggering of the triacs by power line noise, and it reduces the amount of dimmer interference sent back to the power source. I constructed L3–L6 by winding 14-gauge magnet wire around Micrometals powdered-iron toroids. Micrometals specializes in core materials for filter applications, and has a huge selection of materials, shapes, and sizes for filter inductors. Fourteen-gauge wire can be difficult to work with due to its stiffness; wire two or three gauges smaller can be used as long as you maintain the copper's cross-sectional area.

The power supply for the dimmer logic is supplied through T1. The supply is a garden-variety linear 5-volt supply. When the AC line swings through zero volts, the LED in U3 shuts off, which is detected by the control circuitry and used to determine the zero-crossing point. This point becomes the trigger that starts the timer, thus determining the firing angle. Since the control circuit will do some processing on the signal, it's not critical that it occurs at exactly the right point along the AC waveform, as long as that point doesn't change with line level, load, or time.

The heart of the first dimmer is Q1-a 600-volt, 25-amp triac made by Teccor. It has an isolated TO-220 case, which makes it extremely easy to mount and heat sink to a typical metal chassis. Although it should never see more than about 200 volts, the 600-volt rating helps ensure that it won't be subjected to false turn-on when exposed to noise caused by the other dimmers.

Each dimmer is rated for 1.2 kilowatts, which translates to 10 amps maximum through each dimmer. On turn-on, though, the lamp could draw up to 200 amps. Such a surge would certainly blow the fuse (if not the triac) every time the dimmer went to full brightness. Fortunately, several factors make this surge manageable. The total resistance for the dimmer circuit, including the on-resistance of Q1, L1, the fuse, and the input filter is around 0.7 ohms. This limits the maximum surge to under 100 amps. By using preheat, the problem of cold filaments is reduced. Finally, the triacs have a parameter called I_{tsm}, the maximum half-cycle surge rating. This rating is an absolute maximum that the triac should see only during a dead short of the output for as long as it takes for the fuse takes to blow. This parameter (250 amps for Q1) gives an added degree of ruggedness to the circuit, although you shouldn't rely on it for turn-on surges.

F1 protects the circuit from shorts on its output. A standard 3AG glass-

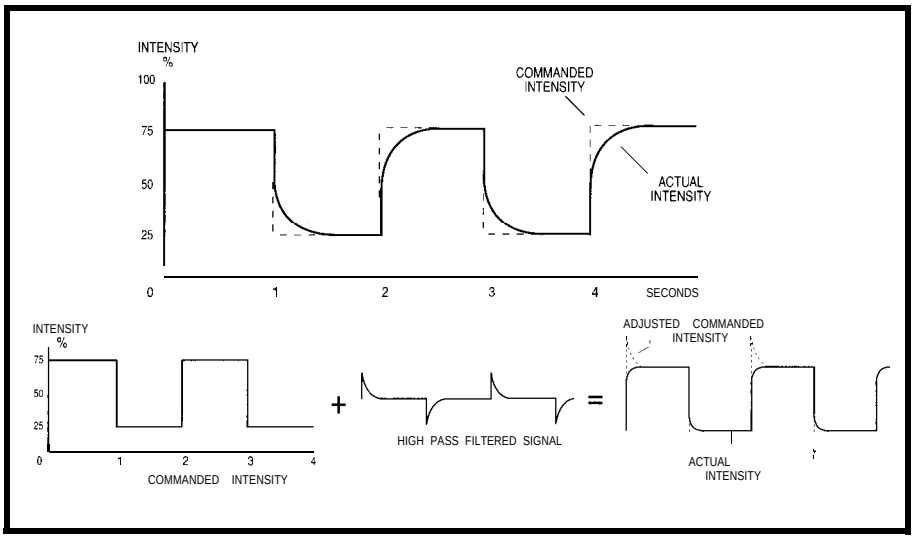


Figure 6—*Because of the physics of incandescent lamp filaments, there is usually a lag between the command to turn on and light being produced. By summing a high-pass-filtered version of the control signal with itself, you can somewhat improve response time.*

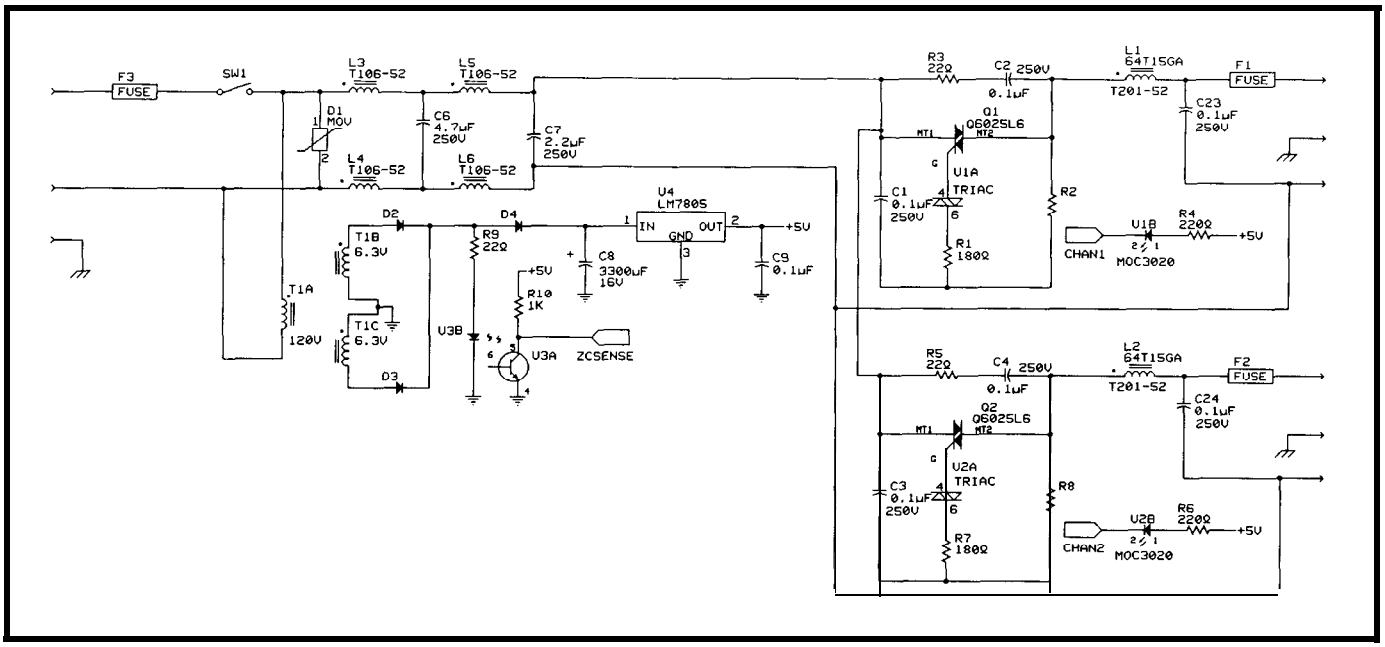


Figure **7a**—*Power coming into the dimmer control unit is filtered to remove line noise that may cause false triggers and to prevent dimmer noise from propagating back onto the line. Low-voltage power for the control circuits comes from the transformer as does a master zero-crossing signal.*

body fuse should work well. The 10-amp 3AG fuse seems to have enough thermal inertia to not blow during turn-on surge. If the fuse blows on turn-on, a 3AB slow-blow fuse may be substituted.

The snubber made up of R3 and C2 prevent false triggering of the triac on turn-off. Although lamps are primarily resistive in nature, L1 is large enough that the snubber is necessary. The trigger snubber consisting of R1, R2, and Cl protects U1, the optocoupled triac trigger, from false triggering.

The MOC3020 is the trigger element used in this dimmer system. There are a number of other parts in the series. The MOC3010 is the basic triac coupler, rated for use in 120-volt AC circuits. I used the 3020 in this circuit (the 240-volt AC version) for an added degree of noise immunity, although with the proper snubbing the 3010 should work fine. Avoid the 3030 series; these devices switch at zero crossing only and are intended for use in solid-state AC relays.

I constructed the output inductor, L1, by winding 64 turns of 15-gauge magnet wire around a Micrometals T201-52 core. The 201 refers to the size of the core, and the 52 refers to the material. These inductors gave a current rise time [time from turn-on to time of 90% current flow) of around 200 microseconds at full load. This smoothing effect goes a long way toward reducing dimmer noise and radio interference. In general, slower is better, but keep in mind that resistance losses, size, and snubber problems increase as you increase inductor size.

ADDING THE CONTROL

The controller section should be familiar to anyone who uses or designs small controllers. It's based on an 803 1 running at 12 MHz, and has 8K of RAM and 8K of EPROM. I used a relatively large amount of memory so I could load a development system (monitor, disassembler, downloader) into the dimmer itself. The interface to the outside world is via an RS-232 interface, buffered by a MAX232. The MAX232 is convenient since it requires only +5 volts to generate the bipolar RS-232 levels.

The controller senses zero crossings via its INT1 line. U9 buffers the zero-crossing signal and ensures reasonable rise and fall times. The triac trigger LEDs are driven by port 1 of the 8031 and buffered by U10, an octal buffer. Keep in mind that I've only shown two channels here for clarity. The prototype I constructed uses all eight.

The assembler I used on this project was Cross-16, a simple cross-assembler by Memocom. Cross-16 has a very basic set of assembler directives (there are 15 or so), is small (31K), fast, and can be used with almost any controller by entering its instruction set in a file. (The program includes about 30 processor files.)

The program is made up of three major blocks. The initialization section sets up the 8031 hardware resources and initializes some variables. The phase-control section is interrupt driven and runs in the background. The main program is a simple command interpreter designed to facilitate dimmer testing. The program is not geared toward a serious theater application; I purposely kept it simple. Keep in mind that the program is designed to be run from a monitor, so many hardware features have already been set up by the monitor.

I begin with variable declarations. All memory locations are in internal RAM to make a transition to a single-chip 805 1 possible. The next section redirects the interrupt vectors to the correct section of code.

The main-line init routine is the entry point into the dimmer program and must be called from the monitor program. It sets all dimmer values to zero, sets timer 0 to free-run with a

period of 33 µs, and enables the interrupts. It then calls the interpreter. The interpreter is a simple-minded program that accepts inputs from the RS-232 line and allows the user to set dimmer values.

The real action is going on in the background. Each dimming channel has its own value (called a reload) that is loaded into a current-value location at every zero crossing. Every 33 us, timer 0 generates an interrupt. The interrupt handler decrements this current value until it reaches zero. At that point, the corresponding output pin is pulsed to zero (on). This provides a mechanism for controlling firing angle. Since 33 µs times 256 possible values equals 8.448 milliseconds (approximately half a cycle), the firing angle can be controlled in 256 steps from 0" to 180".

When the zero-crossing detector input goes high, the zero-crossing routine is called. Since my zero-crossing detector triggers slightly before the actual zero crossing, this routine sets a countdown variable which is decremented every 33 us. When that value equals zero, the timer 0 routine turns all the outputs off and reloads the current values with the reload values. On the next timer 0 interrupt, the cycle begins again.

One problem I had with the zero-crossing routine was making all the code fit in the time available. The routine executes every 33 us, the routine itself (assuming nothing fires that cycle) takes 18 us, and the interrupt call and return take another 4-8 us. Even using six channels instead of eight, this uses up 79% of the processing time available. In this case, it's not much of a problem since the foreground program is so simple. A 16-MHz part or fewer dimming levels would help alleviate this problem.

Another annoying problem is calibrating the zero-crossing detector delay time. I came up with the value I used-OC hex-mainly by trial and error. If the value is off, dimmer operation will become erratic as the triggers for one cycle extend into the next cycle. A better zero-crossing detector would solve that problem.

Since the firing angle is directly related to the desired value, no intensity correction is done at the dimmer. This becomes clear at low intensities, where a change of one count is easily perceptible. Any intensity correction must presently be done at the transmitting end. It may be possible, using a faster processor, to do intensity correction at the dimmer itself, thus making the process more transparent to the user. This would involve changing the 33-µs timeout every cycle to match the required correction time.

Another possible enhancement is the addition of a DMX-512 receiver. The 8031 already has a UART that can handle the serial data stream if the processor clock is pushed up to 16 MHz. An RS-485 receiver would be the only additional component required.

CONCLUSION

I hope this article has been a good introduction to the world of phase-controlled dimmers. They are remarkably reliable, versatile devices, and they have made possible some truly amazing theatrical effects. There are several advances looming on the

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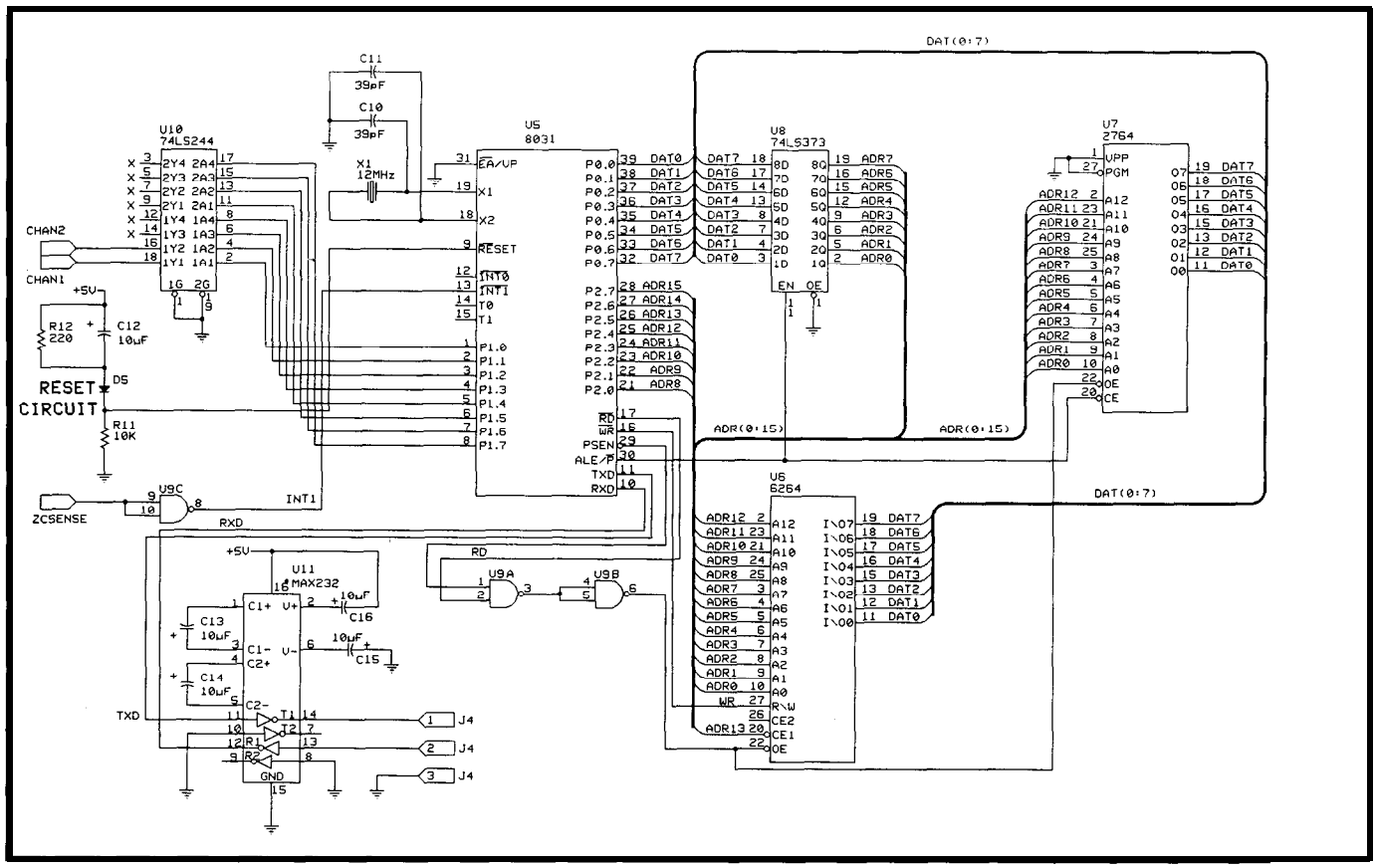


Figure 7b—*Beyond* **the** *dimmer* **section,** *the controller looks like most other 8031-based circuits, with 8K* **of** *EPROM, 8K* **of** *RAM, and a MAX232-based RS-232 interface.*

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horizon--switch-mode dimmers, fluorescent and high-intensity discharge instruments, and RF control schemes, to name a few- but the phase-control dimmer will be around for many years to come. ❑

William Von Novak holds a B.S. in electrical engineering from MIT and is head of R&D at Custom Power Systems. **His** specialties *include dimmer systems, fluorescent ballasts,* motor *control, laboratory data acquisition, and audio DSP.*

SOFTWARE

Software for this article is available from the Circuit Cellar BBS and on Software On Disk for this issue. Please see the end of "ConnecTime" in this issue for downloading and ordering information.

I R S

410 Very Useful
411 Moderately Useful
412 Not Useful

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Barnacles on the ISA Bus: Starting the '386SX Development Card

The first step in adding your own circuits to a standard '386SX motherboard is to come up with a bus interface board. Ed takes that first step as he starts building his Firmware Development card.

FIRMWARE FURNACE

Ed Nisley

The 25-MHz '386SX I'd planned to use for these columns changed to 33 MHz before I placed the order. Four months later, '386SX boards run at 40 MHz for the same price. Even the rate of change is changing.

Curiously, though, higher CPU performance has little to do with your firmware's I/O bandwidth. Just like barnacles on a ship's hull, myriad "PC compatible" cards hold down the speed of the ISA I/O bus. Yes, you can design a faster bus, but customers may not beat a path to your door.

The acronym "ISA" means "Industry Standard Architecture" which, in turn, is a euphemism for "IBM PC/AT Clone." Stripped of the hype, what you're getting is a decade-old design intended for a simple desktop microcomputer. If you need blazing I/O performance, these barnacles are not for you. But ISA bus I/O is entirely fast enough for many controller applications.

In this column, I'll take a look at I/O performance as we begin construction of a Firmware Development card that I'll use as the basis for several future projects. As with the firmware in the last two columns, the fundamentals are more important than presenting a complete design in one shot.

The AMD 80386SXL data book provides the grim details required to actually design a '386SX system starting with a handful of chips. Fortunately for us, that level of detail is irrelevant because the I/O bus barnacles define precisely what the CPU must do to be "PC compatible."

Listing 1--This Micro-C code writes a pair of pulses to the parallel printer port. The first pulse uses C-level functions, while the second pulse uses the in-line assembler to reduce the delay. The porttime.c program containing this fragmenf is available on the Circuit Cellar BBS.

```
while (!chkch()){
    disable();
    outp(PortAddr,0x01);        /* rising edge */
    outp(PortAddr,0x00);        /* falling edge */

    asm {
        MOV     DX,PortAddr
        MOV     AL,#$01
        OUT     DX,AL
        MOV     AL,#$00
        OUT     DX,AL

    enable();
```

We can see the CPU only through several layers of glue circuitry.

For our purposes, the ISA bus cycle definitions in Solari's ***AT Bus Design*** provide enough information to construct a useful card. I used that book as the basis for much of the logic and timing information in this column, although you should refer to the complete bibliography in my column in issue 3 **1** (February '93).

However, it behooves you to verify that these designs will actually work in your system: even when you follow a recipe exactly, you must still taste the soup before dishing it out. I can only hit the high spots here and trust that you will verify the detailed numbers for your own circuits.

I still recall making Oriental Pepper Soup from a recipe that called for "3 T" of black pepper. All present agreed it was plenty hot enough, but perhaps three teaspoons would have been enough. Could a "t" have turned into a "T" by mistake?

ONE BYTE AT A TIME

The simplest bus I/O operation is writing a single byte to an output port. For simplicity, I'll use the parallel printer port at address 0378 to illustrate the process, though it applies to any byte I/O operation. You can use the LED circuit I described in issue ***31*** **to** show the status of the port outputs.

Each iteration of the code snippet in Listing **1** produces two pulses on bit 0 of the parallel port. With a 33-MHz '386SX system clock, the first pulse is 3 µs long and the second is 1 µs. You should see a dim glow from the LED because the pulses repeat every 3 1.5 µs at a 13% duty cycle.

Although the 80386 CPU's bus interface is fairly complex (read the data book!], the ISA I/O bus action is straightforward. I connected a logic analyzer to the bus and took Photo 1 to illustrate this point.

The top trace is BCLK, the 8.33-MHz Bus CLocK. The output operation begins with the rising edge of BCLK just before BALE (Bus Address Latch Enable), the second trace, goes high. When BALE falls, the I/O address lines are valid. The third trace is the negative-active I/O Write signal, -IOW, which clocks the data into the parallel port's output latch.

The port's output data, shown on the bottom trace, actually appears at the pin one BCLK cycle after –IOW ends. Evidently, the integrated I/O chip uses BCLK to update its internal latches. As we'll see later, a discrete latch presents its results immediately after the rising edge of –IOW.

Not counting the internal latch delay, the whole output operation takes six 120-ns bus clock cycles. The first two cycles set up the address and data, while the remainder provide enough time for the I/O device to accept the data. Byte reads require a similar amount of time, except that the device provides the data to the CPU in response to the –IOR signal.

The rather leisurely pace of a single-byte write (or read) may come as a surprise, but the nominal ISA duration really is 720 ns. This cycle time ensures compatibility with cards designed for the original 4.77-MHz 8088 PC, but it's a real stick in the spokes on a 33-MHz 80386SX that might gnaw through a dozen instructions in that time!

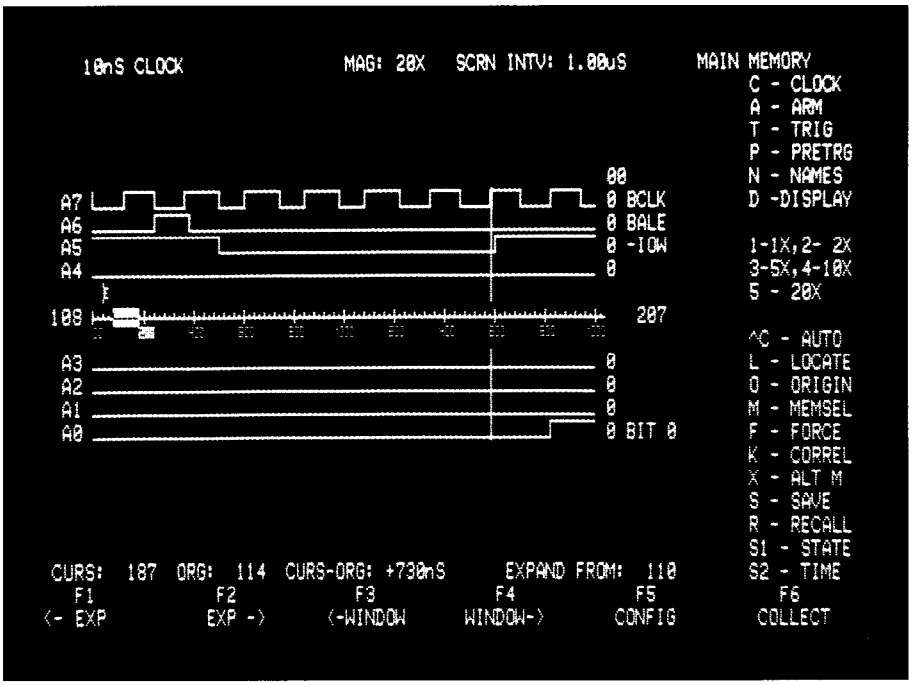


Photo 1--This is the logic analyzer record of a single 8-bit wife to port 378. The output operation begins with the rising edge of BCLK just before BALE goes high. It ends when –IOW goes high to latch the output data into the port. The infegrafed I/O chip used in this '386SX delays the actual ouput one additional BCLK cycle.

Unfortunately, there is no way to speed up byte I/O. The ISA bus includes a Synchronous Ready signal that can force no-wait memory accesses, but -SRDY cannot be used during I/O operations. Note that some of the references refer to -SRDY as -ENDXFR, but in any case it's pin B08 and doesn't help.

The PC/AT's designers widened the I/O bus to 16 bits and, because no PC cards responded on the new lines, the new I/O cycles could run considerably faster. Photo 2 shows that writing a 16-bit value takes only three bus cycles from the first rising BCLK edge until the data appears in LED bit 0. But first, we need some 16-bit hardware..

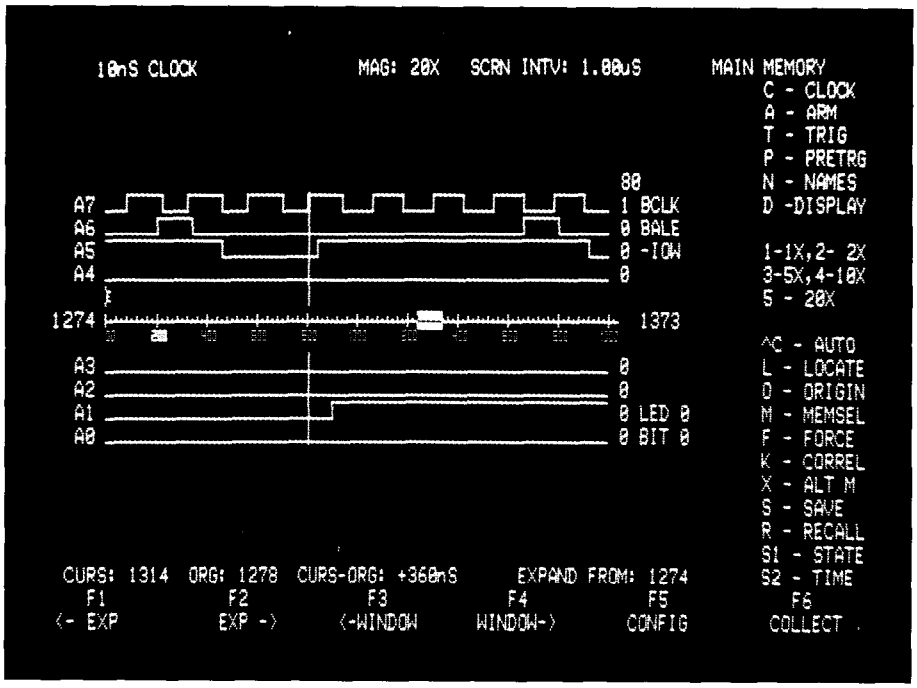


Photo 2-A *single 16-bit* write to *the LED* display on *the* Firmware Development card is complete in three BCLK cycles. The *data appears at the latch output immediately after -IOW rises.*

ISA CARD BASICS

Photo 3 shows the end result: a 16-bit PC/AT prototype card with a handful of ICs, a pair of DIP switches for inputs, and a two-digit LED display for output. Half of the card is empty, which leaves plenty of room for several columns worth of projects.

When you examine the card's schematics, you'll be struck by the absence of "high tech" circuitry. I've deliberately used standard SSI gates and MSI decoders rather than PALs, GALs, PEELs, or other programmable logic devices. While those devices offer significant reductions in board space

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and wiring complexity, they tend to obscure the mechanics of what is really a fairly simple process.

Regardless of which programmable device I might pick, the majority of *Circuit Cellar INK's* readers won't have access to the programmer needed to produce it. But if I use garden-variety logic, you can implement the circuits with whatever devices you have on hand. There have been enough articles about programmable logic devices in these pages that you should have no trouble getting from here to there.

The Firmware Development board's circuitry divides neatly into three sections: a set of buffers to isolate the card from the bus, address decoding and timing circuitry, and the LED and switch interfaces. The first two account for most of the logic; only four ICs are devoted to the I/O devices.

BUFFERING THE BUS

Figure 1 shows the bus buffer circuits. The original IBM PC/AT bus specification allowed up to two LSTTL loads on each card, which the 74LS245 buffers handle quite nicely. ISA bus computers allow up to twice that load on each card, but if you are mixing logic families, be sure to calculate the actual currents for both high and low logic states.

In your own PC card designs, you may be to able omit the buffers on some lines because you know the exact loading. In fact, you may be able to get away with excessive loading on your custom card because you know it will be used in a system with only two other cards. However, that road is fraught with peril, as adding "just one more card" may push the load over the limit. Rule of thumb: conservative design eliminates sleepless nights.

Notice that the three LS245 transceivers used for the address and control lines are always enabled and wired to send the signals in only one direction. You could use LS541 buffers instead, but I'd rather have one less part number to worry about, particularly when LS245s are faster and less expensive.

The signals on the "in-board" side of the LS245s are prefixed with the letter "B" to indicate that they are buffered from the bus. I prefix low-active signals with a minus sign, but the references also use leading or trailing asterisks or front or back slashes. So much for standardization.

The two LS245 buffers on the data lines are enabled only when the address decode circuitry detects an I/O access to this card. When that happens, –BIOR determines the signal direction: data is driven onto the card unless the CPU is reading data from the card. There are only two other signals leaving the card: –IOCS16 tells the ISA bus interface that this card can handle 16-bit I/O accesses, and IOCHRDY can stretch those cycles to accommodate slow devices. It may seem strange to talk about slowing the cycles when we're investigating faster I/O, but I'll explain this in due time.

Both of the control outputs use 7407 open-collector drivers because all eight slots drive each signal. The pull-up resistors are on the system board,

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so the I/O cards need only pull the signals low to activate them.

ACCESS CONTROL

Figure 2 is more interesting because the logic actually does something useful. These few ICs determine the I/O addresses of the devices on the card and control the bus access timing.

Although the 80386SX CPU can access 64K I/O ports, most PC I/O cards decode only address bits A0 through A9. As with the 8088's 1 MB of RAM, the 1024 ports defined by those ten bits seemed like a lot at the time.

Over the last decade, most of those 1024 I/O addresses have been assigned to one device or another. It's a good idea to check the references to see who else is using "your" address before you hardwire your new card's logic. Often you can overlay a device you're sure you'll never use, but be careful if you are producing a commercial product: those old widgets are still out there lying in wait!

The Firmware Development board's default address range is 300 through 3 1 F, which corresponds to the ports on the original IBM prototype card. Just in case you already have a card at those addresses (you aren't trying this in your real PC, are you?), a set of jumpers defines the address range.

The 80386SX CPU and the ISA bus interface can handle all combinations of 8- and 16-bit accesses to even and odd addresses, but each board must include some logic to help out. Because I have complete control over the firmware, I decided to stay with 16-bit accesses at even addresses. As you'll see in upcoming columns, this does *not* mean the board cannot handle 8-bit devices, but it does simplify the logic.

The 74F521 IC compares address bits BA5 through BA9 with five jumper inputs and activates the -10 ADDRESS MATCH line when they coincide. That signal drives –IOCS16 to enable 16-bit accesses, which is the only difference between 8-bit and 16-bit cards.

Notice that F521 activates –IOCS16 during memory accesses when bits BA5–9 just happen to match the jumper settings. That's the way it's supposed to work, because the ISA bus interface ignores spurious –IOCS16 signals during memory accesses.

The two LS138 decoders combine the F521's output with four more address bits to identify each of the sixteen 16-bit ports in the card's address range. The –BIOR and –BIOW

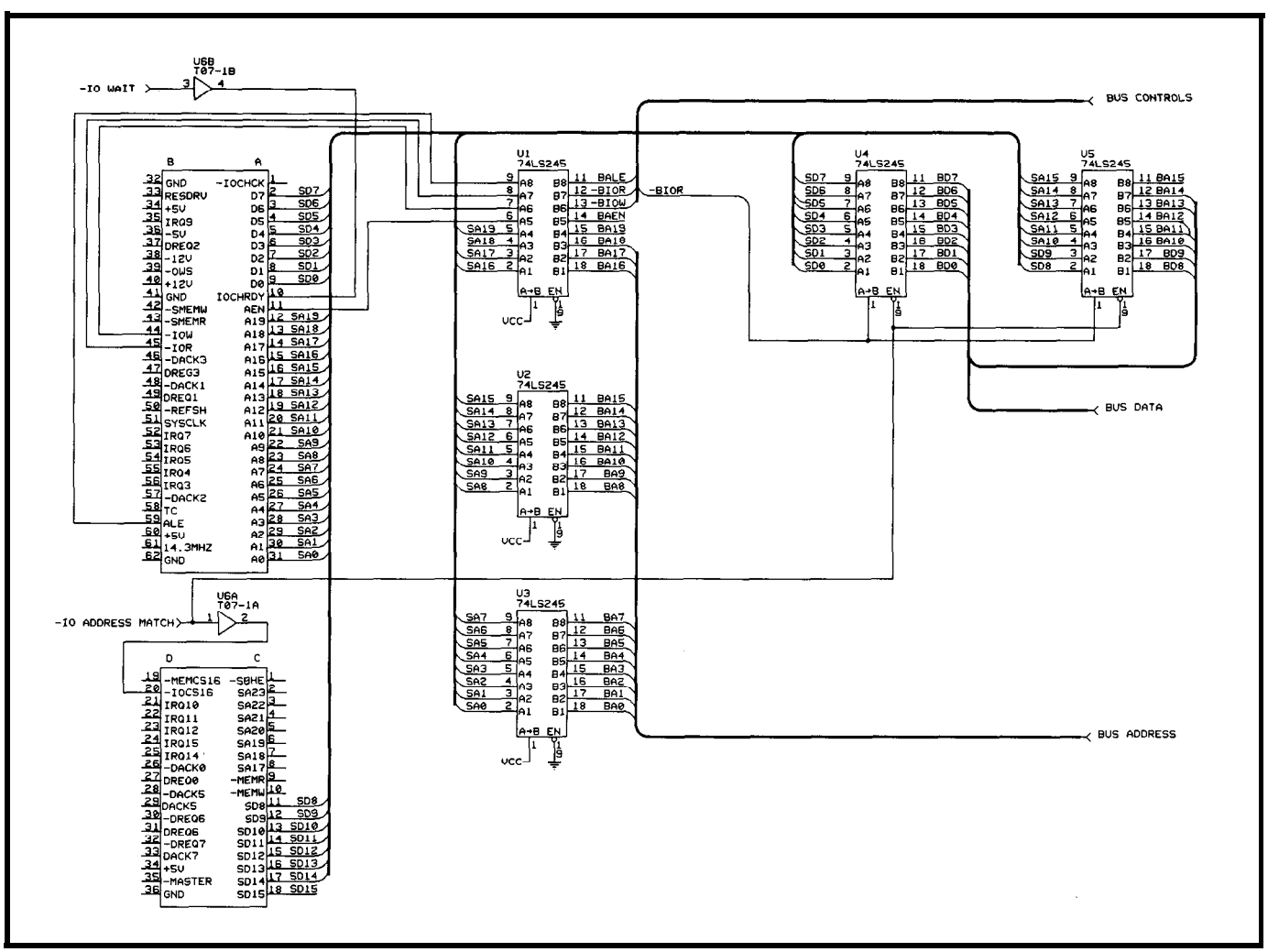


Figure I--The *I/O bus can drive a maximum of two (or four, if it's an ISA bus) low-power Schottky TTL loads. These buffers ensure that the other circuitry on the card doesn't exceed this limit. The LS245 transceivers on the address and control lines are hard-wired to drive the signals onto the card, while the data lines* must *be controlled by the address decoding circuitry.*

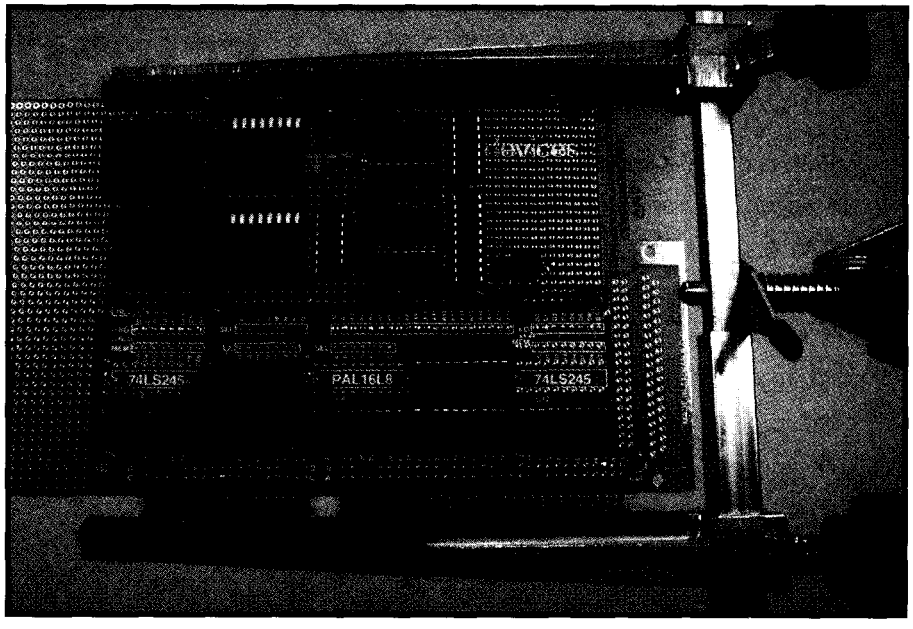


Photo 3—*The* **Firmware Development** *card is built on a JDR Microdevices prototyping card. The bus buffers are arranged parallel to the connectors. The address decoding and timing ICs are near the* **rear** *edge. Since the switch and LED circuits are so* **simple, most of the ICs are "overhead" that will also be used** *unchanged in future projects.*

signals enable the decoders, so the outputs indicate both address selection and bus timing.

The LS139 decoder combines the F521's output with only two address bits, so each output is active for four consecutive 16-bit ports. This chip will come in handy later on when we add ICs with several internal addresses; the chip select signals will come directly from this decoder.

In a real design you would use a programmable logic device to replace all four of these ICs. In effect, the PAL (or whatever) would implement a custom decoder with only the outputs you need. If you have access to a PAL programmer, feel free to adapt what you see here.

For cards that must handle both 8-bit and 16-bit accesses, consult the references to make sure you cover all the possibilities. This type of logic is hard to do with discrete gates, but is tailor-made for a PAL, which is one of the reasons I avoided it. In truth, though, the design you see here is just another example of a tradeoff between hardware and firmware.

The remaining circuit, the LS221 one-shot, is a step in the wrong direction: it triggers wait states to slow down the faster 16-bit I/O cycles. It's not essential for the circuits this month, but I decided to include a wait-state generator so you could experiment with it.

ESSENTIAL I/O

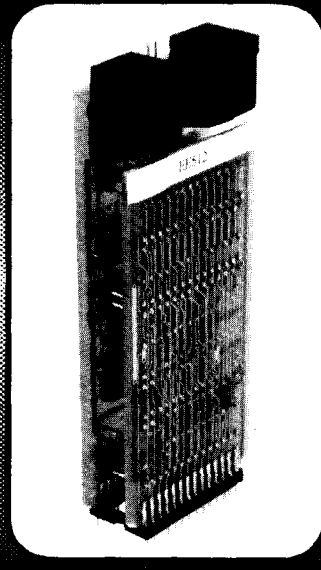
Figure 3 shows the two I/O devices, which are just enough to show that the card works. The LEDs provide a visible indication for the sixteen output bits and the switches control the input bits. Both ports are addressed at 31E/31F, but the LEDs are write-only and the switches are read-only.

You may use sixteen discrete LEDs instead of the two-digit, seven-segment display I picked. The firmware in upcoming columns will display error codes and status indications on these digits, but your application may be different.

Driving LEDs directly from an LS374 latch is unusual, but each output can sink up to 24 mA at normal logic levels. The 10 mA needed to light each segment is thus entirely acceptable. The digits have separate common anode connections that are both tied to the +5-V supply, with current-limiting resistors in series with each LED.

Note that the LS374 outputs cannot *source* more than a few milliamperes, so you cannot use common-cathode LED digits. I'll cover source and sink power drivers more appropriate for real-world applications later on.

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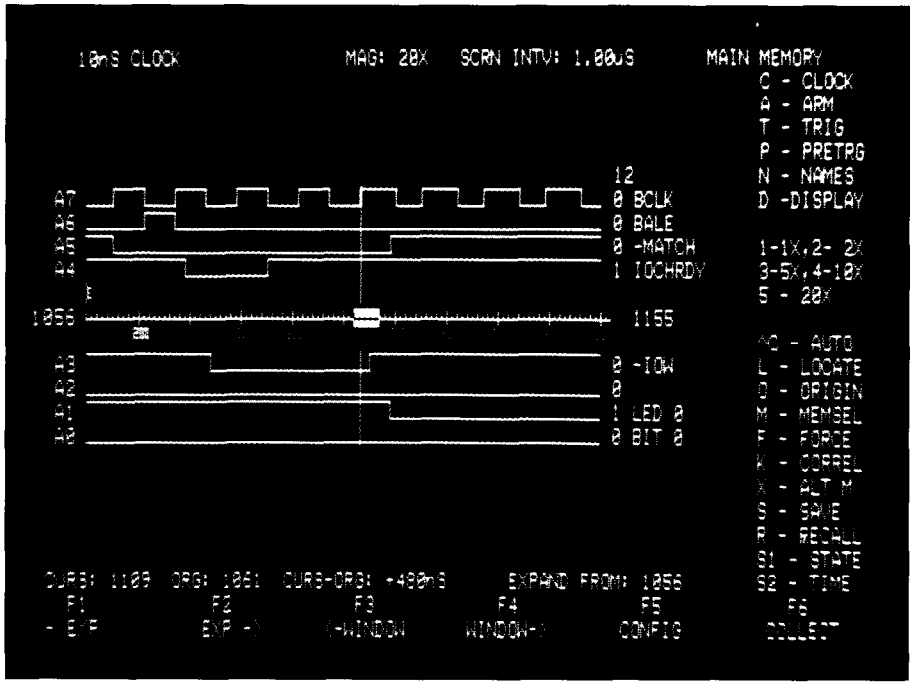


Photo 4—*When* the *IOCHRDY* line is *low,* 76 ns after *the -IOW pulse stark, the ISA bus circuitry will* add *wait states to the 16-bit access. This write takes four BCLK cycles* due *to* the *single waif state.*

STEPWISE CONSTRUCTION

Reading about all this is one thing, but experience is the best teacher. Get those soldering irons warmed up!

I used a JDR Microdevices proto type board as the basis for the circuitry shown in this column. The board etching includes a complete PAL-based bus interface, but I decided to present a slightly different and somewhat more general design. As a result, my board has several cuts and adds that match it to the schematics shown here.

You can also use a bare board (with no etched circuitry) similar to those made by Vector, but I strongly recommend ground and power planes covered by a good solder mask. Boards with etched buffer circuits reduce the number of wires you have to cut, strip, and solder enough to make them worthwhile, even if you don't use their address decoding circuitry.

One of the big advantages of designing a plug-in card for a PC is that you can use the computer to debug the card. I wrote porttest. C to exercise each section of the card as I built it. Proceeding step-by-step may not be as challenging as debugging the whole card at once, but the job gets done faster with less hassle.

The schematics soak up most of the room I normally use for program listings, but the code in Listing 2 should give you an idea of how to proceed. It exercises the LED digits with a visible test pattern so you can tell at a glance whether the hardware is working correctly.

You will, however, need an oscilloscope or logic analyzer to verify some of the tests. For example, checking the F521 comparator requires writing to addresses on the board as well as ones elsewhere, but the only way to see the pulses is on an oscilloscope or well-handled logic probe.

In any event, download the code and check it out before you begin construction. If you build the hardware in the same order as the tests, you should have no problems.

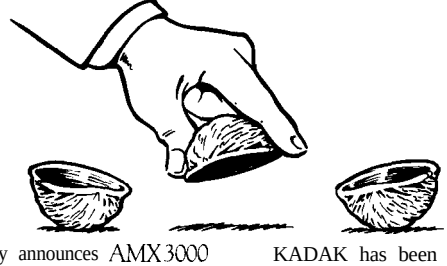
DELAYED I/O

The last section of porttest. C exercises the LS221 wait-state generator I mentioned earlier. Although the LS374 and LS245 ICs can keep up with normal 16-bit I/O rates, they also work with slower accesses. This makes them ideal experimental subjects: nothing can go wrong!

Most of the time you want I/O to run as fast as possible, but occasionally *you* must interface a device that

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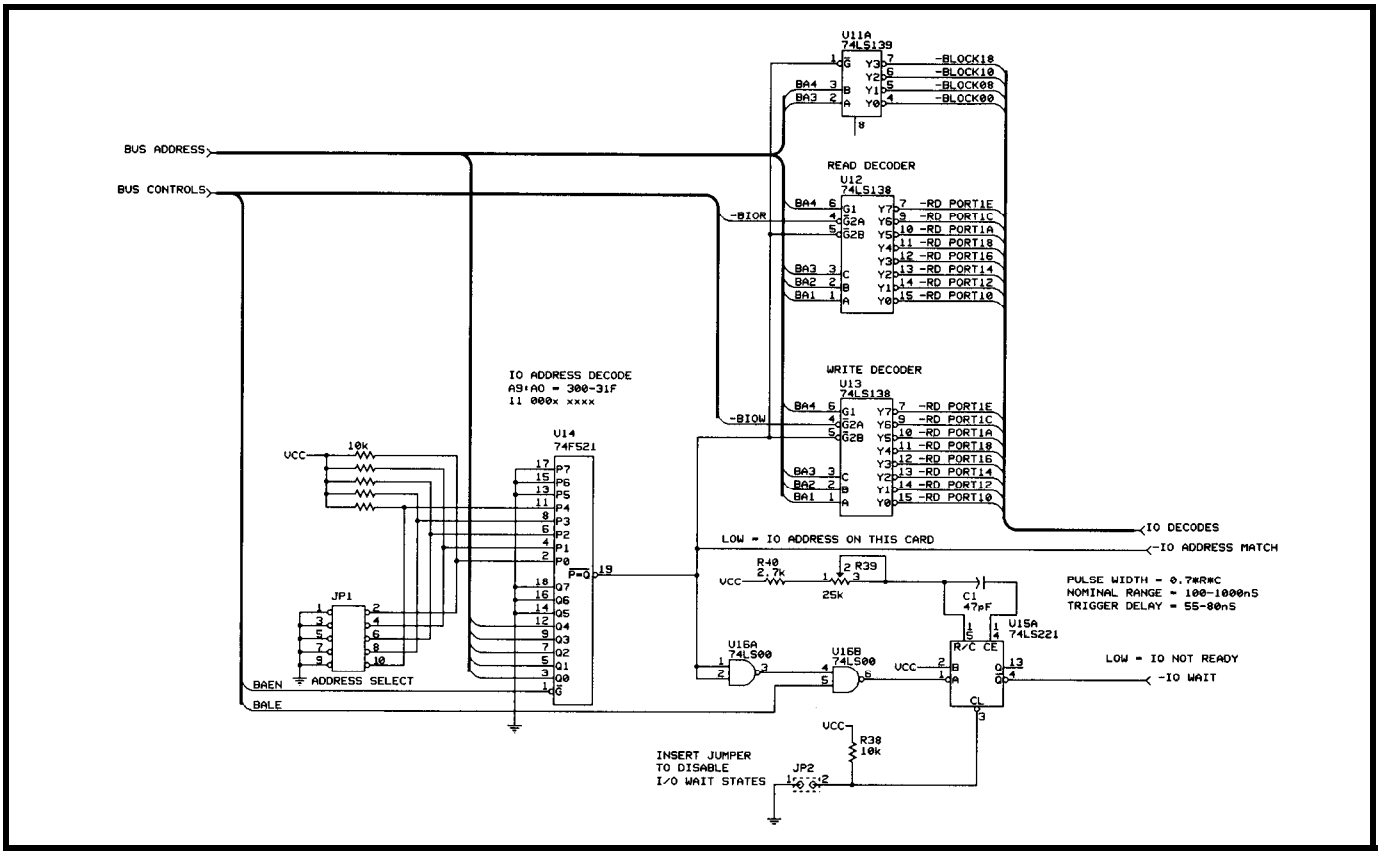


Figure 2-The card address decoders recognize when an I/O port is located on the card and activate the hardware corresponding to that port. Because this card contains on/y 16-bit pork (by definition), the card-selected signal activates the –IOCS16 signal shown in Figure 1 for all addresses on the card. The firmware must avoid 8- and 16-bit accesses to odd addresses.

cannot keep up with the normal bus rate. The IOCHRDY ("I/O Channel Ready") signal is the key to slowing things down.

If IOCHRDY remains high during an access, the ISA bus interface will complete the cycle normally. However, if it goes low ("I/O Channel not Ready"), the interface provides additional time. A pull-up resistor on the CPU board holds the line active ("Ready") so cards that don't need to use it can omit the circuitry entirely.

IOCHRDY must be pulled low within 76 ns after the leading edge of –IOW or –IOR during 16-bit accesses. The bus interface samples IOCHRDY on each rising BCLK edge, so the -IOR/IOW signals are extended in BCLK cycles of 120 ns each.

The LS221 has a maximum trigger delay of about 80 ns, which is far too slow to fire it directly from the –IOW/IOR signals. Instead, I opted for a genuine kludge: it's triggered from the falling edge of BALE when the I/O address comparator signals a match. Because the addresses are not stable during the early part of the BALE pulse, the LS221 may trigger if the F521 comparator glitches while the address settles.

It turns out that this glitch doesn't matter for our present purpose because the only effect is to slow down a bus cycle that should run at full speed. Because there is no data loss, I decided to overlook the glitches in the interest of producing a variable delay for this column.

Photo 4 shows a 16-bit write with one wait state. Compare it with Photo 2 to see how IOCHRDY affects the results. Of course, there is no way to see the slowdown by eye because the additional delay amounts to only 120 ns; the LEDs certainly won't look any different!

However, the wait-state calibrationroutinein `porttest.c` (see Listing 3) provides a way to adjust the number of wait states without a scope or logic analyzer. It consists of a test loop that counts the number of iterations completed in each 54.9-ms BIOS timer tick. As you increase the number of wait states by adjusting the trimpot on the LS221, the number of iterations decreases.

The components I chose for the LS221 limit the IOCHRDY pulse to 100-1000 ns, which should be enough for most devices. IOCHRDY must not be held low more than 15.6 µs during any access to prevent interference with the RAM refresh signals, so we're safe.

The number of iterations obviously depends on the CPU speed, but the 33-MHz '386SX I'm using completes 8080 [I'm not making this up!) iterations with no additional wait states. Remember to install the jumper that disables the LS221 before making this measurement, since component tolerances may produce a pulse long enough to trigger a wait state even with the trimpot fully counterclockwise.

Simple math: 54.9 ms divided by 8080 iterations tells you that each iteration takes about 6.79 µs. I counted 28 instructions in the assembler listing, so the CPU is trundling along at 4.1 million instructions per second

or about 243 ns per instruction. Each instruction is a multiple of the 30-ns CPU clock, so you can see that each instruction averages a little over eight CPU cycles.

Removing the jumper and adding one wait state drops the count to 7970 iterations and 6.89 µs per loop. The difference is 100 ns, which is somewhat less than the 120 ns you'd expect.

I think the difference is actually 90 ns, or three CPU cycles, due to the '386SX prefetch queue being empty when it encounters the OUT instruction. The CPU flushes the queue when it CALLs the `outpw()` routine and the instructions that get the address and data from the stack are fairly fast. As a result, the CPU is actually idle during part of the "no wait" OUT and the added wait state is partially overlapped with the prefetch delay for the next instruction.

Adding a second wait state produces 7830 iterations, or 7.01 µs per loop. The difference here is exactly 120 ns, which suggests that the prefetcher is back on track with the next instruction ready on time.

I'll leave it to you to continue adding wait states and calculating the results. The bottom line is that, even in this contrived example, each additional wait state adds less than 2% to the overall loop time. So little time is actually spent in the I/O operation compared to the other calculations that an additional 120 ns or four CPU cycles is no big deal.

Performance measurement on a complex CPU like the '386SX is not at all trivial, but this simple example shows that if you really care about the results, you have to make some careful measurements. I'll have some further examples in upcoming columns, but for background reading you should get a copy of Abrash's Zen of ***Assembly Language*** and commit the lessons to heart.

A digital delay line is the correct way to produce a short delay when you know how long it should be. Simply send –IOR/IOW through the delay line, XNOR the delayed output with the input, and drive IOCHRDY with the result. The pulse goes low when –IOR/

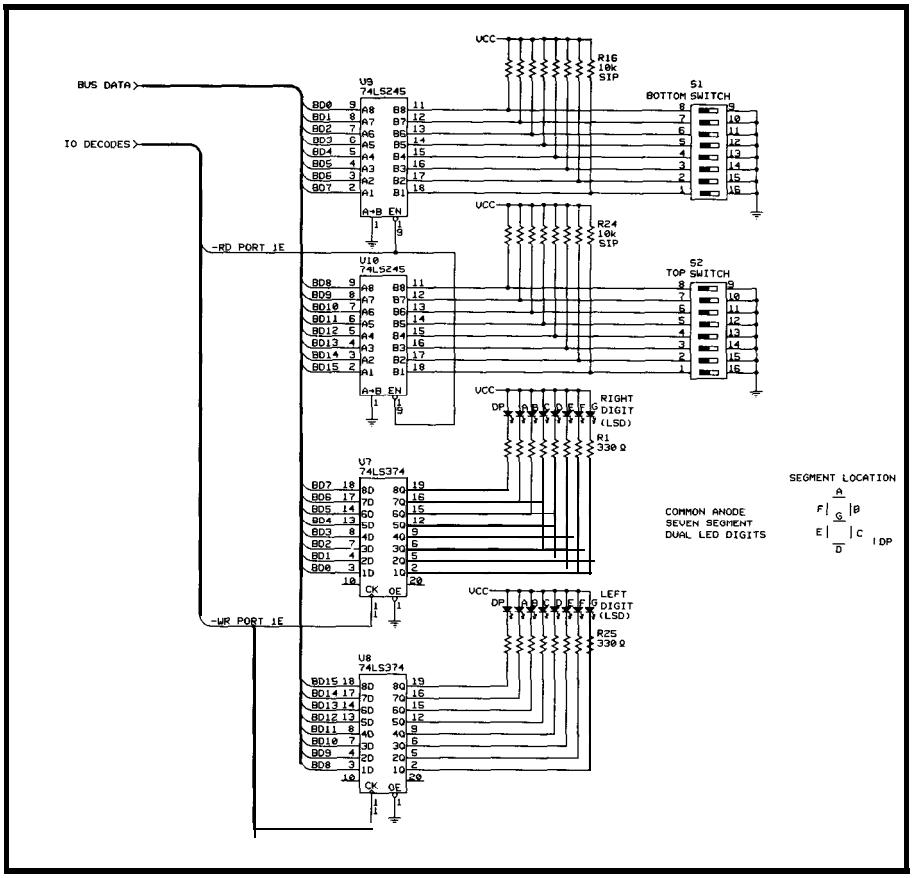


Figure 3-The *I/O* circuitry on the first cut of the board is the bare *minimum* needed to verify *that* the *buffers and address decoders are working correctly. The LEDs may be eifher common-anode, seven-segment digits as shown* or discrete diodes. You can use similar circuitry to build digital inputs and outputs to interface with the real world.

Listing 2—*Writing firmware to exercise new hardware simplifies the debugging process. This section of porttest.c b/inks the LED digits, then lights each segment in turn. Because fhe segments are driven direct/y from digital outputs without intervening seven-segment decoders, the firmware can control each segment independently. Simply watching the digits will reveal shorts or missing wires without any other test equipment.*

```
case  '3' :
 putstr("Single bit chasing through LED\n");
 putstr(" segment order is DP, then ABCDEFG\n");

 do {
    outpw(BOARD_BASE+LED_OFFSET,0xFFFF); /* all segments off */
    WaitTicks(10);
    outpw(BOARD_BASE+LED_OFFSET,0x0000); /* all segments on */
    WaitTicks(10);
    outpw(BOARD_BASE+LED_OFFSET,0xFFFF); /* all segments off */
    WaitTicks(10);
    outp(SYNC_ADDR,0x01);                /* sync on printer port */
    for (Counter = 0x8000; Counter; Counter >>= 1){
         outpw(BOARD_BASE+LED_OFFSET,~Counter);  /* bit low = on */
         WaitTicks(7);
         Option = chkch();
         if (Option) {
          break;
         }
    }
    outp(SYNC_ADDR,0x00);
    WaitTicks(10);
 } while (!Option);

 break;
```

Listing **3-Adding wait states to I/O reduces the bus** *speed so stower I/O devices can keep up. This test loop from porttest.c displays the number of* iterations *completed in a single 54.9 ms BIOS timer tick. Increasing the number of waif states decreases the number of iterations.*

```
while (!chkch()) {
    outp(SYNC_ADDR,0x01);                /* sync on printer port */
    NextTick = WaitTicks(1) + 1;         /* lock on next edge */
    Counter = 0;
    do {
        outpw(BOARD_BASE,Counter++);
    } while (peekw(0x0040,0x006C) != NextTick);
    outp(SYNC_ADDR,0x00);
    printf("Count %5u\r",Counter);
```

IOW goes low and returns high when the delayed signal arrives. You must include address decoding and so forth, but the output is a fast, low-delay, "controlled glitch" just long enough for your I/O device.

Check the Digi-Key catalog for a selection of delay lines; they run $10–$20 in single quantities depending on the delay, number of taps, and precision. You can see why I picked a one-shot for this adjustable delay, but I don't want you using an LS221 in your design just because you saw it here!

RELEASE NOTES

Although I've spent more time on hardware than firmware this time, the programs I used to debug the machinery are available on the Circuit Cellar BBS. As before, I used Micro-C and you can load the **H E X** files with the MO N 8 6 debugger or put the **B** I N files on a diskette with the issue 3 1 boot loader.

Next month, I'll look at interrupt handlers by adding an 8254 timer to the card and explore how to resolve the conflict between IBM's and Intel's interrupt assignments.

Ed Nisley is a Registered Professional Engineer and a member of the Computer Applications Journal's engineering staff. He specializes in finding innovative solutions to *demanding technical problems.*

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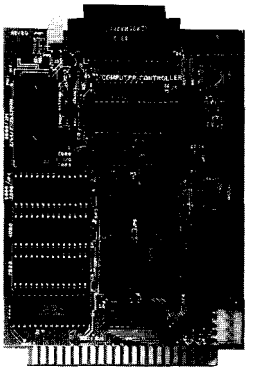
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You Can Count On It

FROM THE BENCH

Jeff Bachiochi

Building on the seven-segment LED display panel he presented last month, Jeff explores some of the potential applications for this versatile output device.

It looks as though "Deep Space Nine" might be taking the place of "Next Generation" next season. True to form, the character development on "DS9" is quickly building a cohesive cast which will silently move in on the Enterprise's reign. Unfortunately, many of us will be forced into obtaining a "Next Gen fix" through syndication reruns. Last night we were watching "Star Trek VI" and my son Ryan asked me if the Enterprise (NCC1701-A) had food replicators, like the "Next Generation" Enterprise (NCC 1701 -D). Without thinking I answered, "Yes, they did have them back then (on the older Enterprise]." He quickly retorted, "Back then? Er, dad, do you know what year this is!" Reality check.

We all need a reality check now and again. But it's certainly no help to ask, "What issue are we on?" around the *CAJ* offices. No two people will give the same answer since we've gone monthly. Every department is working on a different issue, or two, or three! What is necessary is a point of reference. If you haven't seen last month's issue (#32), then start there. Else.. .

START <HERE>

Last month, I discussed a simple and inexpensive eight-digit seven-segment display. You may already have found a use for it. It is a one-chip circuit based on Maxim's MAX7219 IC and will drive up to eight seven-segment displays from a synchronous serial data stream. The circuit is small and the component costs are low. Now let's look at a few of the possible uses for a display of this type using a 68HC705K1 micro as the base (for more on the 68HC705K1, see "From the Bench" in the December '92/ January '93 issue of the ***Computer Applications Journal).***

I. HCS

My first thoughts were of the HCS II presented in issues 25 and 26 (February/March and April/May 1992). When power interruptions occur, every digital clock in my house throws up its hands (or digits, as the case may be) and resets itself. If this should happen overnight, the flurry of activity the next morning is indescribable, especially with a family of six. I'm sure you've been there.

The HCS does not forget the proper time, however, if you don't have your PC dedicated to displaying HOST's status screen, then you can't tell the time anyway. One of the functions slated to be included in the next version of XPRESS is the ability



Photo **1**—*All* the extra processor *and interface circuitry fits right inside the LED display panel's enclosure.*



Photo 2—By making the display panel appear to the HCS II Supervisory Controller like an LCD-Link, you can use it to display the system time.

to attach the time and date to a network message for logging purposes. If I could imitate the LCD-Link on the HCS network, this info could be captured and displayed with my interface. No direct support for this link would have to be added to the Supervisory Controller, which would make Ken one happy guy. A remote time and date display could also deliver messages, although rather cryptic because of the display's limitations. It is also a good way to keep your finger on the pulse of the system to assure yourself it's feeling fine.

Starting with the basic display circuit described last month, add a '705K1 micro and RS-485 converter (RS-232 could be used for stand-alone operation) as shown in Figure 1. The HCS network requires RS-485 for communications. The microcontroller listens to network traffic, waiting for its link address to be broadcast. When it's recognized, the ASCII string which follows is converted and inserted into a digit buffer. The digits are transferred as clocked data to the display.

Serial input is directed to IRQ, which produces an interrupt upon the leading edge of the first bit. The interrupt routine retains control until a complete character has been received. Characters are checked to make sure they fulfill the proper pattern for address recognition or the recognition cycle is restarted. Once a proper ID (net address) is confirmed, all remaining characters up to the carriage return are converted to the appropriate numerical data. Characters O-9, H, E, L, P, –, and <space> are legal. All other characters are converted to blanks. All characters are shifted left FIFO style, so only the last eight will be displayed. Once the carriage return is received, the last eight converted characters are transferred to the display's circuitry. Now the micro is ready to handle the next network message.

II. FREQUENCY COUNTER

Don't have an HCS II you say? Not to worry. How about adding a miniature hand-held frequency counter to go with your logic probe and pulse generator? Hold on, this won't determine what bus speed your PC is running, but it's not too shabby considering the '705K1 has no counters. Instead, a' software loop samples the IRQ line and increments a

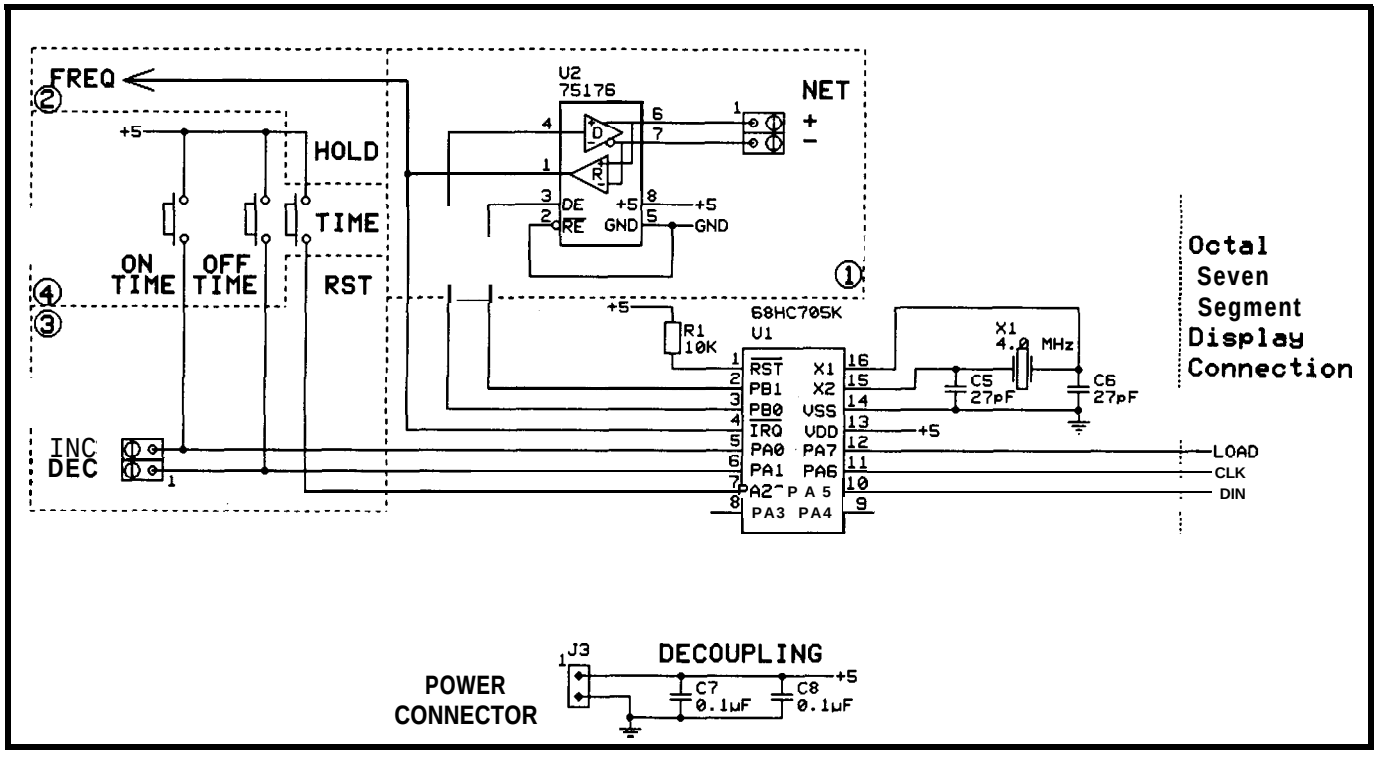


Figure I-By adding a sing/e-chip microcontroller (the 68HC705K1), an RS-485 converter, and some push buttons, the formerly dumb display panel can be used as a stand-a/one device in any number of applications.

register for each full cycle (a logic low state and a logic high state).

The loop doesn't use IRQ as an interrupt, but takes advantage of branch instructions specific to the IRQ input pin: BIL and BIH. Two additional instructions are needed: ADD 1 (add 1 to the accumulator) to keep track of the cycles and BRSET (branch on bit set) to exit the loop. These four instructions require 13 machine cycles-five for the first half cycle and eight for the second. Execution speed is 500 nanoseconds per cycle, which means the maximum theoretical frequency we could count would be 8 x 500 ns or 4 µs for each half cycle. At a period of 8 ps, that would be 125 kHz.

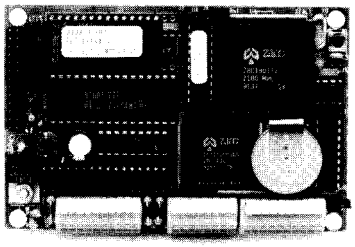
To ease the conversion of period to frequency, I choose to keep track of the cycles for 1 ms and then multiply the total by 1000 (add three zeros). This gives a fairly gross value for frequency, but allows for the capture of the highest possible frequency. Expanding the loop to overflow into an additional register would allow a more

Listing 1--The *basic "write to the display" routine using two* d-bit writes.

```
; SEND THE 16-BIT WORD WORDHI/WORDLO
;
SENDW     LDA     WORDHI          ;MSBYTE (MSBIT) FIRST
          BCLR    LOADF,BITFLGS ;NO LOAD FLAG
          BSR     SB              ;SEND A BYTE
          LDA     WORDLO          ;LSBYTE (LSBIT) LAST
          BSET    LOADF,BITFLGS ;THIS TIME WITH LOAD
          BSR     SB              ;SEND A BYTE
          RTS                     ;RETURN FROM SUBROUTINE
;
SB        LDX     #00001000Q      ;SENDING EIGHT BITS
SB2       DECX
          ROLA                    ;ROTATE DATA INTO CARRY
          BCS     SB_C            ;BRANCH IF CARRY SET (DATA BIT=1)
SB_NC     BCLR    DIN,PORTA       ;NO CARRY SO CLEAR DIN
          BRA     SB3             ;BRANCH
SB_C      BSET    DIN,PORTA       ;CARRY SO SET DIN
SB3       TSTX                    ;TESTING X
          BSET    CLK,PORTA       ;SET CLK BIT
          BNE     SB4             ;LAST BIT NO BRANCH
SB_LSB    BRCLR   0,BITFLGS,SB4 ;YES LOAD FLAG CLEARED
                                  ;NO BRANCH
SB_LOAD   BSET    LOAD,PORTA      ;YES SET LOAD BIT
          BCLR    CLK,PORTA       ;CLEAR CLK BIT
          BCLR    LOAD,PORTA      ;CLEAR LOAD BIT
          BRA     SB5             ;BRANCH
SB4       BCLR    CLK,PORTA       ;CLEAR THE CLK BIT
SB5       TSTX                    ;TESTING X
          BNE     SB2             ;LAST BIT -NO- BRANCH FOR ANOTHER
          RTS                     ;YES, RETURN FROM SUBROUTINE
```


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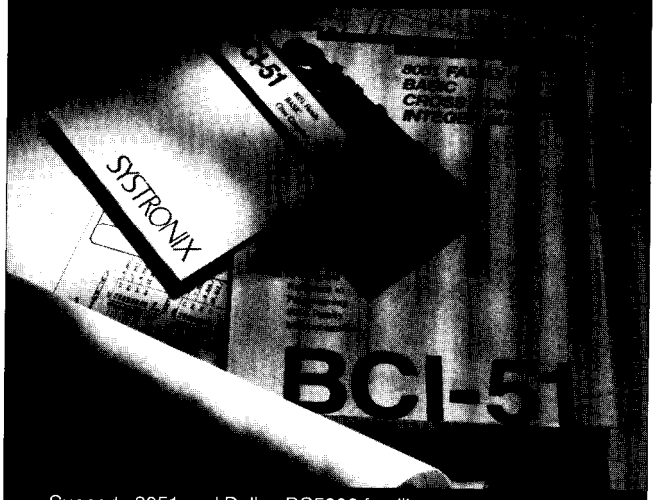
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Listing 2-A *100-ms* sample is taken *to determine whether the input frequency is above or below 60 kHz.*

```
; BEGIN A SAMPLE COURSE

MAIN  BRCLR  SAMPLE,PORTA,MAIN        ;LOOP HERE UNTIL BUTTON IS
                                      ; PUSHED
      LDA    #MS1L          ;1MS COUNTDOWN LOW BYTE
      STA    TIMEL
      LDA    #MS1H          ;1MS COUNTDOWN HIGH BYTE
      STA    TIMEH
      LDA    #00101000Q     ;SET TOIE AND TOFR
      ORA    TCSR
      STA    TCSR

M1_L1 BRCLR  TOF,TCSR,M1_L1   ;LOOP TIL TOF (TIMER OVERFLOW)
      LDA    #MS1           ;1MS COUNTDOWN FRACTION

M1_L2 CMP    TCR            ;HAS THE TIMER REACHED THE FRACTION

      BHS    M1_L2          ;NO   LOOP
      LDA    #00001000Q     ;YES OK NOW COUNTING RESET TOFR
      ORA    TCSR
      STA    TCSR
      CLI                   ;GLOBAL ENABLE
      CLRA                  ;START AT ZERO INPUT CYCLES

M1_L3 BIL    M1_L3          ;LOOP HERE IF INPUT IS LOW
      ADD    #1             ;INCREMENT CYCLE COUNTER

M1_L4 BIH    M1_L4          ;LOOP HERE IF INPUT IS HIGH
      BRCLR  OVERF,BITFLGS,M1_L3    ;BRANCH BACK TO CYCLE LOOP IF
                                    ; NO TIMEOUT FROM INTERRUPT

MAIN2 SEI                   ;TIMEOUT HAS OCCURRED SO STOP INTERRUPTS
      BCLR   OVERF,BITFLGS;CLEAR FLAG
      CMP    #60T           ;CYCLE COUNTER OVERFLOW
      BLS    MAIN4          ;BRANCH IF GROSS COUNTER < 60
      STA    TIMEL          ;STORE THE CYCLE COUNTER  IN THE LOW BYTE
      CLR    TIMEH          ;HIGH BYTE IS 0
      LDX    #2             ;CONVERT HUNDREDS AND TENS ONLY

      LDA    #0FH           ;START WITH A BLANK DIGIT
      STA    DIGPNTR

MAIN3 JSR    CONV1          ;CONVERT FROM HEX TO BCD

      JSR    SCHR           ;SAVE BCD DIGIT
      INCX                  ;NEXT PLACE
      CPX    #4             ;FINISHED?
      BNE    MAIN3          ;NO  CONVERT  ANOTHER
      LDA    TIMEL
      STA    DIGCNTR
      JSR    SCHR
      CLR    DIGCNTR        ;YES GET A "0"  DIGIT
      JSR    SCHR           ;SAVE BCD "0"
      JSR    SCHR           ;AGAIN
      JSR    SCHR           ;ONCE MORE
      BRA    MAIN7          ;DO DISPLAY OF DIGITS


; <60 kHz  FINE  SAMPLE

MAIN4 LDA    #MS1000L       ;1 SEC COUNTDOWN LOW BYTE
      STA    TIMEL
      LDA    #MS1000H       ;1 SEC COUNTDOWN HIGH BYTE
      STA    TIMEH

M4_L1 BRCLR  TOF,TCSR,M4_L1           ;WAIT FOR TOF
      LDA    #MS1000        ;1 SEC COUNTDOWN FRACTION
```

(continued)

accurate count, but at the same time it would expand the loop to the point where the maximum frequency would be only five digits.

To help get both maximum frequency and precision, I chose to use a gross conversion unless it determined the frequency was less than 60,000 Hz. If it is, a second routine using two registers is used and the count is made over the period of 1 second. This count is equal to the actual frequency.

Converting the 8- or 16-bit hexadecimal counts into BCD digits is performed by successive subtractions using hexadecimal equivalents of 10000, 1000, 100, and 10, with the remainder as the last BCD digit. Leading zeros are replaced with blank segments. Lastly, the characters "H2" are appended. The "2" simulates a "Z" in the abbreviation for Hertz.

After using this gizmo, I added a push button on port A bit 0 to initiate the count cycle. The last count is displayed until the next one is called for by a press of the button. Continuous conversions are still available if you simply hold the "Start" button.

III. ACCUMULATOR

Data logging can be as complex as keeping track of what has happened when, and why. It also can be as simple as counting events. In the third example, I use the '705K1 as a totalizer. Events (low-to-high excursions) increment a bank of eight BCD registers. I chose to use individual BCD registers here so I wouldn't have to convert from a hexadecimal total to BCD digits. Since I wasn't looking for 10-µs counting speed, the longer loops used in BCD rollovers were not going to be a problem.

To make things a bit more interesting, I decided to use three inputs: increment, decrement, and reset. One advantage the '705K1 has in its favor is the alternative use of Port A's bits O-3. These four pins can be linked into the IRQ mechanism and function as wire ORed interrupts. This is setup through the MOR register bit 2 (PIRQ). A high bit enables PAO-3 as external interrupt sources. After a reset, port A has pull-down transistors

Listing 2—*continued*

```
M4_L2 CMP     TCR             ;HAS THE TIMER REACHED THE
                              ;  FRACTION

      BHS     M4_L2           ;NO   LOOP
      LDA     #000010000Q     ;YES  RESET  TOF
      ORA     TCSR
      STA     TCSR
      CLI                     ;GLOBAL ENABLE
      CLRA                    ;START AT ZERO INPUT CYCLES
      CLRX

M4_L3 BIL     M4_L3           ;WAIT IF INPUT IS LOW
      INCA                    ;INCREMENT LOW COUNT
      BNE     M4_L4           ;BRANCH IF LOW COUNT IS
                              ;  NOT  ROLLOVER
      INCX                    ;OTHERWISE INCREMENT HIGH
                              ;  COUNT
M4_L4 BIH     M4_L4           ;WAIT IF INPUT IS HIGH
      BRCLR   OVERF,BITFLGS,M4_L3     ;BRANCH IF NO TIME UP

MAIN5 SEI                     ;TIMEOUT HAS OCCURED
                              ;  SO STOP MORE INTERRUPT
      BCLR    OVERF,BITFLGS;CLEAR FOR NEXT SAMPLE
      STA     TIMEL           ;STORE CYCLE COUNTER IN
                              ;  LOW  BYTE
      STX     TIMEH           ;HIGH BYTE
      CLRX                    ;CONVERT ALL PLACES (5)
      LDA     #0FH            ;BLANK
      STA     DIGCNTR
      JSR     SCHR            ;SAVE A LEADING BCD

MAIN6 JSR     CONV1           ;DO PLACE CONVERSION FROM
                              ;  HEX  TO  BCD
      JSR     SCHR            ;STORE THE BCD
      INCX                    ;NEXT PLACE
      CPX     #4              ;FINISHED?
      BNE     MAIN6           ;BRANCH FOR MORE PLACE
                              ;  CONVERSIONS
      LDA     TIMEL           ;REMAINDER IS LAST DIGIT
      STA     DIGCNTR
      JSR     SCHR

MAIN7 LDA     #0CH            ;"H"
      STA     DIGCNTR
      BSR     SCHR            ;STORE "H"
      LDA     #2              ;"2 (Z)"
      STA     DIGCNTR
      BSR     SCHR            ;STORE "2" AS A "Z"
```

Listing 3-f *PORTB.1 is tied high, then a 128-ms contact bounce delay is added to the INC, DEC, CLEAR routine. If the bif is not tied high, TTL inputs are assumed and rapid counting is possible.*

```
;  EXTERNAL  INTERRUPT  BUTTON  PUSHED

EXTINT    LDA     PORTA               ;STATE OF THE INPUTS
          BRCLR   PB.1,PORTB,NODELAY  ;SKIP IF PORTB.1=0
          CLRX                        ;MAX DELAY (128 ms)

DELAY     BRCLR   TOF,TCSR,DELAY      ;WAIT FOR OVERFLOW
          BSET    TOFR,TCSR           ;CLEAR IT
          DECX
          BNE     DELAY               ;FINISHED  NO  GO  BACK

NODELAY   RORA                        ;PORTA.O INTO CARRY
          BCC     CHK1                ;BRANCH IF NOT INCREMENT
```

enabled which will keep these inputs at logic low unless otherwise affected by an external source. The first three inputs are used as increment, decrement, and clear inputs, and can be push buttons or TTL-level signals. A rise to logic "1" will cause an interrupt and a branch to the appropriate routine which depends on port A's bit status.

The interrupt routine is responsible for keeping track of the appropriate counts. Seven segments of the display are used for the count 0–9,999,999 and the eighth is used to indicate when the count is negative. So the actual count is –9,999,999 to 9,999,999. If by slim chance the count overflows, a decimal point is turned on to alert the user that overflow has occurred and the count should not be trusted. Asserting the clear input brings the count back to zero. Leading zeros are converted to blanks to increase legibility.

Another possibility might include dividing the display up into two separate sections of four digits each. Two inputs could be used to increment counters individually. Or, multiple counters could be used internally and an additional input or inputs could select which counter is displayed.

IV. TIME-OF-DAY CONTROL

The final example started out as a countdown timer which would turn a relay on or off. Before I was finished, however, it had evolved into a time-of-day (TOD) controller. The 24-hour clock displays in "HH.MM.SS" format. Two output bits are presented in complementary fashion for the greatest flexibility and can be used to control a relay drive transistor. The '705K1 can sink 8 mA, but it's not enough to directly sink a 5-V relay. A TOD match between the present time and the "on" time sets port B bit 0 and clears port B bit 1 while an "off" TOD match clears port B bit 0 and sets port B bit 1. Three push buttons are used to set the present, on, or off TOD.

The internal RAM size of 32 bytes played havoc with this program. I had to shrink each of the three TOD settings down to three bytes each (hours, minutes, and seconds) to keep

the stack from crashing into them. It was a constant battle to balance the available stack space with the limited code size (400 bytes] by trading off stack-hungry subroutines for lengthy straight-line code.

I chose a 4.096-MHz crystal for this example because the timer's 8-bit register is read only. This limitation makes it impossible to adjust timer overflow interrupts by the normal reload methods. This crystal, though a bit above the maximum frequency of 4 MHz, causes timer overflows every 500 µs.

Setting the times is accomplished through the external push buttons: one for the on time, one for the off time, and one for the present time. When a button is pressed, the seconds, minutes, or hours are incremented until the button is released. Once set, the on and off times are compared to the present time once a second and the outputs [port B) change whenever a match occurs.

OUT OF TIME

I'm convinced. There's a lot of power in one of these micros. Although it could be better demonstrated at the hands of a real programmer, I'm pleased with the hoops I've made it jump through. Then again, I'm not entirely sure it wasn't me doing the jumping. ❑

Jeff Bachiochi (pronounced "BAH-key-AH-key") is an electrical engineer on the Computer Applications Journal's engineering staff. His background includes product design and manufacturing.

SOFTWARE

Software for this article is available from the Circuit Cellar BBS and on Software On Disk for this issue. Please see the end of "ConnecTime" in this issue for downloading and ordering information.

I R S

416 Very Useful
417 Moderately Useful
418 Not Useful

Listing 4—*The* initial *button* press *(1,2,3)* chooses *"on* time," *"off time," or* 'present time." The *second* press *(1,2,3) increments the seconds, minutes, or hours until the button is released.* Pressing multiple *buttons* terminates the *routine.*

```
; EXTERNAL PUSH BUTTON ROUTINE NONINTERRUPT

; SET ON TIME, OFF TIME, OR PRESENT TIME THROUGH PAO-2
; USES A. X, WORDLO, CHKLIM, DIGCNTR, WORDHI
;
EXTINT      RORA                    ;PORTA (BUTTON STATUS)
            LDX     #00H            ;START WITH ON TIME POINTER
            BCS     SET_S           ;FIRST BUTTON PUSHED
                                    ;YES  BRANCH
            RORA                    ;NO ROTATE IN NEXT  BUTTON
            LDX     #03H            ;OFF TIME POINTER
            BCS     SET_S           ;SECOND BUTTON PUSHED
                                    ;YES  BRANCH
            LDX     #06H            ;NO MUST BE THIRD
                                    ;POINT TO PRESENT TIME
            BRA     SET_S           ;BRANCH

SET1        CMP     #03H            ;CHECK FOR MULTIPLE BUTTONS
                                    ; PUSHED TOGETHER
            BEQ     SET2            ;YES  BRANCH
            CMP     #05H
            BEQ     SET2
            CMP     #07H
            BEQ     SET2
            CMP     #01H            ;NO CHECK FOR FIRST
                                    ; BUTTON ONLY
            BEQ     SET_S           ;YES BRANCH TO SET SECONDS
            CMP     #02H            ;NO CHECK SECOND BUTTON
            BEQ     SET_M           ;YES BRANCH TO SET MINUTES
            CMP     #04H            ;NO CHECK THIRD BUTTON
            BEQ     SET_H           ;YES BRANCH TO SET HOURS

SET2        JMP     MAIN4           ;FINISHED LEAVE

SET_S       CLR     WORDHI          ;SET SECONDS ROUTINE
            INC     WORDHI          ;SECONDS DISPLAY REGISTER
            LDA     #60T            ;60 SECONDS CAUSES OVERFLOW
            STA     CHKLIM
            BSR     SPAIR           ;BRANCH TO
                                    ; SET PAIR ROUTINE
            BRA     SET1            ;GO CHECK BUTTON STATUS

SET_M       LDA     #04H            ;SET MINUTES ROUTINE
            STA     WORDHI          ;MINUTES DISPLAY REGISTER
            INCX                    ;POINT TO MINUTES
            LDA     #60T            ;60 MINUTES CAUSES OVERFLOW
            STA     CHKLIM
            BSR     SPAIR           ;BRANCH TO SET PAIR ROUTINE
            DECX                    ;POINT BACK TO SECONDS
            BRA     SET1            ;GO CHECK BUTTON STATUS

SET_H       LDA     #07H            ;SET HOURS ROUTINE
            STA     WORDHI          ;HOURS DISPLAY REGISTER
            INCX                    ;POINT TO HOURS
            INCX
            LDA     #24T            ;24 HOURS CAUSES OVERFLOW
            STA     CHKLIM
            BSR     SPAIR           ;BRANCH TO SET PAIR ROUTINE
            DECX                    ;POINT BACK TO SECONDS
            DECX
            BRA     SET1            ;GO CHECK BUTTON STATUS

; SET A DIGIT   USING PAO-2
; ENTRY WORDLO=DIGIT# CHKLIM=MAXIMUM BCD DIGIT
;  USES  A,  DIGCNTR, WORDHI
```

(continued)

Listing 4—*continued*

```
SPAIR       BRCLR   PAUSEF,BITFLGS,SPAIR    ;SET PAIR (OF DIGITS)
                                            ; AND PAUSE 512 µs
            BCLR    PAUSEF,BITFLGS
            LDA     #0FH            ;GET A BLANK CHARACTER
            STA     WORDLO
            JSR     SENDW           ;SEND IT TO THE DISPLAY
            INC     WORDHI          ;INCREMENT DIGIT
            JSR     SENDW           ;AND BLANK IT TOO
            DEC     WORDHI          ;BACK A DIGIT
            JSR     DT              ;GO DISPLAY THE REAL DIGITS
            DEC     WORDHI          ;BACK A DIGIT AGAIN
            LDA     PORTA           ;GET PRESENT BUTTON STATUS
            AND     #7
            BEQ     SXIT            ;BUTTON STILL PRESSED
                                    ;NO  BRANCH
            JSR     IPAIR           ;YES GO INCREMENT THE PAIR
            BRA     SPAIR           ;BRANCH BACK

SXIT        ORA     PORTA           ;OR ANY BUTTON PRESSES
            BRCLR   TIMEF,BITFLGS,SXIT      ;BRANCH UNTIL 1
                                            ; SECOND PASSES
            BCLR    TIMEF,BITFLGS
            AND     #7
            BEQ     SXIT            ;HAVE ANY BUTTONS BEEN
                                    ;PUSHED NO KEEP LOOKING
            RTS                     ;YES RETURN FROM SUBROUTINE


; INCREMENT DIGIT PAIR
; ENTRY X=OFFSET FROM ON TIME CHKLIM=OVERFLOW VALUE OF PAIR
; O=ON TIME 3=OFF TIME 6=PRESET TIME
; USES A

IPAIR       LDA     ONTIME,X        ;INCREMENT (DIGIT) PAIR
            INCA
            CMP     CHKLIM          ;REACHED TO LIMIT
            BLO     IPAIR_2         ;NO  BRANCH
            CLR     ONTIME,X        ;YES ZERO THE TIME
            BRA     IXIT            ;BRANCH

IPAIR_2     STA     ONTIME,X        ;STORE NEW TIME

IXIT        RTS                     ;RETURN FROM SUBROUTINE


; DISPLAY TWO DIGITS
; ENTRY X=OFFSET FROM ON TIME WORDHI=1ST OF TWO DIGITS
; O-ON TIME       3-OFF TIME      G-PRESENT TIME
; USES A, X, WORDHI, WORDLO, DIGCNTR
;
DT          LDA     ONTIME,X        ;DISPLAY TWO (REAL) DIGITS
            CLR     DIGCNTR

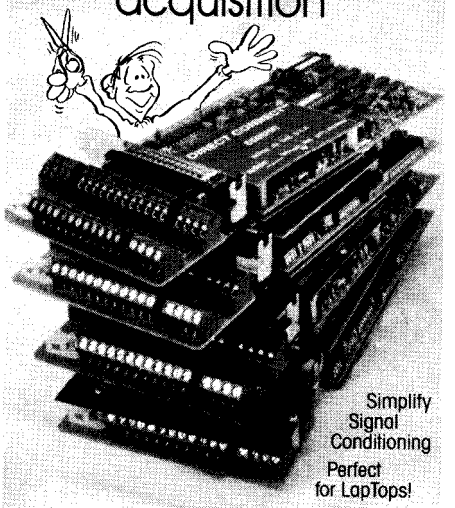
DT_2        CMP     #10T            ;DIVISIBLE
            BLO     DT_3            ;NO  BRANCH
            INC     DIGCNTR         ;YES INCEMENT  DIVIDEND
            SUB     #10T            ;SUBTRACT DIVISOR
            BRA     DT_2            ;BRANCH FOR ANOTHER

DT_3        STA     WORDLO          ;REMAINDER ONES DIGIT
            JSR     SENDW           ;SEND TO DISPLAY
            INC     WORDHI          ;NEXT DIGIT
            LDA     DIGCNTR         ;TENS
            STA     WORDLO
            JSR     SENDW           ;SEND TO DISPLAY
            RTS                     ;RETURN FROM SUBROUTINE
```


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#135

RISC Faces Reality—And Reality Blinks

SILICON UPDATE

Tom Cantrell

For embedded systems designers who want a versatile, yet inexpensive, RISC processor, the AMD29205 proves to be a solid contender with its low power consumption and small size.

Oast month I pointed out how the twin forces of ever more complex applications and the desire to program in C are conspiring to push our near-and-dear 8-bit chips to the limit.

If the 64K barrier is cramping your style, you're going to have to make the big move to a 4-GB (i.e., 32-bit programmer's model] chip. The good news is you have the opportunity to start with a clean slate and choose from a variety of new contenders.

Among your choices are any number of so-called "embedded RISC" chips. Surely, you've been inundated with the RISC hype of the past few years. With so much smoke, there must be a fire, right?

Longtime readers will know where I'm coming from. In "RISC vs. Reality" *(Circuit Cellar INK,* issue #1}I, while carefully acknowledging the basic merits of RISC, pointed out that the propaganda promulgated by its proponents had become so extravagant as to make the term about as useful as the "New and Improved" label on soap.

Later, in "Nuts About RISC" *(Circuit Cellar INK,* issue #23}, I took a few jabs at the then nascent "embedded RISC" concept using the analogy of a UNIX Toaster. At the same time, I gave credit to the ARM Acorn RISC, which actually came closer than more well-known chips to meeting the needs of cost- and power-sensitive designers.

Well, I'm pleased to report that the concept of embedded RISC is finally getting real. The chip suppliers, realizing that the total UNIX workstation market only consumes as many CPUs in a year as the embedded arena in a day, are at last starting to get it.

LIGHTENING THE LOAD

Like many other RISCs, the AMD 29205 is derived from a UNIX chip (the 29000). In general, chips designed to power a UNIX workstation all share the same problems when seeking employ in high-volume, cost-sensitive applications.

Two key factors that influence all other design decisions are the need to reduce system cost and power consumption. It's hard enough to sell a $100 chip into $200 applications, and calling for a hefty power supply and fans doesn't help.

A key way to reduce chip and system cost is to jettison an expensive high-pin-count ceramic package in favor of a lower-pin-count plastic one. The 29205 is offered in a 100-pin plastic quad flat pack (see Photo 1) which occupies only about 1 square inch of board area thanks to tight (<25 mil) pin spacing.

The combined needs for lower power and a plastic package force the next major decision: cutting the clock rate. Turns out that the plastic packages can only take about a watt before meltdown, which effectively limits embeddable RISC chips to about 20 MHz, not the 30, 50, or even 100+ MHz of the desktop superchips.

To illustrate the problem, consider the graph in Figure 1 that relates allowable ambient temperature and required airflow to remain within the plastic package temperature limit (T_{case} MAX = 85°C). As you can see, in hermetic (i.e., no air flow] applications, a 16.67-MHz 29205 can only tolerate about 45°C ambient-a limit that could be problematic for harsh environments like the front seat of your car on a summer day.

In a way, the speed/power limit is helpful since it keeps suppliers focused on the point that the performance is not the only, or even main, requirement for high-volume applications.

Indeed, low clock rate is one of the factors, besides the obvious die size reduction, that inevitably leads to the elimination of on-chip cache. A RISC



Photo I--The *tiny SA-29205 demo board available from AMD allows the engineer to test drive the AM29205 embedded RISC processor without spending time* trying to get *the* hardware working.

without a bunch of cache may sound like heresy, but makes sense in the absence of memory bottleneck. Thanks to desktop performance wars, memory suppliers are quite capable of delivering chips that are fast enough for single-cycle operation at the slower, power-limited clock rates.

Of course, wait states can be added, but remember that the penalty is severe: 100% for the first (i.e., 1-cycle to 2-cycle), 50% for the second (i.e., 2-cycle to S-cycle), and so forth. Instead of wait states, it might be wise to garner extra access time by reducing the clock rate, which has the added benefit of reducing power consumption. For example, it would be better to run 1 cycle on a 12-MHz bus rather than 2 cycles on a 16-MHz bus. Watch out though; the 29205 isn't static and has a minimum required clock rate of 8 MHz.

Another reason to bag the cache is determinism. Hard real-time designers are often required to guarantee system response time *exactly.* Worst case or average predictions may be too wishy-washy. Cache effectiveness is further diluted by the interrupt-intensive nature of control applications.

So, by limiting the clock rate, using a low-cost, low-pin-count plastic package, and losing the cache, the 29205 enters the realm of feasibility for low-end designs. What's left is RISC reduced to its essence.

RISCALLY CORRECT

Much argument has been expended by the computer intelligentsia in an effort to define just what "RISC" means. Originally, the definition relied on a dozen or so factors by which to measure the "RISCiness" quotient of a chip.

The problem with the ranking scheme was that many factors-such as high clock rate, pipelining, cache, and good compilers-were only loosely linkable to instruction set complexity.

It would be nice to say that intellectual honesty overcame the fairly outrageous attempts at historical revisionism by the RISC zealots. Instead, it was the not surprising adoption of these same time-honored techniques by arch CISC rivals-the

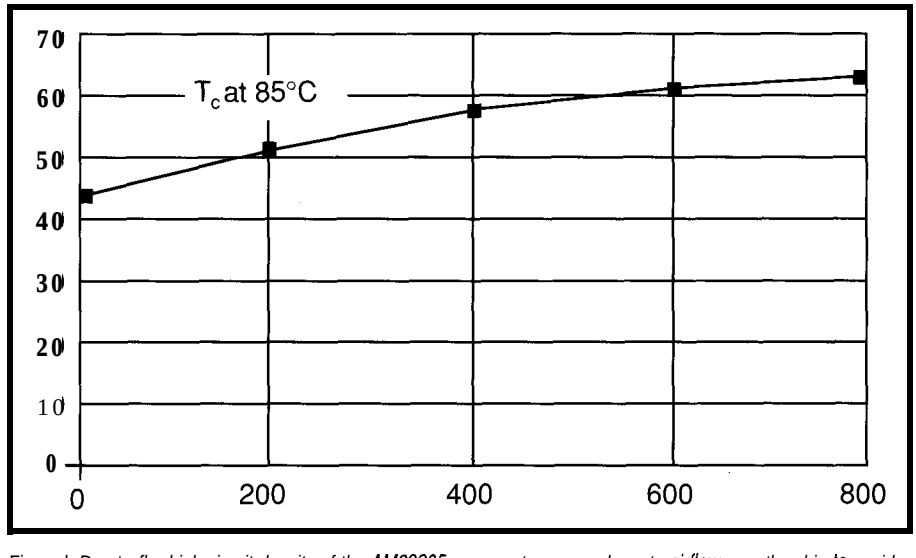


Figure I--Due to *fhe high circuit density of the AM29205, you must ensure adequate airflow over the chip to avoid overheating.*

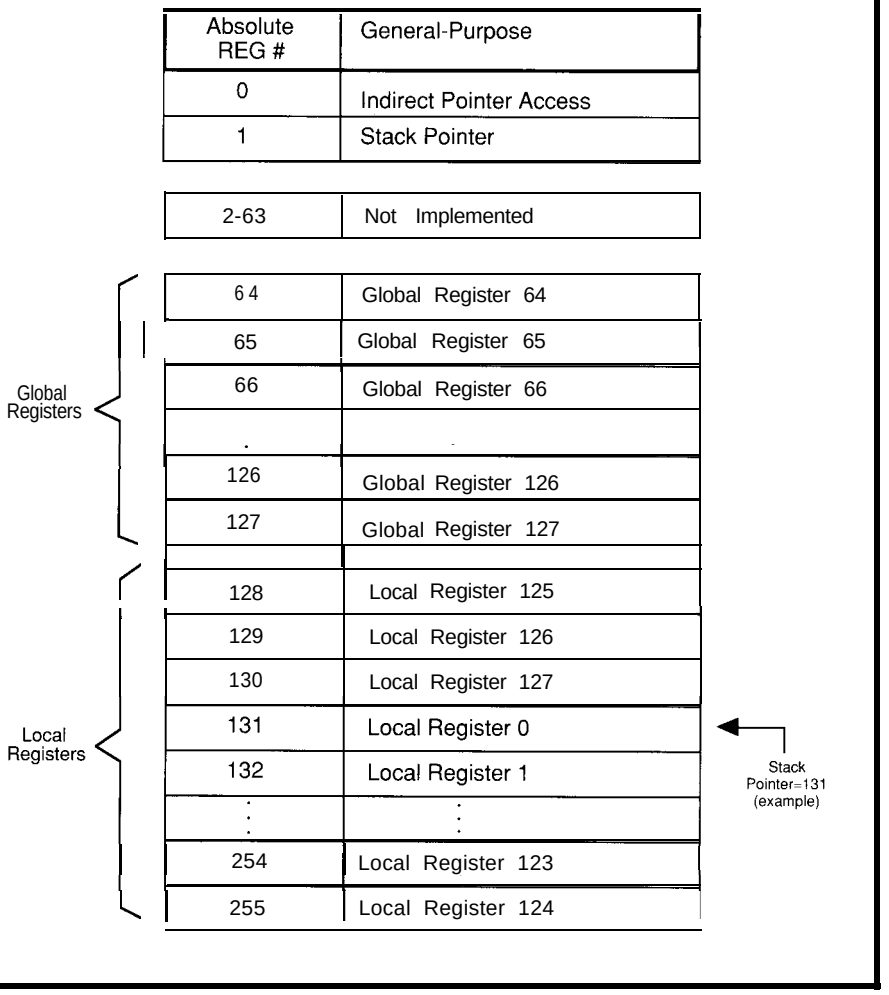


Figure 2—*The AM29205 offers 192 32-bit general-purpose registers, something RISCs need to exploit Load/Store operations.*

80x86 and 68k—that popped the hype balloon.

Skeptics (like me) have said that the RISC revolution was largely a marketing-, not technology-, driven attempt to escape the dominance of Intel and Motorola. Evidence supporting this thesis is the relatively poor acceptance of those companies' RISCs (the '860 and 88k) which, if judged solely on their technical merits, should have done much better.

Nevertheless, stripped of UNIX baggage, the 29205 exposes the meritorious core concepts of RISC including Load/Store architecture and large register set.

One true difference between RISCs and CISCs is that the former only perform logic operations on internal registers while the latters' instructions can operate directly on memory. The term "Load/Store" refers to the fact that RISCs must move memory operands to and from internal registers. The key is that advanced RISC compilers attempt to allocate register so as to minimize memory references.

To exploit Load/Store, RISCs need lots of registers. The admittedly vague dividing line appears to be somewhere between ≤16 for a CISC (e.g., 68k) and ≥32 (e.g., MIPS) for a RISC. Even within the RISC camp, there are religious wars about the ideal quantity and organization of registers. AMD comes down clearly on the pro-register side by offering a whopping 192 32-bit general-purpose registers (Figure 2) with a fancy register window/stack cache scheme.

HARVARD DROPOUT

I've noticed that, whatever the "ISC," performance of a CPU is highly correlated with the amount of bus bandwidth (i.e., the bus width times the cycle rate). RISCs generally exploit this phenomenon by offering faster bus cycles (i.e., 1 clock versus the 2-4 typically required for a CISC). Sure this places more burden on the memory subsystem, but one of the basic premises of RISC is to let the system designer choose his or her poison in terms of memory speed that reflects their own price/performance tradeoff.

The original 29000 design also attacked the first part of the bandwidth equation-bus width-by adopting the Harvard architecture, which is notable for the use of separate instruction and data buses. Since this architecture allows simultaneous instruction fetch and data transfer, it's not surprising that the result is high performance.

Actually, a pure Harvard design calls for four buses composed of address and data for both instructions and data (i.e., instruction address, instruction, data address, and data). To save pins, the 29000 merged the two address buses into one, exploiting the fact that many instruction accesses are sequential, meaning that a full address need only be sent at the beginning of a burst.

Listing I-An *unconditional jmp instruction (1) is followed by another unconditional jmp instruction (2). (In this example, unconditional jmps are used; however, any two immediately adjacent–taken branches exhibit the same behavior.) The sequence of executed instructions in this case is: jmp instruction (7), or instruction (8), and so on. Note fhaf the add instruction (3) is not executed. Also, the target of the first* jmp *instruction (1) was merely* visited; *control* did *not continue sequentially from L 1 but rather continued from L2.*

```
        jmp                                     (1)
        jmp   2                                 (2)
        add         Ir4, Ir4, Ir5               (3)
        •
        •
L1:     sub         gr96, gr96, 1               (4)
        subc        gr97, gr97, 0               (5)

        •
L2      const       gr100,  0xff0f              (6)
        subr        grl01, grl01, 1             (7)
        or          gr100,  grl00,grl01         (8)
```

Despite the trick, 96 lines (32 each for address, instruction, and data) is too much to deal with in a low-cost embedded system. The 29200 streamlined the 29000 design by going to a single 32-bit instruction / data bus. The 29205 goes a step further by cutting the combined data bus to 16 bits which, when mated with a slimmed-down 22-bit address bus, cuts bus pin count to little more than one-third the original 29000.

```
; 32-bit * 32-bit -> 64-bit signed multiply

; Input:     multiplicand in Ir2, multiplier in Ir3
; output:    result most significant word in gr96, result
             least-significant word in gr97

$Mul64
        mtsr  Q,Ir3           ;Put multiplier in the Q register
        mul   gr96,Ir2,0      ; Perform initial multiply step
        .rep  30              ; Expand out 30 copies of the next
                              ; instruction in-line
        mul   gr96,Ir2,gr96   ; Total of 30 more multiply steps
        .endr
        mull  gr96,Ir2,gr96   ; Perform last sign correcting step
        mfsr  gr97,Q          ; Get the least-significant result word
```

Listing 2—*Though the* assembler *defines multiply and* divide instructions, *AMD current/y chooses the purist* approach of *actually implementing them as a sequence of simpler multiply/divide step instructions which are in-line for* maximum performance

The associated performance hit is obviated somewhat by some other characteristics of the '205 architecture. For example, "Harvardness" is maintained to the degree that accesses hit the large register set, which can be accessed internally even as instructions are fetched from the external bus.

Oops-there I go again, slipping into the "performance is everything" mode. Remember, the goal for "reduced RISCs" is to find the easiest and lowest-cost way to get ever more complex products to market.

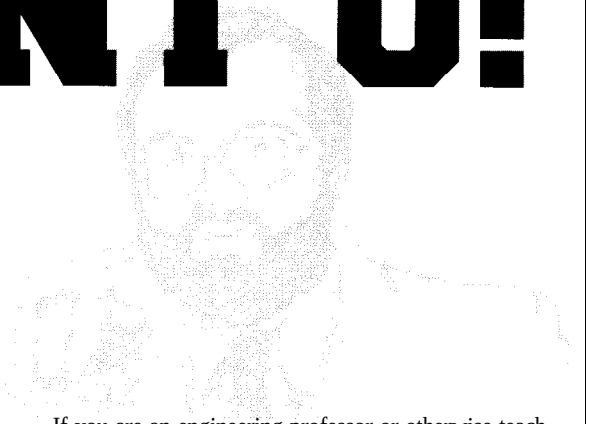
BYE-BYE ASM

The idea that large, complicated application software calls for a beyond 64K chip also implies the use of C. That fits well with RISC reliance on the compiler to generate optimal code.

In fact, though it is certainly OK to write an assembly language driver or two, you'll soon realize why RISC and C are synonymous. One strategy of RISC is to expose the CPU innards to the compiler, allowing the code generator to handle *hazards*, *dependencies*, and *interlocks* that might otherwise consume valuable transistors and slow critical circuit paths.

For example, the 29k uses *delayed branch*, which minimizes pipeline stalls by executing the instruction following a branch whether or not the branch is taken. It's the compiler's

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'Steve Ciarcia

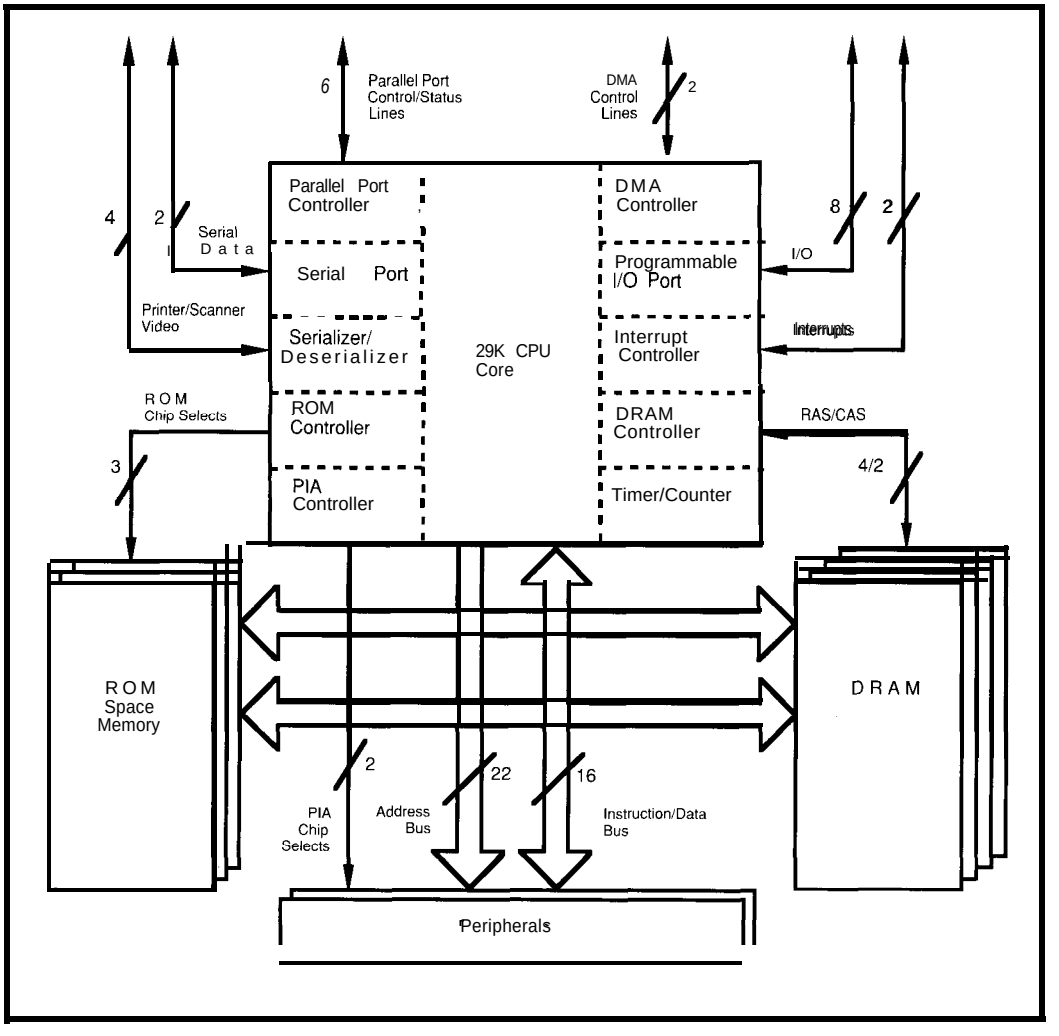


Figure 3—*The* AM29205 uses a *29k core and includes everything necessary to make it an idea/ embedded processor, including parallel ports, serial ports, DMA controller, timer/counter, ROM chip selects, and complete DRAM refresh controller.*

duty to figure out whether a useful instruction, rather than a N 0 P, can be inserted into the delay slot. As shown in Listing 1, branch delays can lead to real head scratching for an assembler programmer.

As for ***load delay,*** AMD adopts a best-of-both-worlds strategy. Consider the case of a load instruction followed immediately by an instruction that uses the loaded value. On the one hand, the compiler can try to move the load-dependent instruction by inserting nondependent instructions that can execute while the load completes. If not, the CPU has an interlock that will stall the pipeline until the loaded data is available.

A similar situation might occur for an internal (register) load / use pair as the pipe execution stage tries to use a register value that is simultaneously being updated by the adjacent write-back stage. In this case, the overworked compiler writers are given a break by hardware ***forwarding*** logic that makes the pending register write data available to the execution stage.

Though the assembler defines multiply and divide instructions, AMD currently chooses the purist approach of actually implementing them as a sequence of simpler multiply / divide step instructions (Listing 2), which are in-lined for maximum performance. The 34-instruction (136 bytes!) multiply routine is no speed demon, but the few-microsecond handicap shouldn't be critical in most applications.

And don't forget keeping track of all those registers, the complexities of which could easily take a full article. The best advice about avoiding all these traps is to use the C compiler that handles the messy details.

EZ HARDWARE

Running the 29205's pipelined 32-bit ALU may call for tricky software, but the board designer gets to take it easy. As shown in the block diagram (Figure 3), all the die space formerly occupied by cache, MMU, and so forth, has been put to good use integrating the glue logic a typical design needs. These features, more than the architectural whizzies, are what make the '205 a good fit for embedded designs.

As is the trend, the '205 offers a connect-the-dots memory and I / O interface including chip selects, wait-state generator, and DRAM control. The DRAM interface is essentially complete, providing refresh timing, address multiplexing, and page-mode operation. The latter feature is key since it can squeeze O-wait-state performance from low-cost DRAMs. Between its chip selects and 22 address lines, the '205 smashes the 64K barrier by supporting up to 52 megabytes of memory.

Another key feature is a two-channel DMA controller. While some applications don't need DMA, those that do are greatly aided by its presence on-chip since DMAC operation cleanly meshes with the above bus interface features. One channel of the DMAC is dedicated to internal / external transfers while the other is available for external requests.

The '205 only offers two dedicated interrupt inputs (INTR3 and INTR2), which isn't enough for most embedded applications. Fortunately, any or all of the eight parallel I / O lines (PIO15–PIO8) can be configured as interrupt inputs that can be defined as edge or

level sensitive. Furthermore, both modes (PIO and interrupt) offer programmable inversion on a bit-by-bit basis.

Any embedded controller worth its salt has a UART, as does the '205. One neat feature is that the UART can work in concert with the on-chip DMAC for high-speed (about 1 megabit/second max) serial transfer without software intervention. However, the UART doesn't include a baud rate generator, so the 16x clock has to be generated externally and input on the UCLK pin.

Beyond these usual suspects, the '205 offers a couple of unique I/O functions reflecting its laser printer heritage.

First, most PCs interface to laser printers via parallel port, so the '205 provides the various handshake signals to implement one. Note that the actual cable connection still calls for a latch and various conditioned inputs (Schmitt-trigger) and outputs (open collector). Various modes of operation configure the parallel port as a transmitter or receiver and also support the PC's ugly-but-it-works bidirectional printer port scheme.

The fact that the '205 "video" interface is designed to connect to laser marking engines makes sense when you realize that beam printers interface much like a CRT. Raster data (VDAT) is clocked out with VCLK with LSYNC (line sync) and PSYNC (page sync) corresponding to a CRT's HSYNC (horizontal sync) and VSYNC (vertical sync). Various counters (i.e., top/side margins and line length) time the requests for data, which can be handled by the on-chip DMAC or under interrupt handler control.

THE PRICE IS RIGHT

Embedded systems designers may be interested in reduced instruction sets, but I guarantee that reduced prices really grab their attention.

At $34 (1k quantity), the '205 is quite a steal compared to other state-of-the-art desktop RISCs whose prices feature at least one, or even two, more significant digits.

For evaluation, AMD offers another bargain. The tiny (3.7" x 2.9") SA-29205 demo board (Photo 1) combines the '205 with 512K bytes of DRAM, 256K bytes of EPROM, RS-232 driver/receiver, and the MiniMON29k debug monitor, all for only $195.

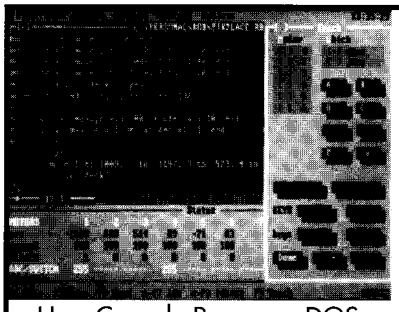
Tom Cantrell has been an engineer in Silicon Valley for more than ten years working on chip, board, and systems design and marketing. He can be reached at (510) 657-0264 or by fax at (510) 657-5441.

CONTACT

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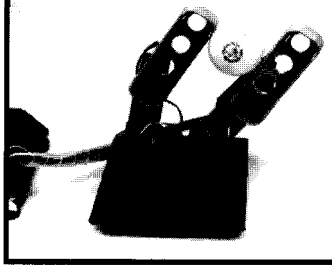
I R S

419 Very Useful
420 Moderately Useful
421 Not Useful



User Console Program, DOS.
Shown: Edit Window at left Teach Window at right, Status Window at bottom.

Manipulator Breadboard. Shown: 2 fingers, each with 2 motors.



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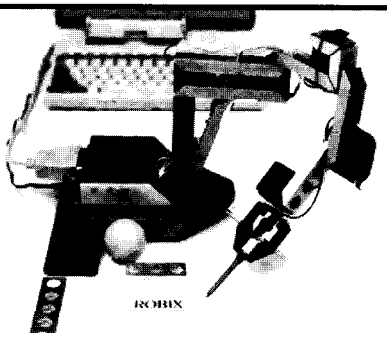
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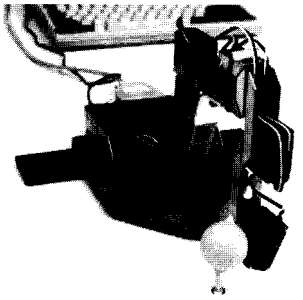
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Table-Tennis Golfer. 3 coordinated "swing" axes, 4th axis controls club "loft".



#136

Bring Your Vacuum Fluorescent Display to Life

EMBEDDED TECHNQUES

John Dybowski

Building on his vacuum fluorescent display theory discussion from last month, John shows what's necessary to interface to and actually light up a VFD.

Last month I discussed the theory behind vacuum fluorescent tubes. Now I will relate how you can get down and electrify a VFD. In this regard, I'll present the basis of a multiple-output power supply that will be used to feed the tube and support circuitry. Then I'll look at the drivers and support circuitry that will interface the tube to the controller. Finally, I will touch upon some sample code that will actually do something useful with the hardware.

The tube I selected for this project has 16 anodes and 32 grids and is called a *character type* tube. The actual characters are formed from 14 segmented anodes and can be used to represent alphabetic, numeric, and some punctuation characters. The two remaining anodes are used for the period and comma symbols. Although dot matrix-based tubes do give a better appearance and allow the representation of more characters (14-segment–type tubes don't lend themselves to depicting lower-case letters and some punctuation symbols tend to look somewhat strange), the principle of operation is the same. Driving dot matrix, 40-character, multiline tubes is well within the capability of modern microcontrollers, but frankly, hand wiring all those anodes and grids requires a bit more patience than I can muster these days. Nonetheless, besides the fact that the software timing gets a bit tighter, the idea is basically the same. If you want, you can easily extend the circuitry and the code presented here to do much larger-and nicer-displays.

FIPs

The VFD tube I am using comes from NEC and is called a FIP32D6R. The "FIP" in the part number stands for Fluorescent Indicator Panel and the "6" denotes the 6-mm character height that results in a very readable display. Tubes are available from many manufacturers, but as usual, the quality of the products varies. This issue of quality is especially apparent in display devices and I have found that NEC produces a particularly fine display panel. For your perusal, I present the nominal electrical characteristics for the NEC FIP in Table 1.

Figure 1 illustrates the anode arrangement of the FIP32D6R. You can see from this illustration how the anodes can be illuminated to form the various characters. The limitations of the available character set attainable from a segmented display may also be evident from a quick study of this figure.

REAL VFD DRIVERS

Unlike some of the example circuits I showed last time, any realistic VFD implementation uses commercial driver ICs specifically designed for this purpose. There are

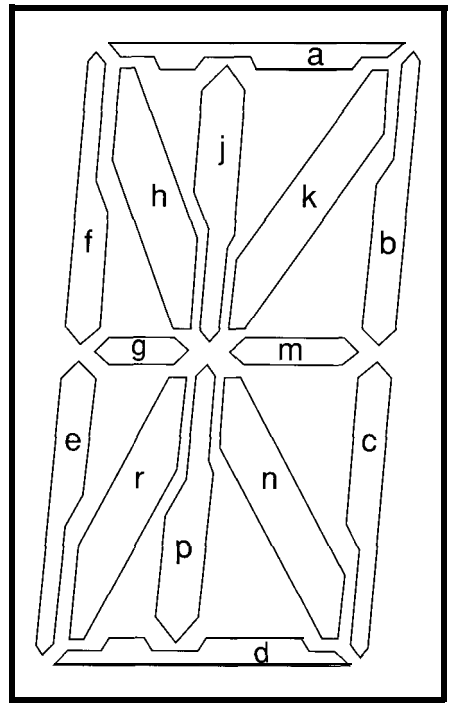


Figure 1—*The* 14 segments available *to form characters is a vast improvement over the traditional seven-segement display, but there are still some characters that can't be displayed.*

ITEM	SYMBOL	CONDITION	TOLERANCE			UNIT
			MIN.	NOM.	MAX	
Filament Current	I_f	E_f = 8.4 V_{ac} e_b = e_c = 0	70.2	78.0	85.8	mA_{ac}
Anode Current	I_b/digit	E_f = 6.4 V_{ac}		7.0	14.0	mA_{p-p}
Grid Current	I_c/digit	e_b = 45 V_{p-p}		7.0	14.0	mA_{p-p}
Brightness	L	e_c = 45 V_{p-p} Du=1/40 t_p = 80µs	445 (130)	890 (260)	-	cd/m (f_t, L)
Brightness Ratio Between Digit	-	All segments are lit.	60	-	-	%
Anode Cut-off Voltage	E_{bco}	E_f = a.4 V_{ac}, e_c = 45 V_{p-p} Du = 1/40, t_p = 80µs All segments are lit.	-7.0	-	-	V_{dc}
Grid Cut-off Voltage	E_{cco}	E_f = 8.4 V_{ac}, E_b = 45 V_{dc} All segments are lit.	-8.0	-	-	V_{dc}

Table I--The voltages *and currents required by Fluorescent Indicator Panels (FIPs) such as the NEC FIP32D6R make the design of the power supply a critical area*

two broad categories of these chips that use a high-voltage power supply of positive or negative polarity. Furthermore, either of these types can have an output structure that can be a simple open drain, an open drain with an internal pull-down resistor, or a full blown totem-pole output with an active sink transistor. With a fully active driver, you can reduce the required intercharacter blanking time from 2030 microseconds for a passively pulled down open-drain driver down to 1-2 microseconds, which is an important consideration when driving some of the larger indicator panels.

The logic interface of these drivers also shows a lot of variety for the different chips available. Here you can get simple parallel devices or parts with built-in shift registers that allow driving many outputs using just a few controller pins. Of course, these are all available with either TTL- or CMOS-compatible inputs.

Most of these parts have desirable features such as blanking inputs, and some serial-shift-register-based devices have latching capabilities (using transparent or edge-triggered latches) that allow you to shift in the bit patterns during idle times between refresh periods. Here you can take your time and set up all the bits, then assert a latch signal that transfers the shift register data to the outputs in one step. This feature is not a big deal when working with smaller panels, but its usefulness becomes clearly evident with larger displays where you tend to run out of time rather quickly.

You might find that in some applications, the refresh requirements truly cramp your style. In such a case, you may have to resort to a full parallel interface for driving the anodes. Alternatively, connecting a bunch of the serial drivers to the data bus and clocking them in parallel may do the deed. Most of the available parts can handle the full data bus transfer rate. Notwithstanding the problems of serial anode updating, there is usually no problem using the serial method for performing the grid selection. Here the shift register approach is nearly ideal since the nature of stepping through the grids is itself serial. Once you've established the initial "1" bit, just

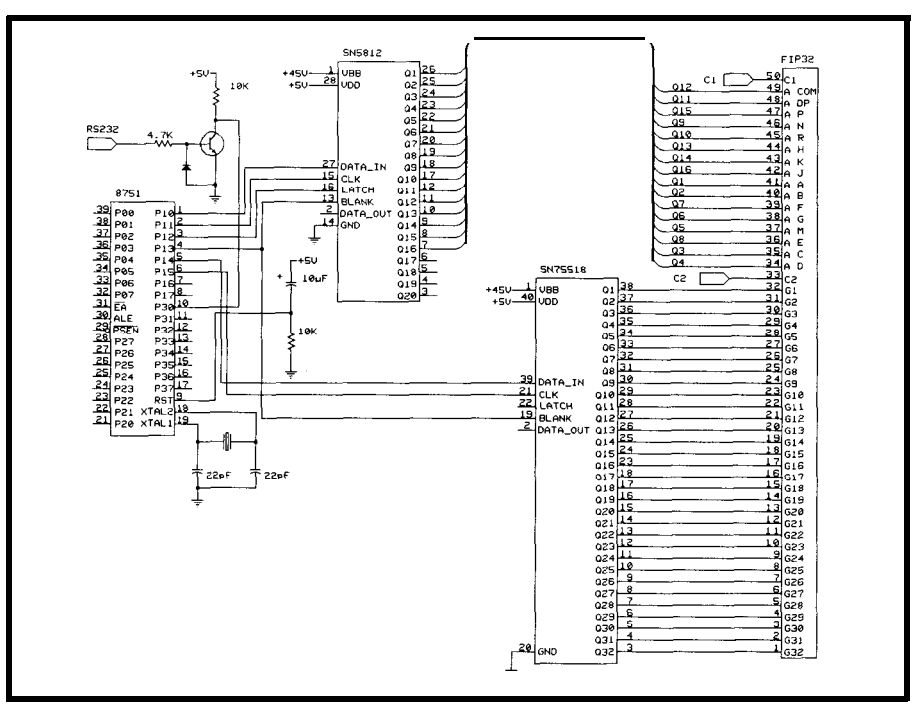


Figure 2a—*While the VFD interface fakes very few components, the number of wires required can make prototype construction tedious.*

hold the shift register input low and issue successive clocks each time you want to select the next character position.

I've already confessed I'm not crazy about wiring up a large panel, so it should come as no surprise that I selected a couple of the serial drivers for my VFD. I decided to use the 40-pin, 32-output SN75518 to serve as the grid driver and used 16 outputs of the smaller 28-pin, 20-output TL5812 to handle the anodes. Both parts have active outputs with built-in sink transistors, so they need no external pull-down resistors. Figure 2a shows the microcontroller, RS-232 receiver, driver, and tube wiring. Figure 2b details the driver chips I used.

THE HARDWARE

It is at times instructive to play with the operational parameters of the subject under experiment. It's normally acceptable as long as you do it in the name of science and don't get too carried away. This diversion is especially attractive when working with a display device and the final effects of the adjustments are immediately apparent.

It is certainly easy to vary the refresh rate, duty cycle, and blanking time in software to see how these changes affect the output of the tube. When working with display devices such as VFDs, a lot also depends on the electrical limits. These include the level of the high-voltage power supply and the amplitude, frequency, and DC bias of the AC cathode power. With these limits in mind, I decided not to set up the power section using conventional means. Instead, I softened up this section in order to be able to vary the more important parameters and investigate what really happens at the boundary conditions. A side effect of doing this enabled me to improvise the required circuitry using parts I had on hand, so I was able to get things up and running quickly. On the down side, this approach uses entirely too many parts.

The normal way of creating a power supply for a VFD centers around some sort of transformer. If running from line power, a step-down trans-

Listing I--The VFD *refresh code runs in the background as an interrupt service routine. Even though the routine requires the processor's attention for 150 µs every 250µs, there is sufficient time for the processor to do other useful work.*

```
                name    vfd
                public  VFD_Int
                public  Refresh_Ptr
                public  Refresh_Ctr
                extern  VFD_Buff

;Internal RAM Allocation
                RSEG    DATA

Refresh_Ctr     ds      1
Refresh_Ptr     ds      1

;Constants
Anode-Data      equ     p1.0
Anode_Clock     equ     p1.1
Anode-Latch     equ     p1.2
Blank           equ     p1.3
Grid-Data       equ     p1.4
Grid-Clock      equ     p1.5

;timer 0 reload value

Refresh-Time    equ     Offffh-230

;DEFINED CODE SEGMENT

                RSEG    CODE

;VFD refresh interrupt, handler, timer 0

VFD_Int:

;First reload the timer

                clr     tr0
                mov     tl0,#low Refresh-Time
                mov     th0,#high Refresh-Time
                setb    tr0

                push    psw
                push    acc
                push    0
                push    dpl
                push    dph

;Initially clear Grid Data bit
;Check if at end of refresh frame

                clr     Grid-Data
                djnz    Refresh_Ctr,Ril

;Reinitialize for a new pass

                mov     Refresh_Ptr,#VFD_Buff
                mov     Refresh_Ctr,#32
                setb    Grid-Data

;Latch the Anode bits
;Get next Ascii character and translate
Ril:
                clr     Anode-Latch
                mov     r0,Refresh_Ptr
                inc     Refresh_Ptr
                mov     a,@r0
                clr     c
                subb    a,#20h
```

(continued)

Listing I-continued

```
            rl      a
            mov     r0,a
            inc     r0
            mov     dptr,#Seg_Table
            movc    a,@a+dpt
            push    acc
            mov     a,r0
            movc    a,@a+dptr

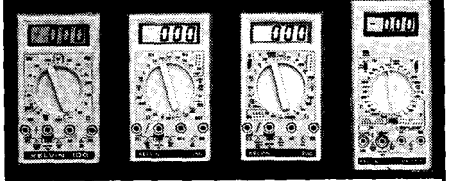
;Clock out the Anode bit pattern

            mov     r0,#8
Ri2:
            rrc     a
            mov     Anode_Data,c
            setb    Anode_Clock
            clr     Anode_Clock
            djnz    r0,Ri2
            pop     acc
            mov     r0,#8
Ri3:
            rrc     a
            mov     Anode_Data,c
            setb    Anode_Clock
            clr     Anode_Clock
            djnz    r0,Ri3

;Blank the panel, setup new Anode pattern
;Step to next Grid and release the Blank bit
            setb    Blank
            setb    Anode-Latch
            setb    Grid-Clock
            clr     Grid-Clock
            clr     Blank
            pop     dph
            pop     dpl
            pop     0
            pop     acc
            pop     psw
            reti

;Anode lookup table
;
Seg_Table   d b     000h,000h,083h,044h,040h,001h,09ch,000h
            db      0beh,003h,02eh,0cch,0b0h,0dch,000h,004h
            db      008h,084h,004h,048h,00ch,0cfh,00ch,003h
            db      000h,030h,00ch,000h,000h,020h,000h,044h
            db      0f3h,044h,000h,003h,0ddh,000h,0fch,000h
            db      06eh,000h,0beh,000h,0bfh,000h,0e0h,000h
            db      0ffh,000h,0feh,000h,01ch,000h,004h,040h
            db      000h,084h,08ch,000h,000h,048h,0c8h,002h
            db      0dbh,001h,0efh,000h,0f8h,003h,093h,000h
            db      0f0h,003h,09fh,000h,08fh,000h,0bbh,000h
            db      06fh,000h,090h,003h,071h,000h,007h,084h
            db      013h,000h,063h,00ch,063h,088h,0f3h,000h
            db      0cfh,000h,0f3h,080h,0cfh,080h,090h,088h
            db      080h,003h,073h,000h,060h,088h,063h,0c0h
            db      000h,0cch,000h,00eh,090h,044h,01dh,000h
            db      000h,088h,03ch,000h,000h,0c0h,010h,000h
            db      000h,008h,0efh,000h,0f8h,003h,093h,000h
            db      0f0h,003h,09fh,000h,08fh,000h,0bbh,000h
            db      06fh,000h,090h,003h,071h,000h,007h,084h
            db      013h,000h,063h,00ch,063h,088h,0f3h,000h
            db      0cfh,000h,0f3h,080h,0cfh,080h,090h,088h
            db      080h,003h,073h,000h,060h,088h,063h,0c0h
            db      000h,0cch,000h,00eh,090h,044h,094h,048h
            db      000h,040h,098h,084h,000h,00ch,0ffh,0cfh
            end
```


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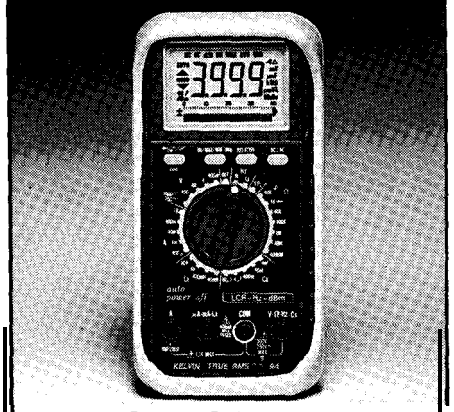
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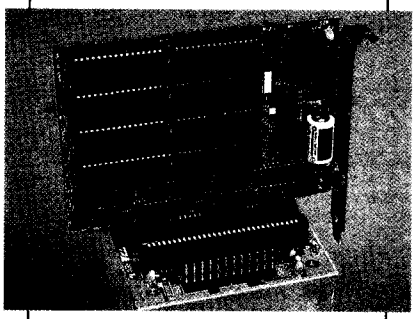
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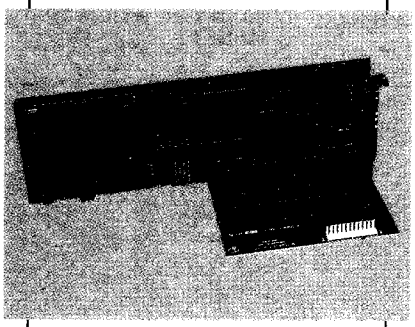
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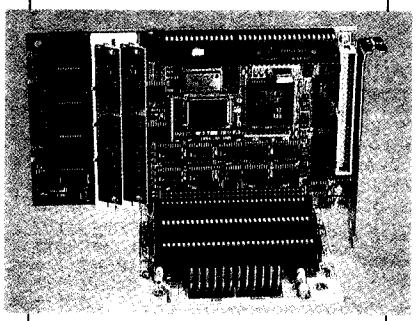
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former is used to obtain the negative high-voltage DC power for the anodes and grids, and a center-tapped AC output drives the cathode. A DC-to-DC converter—again based on a transformer—is used to step up the logic power to generate the positive DC for the grids and anodes, and a center-tapped winding provides AC for the cathode. Furthermore, the DC-based power supplies are often discrete implementations (based on transistor oscillators) that provide inexpensive power. Alternatively, a monolithic switching regulator IC can be used to provide a somewhat higher quality power source. Both types are commonly used in commercial VFD products.

The tack I took for my improvised power supply, which is illustrated in Figure 3, was to use a wall-mounted 24-volt DC power pack as the primary source of power. Up-converting can be expensive in terms of power, so I decided to start at a reasonably high voltage. The 24-volt primary also allowed me to use simple pass stages to generate the cathode supply as well as the 5-volt power supply for the logic elements.

Using a Linear Technology LT1171 switching regulator configured as a boost regulator, I set up an adjustable 45-volt power supply to handle the high-voltage requirements. The LT1171 is one of the newer generation of switchers that operate using a minimum amount of external components. The LT1171 is a current-mode switcher, which means the switch duty cycle is controlled directly by switch current rather than by conventional output voltage. The advantage of this approach is that it has immediate response to input voltage variations and pulse-by-pulse current limiting to provide switch protection under output overload and short circuit conditions. I like the

Listing 2—*A carriage return character moves the cursor to the far left side of the display. A linefeed clears the display. A leading escape character sets the cursor position on the line. Finally, any other character is simply displayed.*

```
/* Idle loop for demonstration of VFD driver */

#define CR 0xd
#define LF 0xa
#define ESC 0x1b

int Cursor = 0;
char VFD_Buff[32] = "                                ";

main ()
{
    char c;
    int n;
    int i = 1;

    while (i) {
        c = getchar();

        if (c == CR)
            Cursor = 0;
        else if (c == LF) {
            for (n = 0; n < 32; n++)
                VFD_Buff[n] = ' ';
            Cursor = 0;
        }
        else if (c == ESC) {
            c = getchar();
            if (c < 32)
                Cursor = c;
        }
        else if ((c >= ' ' && c <= 'z') && (Cursor < 32))
            VFD_Buff[Cursor++] = c;
    }
}
```

LT1171's 100-kHz operation because smaller inductors can be used. This choice is better because other switchers usually operate at lower fixed frequencies.

Since I designed the supply using parts that I had on hand, I had to resort to a trick to generate the AC cathode supply section. First, I set up an LM3 17 as an adjustable pass converter with a nominal output of about 11 volts to serve as the V_{dd} supply for the cathode section. To obtain the proper grid / anode cutoff voltage, I derive V_{ss} from an adjustable PNP emitter-follower that elevates the ground potential to about 3 volts. The contrived V_{dd} and V_{ss} levels feed a CMOS CD4069 hex inverter and its associated driver transistors. Three gates of the CD4069 function as an oscillator with the aid of a 0.01-µF capacitor, a 100k resistor, and a 200k trim pot that allows adjustment of the oscillator frequency. Since frequency is not critical, I found that 5 kHz worked fine. Finally, using the remaining three inverters of the CD4069, two out-of-phase signals feed into identical push-pull circuits composed PNP and NPN transistors. The collectors of each driver circuit connect to either end of the cathode, providing the required pulsed AC.

With this arrangement, you can vary all the important power-related parameters. Reducing the cathode's V_{ss} level clearly shows the problems of an inadequate grid / anode cutoff voltage. Bringing the cathode frequency down near the scan rate illustrates the flicker and beating that occur when this condition exists. Of course, the display uniformity deteriorates if the 45-volt grid / anode supply or the cathode supply's AC amplitude are decreased out of spec.

The final component of the power section is the 5-V logic power. This section truly demonstrates the brute-force approach. Here I simply used an LM7805 pass stage. A 66-ohm, 2-watt series resistor on the 24-volt feed prevents the regulator from disintegrating. The final circuit is not at all a pretty sight, but is the kind of thing you can get away with when you call it a test bed!

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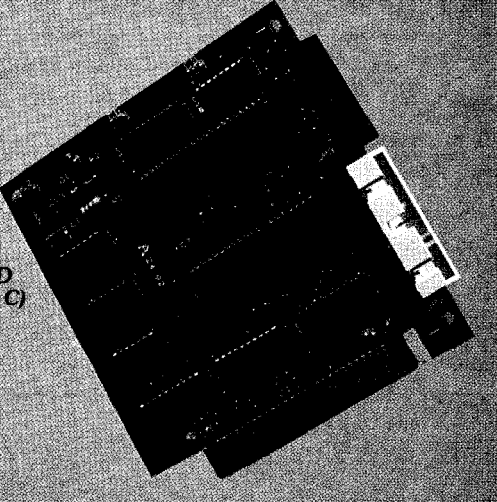
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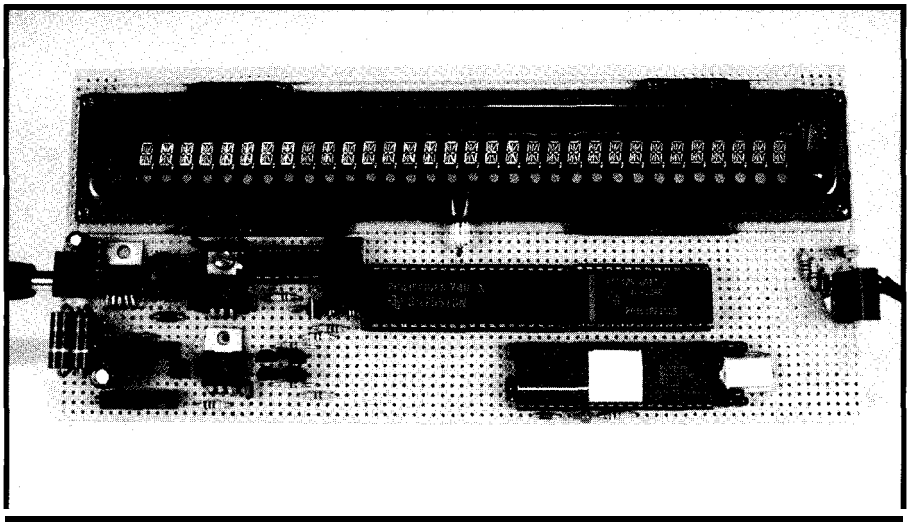


Photo I--The *final display driver prototype is idea//y suited for use in areas where high visibility is a requirement.*

THE DRIVER CODE

Having already discussed the dynamic requirements of refreshing a VFD, it's probably intuitively obvious by now how to proceed in structuring the code to accomplish this task. If there's a common thread to this project, then it must be my unwillingness to lay any more wires than necessary. To this end, I tempered the design by using the single-chip version of the 803 1: the 875 1. Having more than enough capability for the task at hand, you might argue that the controller is overkill. Nonetheless, if you have the development tools and know how to use them, it makes little sense to look further. This tactic is especially true if it's just a matter of proving a point.

The VFD interface consists of the anode data, anode clock, and anode latch outputs; grid data and grid clock outputs; and a blanking signal. In practice, you probably could combine or eliminate some of these control lines. For example, you might get by connecting the grid clock and anode latch lines since you want to advance the grid once each pass when you would be asserting the anode latch anyway. Or perhaps you could eliminate the anode latch signal entirely. On panels as small as this one, the improvement in display aesthetics gained by latching the anodes is almost negligible.

The refresh routine runs as a timer interrupt task that is invoked every 250 µs, yielding a refresh rate of 100 Hz. On entry into the interrupt service routine, the first thing that happens is the timer registers are reloaded. The reload is necessary since auto reload is not available when running the timer in 16-bit mode. (For all practical purposes, running the timer in 8-bit auto-reload mode would work just fine, but I wanted to play with the refresh rate, so I needed the extended range.)

Now after pushing all the registers that will be used by the service routine, the grid data bit is cleared. This bit is the input to the grid shift register and only needs to be set during the clocking of the first character scan of the refresh sequence. Once this bit is established, it is merely shifted through the driver to sequentially select the subsequent characters.

Next, the refresh counter is decremented and checked to see if the refresh frame has completed (which could also be accomplished just by checking the bounds of the refresh pointer). If the refresh counter had expired, it means that it's time to reinitialize the pointer and counter, and assert the grid data bit in preparation for a fresh scan sequence. In any event, the code now falls through to the common processing point that will actually affect the display.

In preparation for the anode update, the anode latch signal is deasserted, which effectively freezes the anode driver and allows the

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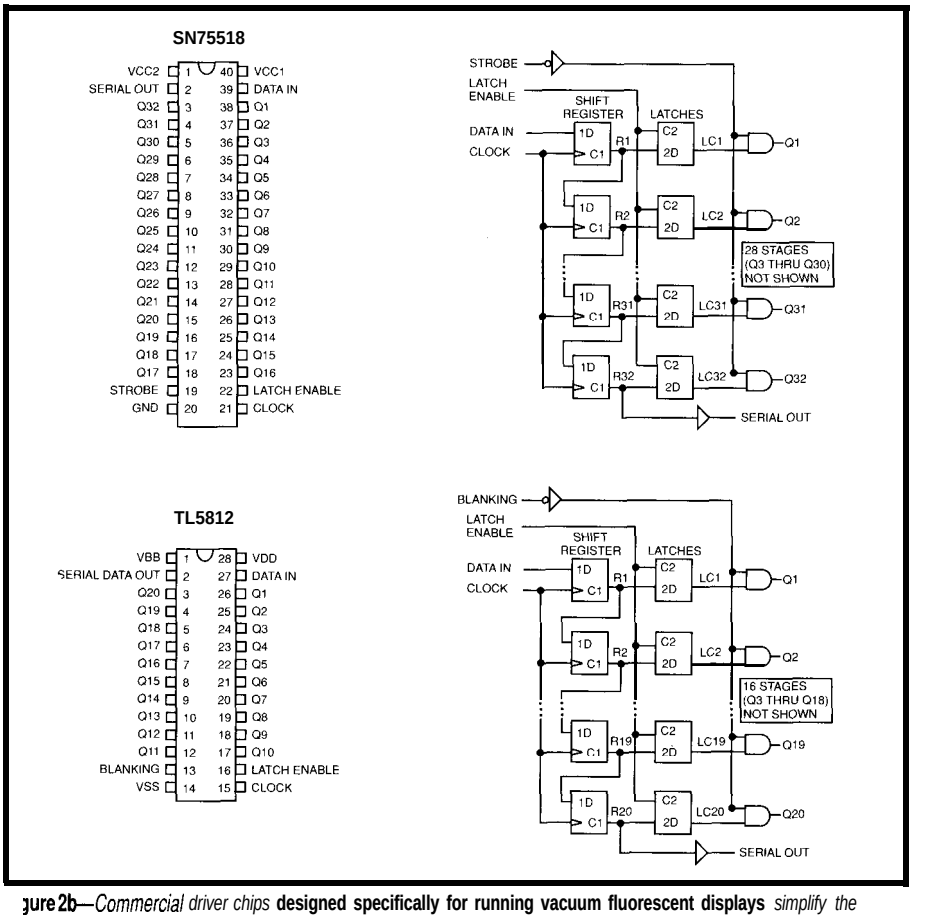
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clocking of the next segment pattern without disturbing the actual outputs. This action has the effect of increasing the VFD's duty cycle, which becomes significant with larger displays. Using the refresh pointer, the next ASCII character to be displayed is then pulled from the buffer. An ASCII space (20h) is subtracted from this character before accessing the anode lookup table since the table represents only displayable ASCII characters. A left rotate effectively multiplies this value by two, resulting in a displacement that is combined with the table's base pointer to do the 16-bit translation via the PROM-based look-up table.

Once the anode segment data has been acquired, the bits are positioned and clocked into the anode driver. After the anode shift register has been set up, the blanking signal is asserted, the registered anode bits are latched into the drivers, and the grid is advanced by pulsing the grid clock. The blanking signal can be immediately released since the active drivers necessitate only about 1 µs for a blanking period. Finally, the routine



gure 2b—*Commercial driver chips* **designed specifically for running vacuum fluorescent displays** *simplify the cuit* **design.**

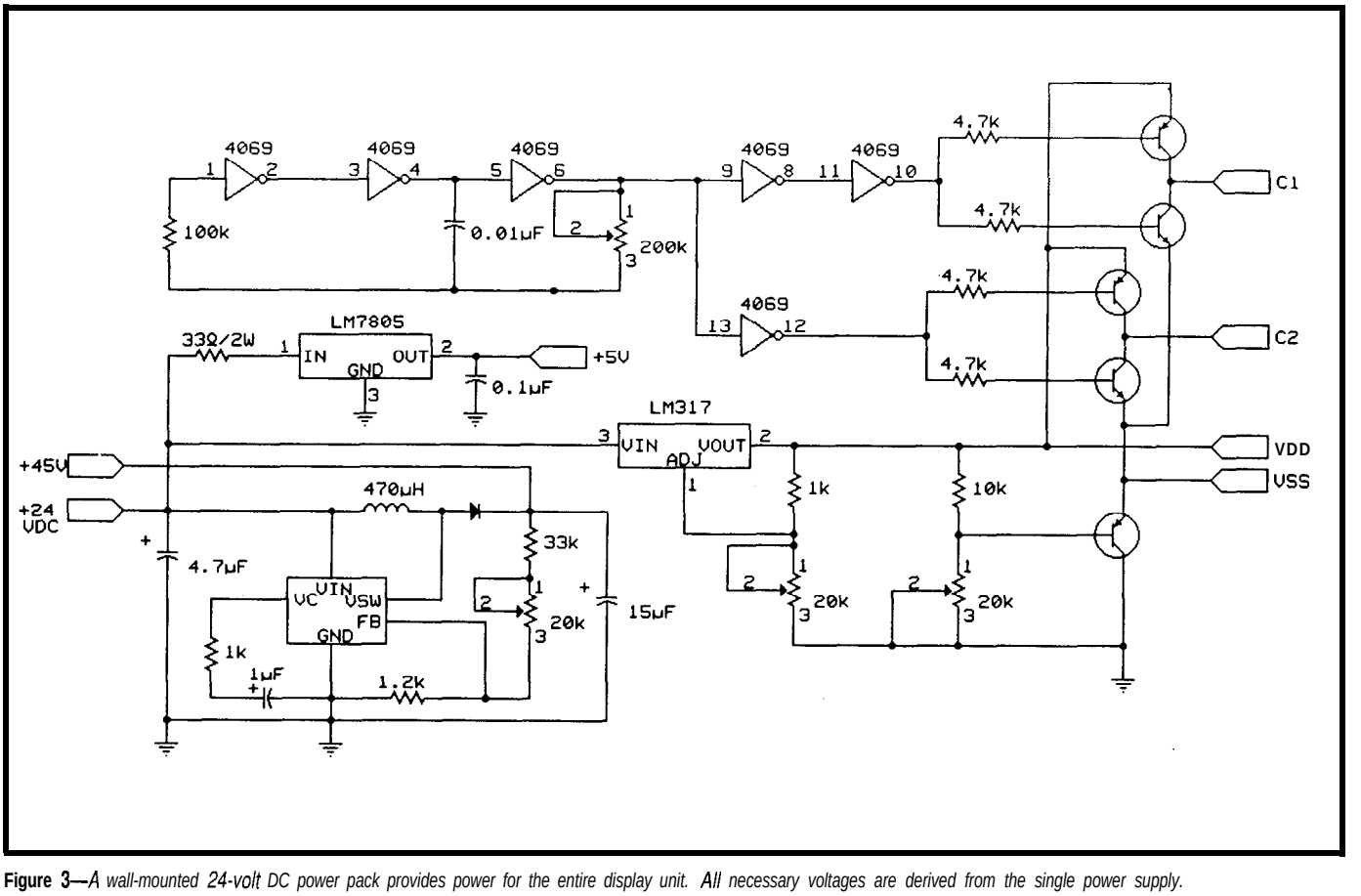


Figure 3—*A wall-mounted 24-volt DC power pack provides power for the entire display unit. All necessary voltages are derived from the single power supply.*

returns after the altered registers have been popped off the stack.

The VFD ISR takes control of the processor for about 150 µs every 250 µs, so there is a fair amount of time remaining to perform other functions. If running other interrupt sources, it's probably a good idea to set the VFD interrupt to the highest priority level to maintain a good display appearance.

Listing 1 is the VFD refresh ISR in its entirety.

OVERHEAD PROCESSING

Most intelligent VFD modules support numerous commands and offer a multitude of input modes, many of which appear to me to be of dubious value. I suppose it's probably a compatibility issue, but one has to wonder how many of these functions are actually used.

With this in mind, I decided to keep things simple and put together a truly rudimentary command interpreter. Written in C and compiled using the Archimedes compiler, my simple interpreter supports only four basic functions: home cursor, clear display, position cursor, and data input. Referring to Listing 2, you can see that a carriage return functions as the home cursor command, a line feed clears the display, and an escape character followed by a binary number between 0 and 31 serves to position the cursor. Displayable ASCII characters are simply placed into the VFD buffer until the buffer fills. Once the buffer is full, no further characters are accepted.

The link to the outside world is handled via the 875 l's serial port, for ease of implementation as they say. The function get c ha r is the epitome of simplicity. The return to simpler times of polled SIO is not unpleasant and proves to be entirely appropriate for the task at hand. See Listing 3a.

It is a simple matter to modify this routine in order to accept the data in a parallel fashion. With the addition of the circuitry illustrated in Figure 4, get c h a r code could be modified as in Listing 3b to provide for parallel data entry.

Aside from the main C library routines, the only remaining code is

Listing 3—*The* **8751's** *serial port functions as the link to the ouside world. With some modifications to the circuit, data can be transmitted in parallel fashion.*

```
; Section a: Return a character from the SIO port
            MODULE   getchar
            PUBLIC   getchar
            RSEG     CODE
getchar:    jnb      ri,$
            clr      ri
            mov      r3,sbuf
            ret
            end

; Section b: Return a character from the PIO port
            MODULE   getchar
            PUBLIC   getchar
            RSEG     CODE
getchar:    jnb      p0.7,$
            mov      a,p0
            clr      acc.7
            mov      r3,a
            clr      p3.2
            setb     p3.2
            ret
            end
```

Listing 4—*The initialization code takes care of setting up both the display and the processor's internal registers.*

```
        NAME    CSTARTUP

        PUBLIC  exit
        EXTERN  main
        EXTERN  VFD_Buff
        EXTERN  Refresh_Ptr
        EXTERN  Refresh-Ctr
        EXTERN  VFD_Int

        RSEG    ISTACK
Stack   ds      45
        RSEG    CSTART
Startup:
        jmp     init_C              ; go initialize

;Timer 0 interrupt
        org     Startup+0bh
        jmp     VFD_Int             ; VFD refresh ISR
; Start of low level initialization
init_C:
        MOV     SP,#Stack           ; setup stack
        EXTERN  ?SEG_INIT_L17
        call    ?SEG_INIT_L17       ; initialize segments
        mov     tcon,#00000000b
        mov     tmod,#00100001b     ; timer 0: 16 bit
                                    ; timer 1: 8 bit, auto reload
        mov     scon,#01010000b     ; 8 bit uart, receiver enabled
        mov     th1,#0fdh           ; 9600 baud
        mov     tl1,#0fdh
        mov     Refresh_Ctr,#32     ; initialize VFD variables
        mov     Refresh_Ptr,#VFD_Buff
        setb    trl                 ; enable baud timer
        setb    tr0                 ; enable VFD timer
        setb    et0                 ; enable VFD interrupt
        setb    ea                  ; enable interrupts
        mov     r1,#0
        call    main                ; main0
exit:   jmp     $
        END     Startup
```

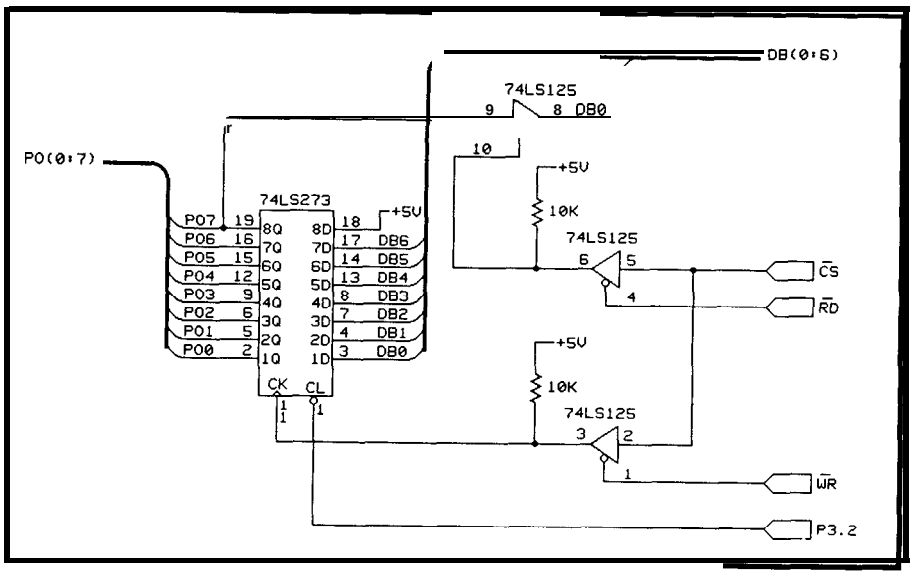


Figure 4-A simple octal D-type latch can be used to make a parallel *interface for* the display.

the initialization routine, as shown in Listing 4.

GOING FURTHER

So there you have it. Admittedly crude, but I hope satisfactory to illustrate a point. Whether you decide to incorporate the VFD as an integral component of your system or elect to come up with a stand-alone indicator panel, you should be able to adapt the concepts I've shown to multiline dot matrix tubes with no trouble. Character-type dot matrix tubes are available in configurations of up to 6 lines by 40 characters. Beyond this you have to resort to a full graphic panel.

Graphic panels are another story, however. Here the refresh requirements fall beyond the capabilities of standard microcontrollers. The commercial graphic panels that I've seen rely entirely on hardwired logic in the form of gate arrays to satisfy their voracious refresh demands. Power consumption also becomes a real problem, and because of this, the high voltage is generally derived from a fairly tight 12-volt supply. That's not to say that logic-powered graphic panels don't exist, but the current required at 5 volts does get quite high when you have a lot of dots.

In closing, I should mention the chip-in-glass (CIG) tubes that have been available for some time now. A CIG tube contains, in its vacuum housing, the associated IC driver chips along with latching shift registers. Drawing on conventional vacuum tube technology, semiconductor technology, and hybrid technology, CIGs are smaller, lighter, and have reduced pinning requirements compared to conventional designs. Since only logic-level control lines are brought out, reliability is also enhanced. Also keep in mind that the ICs are placed in a vacuum environment, eliminating degradation problems that afflict all resin-molded circuits. Unfortunately, the CIGs that I've seen are all produced for internal consumption and are available only in manufactured intelligent indicator panels. Once these GIGs can be obtained individually, they will be a valuable component for those of us who want to engineer VFDs into our products.

If you need a good-quality display that is easy to read under varying ambient lighting conditions, you may want to consider vacuum fluorescent technology. Just remember to design a decent power supply. ❑

John Dybowski is an engineer involved in the design and manufacture of hardware and software for *industrial data collection and communications equipment.*

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PATENT TALK

by Russ Reiss

It never ceases to amaze me how "generic" some patents appear to be. At times it seems as though every imaginable concept has been patented. This unfortunate situation gives rise to a great deal of litigation. And truly, a patent is often no more than a right to fight it out with an infringer in court. At other times, it is a flag to others saying, in effect, "Come and get me!" For these reasons, many inventors chose *not* to patent their invention. They would rather maintain secrecy and simply try to beat others to market. Nevertheless, if you do have a new product in mind, it would be advisable to search for prior patents so you at least know what you will be facing. Often I will present patents here solely because of their generic nature. I don't do it to discourage innovation, but to put you on guard. In all cases, you should obtain copies of the complete patent, review them for claims which conflict with your own, and speak with a patent attorney prior to committing significant funds to the venture.

This month's collection ranges from the somewhat generic to the truly unique. Gold Star's system (see Abstract 1) which uses a conventional camcorder to record a visitor at the door, appeared quite obvious to me. Yet it apparently was deemed by the Patent Office to be a novel application of a standard device. While it mentions using "a switch pushed by the visitor" to activate the camcorder, it would seem more valuable if activation were automatic. One does not know if the lack of mention of using this device as part of a security system was to avoid another patent, an oversight, or an attempt at making the patent more generic.

The pair of patents shown in Abstracts 2 and 3 leaves me wondering just what is different between them. Both describe an interesting device in which a microprocessor embedded within a transaction card generates a magnetic field to simulate or emulate the data on a magnetic-stripe card. Since the later (1988) patent references the one issued a year earlier, we can presume that additional novelty has been added. Perhaps it is their circuitry "for detecting the position and speed of movement of the card." Interestingly, the later patent was applied for in June 1986, before the earlier one was issued. We might presume that the inventors were initially unaware of the former one until it was issued. In any event, with the popularity and growth of "smart cards" you can expect to see these magnetic stripe emulators in the future. They offer compatibility with the multitude of magnetic readers already in place.

Two more examples of "generic" patents that leave me wondering just what is novel about them are in Abstracts 4 and 5. I present these because they are of interest to the microprocessor field and could impact on people working in these areas. Certainly, you would want to obtain full copies of the patents and see just what claims are made there.

The alarm system of Abstract 4 certainly sounds like a generic use of a proximity detector and synthesized speech. The voluminous reference to prior patents is particularly interesting. You might envision some interesting exchanges between the patent reviewer and the inventor on establishing the uniqueness of this one.

The use of microprocessor-based utility meters has been discussed often in electronics publications, and the patent shown in Abstract 5 appears to be just another one identical to what we have read about. Certainly, the use of Hall sensors to measure power, conversion to digital form, processing by a microprocessor, time stamping, and com-

1

Patent Number	5142,604
Issue Date	1992 08 25
Inventor(s)	Lee, Seoung E.
State/Country	KRX
Assignee	Gold Star Co., Ltd.
US References	4,959,713
US Class	358/1 08 358185 358/86
Int. Class	H04N 7118
Title	System and method for picture interphone using camcorder and TV
Abstract	A picture interphone system uses an existing TV and camcorder without any special equipment. The system is able to record a picture of a visitor while the user is not at home or when the user wants to record the picture of the visitor. The camcorder and the TV are turned on by the signal of a switch pushed by the visitor and automatically turns off after the visitor has left.

PATENT TALK

Patent Number	4,701,601
Issue Date	1987 1020
Filed	1985 04 26
Inventor(s)	Francini, Joseph P.; Asbo, Einar L.; Boston, Vincent
State/Country	CA
Assignee	Visa International Service Association
US References	3,938,090 4,007,355 4,498,000 4,507,550 4,575,621 4, 605,844 4,614,861 4,650,981
US Class	2351449 2351380 2351492 2351493
Int. Class	G06K 7/08
Title	Transaction card with magnetic stripe emulator
Abstract	A transaction card is disclosed having a magnetic stripe emulator. The transaction card is adapted for use with presently available transaction terminals that include a sensor for reading a magnetic stripe. The subject card includes a transducer for generating a varying magnetic field corresponding to information typically encoded on a magnetic stripe. In operation, a microprocessor in the card extracts transaction data stored in a memory and supplies output signals to the transducer. The transducer generates a varying magnetic field corresponding to the transaction information which is read by the sensor in the transaction terminal.



municating this information sounds like "old hat"! Perhaps it is their reference to multiplexing the data from many meters through a hierarchical computer network that lends novelty to this patent.

In the software area, the patent in Abstract 6 is interesting. It uses a table-driven, decision-tree approach to "disassembling" microprocessor code. The technique seems very general, and appears as though it would be an excellent means of quickly and flexibly handling a number of different microprocessors within a common program. Has anyone seen a product offering using this technique as yet?

Finally, I could not resist Abstract 7, which is for a "prenatal learning device"! No longer must the fetus suffice with muffled music. The mother now can be "wired for sound" complete with cassette, AM/FM radio, and speakers. I wonder if the patent covers stereo and "surround

Patent Number	4,791,283
Issue Date	1988 12 13
Filed	1986 06 03
Inventor(s)	Burkhardt, Norman S.
State/Country	c o
Assignee	Intellicard International, Inc.
US References	3,700,826 4,253,017 4,264,934 4,277,837 4,353,064 4, 354,099 4,390,905 4,414,554 4,470,051 4,494,125 4,506,148 4,539,472 4,605,844 4,661,691 4,692,604 4,701,601
US Class	2351438 2351449 2351493 2351492 2351436 2351488
Int. Class	G06K 7/08 G06K 19/06
Title	Transaction card magnetic stripe emulator
Abstract	A device and method for transferring data from a microprocessor located in a transaction card through a card reader by emulating a prerecorded magnetic stripe on a conventional transaction card such as a credit or debit card. Data is sequentially produced by the microprocessor within the card and applied to a magnetic field generator which produces magnetic fields that emulate prerecorded data on a conventional magnetic stripe of a transaction card. This allows transfer of data from a microprocessor to standard card readers without the necessity of substantially modifying the card reader device. Circuitry is also provided for detecting the position and speed of movement of the card through the card reader to ensure that all of the data is transmitted from the microprocessor to the magnetic field generators within the scanning time of the card across read head of the card reader.



PATENT TALK

Patent Number	5,117,217
Issue Date	1992 05 26
Inventor(s)	Nykerk, Michael
State/Country	CA
Assignee	Electronic Security Products of California
US References	3,471,652 3,560,978 3,581,014 3,855,574 3,925,751 3,987,408 4,205,300 4,218,763 4,325,058 4,337,462 4,346,427 4,359,714 4,383,242 4,393,365 4,395,135 4,401,971 4,410,884 4,414,541 4,450,437 4,455,551 4,464,651 4,465,904 4,531,527 4,538,135 4,539,557 4,558,181 4,571,583 4,581,605 4,642,612 4,709,330 4,716,582 4,725,827 4,748,654 4,754,266 4,772,875 4,794,368 4,821,027 4,845,464 4,853,678 4,887,064 4,887,064 4,897,630 4,901,054 4,922,224 4,987,402
US Class	3401426 3401430 3401460 3401429 3401309.15 3401692 3401531 3401539 3401561 3401565 3401551 379/40 381/51307/1 0.2
Int. Class	B60R 25/10 B60Q 1 /00
Title	Alarm system for sensing and vocally warning a person to step back from a protected object
Abstract	An alarm system senses the presence of a person sufficiently near a protected object, such as an automobile, to inflict damage thereto, and provides verbal warnings to the person that he or she must step back from the object or an alarm will be sounded. The alarm system includes a proximity detector that senses the proximity of a person to the protected object and means for generating vocal signals using synthetic speech generation circuits. Such vocal signals instruct the person to back away from the protected object, thereby preventing the person from inflicting any damage to the object. The user may select various operating modes and performance options in how the system is used.

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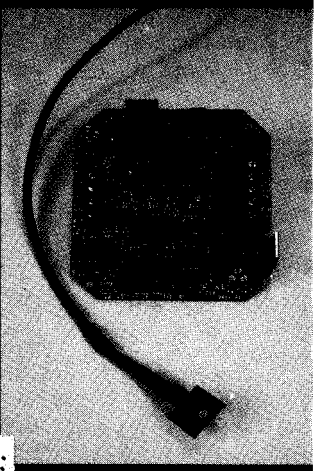
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#119

PATENT TALK



Patent Number	4,804,957
Issue Date	198902 14
Inventor(s)	Selph, Marvin P.; Hughes, Derek B.
State/Country	NM
Assignee	Triad Communications, Inc.
US References	3,388,388 3,531,771 4,218,737 4,504,831 4,628,313 4,701,858
US Class	3401870.03 379/107
Int. Class	G08C 15106 G08C 19/20
Title	Utility meter and submetering system
Abstract	The utility meter is a microprocessor-based circuit using Hall effect electric current sensors to measure power usage by residential and commercial customers. An analog signal from the Hall effect sensor is converted to a digital signal which is fed to the microprocessor for analysis and storage in random access memory. Using a real-time clock, the microprocessor determines time of use information which is also stored in random access memory. The memory may be remotely interrogated via a telephone line or serial communication link. If desired, the meter can receive utility usage inputs from other utility meters, such as water, gas, etc. and to fire and intrusion alarms. To effect a submetering configuration useful in apartment complexes, institutional and manufacturing applications, a multiplicity of meters are multiplexed to a data collection computer which is in turn networked with other data collection computers to a central billing computer.



Patent Number	4,694,420
Issue Date	1987 09 15
Inventor(s)	Pettet, Mark E.; Hoeren, Gerd H.
State/Country	OR
Assignee	Tektronix, Inc.
US References	3,105,143 3,883,847 3,918,047 3,987,420 4,099,230 4,205,371 4,231,087 4,309,756 4,312,066 4,398,249 4,475,174 4,493,044 4,498,148 4,533,997 4,541,069
US Class	3641900 371 /19
Int. Class	G06F 15/00
Title	Inverse assembly method and apparatus
Abstract	An inverse assembly method for converting binary executable microprocessor code into corresponding assembly language mnemonics provides for the storage of all the possible binary codes and corresponding assembly language mnemonics in a plurality of tables set up in a decision tree form which corresponds to the format of a user document provided by the manufacturer of a target microprocessor. The instructions and data information contained within the executable code acquired from the target microprocessor are distinguishably tagged prior to being stored in an acquisition memory. The code from the acquisition memory, in binary or hex form, indexes a primary table which contains a plurality of entries containing a binary value which may have a mask portion, each entry containing a plurality of actions having an optional string to be displayed, optional parameter masks and an optional table to call. The unmasked portion of the binary value is compared with the code from the acquisition memory and, if a match occurs, this entry is used for further processing, otherwise the comparison process moves on to the next entry in the table. Once a match is found a character string is displayed, parameter bits are picked off to be passed to another table, and another table is called within the decision tree. This continues until all actions are completed, including calls to additional tables which are similarly processed. After the processing of each called, or current, table is completed, a return to the calling table is made, and if there is no calling table then disassembly for the current code from the acquisition memory is completed. In like manner all the acquired executable code is processed to obtain the corresponding assembly language mnemonic.

PATENT TALK

Patent Number	4,798,539
Issue Date	198901 17
Inventor(s)	Henry, Verlyn; Henry, Danise
State/Country	MI
Title	Prenatal learning device and method
Abstract	A method and device for transmitting sonic vibrations, such as music, to a fetus includes an abdominal belt to be worn by the mother. The belt is equipped with either a compact cordless cassette player or a radio receiver or simply a speaker or speakers powered from a remote player and power pack. The belt is provided with pockets for detachably receiving the equipment so that it can be removed for laundry or dry cleaning of the belt.

sound" too? But what of the poor mother, belly bulging, who now must haul around a complete hi-fi system on her tummy so her offspring will have every chance of advanced placement in college (or nursery school?). The inventors surely sound to me like a couple who got really "involved" in their new addition. But then, I can recall my own excitement when I listened to my first-born's prenatal heartbeat on a surplus Doppler ultrasound monitor.

In other news, MicroPatent just announced an upgrade to the APS system being used to create these columns. The new version is now called CAPS (Claim and Abstract Patent Searching) and adds inventor's claim data to the database. This extra data is quite useful in determining the uniqueness of a patent abstract prior to obtaining and reviewing the full text. Where practical and appropriate, future abstract listings in this column will include these claim data. The CAPS system also includes additional search fields and more user-friendly operation including a "clipboard" for exporting data. It's nice to see that the product is "alive and well" and constantly improving. CAPS format should be available starting with patents issued after January 1993; however, it is as yet unclear when back files (to 1975) will be converted to this format. I'm hopeful more information will be available by next month.

SOURCE

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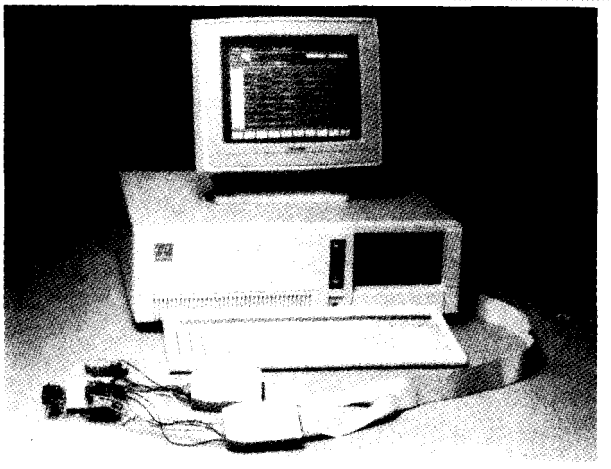
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Russ Reiss holds a Ph.D. in EE/CS and has been active in electronics for over 25 years as industry consultant, designer, college professor, entrepreneur, and company president. Using microprocessors since their inception he has incorporated them into scores of custom devices and new products. He may be reached on the Circuit Cellar BBS or on CompuServe as 70054,1663.

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I received a very nice call the other day from a Circuit Cellar reader named John Pinkas who had some concerns about the current transformer discussion in the February '93 issue. He wanted me to emphasize to our readers that current transformers can be very dangerous under some circumstances. Specifically, if the load on the secondary is removed, even momentarily, the voltage will try to go to infinity to compensate. The result is usually a very large spark that is potentially lethal to anyone working on the unit. John was able to **relate more than one story of even experienced engineers being** *burned (literally and figurative/y) by such an incident. While experience is often the best teacher, some things are better left unexperienced.*

I received a call from another reader who has had difficulty trying to pick out subjects from the threads we publish here. As a result, I'm frying a slightly different format this month that starts off each thread with a several-word subject heading rather than my short introduction. I'll leave the introductions up front to make scanning through messages easier.

Virtually everyone who has designed a microprocessor info a **circuit has had** *to* **deal** *with* **ifs oscillator circuit. The first thread this** *month takes a look at some issues related to crystal selection and specifically how it relates to the Microchip P/C processor.*

In the second thread, we venture info an area that is near and dear to many of our readers' hearts: robotics. See what some insiders have to say about the industry and what some of ifs problems have been.

Third, we head back into X-10 territory with a novel solution to the remote control of a ceiling paddle fan. The new fan control module from Leviton **isn't** *all* **it's cracked up to be.**

Finally, we follow up on Steve's very popular temperature sensor *article* **with a discussion about thermistors.**

Crystal cuts and the PIC processor

Msg#: *8526*
From: TOM MAIER To: ALL USERS

In the PIC data sheets it mentions that *sometimes* a series resistor is needed in line with the crystal to prevent over driving it. The data sheet then goes on to state that the manufacturer of the crystal should suggest the value of this resistor. The data sheet says that this doesn't always have to be done.

Is this making sense?

I understand that the series resistor is to prevent too much wattage dissipation in the crystal and it would have to do with the drive current of the oscillator, but I should think that Microchip, who made the oscillator, would suggest the drive levels and such.

I've never used a series resistor on any processor that had a internal oscillator. What is Microchip doing and when do I need to use the series resistor? How do I determine its value?

Msg#: 9176
From: JOHN WETTROTH To: TOM MAIER

All the semiconductor companies point you in the direction of the crystal manufacturers who usually know little about the parts, especially processors. I think that what Microchip is specifically addressing is low-frequency tuning-fork-type crystals (watch crystals or Statek CX-1 series). These crystals have very low maximum power levels. Usual values in 32-kHz circuits with CMOS inverters are 220k or so on the drive side (inverter output). Most crystals typically used with processors are AT-cut or similar and have liberal power limits. That's why you've never used resistors on them. Welcome to the world of low-frequency processors. Here's a tip on PICs: try a ceramic resonator unless you're trying to keep time of day. They're cheap, they start quickly, are very shock resistant and less finicky in general to design with (Digi-Key has quite a few).

Msg#: 9520
From: TOM MAIER To: JOHN WETTROTH

Thanks for the advice. Ceramic resonators are not available for higher frequencies, are they? I don't see any higher than 8 MHz in the Digi-Key catalog. Also, are ceramics as good as crystals on frequency tolerance?

What do the designations such as AT, XT, HS, and so forth mean?

Msg#: 9631
From: JOHN WETTROTH To: TOM MAIER

Best frequency tolerance of AT-cut crystals is like 50 ppm (tuned), which is necessary for keeping real time (1 minute per month rate]. Frequency tolerance on resonators is about 0.5%. This is good for anything but real time, as I said. Even "critical" items like baud rates are fine at 1%.

Highest standard ceramic resonators are 10.7 MHz. A good practical limit might be 8 MHz for other reasons.

The XT and HS designation on the PIC parts doesn't relate to the cut of the crystal. They are Microchip's way of designating oscillator type. The HS designation is for the high-speed device (up to 20 MHz) which usually uses an AT-cut crystal. The AT designation has to do with the angle that the manufacturer slices the actual quartz at. It is by far the most common cut these days. The LP PIC designation is for low-power/low-frequency tuning fork crystals (mostly 32,768 Hz). I think what they do is starve the oscillator for current to limit its bandwidth at high frequencies to make these things start up. Low-frequency, high-Q crystals can take a very long time to start up (up to a quarter second!).

If you're really undemanding on the PIC, use the RC oscillator option. They work great if you can put up with tolerances in the 5% range (with good parts and careful design). I built a car security system around the PIC that used a 10k resistor and 330-pF cap for a reliable 250-kHz clock. The timing is totally noncritical, just blinking lights and entry/exit delays. Over time and temp, with junk components, the tolerance is about 10%. RC oscillators on the PIC start instantly and always and are CHEAP. The other nice thing is that the "oscillator divided by 4" output is available for other parts of the system if required.

Msg#: 9797
From: TOM MAIER To: JOHN WETTROTH

When I mentioned HS and such, I meant the crystal cuts, not the PIC type. I bought some little crystals from Digi-Key and they are about one-quarter the size of the ATs I usually use. They work with the 805 1. Haven't tried it on the PIC yet.

Another thing I was going to try was to tune the RC frequency with a trimpot instead of a resistor. I suppose the temperature coefficients of the RC will not make it as good as a crystal, but it would make the frequency better than the ±30% spec given in the book.

By the way, where are people getting those new version PICs, the C71? Small quantities.

Msg#: 9814
From: JOHN WETTROTH To: TOM MAIER

Gotcha on the crystal cuts. What you probably have is HC-49-US (short HC-49s) probably by ECS. They are some kind of modified AT cut so they can make them a little slab rather than a big disk as in most case styles.

I don't know where to get 16C71s now. I will probably try Microchip for samples. I'm sure Digi-Key will have them very soon (if not already). The other source would be Pure Unobtainium. I don't have any way to program them right now anyway and, unfortunately, don't have enough personal experimentation time.

Msg#: 9864
From: ED NISLEY To: JOHN WETTROTH

Nope.. .Pure Unobtainium won't carry those new PICs. The catch is that Digi-Key will just add 'em to their line and I'd be left with a ton of dead stock.

My guess is a call to Digi-Key will pay off; if they're not carrying the new ones, they'll get the message pretty quickly!

Robotics-The past and the future

Msg#: 8436
From: RONALD HORNER To: ALL USERS

Does anyone have information on the magazine *Robotics Age!*

Msg#: 8438
From: WALTER BANKS To: RONALD HORNER

Helmers Publishing, Peterborough, NH, used to publish Robotics *Age*, but it ceased publication 4 or 5 years ago. I used to own part of North American Technology, now Helmers Publishing. *Robotics Age* stopped being viable after the total number of robotics suppliers dropped to a handful and their market was small. Magazines live by advertising, subscriptions usually cover mailing and sometimes printing costs but not the people needed to put the stuff together.

Msg#: 8816
From: RONALD HORNER To: WALTER BANKS

Oh well. Do you know of anything similar? Why do you think they went out of publication anyway! Is it something to do with the robot market? Just curious.

Msg#: 8819
From: BRIAN KRAUT To: WALTER BANKS

Darn, I was also hoping to get a subscription to *Robotics Age* one of these days. There is a magazine called *Robot Explorer* for $14.95 for eight issues that I have seen advertised [(603)924-6079]. By the way, I have a book called "Robotics Age-In The Beginning," by Carl Helmers. There are a lot of early reprints from the magazine.

Msg#: 9487
From: PELLERVO KASKINEN To: RONALD HORNER

What happened to the robotics industry was that it got out on the wrong side of bed!

We were part of the early attempts to get welding robots into general use. But we could not make enough noise to put the business perspective into shape. In the U.S., the general perception that the newsprint and magazines plus robot manufacturers all promoted was that the robots are for the big three in Detroit and a couple other users. Besides, the idea was that the robots would replace humans. So, there was a natural opposition to the introduction of robots in general and moreover, the whole idea of versatility was lost. The high-volume producers can better make use of hard automation. It is the small job shops that make a day's or a week's run of any one part at a time and then switch to the next part-they would benefit from robots and the versatility. Also, a robot should be considered a tool for the sole purpose of enhancing the productivity of the human operator, not as a replacement for him.

I have seen these concepts working in Japan and I believe they still have the same 10: 1 ratio of robots in use over what we have in the U.S.

I once discussed these issues with the manager of robot sales in GE. He admitted my views were absolutely correct and was sad that even his organization seemed powerless to turn the general perception around. It was just too expensive a task after all the wrong hype. If my memory serves me right, less than a year later GE pretty much dropped out of the robot sales.

Msg#: 9752
From: RONALD HORNER To: PELLERVO KASKINEN

I work in automotive assembly plants and when I first started to work there, I wanted to see a robot in action! They told me to look over there and watch one. It was so tangled in the automation that I didn't even see it until it started to move! That had quite an impression on me. The attitude I see is that the robots are great tools, but of limited use. So I have been talking to people, trying to find the history of what went wrong.

Msg#: 9794
From: TOM MAIER To: RONALD HORNER

I don't think anything went wrong exactly. It's more a matter of robotics being more complex than people appreciate. Organic beings are amazingly complex, and our attempts to emulate nature have been rather weak. Case in point is trying to get a two-legged robot to walk. Very complex problem. When it is accomplished, people don't think much of it because they don't see the underlying complexity.

I used to do automation programming and sometimes I would be "over-the-moon" about something I just accomplished, so I would run over and grab a floor worker and show them. They would say, "Big deal."

Robotics is very complex. If I saw a robot walk and wash dishes, I would drop over backwards, dead. This statement alone will probably encourage a dozen people to make such a robot. :-)

Msg#: 9362
From: JAKE MENDELSSOHN To: RONALD HORNER

It turns out that robotics is much harder the anyone (including me) thought it would be. Lots of people (including me) started robotics companies and lost a ton of money. Lots of people (including me] started robotics magazines and soon went out of business. However, lots of people (including me) never seem to learn from their past failures and are still trying to do something in this area.

If you live near Hartford, there is the Connecticut Robotics Society that meets once a month. It is a good group and you should try to attend a meeting. Contact Adrian Drury, P.O. Box 127, Canaan, CT 06018 for more information.

There are other groups scattered all around the country if you live somewhere else. Contact me and I'll send you more info of a group near you.

Robot *Explorer* is more of a newsletter than a magazine. All of the true robotics magazines have gone belly up.

Msg#: 9380
From: STEVE CIARCIA To: JAKE MENDELSSOHN

You may have mentioned this before, so forgive me, but what magazine and what company (robotics, that is) did you start/finish?

Msg#: 9562
From: JAKE MENDELSSOHN To: STEVE CIARCIA

I have always been fascinated with building automatic devices and gadgets and I am old enough to remember the robot on the "Howdy Doody Show." I loved that robot.

In 1985, I started a company in Pennsylvania that made and rented out Showbots, which were radio-controlled robots used for trade shows, shopping centers, and parties. The company, Nationwide Robots, was very successful, but I was unsatisfied. I wanted to build "real" robots. In the late '70s as cheap microprocessors became available, I saw my chance and sunk all of my money into designing and building real, computer-controlled robots. The robots worked all right, but the company was a failure since people expected just too much from them. We made a robot that could avoid bumping into furniture, and people wanted one that could wash windows and make beds.

In 1985, I sold what was left of the company and moved to Connecticut.

Since then, I have submitted articles to *Robot Reader* and *Robotics Age,* both of which went out of business

before they could print them. I wrote five articles for *Robot Experimenter,* which went out of business after they printed them. I also edited the newsletter *Robot Review,* which was published by the Science Museum of Connecticut for two years.

In the past few years I have even built a few devices for people who have asked for them. People may think the future robot will push a vacuum cleaner to clean the rug, but instead the vacuum cleaner will be intelligent and it will move itself around the room. You will not have a robot chauffeur to drive your car, but the car will drive itself. This is the wave of the future.

Your HCS II is the best example of this trend happening today. In 1978, I was approached about building a robot that could maintain and guard a home. As a caretaker, it should control the heat, turn on and off lights, take telephone messages, and tell the homeowner when visitors arrive. As a guard, it should watch out for fire, break-ins, power failures, or flooding and respond appropriately. In 1978, I tried to build a stand-alone robot to do all of those things, and I failed.

Your HCS II can do all of that and more. It is the direction that robotics is heading and it is what robotics will be in the future: not an R2D2, but a "smart" home controlling and talking to even smarter appliances.

Msg#: 9587
From: ED NISLEY To: JAKE MENDELSSOHN

Yeesh! Talk about a report from the trenches!

I agree that the key part of the puzzle is making everything smart enough to mind its own business.. .but the missing link is error correction and control: debugging the system remains the key problem.

There's an HCS War Story you won't see in print, but, basically, the punch line is that Steve still hasn't quite forgiven me for disabling the basement alarm horn with a wire cutter. Turns out there was this little bug about not having a way to turn the system off after an alarm...and it's essentially impossible to "pull the plug" on his HCS because it has multiple, independent backup power supplies.

Verifying that software works is exceedingly difficult, particularly for code that drive machinery.. .like a house. It's even worse when you need to cover all the exceptional conditions.. .like in a security system.

Msg#: 9616
From: STEVE CIARCIA To: JAKE MENDELSSOHN

Ed is quite correct. The one time I had a false alarm on the regular alarm system, complete with the police and neighbors present, I also had a compounding HCS problem. In beta testing a new iteration of the HCS software for Ken, I added a bunch of code that would turn on individual 140-db sirens in each room if the alarm was on and motion was detected. I had just wired all the rooms, so I added the code during that test. My logic was that if a crook has to contend with 140 db in a closed room, he vacates faster.

Well, a door that wasn't quite closed (it now has an HCS routine that specifically checks it) triggered the regular alarm. This, of course, set the "go" condition for my new code. As the cop with drawn gun was walking through the house inspecting what's wrong, his movements started tripping all these other sirens. Instead of one normal outside siren, suddenly they had six going inside and two outside. Unfortunately, resetting the real alarm system only shut off its own siren because I neglected to add the code that said if the alarm is off then turn the sirens off. Just as I arrived in the midst of this crowd, Ed was ready with a pair of wire cutters. Fortunately, he only cut the garage siren (the one facing the crowd) before I could pull the appropriate relay cables.

Msg#: 9825
From: LARRY G NELSON SR To: JAKE MENDELSSOHN

Where were you when I was looking for articles to publish in *Robotics Interest News!* I published a newsletter and was starting to get a number of subscribers, but had a hard time getting articles written. I had some written by students in a robotics course I created and taught for a now-gone college. The equipment I used for publishing the newsletter created a product I was less than pleased with, but after I shut down operation, I hadn't lost my shirt-just a few buttons. :-)

Unfortunately, expectations and what can be realistically delivered in the area of robotics haven't converged yet. When that happens, then the fun will begin.

X-10 control of ceiling fans

Msg#: 9831
From: RUSSELL SALERNO To: ALL USERS

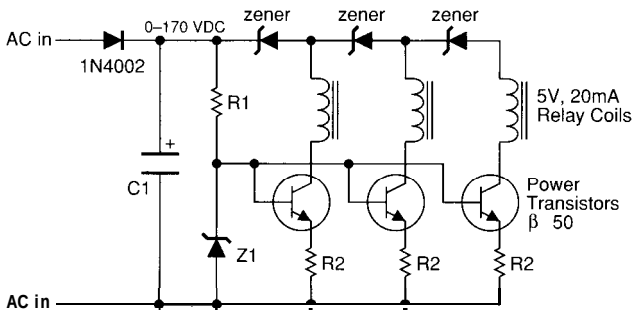
I'm looking for suggestions on how best to accomplish the following: I'd like to sequentially close three 5-V relays in succession as the output of an X-10 lamp (dimmer) module goes from 0 to 100% brightness. The reason I need to use 5-V relays is that they're tiny, and that's important.

Msg#: 9840
From: DAVE TWEED To: RUSSELL SALERNO

Let me take a stab at it. The key parameter for the relays is actually the coil current, not the coil voltage. Let's assume 20 mA. If you want to turn on three relays, at some

point the circuit is going to have to dissipate 60 mA * 120 V = 7.2 W as heat (assuming you don't want to get into switch-mode power converters). This heat is going to have to be dissipated somehow, and this is going to work against your goal of keeping things tiny.

Keeping this in mind, here's one way to approach the problem. We set up a simple constant-current driver for each relay coil so that a transistor dissipates the excess power where needed. We use zener diodes to set the decision points for each relay. The circuit looks something like this:



Z1 is a 5.1-V zener diode, generating a bias voltage for all three transistors.

R1 is a 100k resistor (0.5 mA bias current at 50 V).

Cl is a 100-µF, 200-V capacitor, whose voltage represents the average voltage of the AC waveform (see below).

The R2s are the current-setting resistors for the relay coils: The voltage at the emitters of the transistors will be about 4.4 V; this value divided by the current required by the relays is the value of the R2 resistors. For example, 4.4 V/20 mA = 220 ohms.

The zeners across the top of the diagram set the turn-on voltages for the individual relays. If they are 45 V each, then the first relay will turn on at roughly 55 V, the second at 100 V, and the third at 145 V.

The problem with this setup is that the leftmost transistor will be dissipating 20 mA * 115 V = 2.3 W when the circuit is full on, and will require a medium-sized heat sink. Another problem is the overly-simplistic half-wave power supply, whose output does not truly represent the average voltage of the AC waveform. Actually, this circuit will be fully charged at anything over a 50% setting of the dimmer. This means that the relays will come on, in sequence, as the dimmer goes from 0% to 50%, and will remain on for all settings above 50%. If you really need readout from 0% to 100%, you'll need to add some resistors around Cl to turn it into a low-pass filter (one in series with the 1N4002 and one in parallel with Cl). This will further increase the power dissipation of the overall circuit.

You never said what these contact closures are going to be used for. Perhaps a different approach would be better: Let's take advantage of the fact that the X- 10 dimmer is basically a standard triac-based dimmer that works by chopping the AC waveform. Set up a bridge rectifier, no capacitor, and a 5-mA constant-current source similar to above, but use an optoisolator instead of a relay. The output of the optoisolator will be a 120-Hz pulse train whose duty cycle varies with the setting of the dimmer. You can either filter this waveform and do DC level comparisons on it, or do pulse-width discrimination directly.

Msg#: 9892
From: RUSSELL SALERNO To: DAVE TWEED

Thanks for your reply. I'm using the relays to control a "silent" fan speed control. Each relay switches the 115-V line voltage through a cap (well, the first two relays will switch in a cap, the last will switch the AC line directly). As the X- 10 dimmer increases its output, the relays close in succession, and the fan motor accelerates. Why, you may ask, am I going through all this trouble!? Because the fans I have hum intolerably loud when used with the X-10 fan/motor control module, which varies the AC voltage instead of chopping it triac style.

Interfacing thermistors

Msg#: 8776
From: CHRIS TYLKO To: STEVE CIARCIA

Thank you for your article on temperature sensing *(Circuit Cellar INK,* February '93 issue). I found it very helpful. A question if I may. When looking at the ADC window in HOST on the HCS II, the values constantly change upwards and downwards by one or two units every "refresh." This occurs for empty channels as well as the two I am using for temperature and light sensing. I've hooked a thermistor and resistor together to get O-5 volts as the temperature changes. Did the same with a photoresistor (both share a 40-foot cable run). What can I say? It works...I don't need precision, as long as I'm ±2 degrees that's fine. The constant changing thus far presents no real problem, and if it did I could delay temperature and light recalculations to every so many minutes.

Question, if I used an LM34 with the conditioning you described, would I still get that fluctuation on the ADC reading? By the way my empty ADC inputs are not terminated.

Msg#: 8912
From: STEVE CIARCIA To: CHRIS TYLKO

Typical processor noise plus the inherent accuracy of the ADC causes the changing readings. With the new 2.0

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release you'll be able to do math in XPRESS. The you can average readings or truncate the last bit or two.

Msg#: 9417
From: **BOB ARMSTRONG To: CHRIS TYLKO**

I've been trying to figure out a simple algorithm for determining the resistance of a thermistor at each temperature step. I've found that they are both nonlinear, and nonlog. How did you compensate for these in your setup? I've ordered some LM34DZ sensors, but the thermistors are less than a buck at good old Radio Shack and I hate to give up on this..

I'm using the RS 271-110(10k ohms at 25°C) thermistor.

Hmmm...just had a thought... RS provides a list of readings. Maybe I just need a good curve-fitting algorithm.

Msg#: 9451
From: STEVE **CIARCIA** To: BOB ARMSTRONG

Commercial thermistors come with a graph that plots their resistance versus temperature. Unless you have that plot, you'll have to physically take resistance versus temperature readings at a bunch of temperatures and make your own table. Thermistors are not linear. At best, between short ranges of temperature they can be considered piecewise-linear. While most thermistors follow a similar characteristic response, there is no specific equation I know that allows you to simply plug in resistance at 25°C and go.

Msg#: 9780
From: PELLERVO **KASKINEN** To: BOB ARMSTRONG

In their "Temperature Handbook" (or some such name), Omega suggests a formula for your curve fitting: $1/T = A + B(\text{Ln } R) + C(\text{Ln } R)^3$ where T is temperature in kelvins, R is the resistance, and A, B, and C are the constants that you need for the interpolation.

They also state that within -40°C to +150°C and an actual span of less than 100°C, you get better than 0.01°C interpolation, provided you chose the three reference points evenly and with less than 50°C difference from the center point to either end.

This obviously still requires math-three unknowns and three temperatures-but it looks like a normal single-order elimination process would do the job. If you want, there is a commercial curve-fitting program from Jandel, called TableCurve or something like that. I tried a demo a couple of years ago and it works great, but of course it is a bit expensive. Was about $700 when I checked it. Could not justify quite that much at the time and even less now with the new mortgage pressing. So, the old tedious ways have to serve me still some time to come :-)

We invite you call the Circuit Cellar BBS and exchange messages and files with other Circuit Cellar readers. It is available 24 hours a day and may be reached at (203) 871-1988. Set your modem for 8 data bits, 1 stop bit, no parity, and 300, 1200, 2400, 9600, or 14.4k bps.

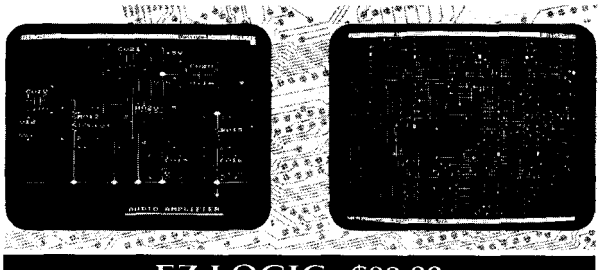
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#145

STEVE'S OWN INK

Voice Recognition and Professional Reinvestment

It seems like barely a day goes by without someone calling or leaving a BBS message concerning new functions on the Circuit Cellar Home Control System (HCS II). When we started this as a staff engineering project we knew it would be provocative and stimulate a lot of interest, but we didn't entirely comprehend reader zealousness for perpetual system expansion.

We have two HCS-related projects in the queue right now. First, is the interactive telephone DTMF interface that we have been promising all along. The delay is not the result of beating around the bush. We're not talking about a black box you dial and blindly punch in a couple DTMF codes. Our expectation is that the unit will be DTMF/voice interactive. Press a DTMF code to request data from the HCS, set specific outputs, trigger detailed control sequences, or tell it to call you back when specific events occur. The data you request will be spoken with a voice synthesizer.

The problems we've been having are what you'd find in any design group responsible for actually manufacturing a product. The idea is trivial. Making it work cost-effectively is the only accomplishment. Give us a few more months and you won't be disappointed.

The second interface falls in the category of personal interest. While the HCS already has the capability of receiving wireless commands, I've always been intrigued by the concept of vocally interacting with my home controller. Although I don't propose to mimic the starship Enterprise, I anticipate at least being able to do the same functions verbally that I could do through the DTMF interactive interface.

The incentive to even attempt such a project is due in part to a new voice recognition system from Sierra Semiconductor ([408] 263-9300) which, based on our initial tests, appears to be surprisingly speaker independent. Combining the recognition electronics with a text-to-speech synthesizer should make a dynamite technology article.

One final item on our itinerary involves making an investment in the future. With the exception of support from a few large technology companies, engineering students are hard pressed to obtain up-to-date industrial-quality application information. Heaven forbid that they should ever request free data manuals or try subscribing to a trade magazine.

Endorsing this second-class status is not only shortsighted but it neglects the fact that American business ultimately has to expend the effort to fill in the gaps before it can itself advance and benefit. The engineer you educate today is the one America depends upon tomorrow.

The *Computer* **Applications** *Journal* is an exceptional source of quality technical applications material (who else presents such exhaustive scientific dissertations complete with software at this price?). While it sounds trite to suggest that if every engineering student had a subscription to *Circuit Cellar INK,* it might help relieve an exasperating impasse, I am ready to put my money where my mouth is.

We get a very gratifying feeling around here when we are contacted by teachers and college professors for reprint rights so they can use Circuit Cellar materials in a class project. To encourage this and similar endeavors, I want to go one better. As described in detail on page 65, have your professor or teacher contact us so we can arrange to provide magazines for the entire class.

I encourage you to post this editorial in every technical college in America.

Steve