

# **Apple II and Apple II-Plus Level II Service Reference Manual**

**Pre-Release Version**

A compendium of notes, diagrams and instructions for diagnosing and repairing the Apple II and Apple II-Plus computer systems.

## **AUTHOR**

Apple Computer Inc.

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# INTRODUCTION

## What is this manual?

The Apple II / Apple II-Plus Level II Service Reference Manual is a compendium of notes, diagrams and instructions for diagnosing and repairing the Apple II and Apple II-Plus computer systems. This is an internal document written by Apple Computer's service department for use by Apple's internal Level II service personnel.

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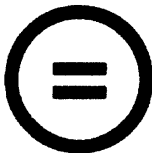
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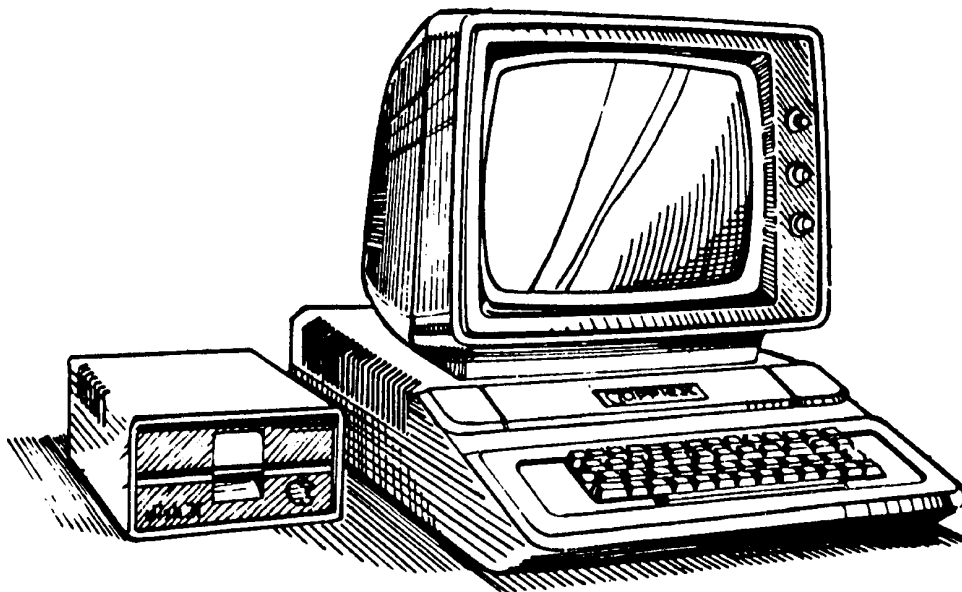
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## Apple II Computer Technical Information

# APPLE II / APPLE II-PLUS LEVEL II SERVICE REFERENCE MANUAL

**Pre-Release Version**



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Apple Computer, Inc. • Level II Service Center  
1981**

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## APPLE II SERVICE REFERENCE MANUAL

This is a Service Reference Manual which describes the Apple II and Apple II Plus Computers, manufactured by Apple Computer Inc. This manual contains a general description of the Apple II followed by theory of operation, troubleshooting guides and spare parts information which will enable the technician at a Level II Service Center to repair these computers. This Manual is aimed at component level maintenance.

This Manual only covers the Computers. It does not include videos, disk drives, peripheral devices, or interface cards. At the end of this manual is an appendix containing IC maps and specifications, ROM listings, spare part information, and removal and replacement procedures. There are sections on the System Monitor, the input/output devices and their operation, the internal organization of memory and input/output devices, and the actual electronic design of the Apple itself.

The real secret to this manual is using a scope, as signals are described they can be observed as well, thus speeding up learning. It is suggested that an "open Apple II" be created using a logic board, keyboard, power supply and monitor. I hope you will enjoy and learn from this manual as I have.

THIS IS A ROUGH DRAFT PRE-RELEASE VERSION OF THE MANUAL. WE FELT THAT THE INFORMATION CONTAINED IN THIS MANUAL WAS VITAL TO THE LEVEL II SERVICE CENTERS. THAT IS THE REASON FOR THE EARLY RELEASE. I AM WORKING ON IMPROVEMENTS TO THE MANUAL, MORE FIGURES, BLOCK DIAGRAMS, AND UP-TO-DATE INFORMATION INCLUDING A RFI SECTION. I WOULD LIKE TO ENCOURAGE COMMENTS, OR IF YOU HAVE INFORMATION WHICH YOU FEEL WOULD BE VITAL TO THIS MANUAL PLEASE SEND THEM TO CAROL JINKS 10260 BANDLEY DR. MAIL STOP 41 CUPERTINO, CALIFORNIA OR PHONE 408-973-2850.

THANK YOU IN ADVANCE FOR YOUR COOPERATION.

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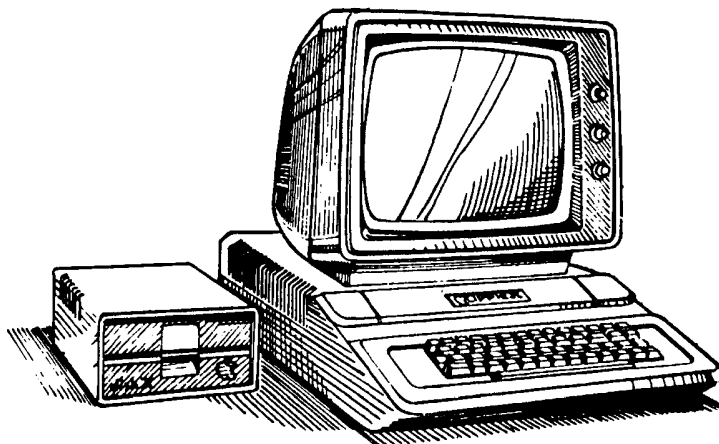


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## CHAPTER 1 GENERAL DESCRIPTION



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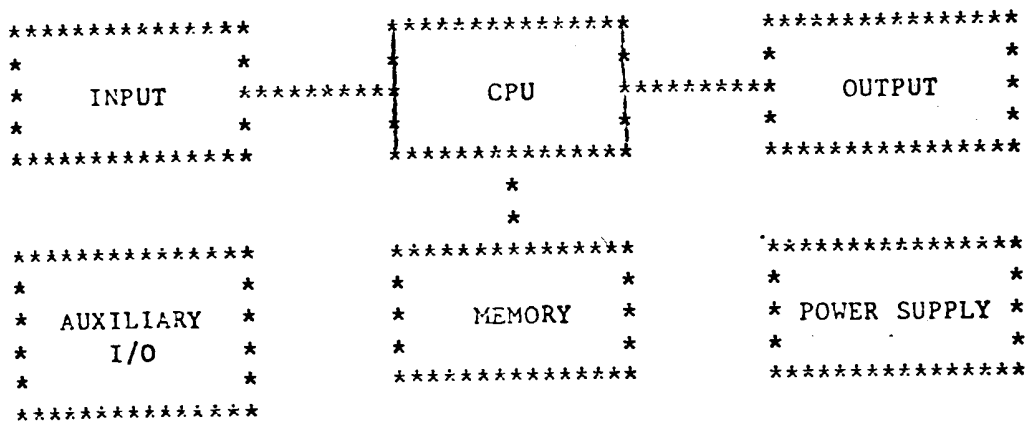
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APPLE II (PLUS)

PERSONAL COMPUTER SYSTEMS

General Description:

The Apple II and Apple II Plus systems, are composed of a CPU or central processing unit, RAM or random access memory, power supply, keyboard, video display and auxiliary I/O (input/output). This last category is made up of the game I/O, with the game paddles, buttons and annunciators. Sound output is generated by a built-in speaker. Programs and data may be saved and retrieved by means of the disk and cassette interface. Here a standard audio cassette tape recorder or Apple Disk II can be used. The Apple communicates with the outside world through 8 (50 pin) plugs or slots located along the rear edge of the system. This forms the nucleus of a Microcomputer system.



The Apple CPU or central processing unit is the 6502 Microprocessor. This LSI (Large-Scale Integration) Circuit gives the system control and processing ability. It moves character and numeric data around within the system and performs mathematic computations at microsecond speeds.

The instructions or software that controls the 6502 are located in the system memory. This memory is actually made up of small ICs of two distinct types, ROM and RAM. The RAM or random access memory contains the variable instructions and information. These memory locations can be changed at will by the 6502 and may be constantly updated. Another form of memory contained in the Apple is ROM. This memory is permanently recorded and may not be altered. It is read only memory, thus the designation ROM. When we are dealing with the Apple II or Apple II Plus, we can tell the two models apart by checking to see if the Integer Basic ROMs are present (making it an Apple II) or the Applesoft II Basic ROMs are present (making it an Apple II Plus).

The whole system is powered by a Switching Power Supply. This module supplies the 4 voltages necessary to run the Apple. They are:

- Input
- 107 to 132 VAC or
- 214 to 264 VAC

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Line frequency is not important.

Output

- +5 Volts at 2.5 amps
- 5 Volts at 500 ma
- +12 Volts at 1.5 amps (~2.5 amps intermittent)
- 12 Volts at 500 ma

In order to get information into the Apple we need the keyboard. This device is composed of 52 keys (switches) that generate all of the ASCII Characters. ASCII is the character code that the Apple understands. It stands for American Standard Code for Information Interchange. Any device that might be attached to the Apple must use this code. The Keyboard allows the user to talk to the Apple and issue commands to it. There are other forms of Input devices, that will be covered later.

Now that we have a means of getting information into the Apple, we need a way to get information and responses out. This output is generally in the form of video information sent to a video monitor or TV set. In the video mode we can present data in three different formats:

- A. Text (40 characters by 24 lines)
- B. Low Resolution Graphics (40 by 40 or 40 by 48 cell matrix)
- C. High Resolution Graphics (280 by 162 or 280 by 192 cell matrix)

When the Apple wishes to output data to the user, it presents that data in a video format. The video signal generated by the Apple is similar, but not quite the same as NTSC. It has a horizontal scan rate of 15 KHZ with 262 horizontal scan lines. It is non-interlaced with 1 field per frame and 192 active horizontal scan lines verticle. The total screen time is 65 microseconds horizontal time with 40 miicroseconds active. It will work with almost every NTSC type video monitor or TV set.

The Apple has some additional I/O devices, such as the Game Paddles, Annunciators, Speaker, and Tape Cassette Jacks. The Game Paddles allow the user to provide a form of analog input to programs running on the Apple. Buttons are provided on the paddles for momentary contact switches that can be read by the Apple. The Apple may indicate to the user electrically that a condition is on or off, by turning the Annunciators on or off. If the Apple wishes to signal or interact audibly with the user, it can use it's built in miniature speaker. Music and voice can be generated here. Lastly programs and data may be recorded and played back, by means of the Tape Cassette Ports. Data in a binary form is recorded on the tape using audio tones to represent 1s and 0s.

All of these are built in and included with the Apple II or Apple II Plus systems. The user need only add a video monitor and cassette recorder or disk drive to have a complete basic system. Other flexabilities are available by adding additional modules to the 8 (50 pin) plugs or slots on the rear edge of the Apple II system.

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	*****	*****	*****	*****	*****	*****
ROM CARD	* * *	* * *	* * *	* * *	* * *	* * *
APPLESOFT	* F8 *	* F0 *	* E8 *	* E0 *	* D8 *	* D0 *
BASIC	341-0020*	341-0015*	341-0014*	341-0013*	341-0012*	341-0011*
	*****	*****	*****	*****	*****	*****
	F800	F000	E800	E000	D800	D000

AUTO BOOT ROM ----- APPLESOFT II BASIC ROM SET -----

	*****	*****	*****	*****	*****	*****
ROM CARD	* * *	* * *	* * *	* * *	* * *	* * *
INTEGER	* F8 *	* F0 *	* E8 *	* E0 *	* D8 *	* D0 *
BASIC	341-0004*	341-0003*	341-0002*	341-0001*	* empty *	* 341-0016*
	*****	*****	*****	*****	*****	*****
	F800	F000	E800	E000	D800	D000

OLD F8 ROM ----- INTEGER BASIC ROM SET ----- EMPTY POSITION PROGRAMMER'S AID ROM

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## THE APPLE VIDEO DISPLAY

### The Apple Video Display

Display type:	Memory mapped into system RAM
Display modes:	Text, Low-Resolution Graphics, High-Resolution Graphics
Text capacity:	960 characters (24 lines, 40 columns)
Character type:	5 × 7 dot matrix
Character set:	Upper case ASCII, 64 characters
Character modes:	Normal, Inverse, Flashing
Graphics capacity:	1,920 blocks (Low-Resolution) in a 40 by 48 array 53,760 dots (High-Resolution) in a 280 by 192 array
Number of colors:	16 (Low-Resolution Graphics) 6 (High-Resolution Graphics)

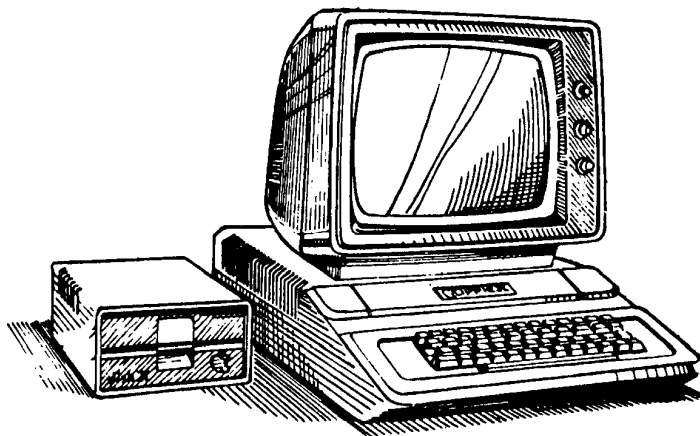


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## CHAPTER 2 VIDEO DISPLAY



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## SCREEN FORMAT

Three different kinds of information can be shown on the video display to which your Apple is connected:

- 1). Text. The Apple can display 24 lines of numbers, special symbols, and upper case letters with 40 of these characters on each line. These characters are formed in a dot matrix 7 dots high and 5 dots wide. There is a one-dot wide space on either side of the character and a one-dot high space above each line.
- 2). Low-Resolution Graphics. The Apple can present 1,920 colored squares in an array 40 blocks wide and 48 blocks high. The color of each block can be selected from a set of sixteen different colors. There is no space between blocks, so that any two adjacent blocks of the same color look like a single, larger block.
- 3). High-Resolution Graphics. The Apple can also display colored dots on a matrix 280 dots wide and 192 dots high. The dots are the same size as the dots which make up the Text characters. There are six colors available in the High-Resolution Graphics mode: black, white, red, blue, green, and violet. For Apples with Revision 0 boards, there are four colors: black, white, green and violet. Each dot on the screen can be either black, white, or a color, although not all colors are available for every dot.

When the Apple is displaying a particular type of information on the screen, it is said to be in that particular "mode". Thus, if you see words and numbers on the screen, you can reasonably be assured that your Apple is in Text mode. Similarly, if you see a screen full of multicolored blocks, your computer is probably in Low-Resolution Graphics mode. You can also have a fourline "caption" of text at the bottom of either type of graphics screen. These four lines replace the lower 8 rows of blocks in Low-Resolution Graphics, leaving a 40 by 40 array. In High-Resolution Graphics, they replace the bottom 32 rows of dots, leaving a 280 by 160 matrix. You can use these "mixed modes" to display text and graphics simultaneously, but there is no way to display both graphics modes at the same time.

## SCREEN MEMORY

The video display uses information in the system's RAM memory to generate its display. The value of a single memory location controls the appearance of a certain, fixed object on the screen. This object can be a character, two stacked colored blocks or a line of seven dots. In Text and Low-Resolution Graphics mode, an area of memory containing 1,024 locations is used as the source of the screen information. Text and Low-Resolution Graphics share this memory area. High-Resolution Graphics mode, a separate, larger area (8,192 locations) is needed because of the greater amount of information which is being displayed. These areas of memory are usually called "pages". The area reserved for High-Resolution Graphics is sometimes called the "picture buffer" because it is commonly used to store a picture or drawing.

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SCREEN PAGES

There are actually two areas from which each mode can draw its information. The first area is called the "primary pages" or "Page 1". The second area is called the "secondary page" or "page 2" and is an area of the same size immediately following the first area. The secondary page is useful for storing pictures or text which you want to be able to display instantly. A program can use the two pages too perform animation by drawing on one page while displaying the other and suddenly flipping pages.

Text and Low-Resolution Graphics share the same memory range for the secondary page, just as they share the same range for the primary page. Both mixed modes which were described above are also available on the secondary page, but there is no way to mix the two pages on the same screen.

SCREEN SWITCHES

The devices which decide between the various modes, pages, and mixes are called "soft switches". They are switches because they have two positions (for example: on or off, text or graphics) and they are called "soft" because they are controlled by the software of the computer. A program can "throw" a switch by referencing the special memory location for that switch. The data which are read from or written to the location are irrelevant; it is the reference to the address of the location which throws the switch.

There are eight special memory locations which control the setting of the soft switches for the screen. They are set up in pairs; when you reference one location of the pair you turn its corresponding mode "on" and its companion mode "off". The pairs are:

**Table 5: Screen Soft Switches**

Location:		Description:	
Hex	Decimal		
SC050	49232	-16304	Display a GRAPHICS mode.
SC051	49233	-16303	Display TEXT mode.
SC052	49234	-16302	Display all TEXT or GRAPHICS.
SC053	49235	-16301	Mix TEXT and a GRAPHICS mode.*
SC054	49236	-16300	Display the Primary page (Page 1).
SC055	49237	-16299	Display the Secondary page (Page 2).
SC056	49238	-16298	Display LO-RES GRAPHICS mode.*
SC057	49239	-16297	Display HI-RES GRAPHICS mode.*

There are ten distinct combinations of these switches:

**Table 6: Screen Mode Combinations**

Primary Page				Secondary Page			
Screen	Switches			Screen	Switches		
All Text	SC054	SC051		All Text	SC055	SC051	
All Lo-Res Graphics	SC054	SC056		All Lo-Res Graphics	SC055	SC056	SC050
All Hi-Res Graphics	SC054	SC057		All Hi-Res Graphics	SC055	SC057	SC050
Mixed Text and Lo-Res	SC054	SC056	SC053	Mixed Text and Lo-Res	SC055	SC056	SC053
Mixed Text and Hi-Res	SC054	SC057	SC053	Mixed Text and Hi-Res	SC055	SC057	SC053

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TEXT MODE

In the Text mode, the Apple can display 24 lines of characters with up to 40 characters on each line. Each character on the screen represents the contents of one memory location from the memory range of the page being displayed. The character set includes the 26 upper-case letters, the 10 digits, and 28 special characters for a total of 64 characters. The characters are formed on a dot matrix 5 dots wide and 7 dots high. There is a one-dot wide space on both sides of each character to separate adjacent lines. The characters are normally formed with white dots on a dark background; however, each character on the screen can also be displayed using dark dots on a white background or alternating between the two to produce a flashing character. When the Video Display is in Text mode, the video circuitry in the Apple turns off the color burst signal to the television monitor, giving you a clearer black-and-white display. (This feature is not present on the Revision 0 board).

The area of memory which is used for the primary text page starts at location number 1024 and extends to location number 2047. The secondary screen begins at location number 2048 and extends up to location 3071. In machine language, the primary page is from hexadecimal address \$400 to address \$7FF; the secondary page is from \$800 to \$BFF. Each of these pages is 1,024 bytes long. Those of you intrepid enough to do the multiplication will realize that there are only 960 characters displayed on the screen. The remaining 64 bytes in each page which are not displaced on the screen are used as temporary storage locations by programs stored on PROM on Apple Intelligent Interface peripheral boards.

Photo 6 shows the sixty-four characters available on the Apple's screen.

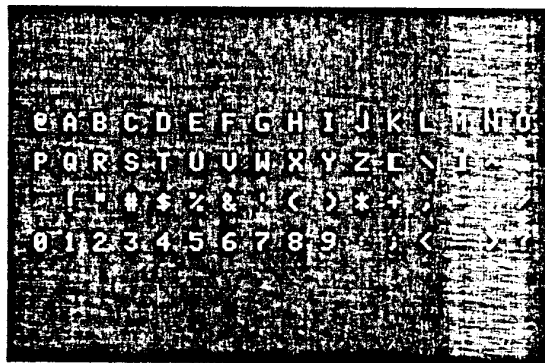


Photo 6. The Apple Character Set.

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\$400	1024	
\$480	1152	
\$500	1280	
\$580	1408	
\$600	1536	
\$680	1664	
\$700	1792	
\$780	1920	
\$428	1064	
\$4A8	1192	
\$528	1320	
\$5A8	1448	
\$628	1576	
\$6A8	1704	
\$728	1832	
\$7A8	1960	
\$450	1104	
\$4D0	1232	
\$550	1360	
\$5D0	1488	
\$650	1616	
\$6D0	1744	
\$750	1872	
\$7D0	2000	

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Figure 1. Map of the Text Screen

Table 7: ASCII Screen Characters

Decimal	Inverse				Flashing				Normal				(Lowercase)			
	0	16	32	48	64	80	96	112	128	144	160	176	192	208	224	240
Hex	\$00	\$10	\$20	\$30	\$40	\$50	\$60	\$70	\$80	\$90	\$A0	\$B0	\$C0	\$D0	\$E0	\$F0
0 \$0	@	P	0	@	P	!	1	@	P	!	1	@	P	!	1	0
1 \$1	A	Q	!	A	Q	"	2	A	Q	"	2	A	Q	"	2	1
2 \$2	B	R	"	B	R	#	3	B	R	#	3	B	R	#	3	2
3 \$3	C	S	#	C	S	\$	4	C	S	\$	4	C	S	\$	4	3
4 \$4	D	T	\$	D	T	%	5	D	T	%	5	D	T	%	5	4
5 \$5	E	U	%	E	U	&	6	E	U	&	6	E	U	&	6	5
6 \$6	F	V	&	F	V	'	7	F	V	'	7	F	V	'	7	6
7 \$7	G	W	'	G	W	(	8	G	W	(	8	G	W	(	8	7
8 \$8	H	X	(	H	X	)	9	H	X	)	9	H	X	)	9	8
9 \$9	I	Y	)	I	Y	.	:	I	Y	.	:	I	Y	.	:	9
10 \$A	J	Z	.	J	Z	+	:	J	Z	+	:	J	Z	+	:	10
11 \$B	K	[	+	K	[	\	<	K	[	+	:	K	[	+	:	11
12 \$C	L	\	\	L	\	]	>	L	\	]	>	L	\	]	>	12
13 \$D	M	]	]	M	]	^	~	M	]	]	>	M	]	]	>	13
14 \$E	N	^	^	N	^	_	~	N	^	]	>	N	^	]	>	14
15 \$F	O	_	~	O	_	/	?	O	_	/	?	O	_	/	?	15

Table 7. ASCII Screen Character Set

THE LOW-RESOLUTION GRAPHICS (LO-RES) MODE

In the Low-Resolution Graphics mode, the Apple presents the contents of the same 1,024 locations of memory as is on the Text mode, but in a different format. In this mode, each byte of memory is displayed not as an ASCII character, but as two colored blocks, stacked one atop the other. The screen can show an array of blocks 40 wide and 48 high. Each block can be any of sixteen colors. On a black-and-white television set, The colors appear as patterns of grey and white dots.

Since each byte in the page of memory for Low-Resolution Graphics represents two blocks on the screen, stacked vertically, each byte is divided into two equal sections, called (appropriately enough) "nybbles". Each nybble can hold a value from zero to 15. The value which is in the lower nybble of the byte determines the color for the upper block of that byte on the screen, and the value which is in the upper nybble determines the color for the lower block on the screen, and the value which is in the upper nybble determines the color for the lower block on the screen. The colors are numbered zero to 15, see table 8.

Colors may vary from television to television, particularly on those without hue controls. You can adjust the tint of the colors by adjusting the COLOR TRIM control on the right edge of the apple board.

So, a byte containing the hexadecimal value \$D8 would appear on the screen as a brown block on top of a yellow block. Using decimal arithmetic, the color of the lower block is determined by the remainder.

Figure 2 is a map of the Apple's display in Low-Resolution Graphics mode, with the memory location addresses for each block on the screen.

Since the Low-Resolution Graphics screen displays the same area in memory as is used for the Text screen, interesting things happen if you switch between the Text and Low-Resolution Graphics modes. For example, if the screen is in the Low-Resolution Graphics mode and is full of colored blocks, and then the TEXT/GRAPHICS screen switch is thrown to the Text mode, the screen will be filled with seemingly random text characters, sometimes inverse or flashing. Similarly, a screen full of test when viewed in Low-Resolution Graphics mode appears as long horizontal grey, pink, green or yellow bars separated by randomly colored blocks.

Table 8: Low-Resolution Graphics Colors

Decimal	Hex	Color	Decimal	Hex	Color
0	\$0	Black	8	\$8	Brown
1	\$1	Magenta	9	\$9	Orange
2	\$2	Dark Blue	10	\$A	Grey 2
3	\$3	Purple	11	\$B	Pink
4	\$4	Dark Green	12	\$C	Light Green
5	\$5	Grey 1	13	\$D	Yellow
6	\$6	Medium Blue	14	\$E	Aquamarine
7	\$7	Light Blue	15	\$F	White

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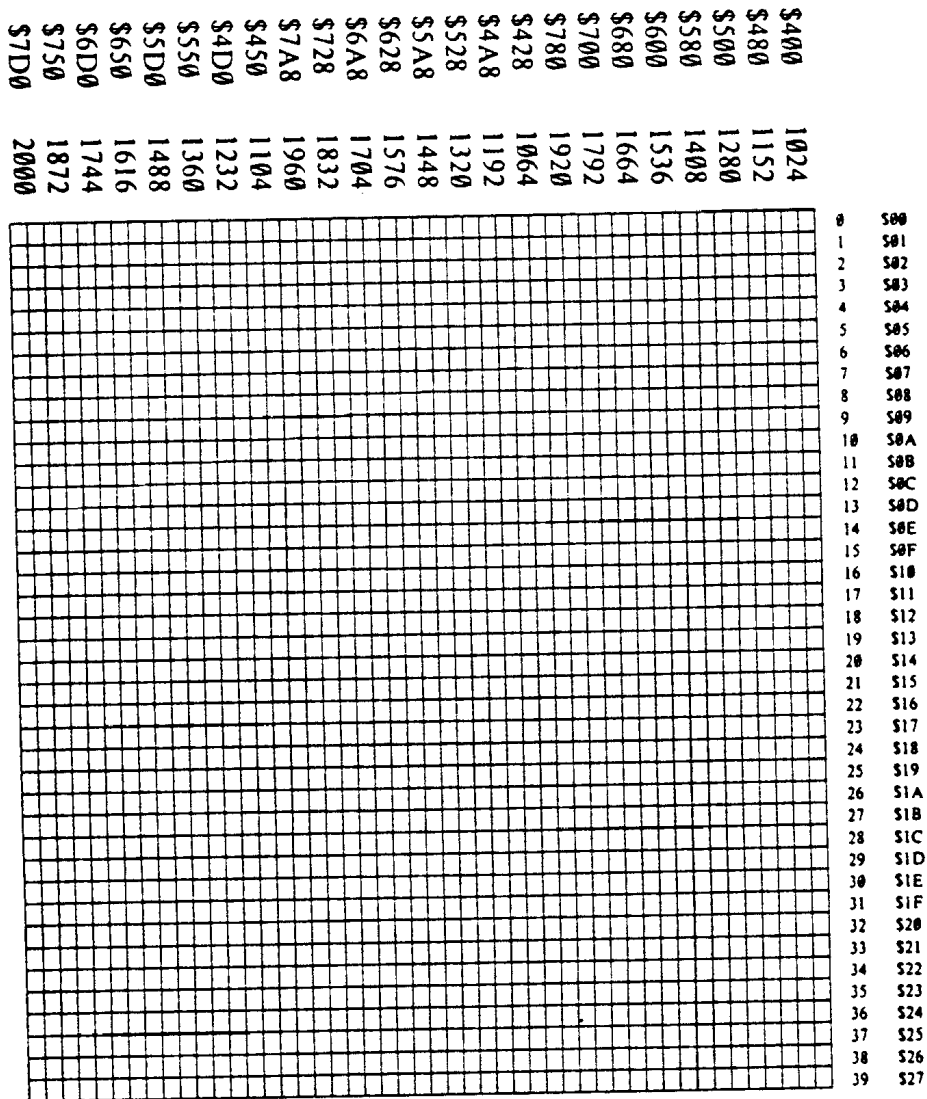


Figure 2. Map of the Low-Resolution Graphics Mode

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## THE HIGH-RESOLUTION GRAPHICS (HI-RES) MODE

The Apple has a second type of graphics display, called High-Resolution Graphics ("HIRES"). When your Apple is in the High-Resolution Graphics mode, it can display 53,760 dots in a matrix 280 dots wide and 192 dots high. The screen can display black, white, violet, green, red, and blue dots, although there are some limitations concerning the color of individual dots.

The High-Resolution Graphics mode takes its data from an 8,192-byte area of memory, usually called a "picture buffer". There are two separate picture buffers: one for the primary page and one for the secondary page. Both of these buffers are independent of and separate from the memory areas used for Text and Low-Resolution Graphics. The primary page picture buffer for the High-Resolution Graphics mode begins at memory location number 8192 and extends up to location number 16383; the secondary page picture buffer follows on the heels of the first at memory location number 16384, extending up to location number 24575. For those of you with sixteen fingers, the primary page resides from \$2000 to \$3FFF and the secondary page follows in succession at \$4000 to \$5FFF. If your Apple is equipped with 16k (16,384 bytes) or less of memory, then the secondary page is inaccessible to you; if its memory size is less than 16k, then the entire High-Resolution Graphics mode is unavailable to you.

Each dot on the screen represents one bit from the picture buffer. Seven of the eight bits in each byte are displayed on the screen, with the remaining bit used to select the colors of the dots in that byte. Forty bytes are displayed on each line of the screen. The least significant bit (first bit) of the first byte in the line is displayed on the left edge of the screen, followed by the second bit, then the third, etc. The most significant (eight) bit is not displayed. Then follows the first bit of the next byte, and so on. A total of 280 dots are displayed on each of the 192 lines of the screen.

On a blank-and white-monitor or TV set, the dots whose corresponding bits are "On" (or equal to 1) appear white; the dots whose corresponding bits are "off" or (equal to 0) appear black. On a color monitor or TV, it is not so simple. If a bit is "OFF", its corresponding dot will always be black. If a bit is "ON" however, its color will depend upon the position of that dot on the screen. If the dot is in the leftmost column on the screen, called "column 0", or in any even-numbered column, then it will appear violet. If the dot is in the rightmost column (column 279) or any odd-numbered column then it will appear green. If two dots are placed side-by-side, they will both appear white. If the undisplayed bit of a byte is turned on, then the colors blue and red are substituted for violet and green, respectively. Thus, there are six colors available in the High-Resolution Graphics mode, subject to the following limitations:

- 1) Dots in even columns must be black, violet, or blue.
- 2) Dots in odd columns must be black, green, or red.
- 3) Each byte must be either a violet/green byte or a blue/red byte. It is not possible to mix green and blue, violet and blue, or violet and red in the

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same byte.

4) Two colored dots side by side always appear white, even if they are different bytes.

5) On European-modified Apples, these rules apply but the colors generated in the High-Resolution Graphics mode may differ.

Figure 3 shows the Apple's display screen in High-Resolution Graphics mode with the memory addresses of each line on the screen.

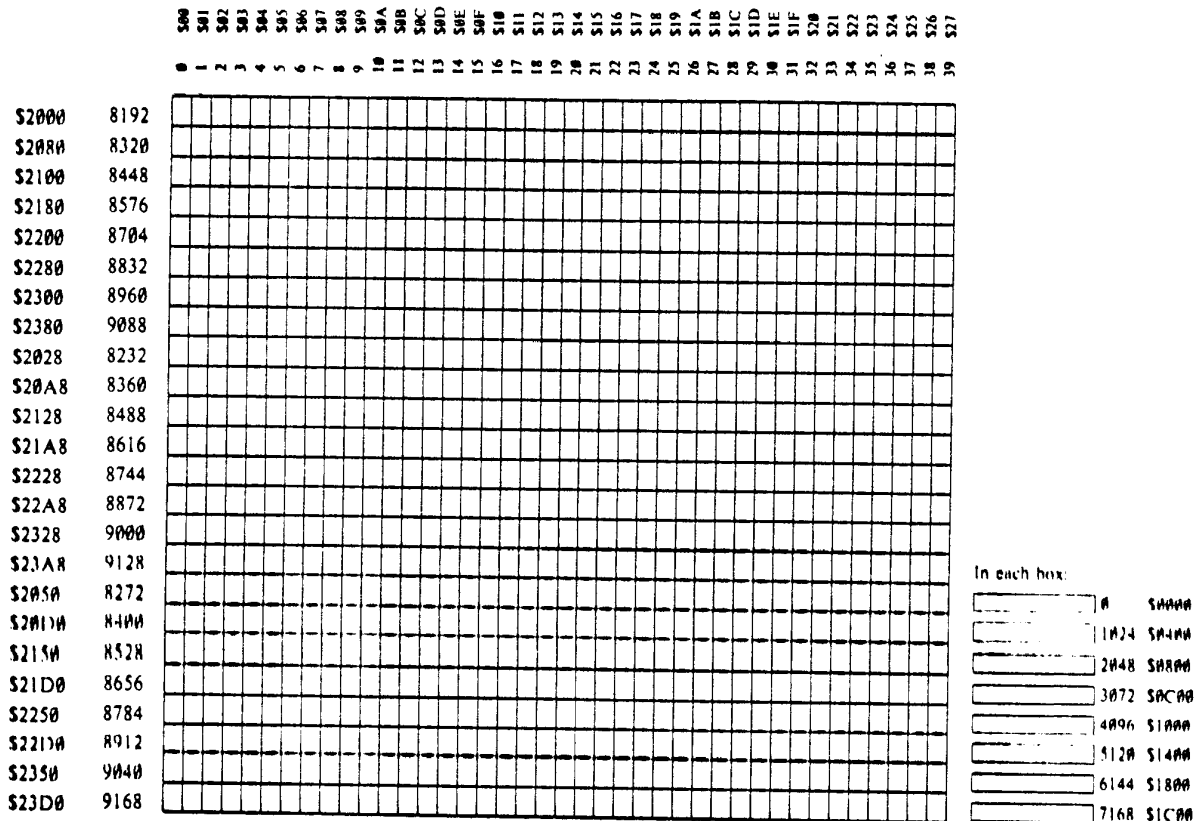


Figure 3. Map of the High-Resolution Graphics Screen

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### EURAPPLE (50 HZ) MODIFICATION

APPLE II's can be modified to generate a video signal compatible with the CCIR standard used in many European countries. To make this modification, just cut the two X-shaped pads on the right edge of the board about nine inches from the back of the board, and solder together the three O-shaped pads in the same locations (See photo 5). You can then connect the video connector of your Apple to a European standard closed-circuit black-and-white or color video monitor. If you wish, you can obtain a "Eurocolor" encoder to convert the video signal into a PAL or SECAM standard color television signal suitable for use with any European television receiver. The encoder is a small printed circuit board which plugs into the rightmost peripheral slot (slot 7) in the Apple and connects to the single video output pin.

THE EUROPEAN MODIFICATION IS NOT COMPLETE AND WE DO NOT SUPPORT OR RECOMMEND MODIFICATION OF APPLES FOR EUROPEAN TELEVISION SIGNALS.

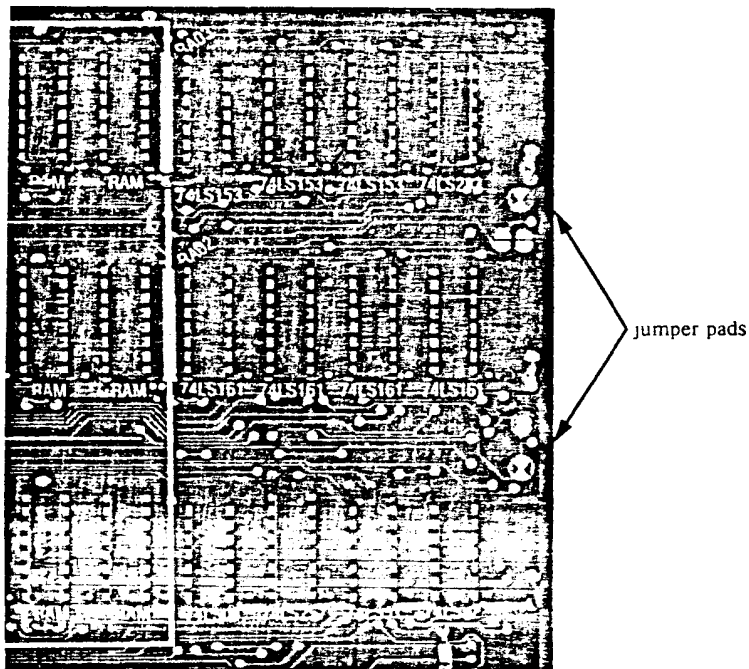


Photo 5. Eurapple (50 hz) Jumper Pads.

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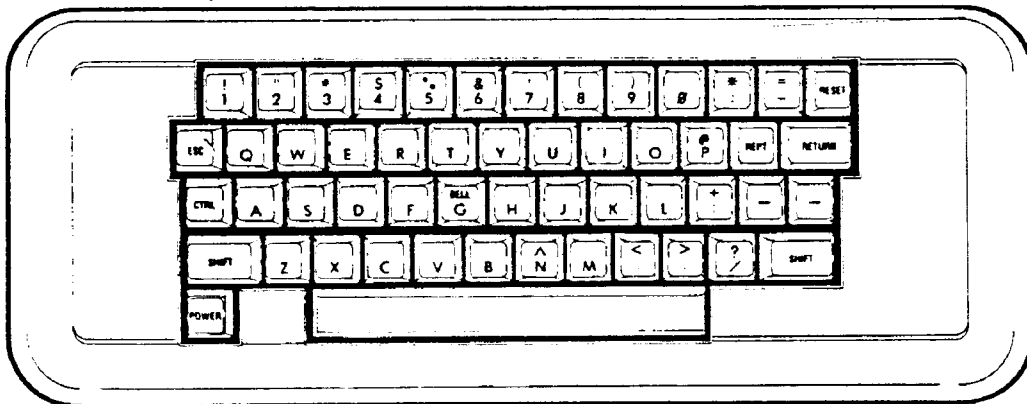
## THE KEYBOARD

### The Apple Keyboard

Number of Keys: 52  
Coding: Upper Case ASCII  
Number of codes: 91  
Output: Seven bits, plus strobe  
Power requirements: +5v at 120mA  
                          -12v at 50mA  
Rollover: 2 key  
Special keys: CTRL  
                  ESC  
                  RESET  
                  REPT  
                  ---

Memory mapped locations:	Hex	Decimal	
Data	5C000	49152	-16384
Clear	5C010	49168	-16368

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"Photo" 3. The Apple Keyboard.

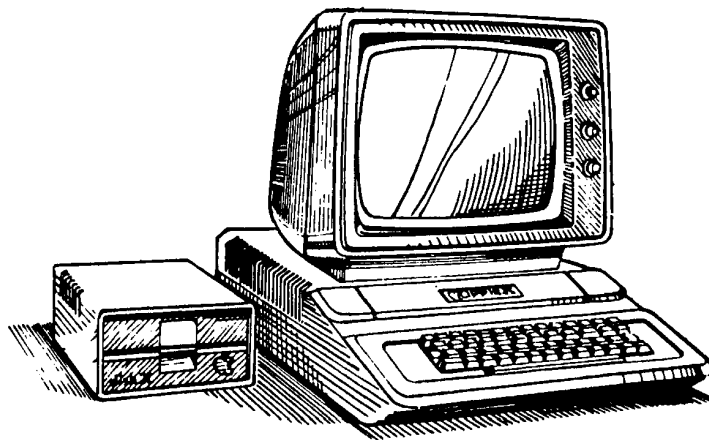


## Apple II Computer Technical Information

# APPLE II / APPLE II-PLUS LEVEL II SERVICE REFERENCE MANUAL

Pre-Release Version

## CHAPTER 3 KEYBOARD



Written by  
Apple Computer, Inc. • Level II Service Center  
1981

( This page is not part of the original service manual )

## KEYBOARD

## Theory of Operation

The APPLE II has a built-in 52-key typewriter-like which communications using the American Standard Code for Information Interchange (ASCII)\*. Ninety-one of the 96 upper-case ASCII characters can be generated directly by the keyboard. Table 2 shows the keys on the keyboard and their associated ASCII codes. Photo 3 is a diagram of the keyboard.

The keyboard is electrically connected to the main circuit board by a 16-conductor cable with plugs at each end that plug into standard integrated circuit sockets. One end of this cable is connected to the keyboard, the other end plugs into the APPLE board's keyboard connector, near the very front edge of the board, under the keyboard itself. The electrical specifications for this connector are given in Chapter 2.

The keyboard sends seven bits of information which together form one character. These seven bits, along with another signal which indicates when a key has been pressed, are available to most programs as the contents of a memory location. Programs can read the current state of the keyboard by reading the contents of this location. When you press a key on the keyboard, the value in the location becomes 128 or greater, and the particular value it assumes is the numeric code for the character which was typed. Table 3 shows the ASCII characters and their associated numeric codes. The location will hold this one value until you press another key, or until your program tells the memory location to forget the character it's holding.

Once your program has accepted and understood a keypress, it should tell the keyboard's memory location to "release" the character it is holding and prepare to receive a new one. Your program can do this by referencing another memory location. When you reference this other location, the value contained in the first location will drop below 128. This value will stay low until you press another key. This action is called "clearing the keyboard strobe". Your program can either read or write to the special memory location; the data which are written to or read from that location are irrelevant. It is the mere reference to the location which clears the keyboard strobe. Once you have cleared the keyboard strobe, you can still recover the code for the key which was last pressed by adding 128 (hexadecimal \$80) to the value in the keyboard location.

Table 11 shows the special memory locations used by the keyboard:

The RESET key at the upper right-hand corner does not generate an ASCII code, but instead is directly connected to the microprocessor. When this key is pressed, all processing stops. When the key is released, the computer starts a reset cycle.

When you turn your APPLE'S power switch ON or press and release the RESET key, the APPLE'S 6502 microprocessor initiates a RESET cycle. It begins by jumping into a subroutine in the APPLE'S Monitor ROM. In the two different versions of the ROM, the Monitor ROM and the Autostart ROM, the RESET cycle does very different things.

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The CTRL and SHIFT keys generate no codes by themselves, but only alter the codes produced by other keys.

The REPT key, if pressed alone, produces a duplicate of the last code that was generated. If you press and hold down the REPT key while you are holding down a character key, it will act as if you were pressing that key repeatedly at a rate of 10 presses each second. This repetition will cease when you release either the character key or REPT.

The ESC key, when pressed causes the APPLE'S input subroutines to go into an escape mode. In this mode, eleven keys have separate meanings, called "escape codes". When you press one of these eleven keys, the APPLE will perform the function associated with that key. After it has performed the function, The APPLE will either continue or terminate escape mode, depending upon which escape code was performed. If you press any key in escape mode which is not an escape code, then that keypress will be ignored and escape mode will be terminated. The APPLE recognizes eleven escape codes, eight of which are pure cursor moves, which simply move the cursor without altering the screen or the input line, and three of which are screen clear codes, which simply blank part or all of the screen.

The backspace key <---- when pressed moves the cursor over the printed text and deletes unwanted chars. This is extremely useful when correcting a typographical error.

The RETYPE key ----> when pressed has the same effect as typing the character which is under the cursor. This is extremely useful for re-entering the remainder of a line which you have backspaced over to correct a typographical error.

Table 2: Keys and Their Associated ASCII Codes

Key	Alone	CTRL	SHIFT	Both	Key	Alone	CTRL	SHIFT	Both
space	\$A0	\$A0	\$A0	\$A0	RETURN	\$8D	\$8D	\$8D	\$8D
0	\$B0	\$B0	\$B0	\$B0	G	\$C7	\$87	\$C7	\$87
!	\$B1	\$B1	\$A1	\$A1	H	\$C8	\$88	\$C8	\$88
2"	\$B2	\$B2	\$A2	\$A2	I	\$C9	\$89	\$C9	\$89
3#	\$B3	\$B3	\$A3	\$A3	J	\$CA	\$8A	\$CA	\$8A
4\$	\$B4	\$B4	\$A4	\$A4	K	\$CB	\$8B	\$CB	\$8B
5%	\$B5	\$B5	\$A5	\$A5	L	\$CC	\$8C	\$CC	\$8C
6&	\$B6	\$B6	\$A6	\$A6	M	\$CD	\$8D	\$DD	\$9D
7'	\$B7	\$B7	\$A7	\$A7	N"	\$CE	\$8E	\$DE	\$9E
8(	\$B8	\$B8	\$A8	\$A8	O	\$CF	\$8F	\$CF	\$8F
9)	\$B9	\$B9	\$A9	\$A9	P@	\$D0	\$90	\$C0	\$80
:*	\$BA	\$BA	\$AA	\$AA	Q	\$D1	\$91	\$D1	\$91
;+	\$BB	\$BB	\$AB	\$AB	R	\$D2	\$92	\$D2	\$92
,<	\$AC	\$AC	\$BC	\$BC	S	\$D3	\$93	\$D3	\$93
-=	\$AD	\$AD	\$BD	\$BD	T	\$D4	\$94	\$D4	\$94
.>	\$AE	\$AE	\$BE	\$BE	U	\$D5	\$95	\$D5	\$95
/?	\$AF	\$AF	\$BF	\$BF	V	\$D6	\$96	\$D6	\$96
A	\$C1	\$81	\$C1	\$81	W	\$D7	\$97	\$D7	\$97
B	\$C2	\$82	\$C2	\$82	X	\$D8	\$98	\$D8	\$98
C	\$C3	\$83	\$C3	\$83	Y	\$D9	\$99	\$D9	\$99
D	\$C4	\$84	\$C4	\$84	Z	\$DA	\$9A	\$DA	\$9A
E	\$C5	\$85	\$C5	\$85	-	\$88	\$88	\$88	\$88
F	\$C6	\$86	\$C6	\$86	-	\$95	\$95	\$95	\$95
					ESC	\$9B	\$9B	\$9B	\$9B

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All codes are given in hexadecimal. To find the decimal equivalents, use Table 3.

**Table 3: The ASCII Character Set**

Decimal:	128	144	160	176	192	208	224	240
Hex:	\$80	\$90	\$A0	\$B0	\$C0	\$D0	\$E0	\$F0
0	\$0	nul	dle		@	P		P
1	\$1	soh	dcl	!	A	Q	a	q
2	\$2	stx	dc2	"	B	R	b	r
3	\$3	etx	dc3	#	C	S	c	s
4	\$4	eot	dc4	\$	D	T	d	t
5	\$5	enq	nak	%	E	U	e	u
6	\$6	ack	syn	&	F	V	f	v
7	\$7	bel	etb	'	G	W	g	w
8	\$8	bs	can	(	H	X	h	x
9	\$9	ht	em	)	I	Y	i	y
10	\$A	lf	sub	*	J	Z	j	z
11	\$B	vt	esc	+	K	[	k	[
12	\$C	ff	fs	,	L	\	l	]
13	\$D	cr	gs	-	M	]	m	]
14	\$E	so	rs	.	N	^	n	^
15	\$F	si	us	/	O	_	o	~

**Table 1: Keyboard Special Locations**

Location:			Description
Hex	Decimal		
\$C000	49152	-16384	Keyboard Data
\$C010	49168	-16368	Clear Keyboard Strobe

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### KEYBOARD VARIETIES

The first Apple keyboard was built by Datametics, assembly number 01-0425. The built-in keyboard was built around a MM5740 monolithic keyboard decoder ROM. The inputs to this Rom, on pins 4 through 12 and 22 through 31, are connected to the matrix of keyswitches on the keyboard. The outputs of this Rom are buffered by a 7404 and are connected to the Apple's Keyboard Connector.

The keyboard decoder rapidly scans through the array of keys on the keyboard, looking for one which is pressed. This scanning action is controlled by the free-running oscillator made up of three sections of a 7400 at keyboard location U4. The speed of this oscillation is controlled by C6, R6, and R7 on the keyboard's printed -circuit board. This keyboard is non-serivable.

The second Apple keyboard was also built by Datametics, assembly number 01-0551-0. The keyboard comes with a redesigned keyboard made up of two parts, mechanical assembly (power light and 52 key switch matrix), and encoder board (contains all electronic components). This style uses the same key switch that was used on the old style keyboard (Assembly #01-0425). The replacement procedure for this key switch is found in Appendix D.

The third Apple keyboard was built by the keyboard Company which is located in Garden Grove, California. This style uses a new key switch whose replacement procedure is described in Appendix D. This style does not require the aluminum bracket stand-offs. This keyboard is referred to as an ALPS switchable with low profile or sculptured key caps. It also contains an encoder board separate from the mechanical assembly.

The fourth Apple keyboard was also built by the Keyboard Company. This keyboard is described as a bucket keyboard. It also is a two piece keyboard with a detachable encoder board and a non-repairable mechanical assembly. This keyboard offers two types of keycaps low profile and sculptured.

All the keyboards described above use the same encoder board except the first keyboard built by Datametics. Each keyboard is built around a AY-5-3600 keyboard encoder Rom. The inputs to this ROM, on pins 17 through 26 and 36 through 40 are connected to the matrix of keyswitches on the keyboard. The outputs of this ROM are buffered by a 74LS04 and are connected to the Apple keyboard connector.

The keyboard decoder rapidly scans through the array of keys on the keyboard, looking for one which has been pressed. This scanning action is controlled by the free running oscillator made up of three sections of a 74LS00 at location B3 on the separate encoder board. The speed of this oscillation is controlled by C7, R7, and R8 on the encoder board.

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## ENCODER BOARD

### Theory of Operation:

The keyboard is a scanning encoder scheme. It uses a clock formed by 3 gates from B4 (74LS00), and 2 resistor with a capacitor to generate a 75 KHZ scan rate. The scan sequences through all of it's inputs looking for a transition. When it finds a transition it takes the X,Y co-ordinance of the key pressed and produces an ASCII character. This character corresponds to the key pressed.

The keyboard is also capable of repeating a particular character by activating the REPEAT key. This causes the some character to output with the strobe pulsing at 1 HZ or 1 character per/second. This repeat circuit is formed by a LM555 Monolithic Timer chip. It forms a square wave clock that pulses the data strobe line on and off for each repeat or a desired character.

The Encoder is a AY-5-3600-931 MOS chip which converts X,Y co-ordinates into ASCII Characters. It has inputs for Scan Clock, Repeat Clock, and Control Key functions. The output is held in the enable mode by pulling it to ground.

The keys are arranged in a matrix that has 5 columns and 10 rows. Each key on the board is a cross point switch which shorts a unique X,Y location on the matrix. Each key has it's own X and Y. This produces a unique address for each key. The encoder sequences through it's key addresses until an X causes a Y to go to logic 1. When this occurs we have a key press and the encoders current address in the sequence corresponds to a data byte which is the ASCII Character desired. It then presents this ASCII Character as it's output and generates a strobe.

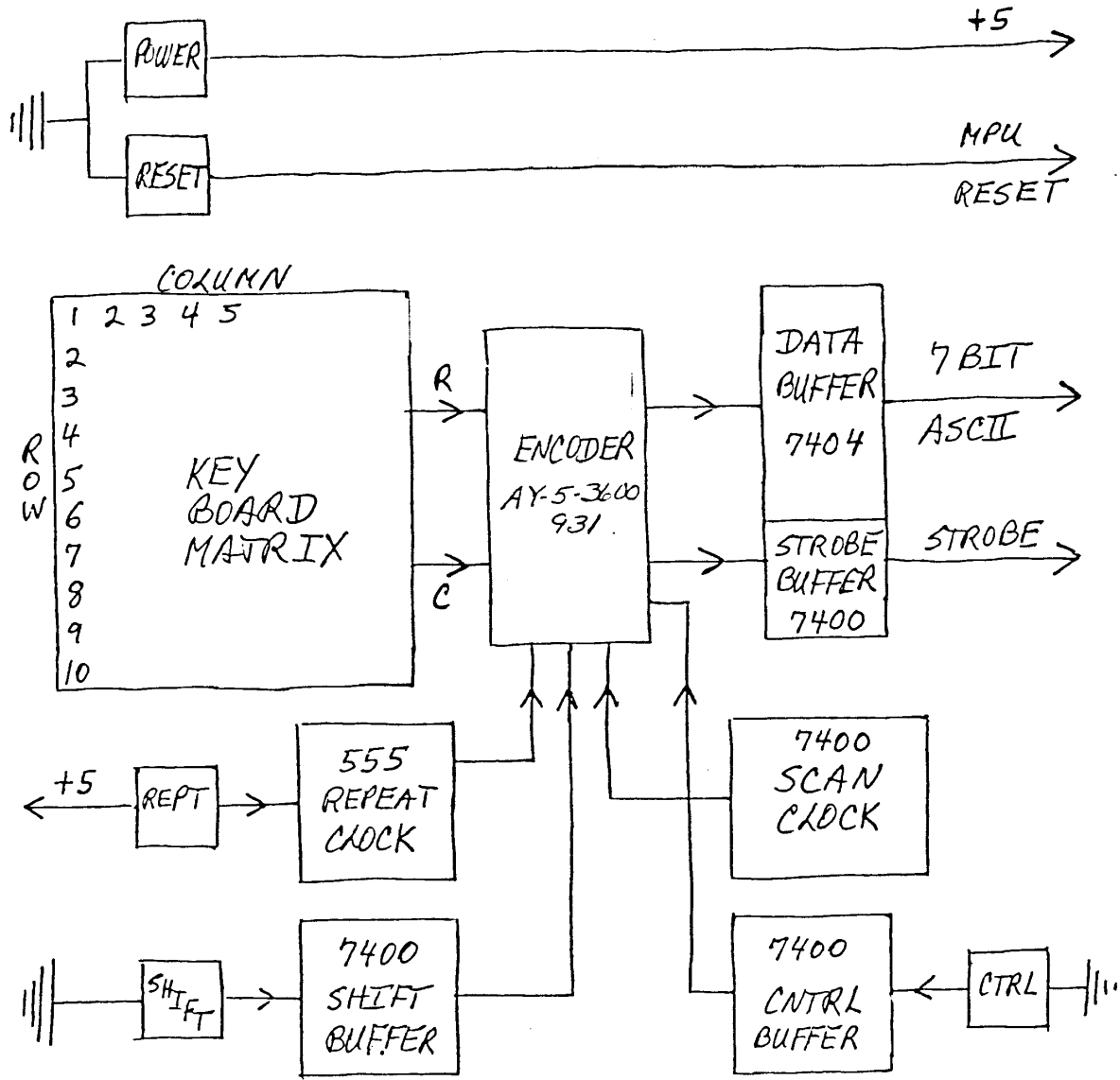
When a Shift or Control Character is desired the appropriate CTRL or SHIFT key is pressed in conjunction with the selected key value. This alters the addressing of the encoder to produce the character with the bit pattern of a control character. The SHIFT key and CTRL key give us the function of many keys with few keep switches.

On the input to the encoder there is a debounce circuit. This circuit prevents the same key from being read two or more times. If it see's a second key press of the same key too soon it will ignore that signal. This delay in sampling is approximately the time it takes to depress and release a key switch. When a key is bouncing it will give a transition on the way down when pressed and also on the way up when it springs back into place. This sampling is quick enough that a litigitimate multipule character will be accepted.

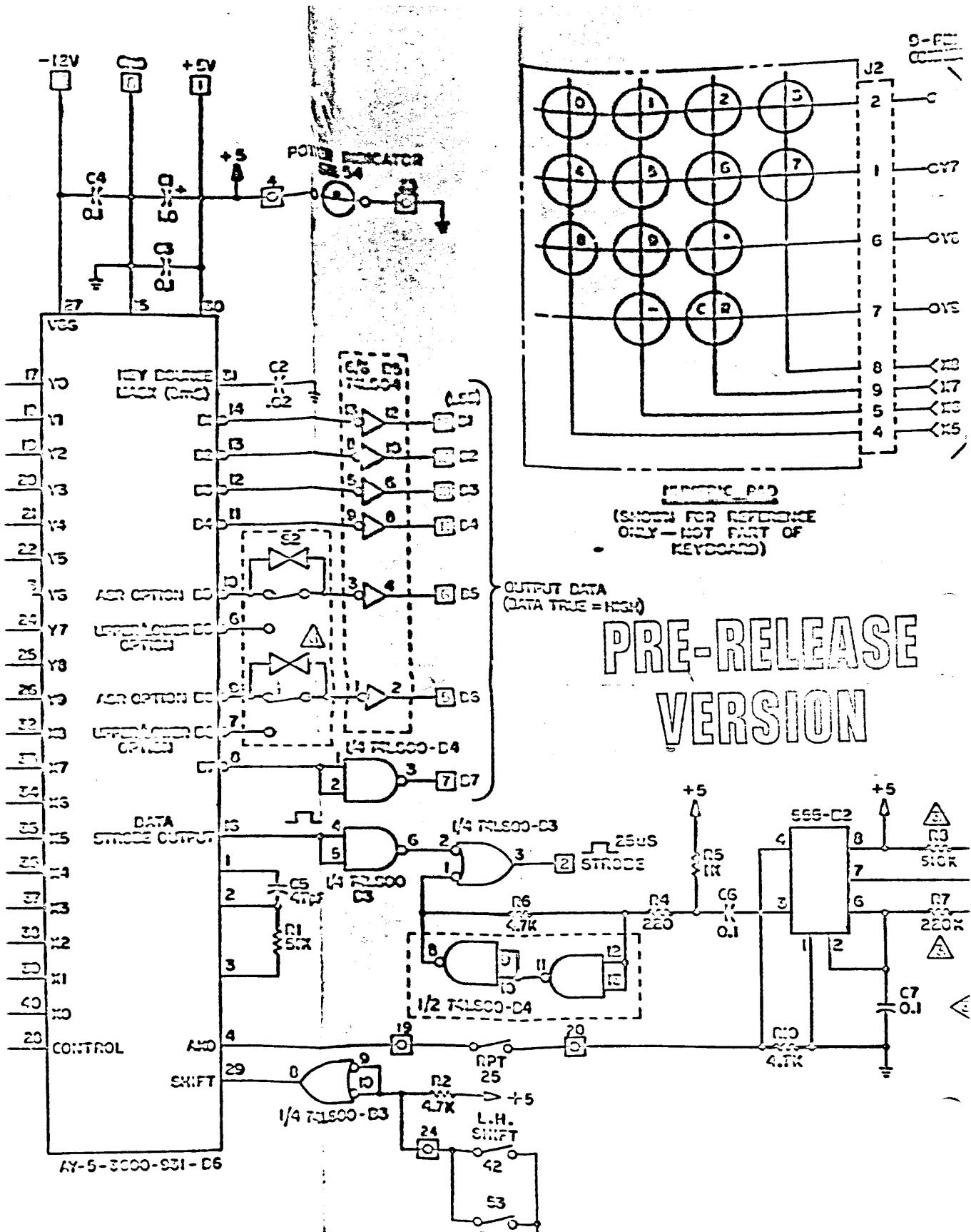
When typing on the Apple II keyboard the fastest human operator will never loose a character as the key board has N Key roll over. This means that the keyboard is scanned at a faster rate than a human typist can generate characters.

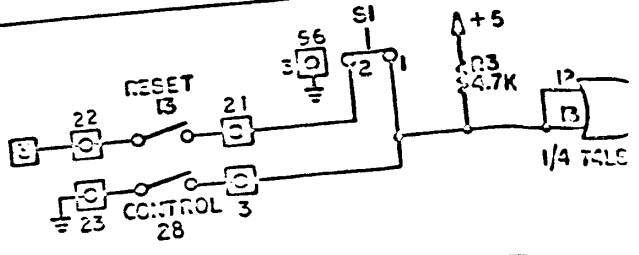
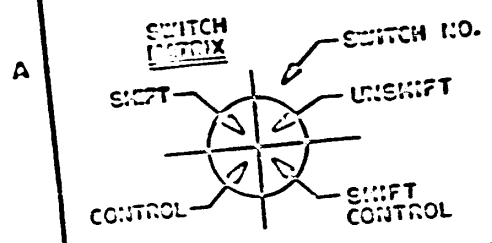
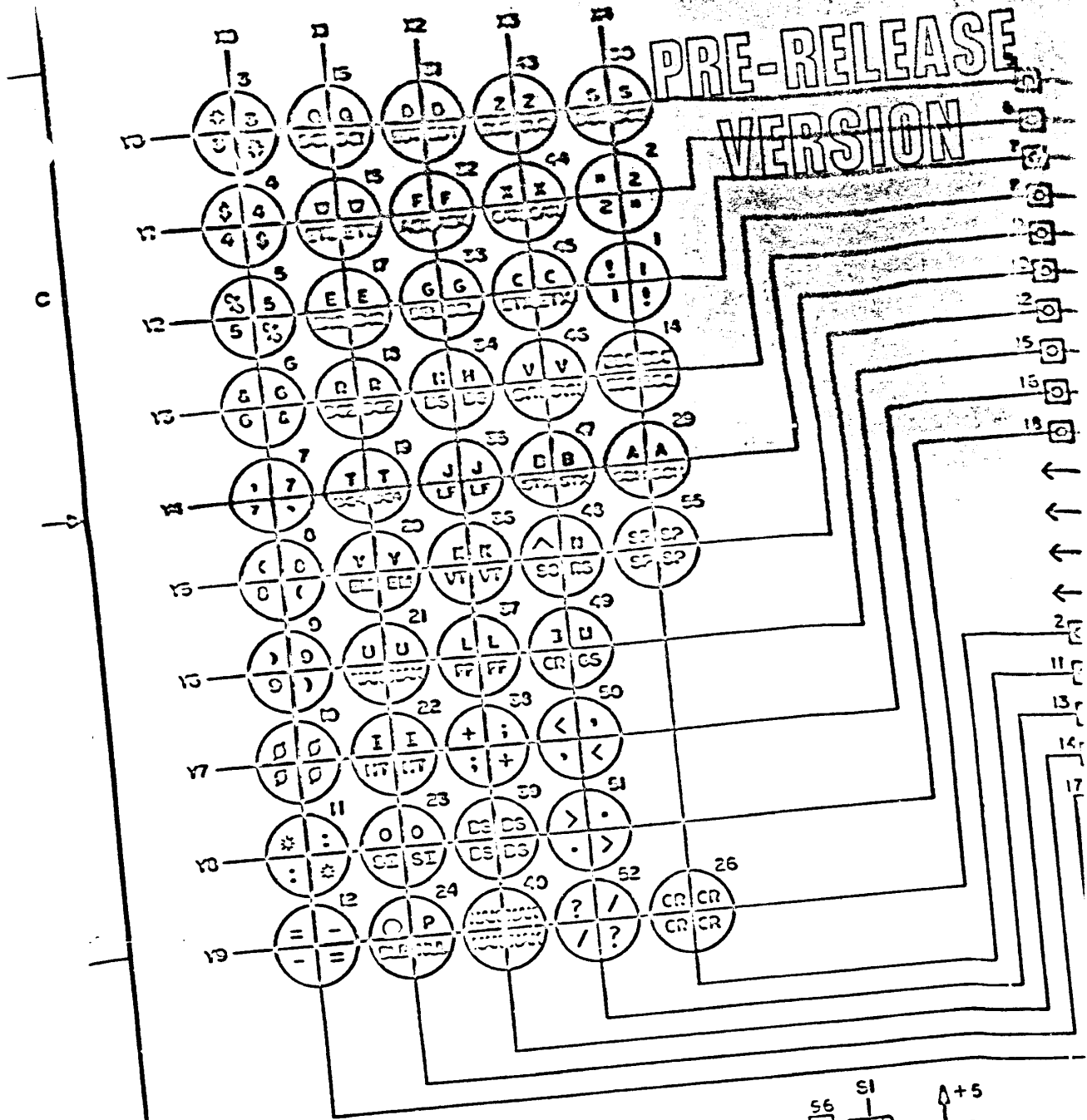
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# KEY BOARD BLOCK DIAGRAM



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4

### AUTOSTART ROM/MONITOR ROM

All Apple II Plus Systems include the Autostart Monitor ROM. All other Apple systems do not contain the Autostart ROM, but instead have the Apple System Monitor ROM. This version of the ROM lacks some of the features present in the Autostart ROM, but also has some features which are not present in that ROM. The main differences in the two ROMS are listed below.

**Editing Controls:** The ESC-I,J,K, and M sequences, which move the cursor up, left, right, and down, respectively, are not available in the Old Monitor ROM.

**Stop-List:** The Stop-List feature (invoked by a CTRL S, which allows you to introduce a pause into the output of most BASIC or machine language programs or listings, is not available in the Old Monitor ROM.

**The RESET cycle:** When you first turn on your Apple or press RESET, the Old Monitor ROM will send you directly into the Apple System Monitor, instead of initiating a warm or cold start as described in AUTOSTART ROM RESET.

### AUTOSTART ROM RESET

Apples with the Autostart ROM begin their RESET cycles by flipping the soft switches which control the video screen to display the full primary page of Text mode, with Low-Resolution Graphics mixed mode lurking behind the veil of text. It then opens the text window to its full size, drops the output cursor to the bottom of the screen, and sets Normal video mode. Then it sets the COUT and KEYLN switches to use the APPLE'S internal keyboard and video display as the standard input and output devices. It flips annunciators 0 and 1 OFF and annunciators 2 and 3 ON the Game I/O connector, clears the keyboard strobe, turns off any active I/O Expansion ROM and sounds a "beep!".

These actions are performed every time you press and release the RESET key on your APPLE. At this point, the Autostart ROM peeks into two special locations in memory to see if it's been RESET before or if the APPLE has just been turned on, then the Autostart ROM performs a "cold start" otherwise, it does a "warm start".

1)Cold Start. On a freshly activated Apple, RESET cycle continues by clearing the screen and displaying "APPLE II" top and center. It then sets up the special locations in memory to tell itself that it's been powered up and RESET. Then it starts looking through the rightmost seven slots in your APPLE'S backplane, looking for a Disk II Controller Card. It starts the search with Slots 7 and continues down to Slot 1. If it finds a disk controller card, then it proceeds to bootstrap the Apple Disk Operating System (Dos) from the diskette in the disk drive attached to the controller card it discovered. You can find a description of the disk bootstrapping procedure in Do's and Don't of DOS. Apple part number A2L0012, page 11.

If the Autostart ROM cannot find a Disk II controller card, or you press RESET again before the disk booting procedure has completed, then the RESET cycle will continue with a "lukewarm start". It will initialize and jump into the language which is installed on ROM on your APPLE. For a Revision 0 APPLE, either without an Applesoft II firmware card or with such a card with

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its controlling switch in the DOWN position, the Autostart ROM will start Apple Integer Basic. For Apple II-plus systems, or Revision 0 Apple IIs with the Applesoft II Firmware card with the switch in the UP position, The Autostart ROM will begin Applesoft II Floating-Point BASIC.

2) Warm Start. If you have an Autostart ROM which has already performed a cold start cycle, then each time you press and release the RESET key, you will be returned to the language you were using, with your program and variables intact.

#### "OLD MONITOR" ROM RESET

A RESET cycle in the Apple II Monitor ROM begins by setting Normal video mode, a full screen of Primary Page text with the Color Graphics mixed mode behind it, a fully-opened text window, and Apple's standard keyboard and video screen as the standard input and output devices. It sounds a "beep!", the cursor leaps to the bottom line of the uncleared text screen, and you find yourself facing an asterisk (\*) prompt and talking to the Apple System Monitor.

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## SUBROUTINES

Almost every program and language on the APPLE needs some sort of input from the keyboard, and some way to print information on the screen. There is a set of subroutines stored in the APPLE'S ROM which handle most of the standard input and output from all programs and languages on the APPLE.

The subroutines in the APPLE'S ROM which perform these input and output functions are called by various names. These names were given to the subroutines by their authors when they were written. The APPLE itself does not recognize or remember the names of its own machine language subroutines, but it's convenient for us to call these subroutines by their given names.

### Standard Output:

The standard output subroutine is called COUT. COUT will display upper-case letters, numbers, and symbols on the screen in either Normal or Inverse mode. It will ignore control characters except RETURN, the bell character, the line feed character, and the backspace character.

The COUT subroutine maintains its own invisible "output cursor"\* (the position at which the next character is to be placed). Each time COUT is called, it places one character on the screen at the current cursor position, replacing whatever character was there, and moves the cursor one space to the right. If the cursor is bumped off the right edge of the screen, then COUT shifts the cursor down to the first position on the next line. If the cursor passes the bottom line of the screen, the screen "scrolls" up one line and the cursor is set to the first position on the newly blank bottom line.

When a RETURN character is sent to COUT, it moves the cursor to the first position of the next line. If the cursor falls off the bottom of the screen, the screen scrolls as described above.

### The Stop-List Feature:

When any program or language sends a RETURN code to COUT, COUT will take a quick peek at the keyboard. If you have typed a CTRL S since the last time COUT looked at the keyboard, then it will stop and wait for you to press another key. This is called the Stop-List Feature. This feature is not present on APPLES without the Autostart ROM. When you press another key, COUT will then output the RETURN code and proceed with normal output. The code of the key which you press to end the Stop-List mode is ignored unless it is a CTRL C. If it is, then COUT passes this character code back to the program or language which is sending output. This allows you to terminate a BASIC program or listing by typing CTRL C while you are in Stop-List mode.

A line feed character causes COUT to move its mythical output cursor down one line without and horizontal motion at all. As always, moving beyond the bottom of the screen causes the screen to scroll and the cursor remains at its same position on a fresh bottom line.

A backspace character moves the imaginary cursor one space to the left. If the cursor is bumped off the left edge, it is reset to the rightmost

position on the previous line. If there is no previous line (if the cursor was at the top of the screen), the screen does not scroll downwards, but instead the cursor is placed again at the rightmost position on the top line of the screen.

When Cout is sent a "bell" character (CTRL G), it does not change the screen at all, but instead produces a tone from the speaker. The tone has a frequency of 100 Hz and lasts for 1/10th of a second. The output cursor does not move for a bell character.

#### Standard Input:

There are actually two subroutines which are concerned with the gathering of standard input: RDKEY, which fetches a single keystroke from the keyboard, and GETLN, which accumulates a number of keystrokes into a chunk of information called an input line.

#### RDKEY:

The primary function of the RDKEY subroutine is to wait for the user to press a key on the keyboard, and then report back to the program which called it with the code for the key which was pressed. But while it does this, RDKEY also performs two other helpful tasks:

1). Input Prompting. When RDKEY is activated, the first thing it does is make visible the hidden output cursor. This accomplishes two things: it reminds the user that the APPLE is waiting for a key to be pressed, and it also associates the input it wants with a particular place on the screen. In most cases, the input prompt appears near a word or phrase describing what is being requested by the particular program or language currently in use. The input cursor itself is a flashing representation of whatever character was at the position of the output cursor. Usually this is the blank character, so the input cursor most often appears to be a flashing square. When the user presses a key, RDKEY dutifully removes the input cursor and returns the value of the key which was pressed to the program which requested it. Remember that the output cursor is just a position on the screen, but the input cursor is a flashing character on the screen. They usually move in tandem and are rarely separated from each other, but when the input cursor disappears, the output cursor is still active.

2). Ramdon Number Seeding. While it waits for the user to press a key, RDKEY is continually adding 1 to a pair of numbers in memory. When a key is finally pressed, these two locations together represent a number from 0 to 65,535, the exact value of which is quite unpredictable. Many programs and languages use this number as the base of a random number generator. The two locations which are randomized during RDKEY are numbers 78 and 79 (hexadecimal \$4E and \$4F).

#### GETLN:

The vast majority of input to the APPLE is gathered into chunks called input lines. The subroutine in the APPLE'S ROM called GETLN requests an input line from the keyboard, and after getting one, returns to the program which called it. GETLN has many features and nuances, and it is good to be

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familiar with the services it offers.

When called, GETLN first prints a prompting character, or "prompt". The Prompt helps you to identify which program has called GETLN requesting input. A prompt character of an asterisk (\*) represents the System Monitor, a right caret (>) indicates Apple Integer BASIC, a right bracket (]) is the prompt for Applesoft II BASIC, and an exclamation point (!) is the hallmark of the APPLE Mini-Assembler. In addition, the question-mark prompt (?) is used by many programs and languages to indicate that a user program is requesting input. From your (the user) point of view, the Apple simply prints a prompt and displays an input cursor. As you type, the characters you type are printed on the screen and the cursor moves accordingly. When you press RETURN, the entire line is sent off to the program or language you are talking to, and you get another prompt.

Actually, what really happens is that after the prompt is printed, GETLN calls RDKEY, which displays an input cursor. When RDKEY returns with a keycode, GETLN stores that keycode in an input buffer and prints it on the screen where the input cursor was. It then calls RDKEY again. This continues until the user presses RETURN. When GETLN receives a RETURN code from the keyboard, it sticks the RETURN code at the end of the input buffer, clears the remainder of the screen line the input cursor was on, and sends the RETURN code to COUT (see above). GETLN then returns to the program which called it. The program or language which requested input may now look at the entire line, all at once, as saved in the input buffer.

At any time while you are typing a line, you can type a CTRL X and cancel that entire line. GETLN will simply forget everything you have typed, print a backslash (\), skip to a new line, and display another prompt, allowing you to retype the line. Also, GETLN can handle a maximum of 255 characters in a line. If you exceed this limit, GETLN will cancel the entire line and you must start over. To warn you that you are approaching the limit, GETLN will sound a tone every keypress starting with the 249th character.

GETLN also allows you to edit and modify the line you are typing in order to correct simple typographical errors. A quick introduction to the standard editing functions and the use of the two arrow keys, <---- and ---->, appears in the section entitled Keyboard Theory.

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VERSION

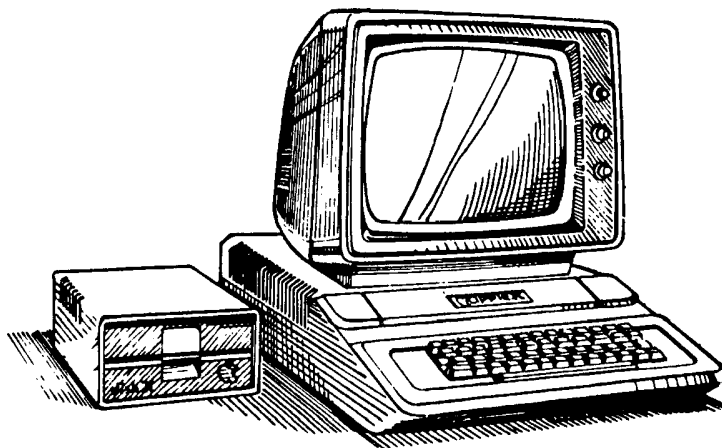


## Apple II Computer Technical Information

# APPLE II / APPLE II-PLUS LEVEL II SERVICE REFERENCE MANUAL

Pre-Release Version

## CHAPTER 4 POWER SUPPLY



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Apple Computer, Inc. • Level II Service Center  
1981

( This page is not part of the original service manual )

# PRE-RELEASE VERSION

## POWER SUPPLY

### Theory of Operation

The metal box on the left side of the interior is the power supply. It supplies four volages +5v, -5.2v, +11.8v, and -12.0v. It is a high-frequency "switching" type power supply, with many protective features to ensure that there can be no imbalances between the different supplies. The main power cord for the computer plugs directly into the back of the power supply. The power on switch is also on the power supply itself, to protect you and your fingers from accidently becoming part of the high voltage power supply circuit.

The Apple power supply first converts the AC line voltage into a DC voltage and then uses this DC voltage to drive a high-frequency oscillator. The output of this oscillator is fed into a small transformer with many windings. The volages on the secondary windings are then regulated to become the output volages.

The +5 volt output voltage is compared to a reference voltage, and the difference error is fed back into the oscillator circuit. When the power supply's output starts to move out of its tolerances the frequency of the oscillator is altered and the volages return to their normal levels. If by chance one of the output volages of the power supply is short-circuited a feed back circuit in the power supply stops the oscillator and cuts all output circuits. The power supply then pauses for about 1/2 second and then attempts to restart the oscillations. If the output is still shorted, it will stop and wait again. It will continue this cycle until the short circuit is removed or the power is turned off.

If the output connector of the power supply is disconnected from the Apple board, the power supply will notice this "no load" condition and effectively short-circuit itself. This activates the protection circuits described above, and cuts all power output. This pervents damage to the power supply's internals.

If one of the output volages leaves its tolerance range, due to any problem either within or external to the power supply, it will again shut itself down to prevent damage to the components on the Apple board. This insures that all volages will either be correct and in porportion, or they will be shut off.

When one of the above fault conditions occurs, the internal protection circuits will stop the oscillations which drive the transformer. After a short while, the power supply will perform a restart cycle, and attempt to oscillate again. If the fault condition has not been removed, the supply will again shut down. This cycle can continue infinitely without damage to the power suply. Each time the oscillator shuts down and restarts, its frequency passes through the audible range and you can hear the power supply squeal and squeak. Thus, when a fault occurs, you will hear a steady "click click click" emanating from the power supply. This is your warning that something is wrong with one of the voltage outputs.

Under no circuntances should you apply more than 140 VAC to the input

of the transformer (or more than 280 VAC when the supply's switch is in the 220V position, if so equipped). Permanent damage to the supply will result.

THE APPLE POWER SUPPLY

Input Voltages: 107vac to 132vac  
214vac to 264vac

Supply voltages: +5.0  
+11.0  
-12.0  
+5.2

Power Consumption: 60 watts max. (full load)  
79 watts max. (intermittent)

Full Load Power Output:  
+5v: 2.5amp  
-5v: 250ma  
+12v: 1.5amp (~2.5amp intermittent)  
-12v: 250ma

Operating Temperature:  
55c (131 degrees fahrenheit)

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### POWER SUPPLY VARIETIES

#### Physical Description:

Four basic power supplies have been used on the Apple II since it was first introduced. Modifications and changes to the power supplies have been incorporated during the normal evolution of Apple II, which have made new part numbers necessary to identify modifications to each basic model. The four basic power supplies, modifications, changes and part numbers in order of production are:

Note: Apple supports all of the power supplies listed below except the first one which is being phased out. The RFI version is the only available new power supply.

1) Apple Power Supply (P/N 600--0026) (EM/N 600-9026)

The first power supply used in the Apple II computers was manufactured by Apple. A description on how the power supply functions is found in the theory portion of this chapter. To physically distinguish the first Apple power supply from the others note the toggle on/off switch on the outside of the case.

2) Apple Power Supply (P/N 605-5001) (EM/N 605-9001)

Designed and marketed by Apple Computer. Identified by the Apple Part number A2M001 on the back of the case. The case is Silver in color. On the back of the case indicates UL recognition.

3) Astec Model AA11040 Standard (P/N 605-5703) (EM/N 605-9703)

Astec is a manufacturer of power supplies in Hong Kong. The third power supply used in the Apple II computers was model 11040 built by Astec. The 11040 standard power supply was more cost effective and had a higher reliability rate than the Apple power supply. The physical difference can be seen in photo 2.

a. Switchable Version Astec Model AA11040 Standard (P/N 605-6001) (EM/N 605-9001)

Note the on/off switch and the black cover protecting the switchable 115v/230v switch. The model number AA 11040 is located on the power supply. The 11040 standard power supply is not U/L approved but U/L recognized.

4) Astec Model AA11040B (P/N 652-0337) (EM/N 652-9337)

European Version Astec Model AA11040B (P/N 699-0049) (EM/N 699-9049)

The fourth power supply which is model number 11040-B was built by Astec to meet U/L approval. Astec removed the outside 115v/230v switch and now uses jumpers on the PCB to determine whether it is to be a 115v or 230v power supply.

a) RFI Version Astec Model AA11040B:

110 volt (P/N 652-0337) (EM/N 652-9337)

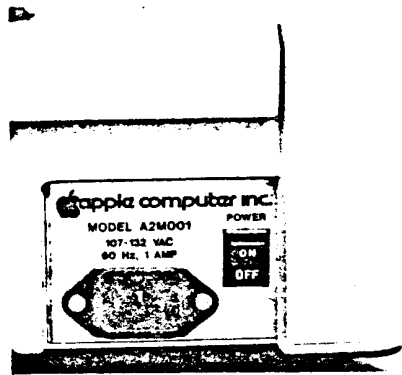
PRE-RELEASE  
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220 volt (P/N 699-0049) (EM/N 699-9049)

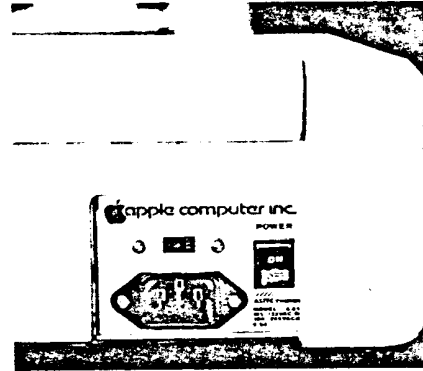
Astec Model AA11040B with Astec production numbers 55073241 through 55074240 and all AA11040B units beginning with 55079547 are RFI. Astec production numbers are stamped in the case on the left side of the unit. RFI units are also identified by a red dot on the back of the power supply.

All RFI power supplies are UL Recognized.

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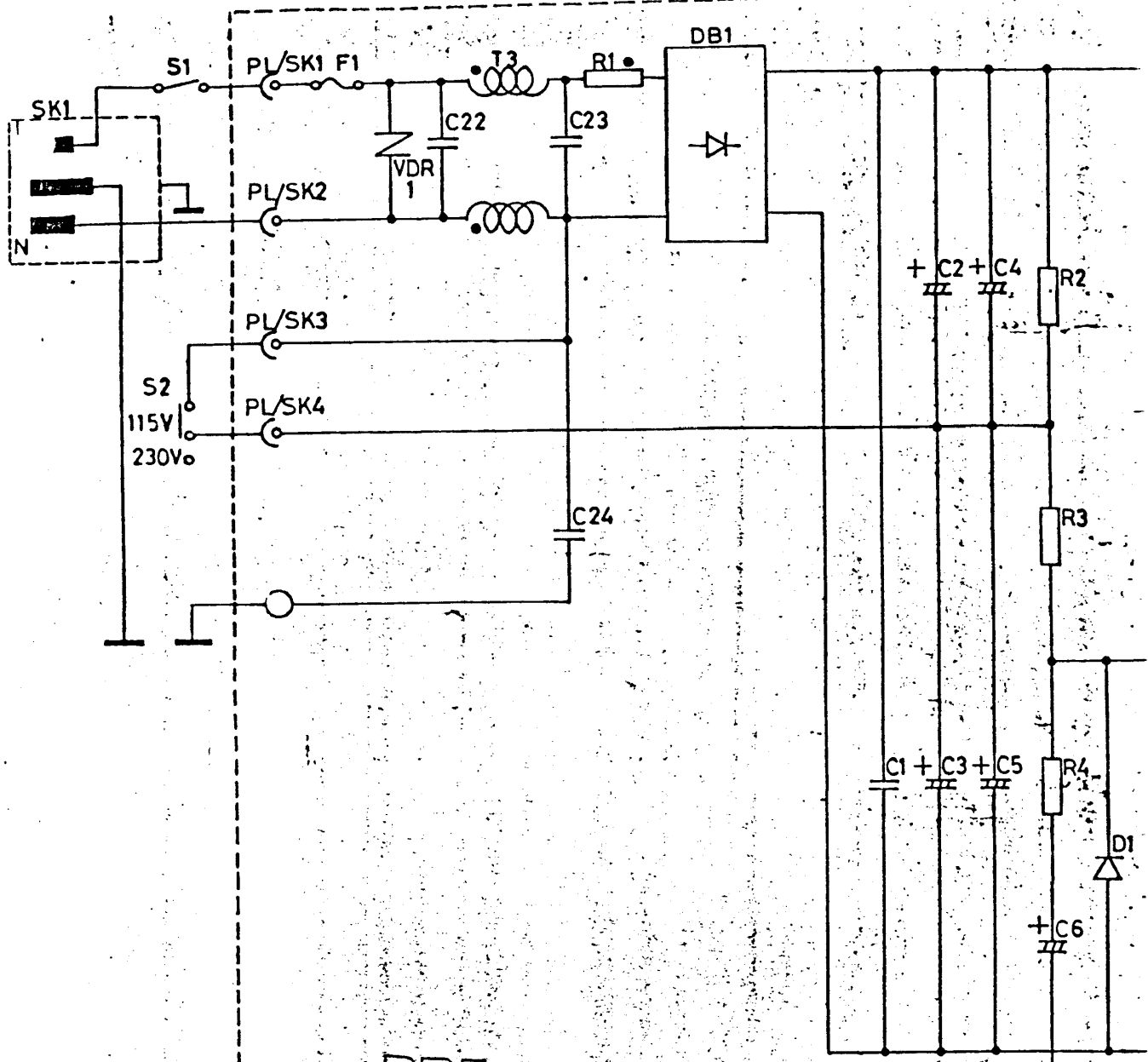


110 volt model



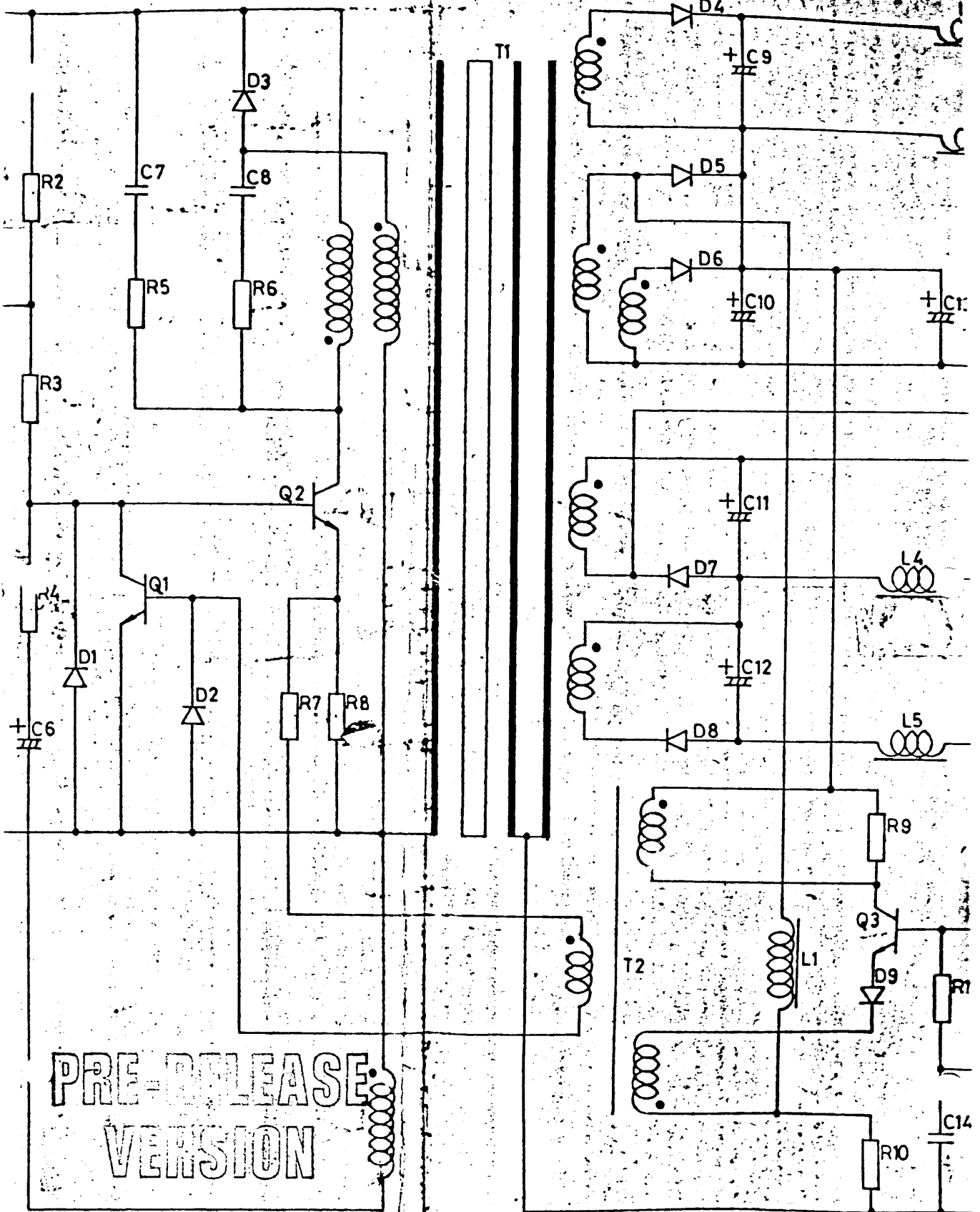
110/220 volt model

Photo 2. The back of the Apple Power Supply.

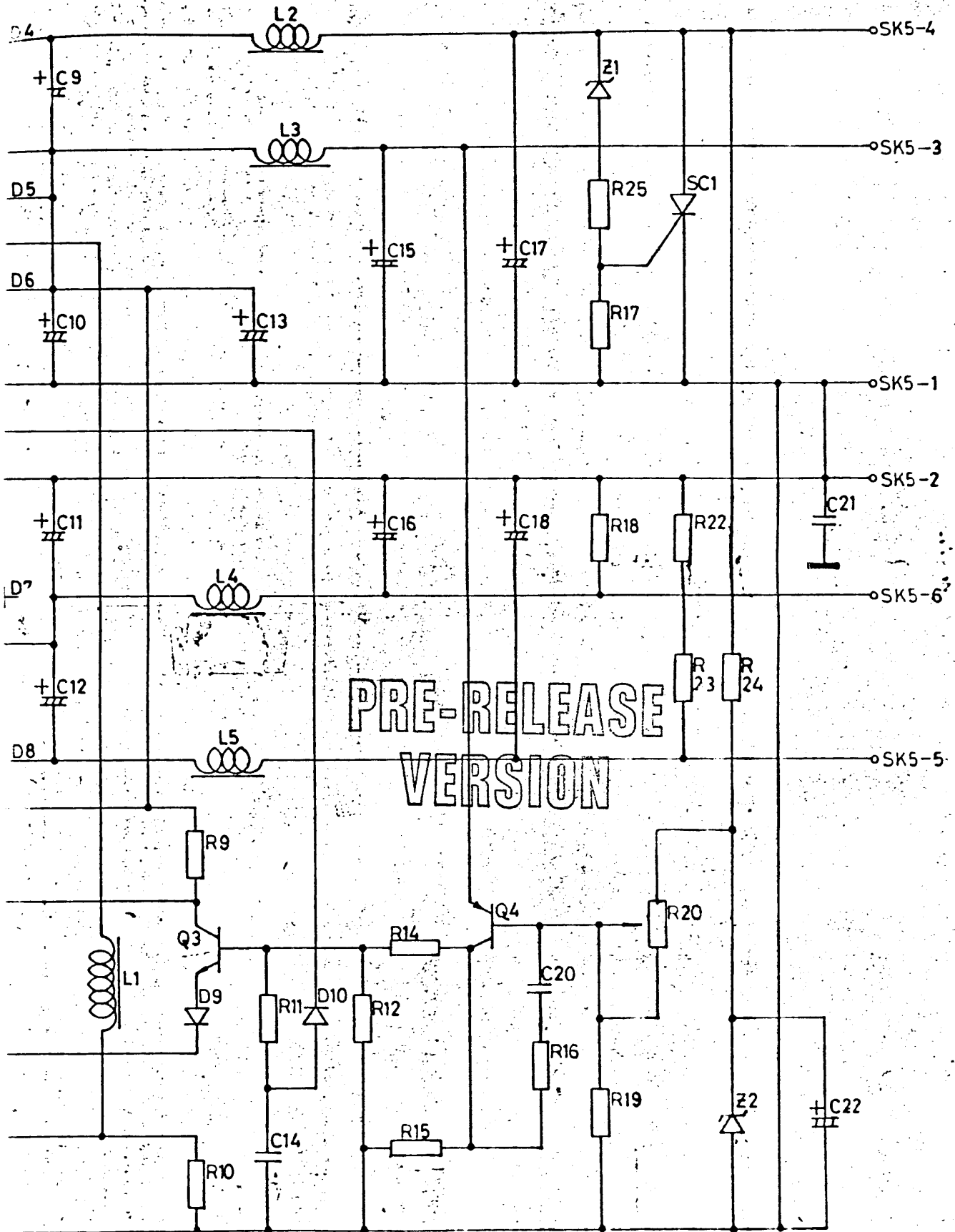


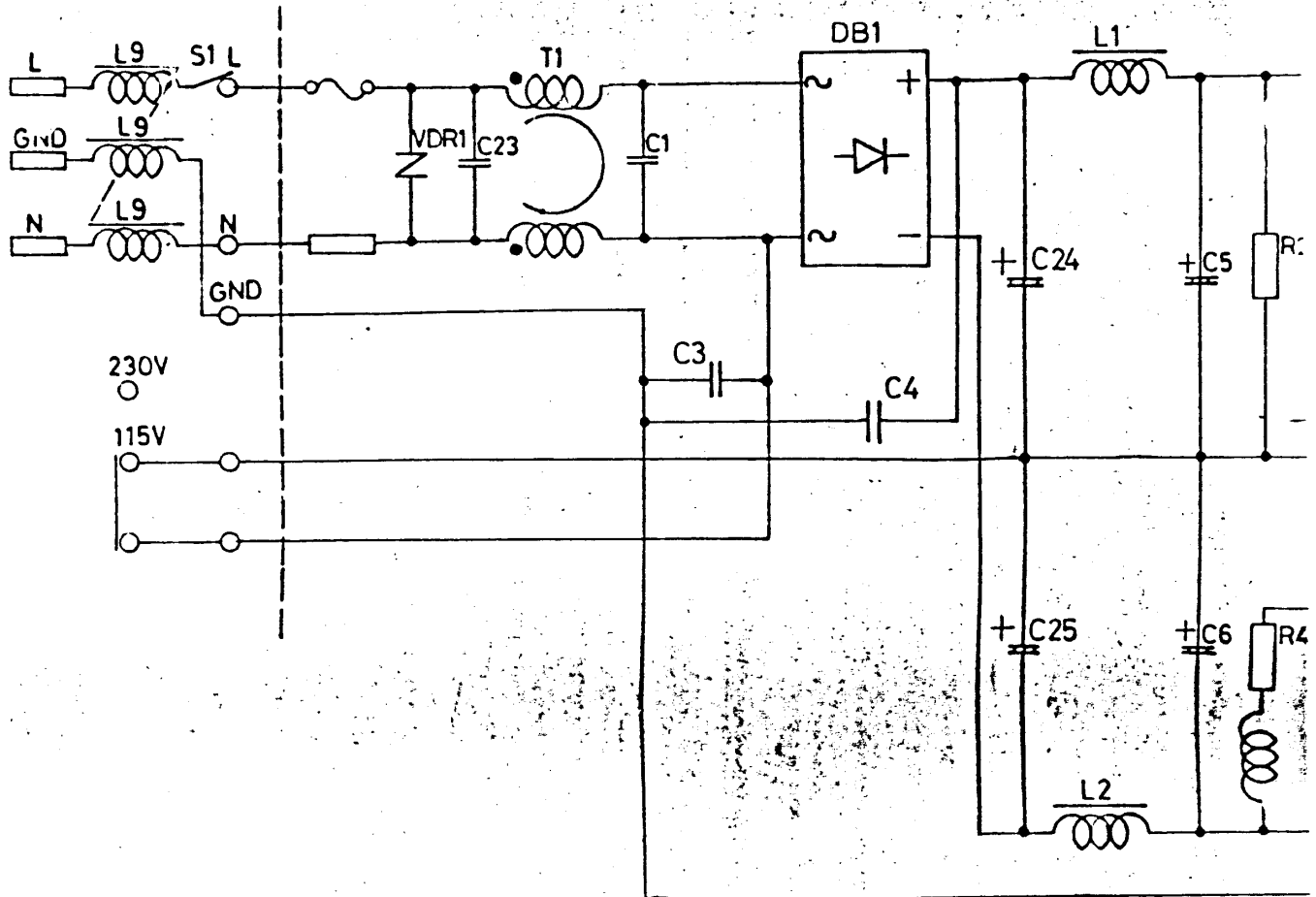
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ASTEC Power Supply  
Model AA11040



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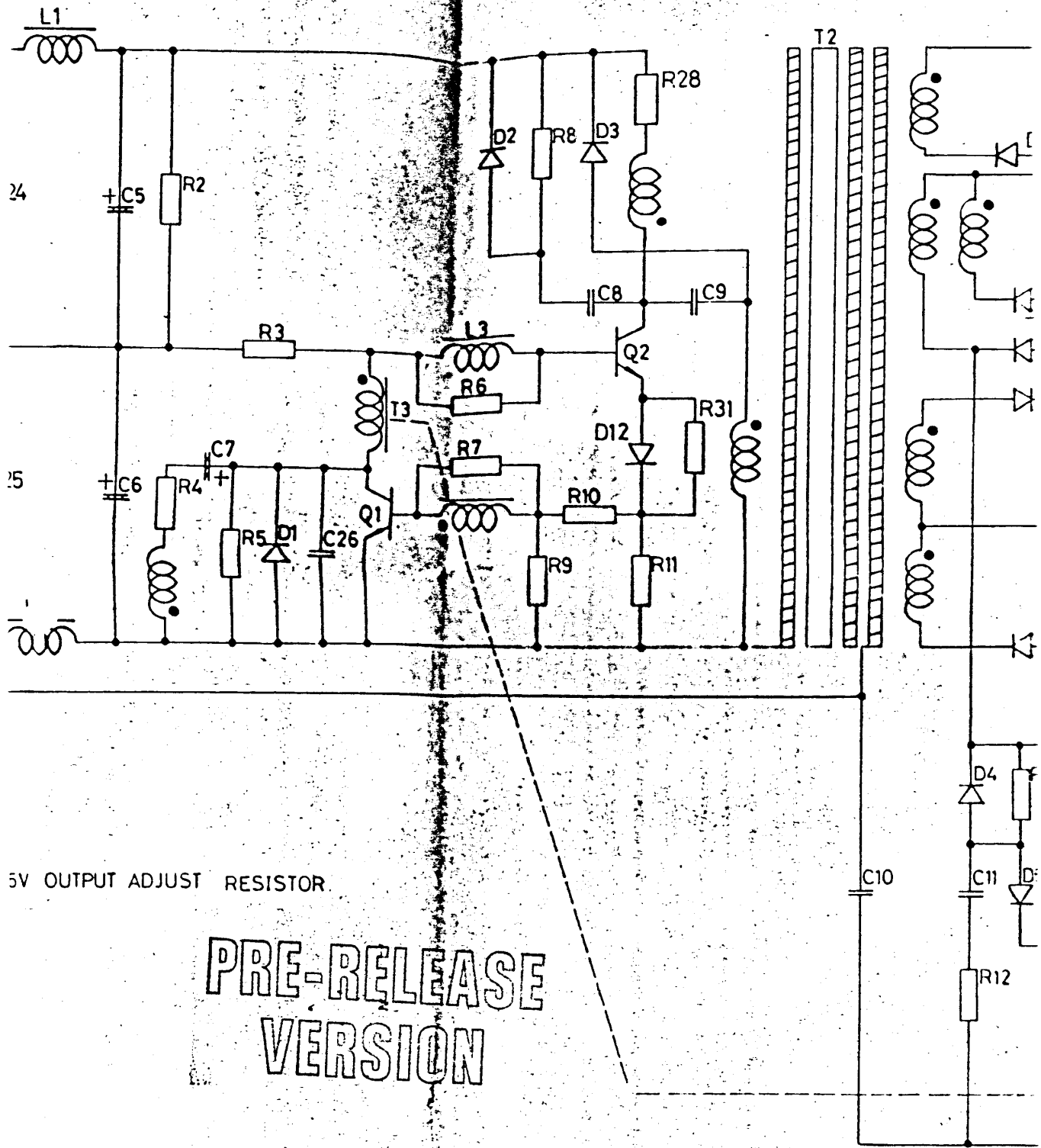


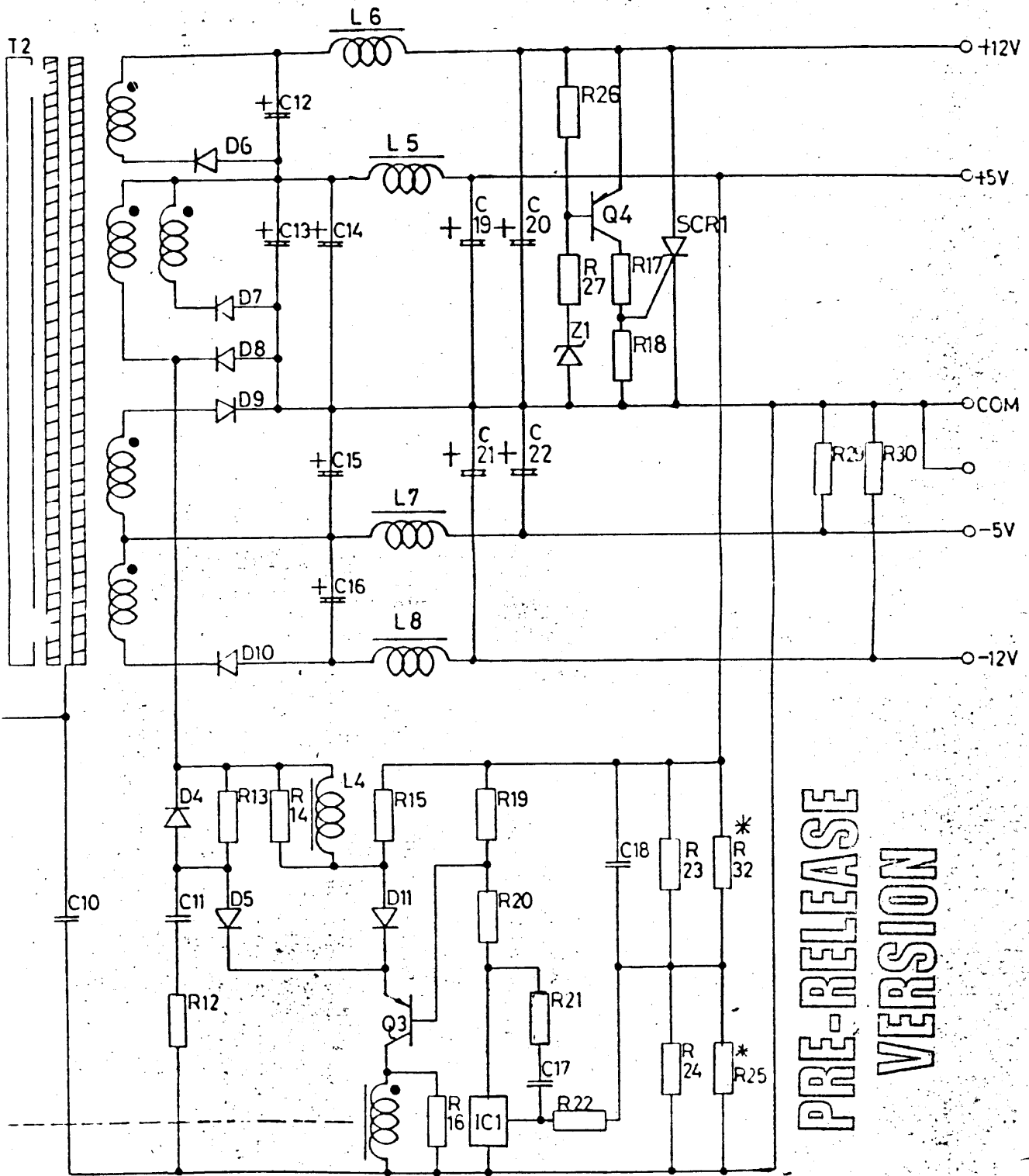


\* R32 AND \* R25 +5V OUTPUT ADJUST

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*Astec Power Supply  
Model AA11040B*





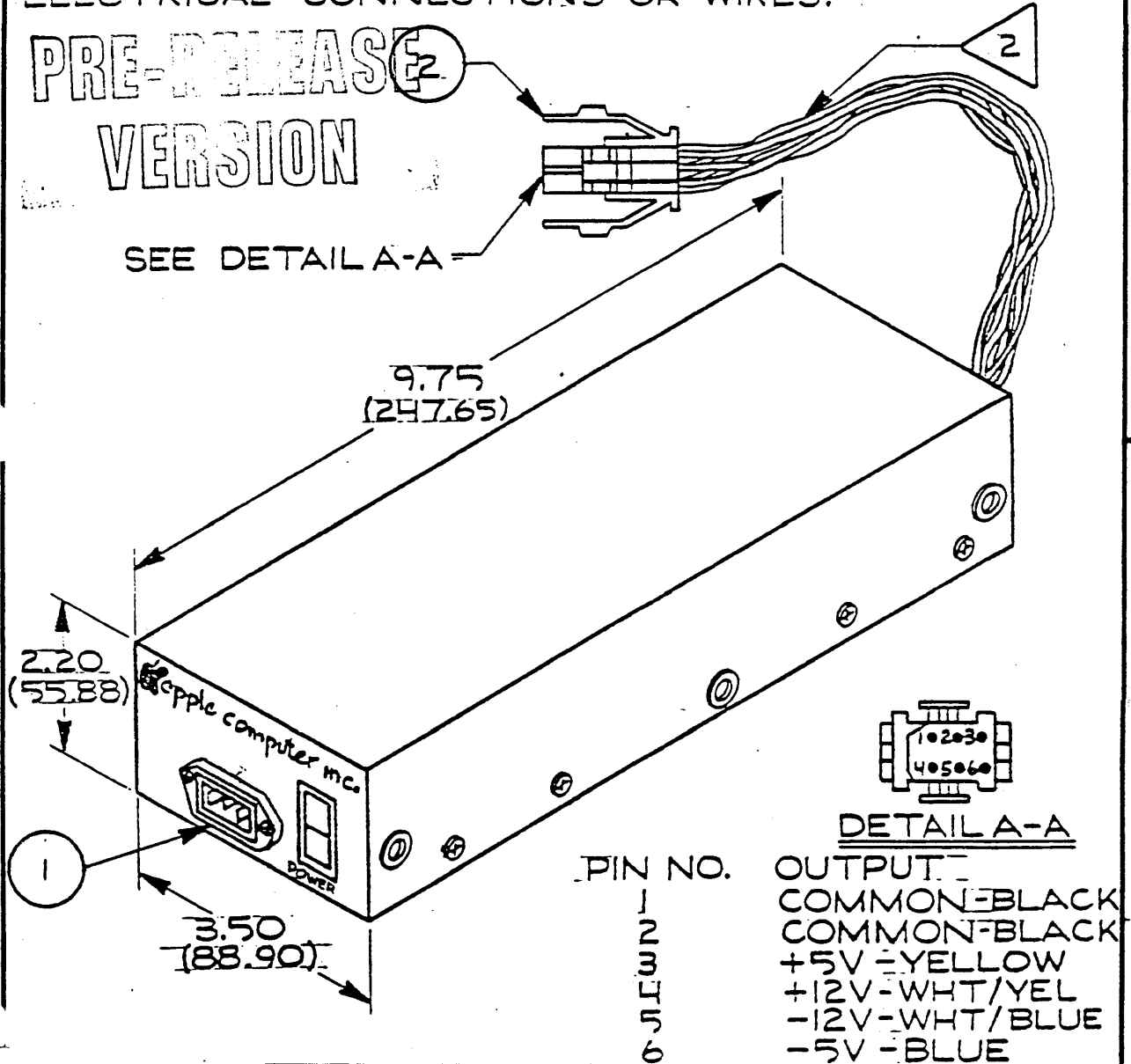
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NOTES: UNLESS OTHERWISE SPECIFIED.

1. POWER CONNECTOR: (1) PRIMARY-3 PRONG INTERNATIONAL STANDARD POWER CORD RECEPTACLE
- 2) SECONDARY: AMP P/N 1-350241-9 (HOUSING) & 350665-1. (PIN)
2. CABLE ASSY. FROM EXIT POINT TO END OF CONNECTOR SHALL BE 12" ± .5" (304.8 ± 12.7)
3. CABLE SHALL BE ABLE TO WITHSTAND 10 LBS. OF FORCE IN ANY DIRECTION WITHOUT DAMAGE TO ELECTRICAL CONNECTIONS OR WIRES.

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SEE DETAIL A-A

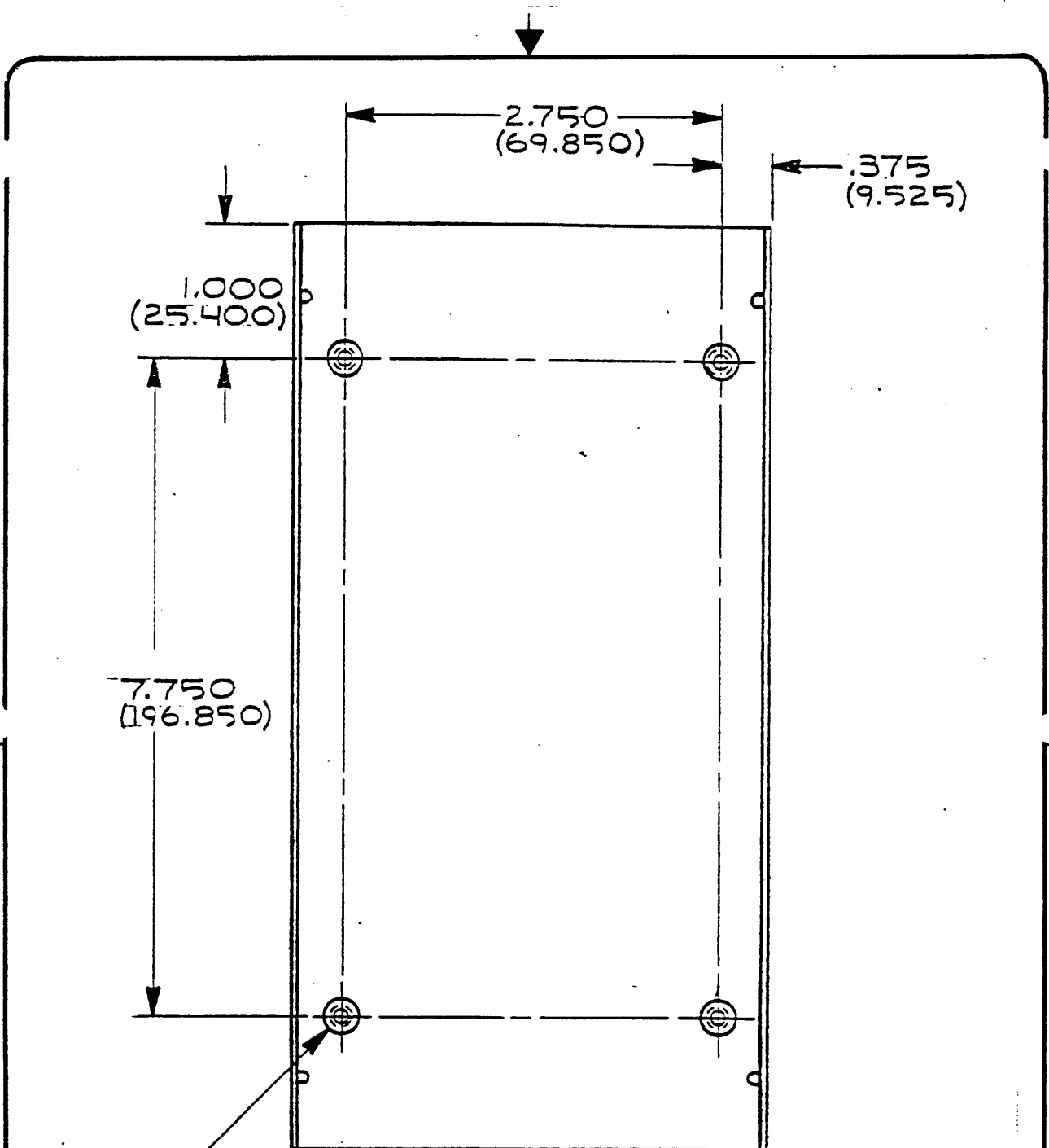


apple computer inc.

SIZE A DRAWING NUMBER 699-0049-A

SCALE: NONE


SHEET 10 OF 11



#4-40 PEM NUT  
4 PLCS

NOTE: ALL DIMENSIONS ±.010 (±.254)

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 <b>apple computer inc.</b>	SIZE A	DRAWING NUMBER 699-0049-A
	SCALE: NONE	SHEET 11 OF 11

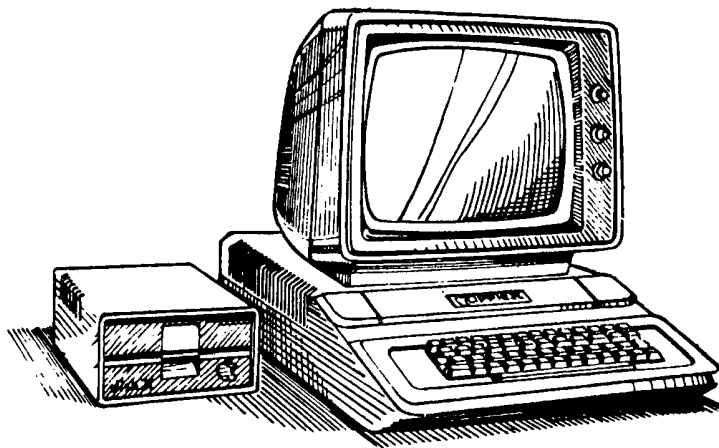


## Apple II Computer Technical Information

# APPLE II / APPLE II-PLUS LEVEL II SERVICE REFERENCE MANUAL

Pre-Release Version

## CHAPTER 5 CONNECTORS



Written by  
Apple Computer, Inc. • Level II Service Center  
1981

( This page is not part of the original service manual )

PERIPHERAL CONNECTORS

Along the back of the Apple's main board is a row of eight long "slots", or Peripheral Connectors. Into seven of these eight slots, you can plug any of many Peripheral Interface boards designed especially for the Apple. In order to make the peripheral cards simpler and more versatile, the Apple's circuitry has allocated a total of 280 byte locations in the memory map for each of the seven slots. There is also a 2K byte "common area", which all peripheral cards in your Apple can share.

Each slot on the board is individually numbered, with the leftmost slot called "Slot 0" and the rightmost called "Slot 7". Slot 0 is special it is meant for RAM, ROM, or Interface expansion. All other slots (1 through 7) have special control lines going to them which are active at different times for different slots.

The pin out for these connectors is given in Figure 21, and the signal descriptions are given in Table 33.

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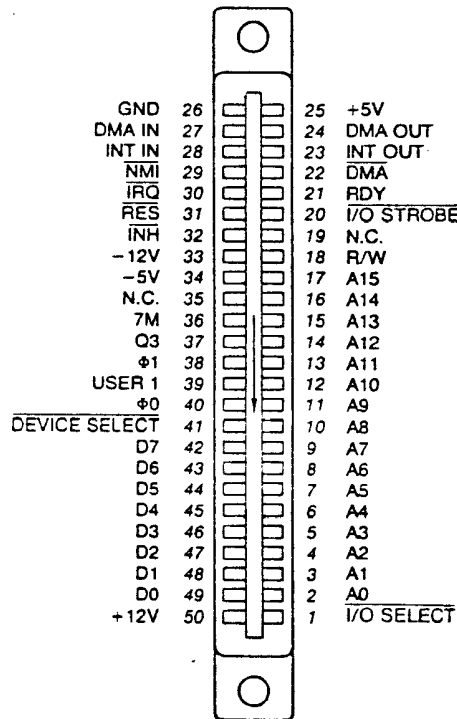


Figure 21. Peripheral Connector Pinout

**Table 33: Peripheral Connector Signal Description**

Pin:	Name:	Description:
1	I/O SELECT	This line, normally high, will become low when the microprocessor references page $5Cn$ , where $n$ is the individual slot number. This signal becomes active during $\Phi 0$ and will drive 10 LSTTL loads*. This signal is not present on peripheral connector 0.
2-17	A0-A15	The buffered address bus. The address on these lines becomes valid during $\Phi 1$ and remains valid through $\Phi 0$ . These lines will each drive 5 LSTTL loads*.
18	R/W	Buffered Read/Write signal. This becomes valid at the same time the address bus does, and goes high during a read cycle and low during a write. This line can drive up to 2 LSTTL loads*.
19	SYNC	On peripheral connector 7 <i>only</i> , this pin is connected to the video timing generator's SYNC signal. <i>IN IS FOR INTERNATIONAL AFFAIRS ONLY</i>
20	I/O STROBE	This line goes low during $\Phi 0$ when the address bus contains an address between $5C800$ and $5CFFF$ . This line will drive 4 LSTTL loads*.
21	RDY	The 6502's RDY input. Pulling this line low during $\Phi 1$ will halt the microprocessor, with the address bus holding the address of the current location being fetched.
22	DMA	Pulling this line low disables the 6502's address bus and halts the microprocessor. This line is held high by a $1K\Omega$ resistor to +5v.
23	INT OUT	Daisy-chained interrupt output to lower priority devices. This pin is usually connected to pin 28 (INT IN).
24	DMA OUT	Daisy-chained DMA output to lower priority devices. This pin is usually connected to pin 22 (DMA IN).
25	+5v	+5 volt power supply. 500mA current is available for <i>all</i> peripheral cards.
26	GND	System electrical ground.

\* Loading limits are for each peripheral card.

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Table 33 (cont'd): Peripheral Connector Signal Description		
Pin:	Name:	Description:
27	DMA IN	Daisy-chained DMA input from higher priority devices. Usually connected to pin 24 (DMA OUT).
<del>28</del> 28	INT IN	Daisy-chained interrupt input from higher priority devices. Usually connected to pin 23 (INT OUT).
29	$\overline{\text{NMI}}$	Non-Maskable Interrupt. When this line is pulled low the Apple begins an interrupt cycle and jumps to the interrupt handling routine at location \$3FB.
30	$\overline{\text{IRQ}}$	Interrupt ReQuest. When this line is pulled low the Apple begins an interrupt cycle only if the 6502's I (Interrupt disable) flag is not set. If so, the 6502 will jump to the interrupt handling subroutine whose address is stored in locations \$3FE and \$3FF.
31	$\overline{\text{RES}}$	When this line is pulled low the microprocessor begins a RESET cycle (see page 36).
32	$\overline{\text{INH}}$	When this line is pulled low, all ROMs on the Apple board are disabled. This line is held high by a $1\text{K}\Omega$ resistor to +5v.
33	-12v	-12 volt power supply. Maximum current is 200mA for all peripheral boards.
34	-5v	-5 volt power supply. Maximum current is 200mA for all peripheral boards.
35	COLOR REF	On peripheral connector 7 <i>only</i> , this pin is connected to the 3.5MHz COLOR REFERENCE signal of the video generator.
36	7M	7MHz clock. This line will drive 2 LSTTL loads*.
37	Q3	2MHz asymmetrical clock. This line will drive 2 LSTTL loads*.
38	$\Phi 1$	Microprocessor's phase one clock. This line will drive 2 LSTTL loads*.
39	USER 1	This line, when pulled low, disables <i>all</i> internal I/O address decoding**.

\* Loading limits are for each peripheral card.  
 \*\* See page 99.

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**Table 33 (cont'd): Peripheral Connector Signal Description**

Pin:	Name:	Description:
40	$\Phi 0$	Microprocessor's phase zero clock. This line will drive 2 LSTTL loads*.
41	<u>DEVICE SELECT</u>	This line becomes active (low) on each peripheral connector when the address bus is holding an address between $SC0n0$ and $SC0nF$ , where $n$ is the slot number plus $S8$ . This line will drive 10 LSTTL loads*.
42-49	D0-D7	Buffered bidirectional data bus. The data on this line becomes valid 300ns into $\Phi 0$ on a write cycle, and should be stable no less than 100ns before the end of $\Phi 0$ on a read cycle. Each data line can drive one LSTTL load.
50	+12v	+12 volt power supply. This can supply up to 250mA total for all peripheral cards.

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### SPEAKER CONNECTOR

The Apple's internal speaker is driven half of a 74LS74 flip-flop through a Darlington amplifier circuit. The speaker connector is a Molex KK100 series connector, with two square pins, .25 inch tall, on .10 inch centers.

The connector coming from the speaker is plugged into the socket labeled speaker between rows A and B on the rightmost section of the motherboard.

Pin:	Name:	Description:
1	SPKR	Speaker signal. This line will deliver about .5 watt into an 8 Ohm load.
2	+5v	+5 volt power supply.

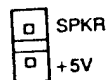


Figure 20. Speaker Connector

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KEYBOARD CONNECTOR

The data from the Apple's keyboard goes directly to the RAM data multiplexers and latches, the two 74LS257's at locations B6 and B7. The STROBE line on the keyboard connector sets a 74LS74 flip-flop at location B10. When the I/O selector activates its "0" line, the data which is on the seven inputs on the keyboard connector, and the state of the strobe flip-flop, are multiplexed onto the Apple's data bus. The keyboard connector plugs into the A-7 socket on the main logic board.

Table 30: Keyboard Connector Signal Descriptions

Pin:	Name:	Description:
1	+5v	+5 volt power supply. Total current drain on this pin must be less than 120mA.
2	STROBE	Strobe output from keyboard. This line should be given a pulse at least 10μs long each time a key is pressed on the keyboard. The strobe can be of either polarity.
3	RESET	Microprocessor's RESET line. Normally high, this line should be pulled low when the RESET button is pressed.
4,9,16	NC	No connection.
5-7, 10-13	Data	Seven bit ASCII keyboard data input.
8	Gnd	System electrical ground.
15	-12v	-12 volt power supply. Keyboard should draw less than 50mA.

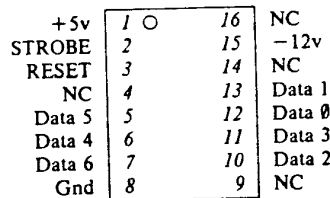
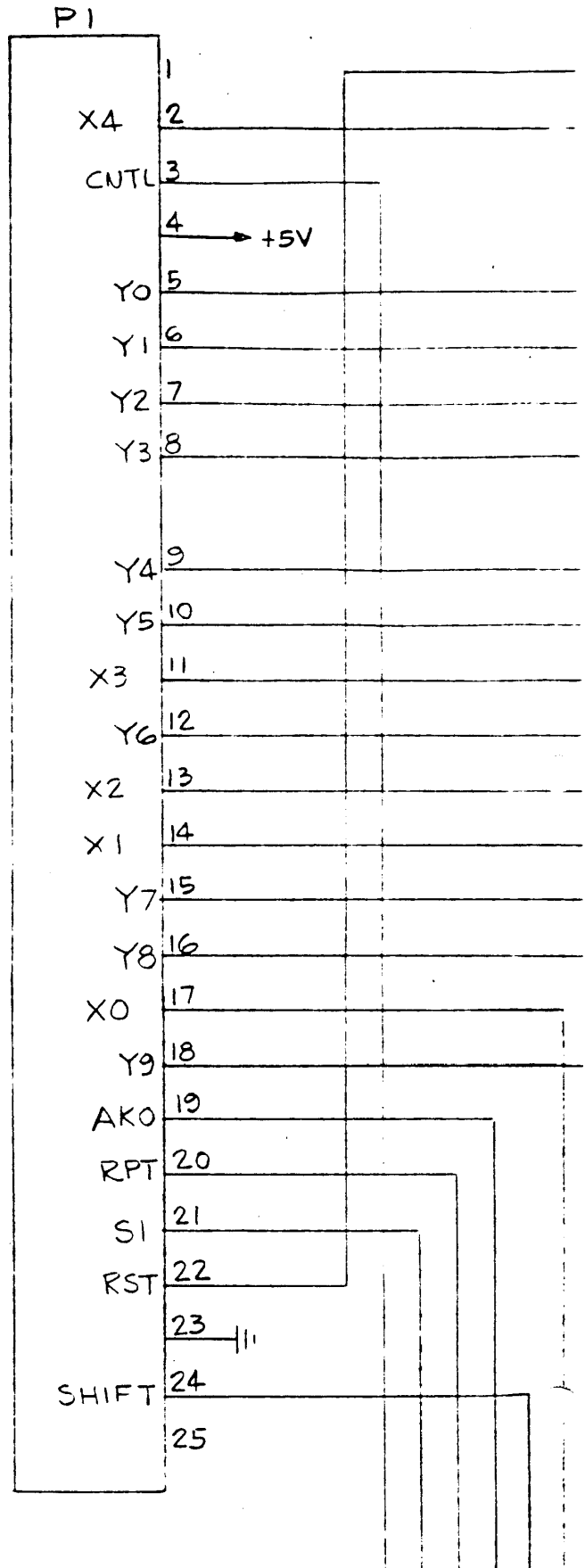


Figure 18.  
Keyboard Connector Pinouts

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# ENCODER BOARD CONNECTOR

## PRE-RELEASE VERSION



**POWER CONNECTOR**

This connector mates with the cable from the Apple power supply. This is an Amp #9-3028-1 six pin male connector. The connector leads from the power supply and plugs into the K-1 socket of the main logic board.

Table 31: Power Connector Pin Descriptions		
Pin:	Name:	Description:
1,2	Ground	Common electrical ground for Apple board.
3	+5v	+5.0 volts from power supply. An Apple with 48K of RAM and no peripherals draws ~1.5 amp from this supply.
4	+12v	+12.0 volts from power supply. An Apple with 48K of RAM and no peripherals draws ~400ma from this supply.
5	-12v	-12.0 volts from power supply. An Apple with 48K of RAM and no peripherals draws ~12.5ma from this supply.
6	-5v	-5.0 volts from power supply. An Apple with 48K of RAM and no peripherals draws ~0.0ma from this supply.

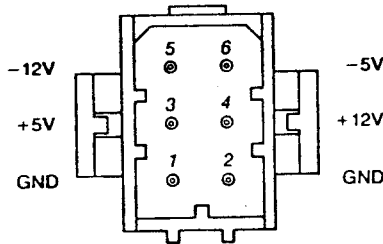


Figure 19. Power Connector

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### GAME I/O CONNECTOR

The purpose of the Game I/O Connector is to allow you to connect special input and output devices to heighten the effect of programs in general, and specifically, game programs. This connector allows you to connect three one-bit inputs, four one-bit outputs, a data strobe, and four analog inputs to the Apple, all of which can be controlled by your programs. Supplied with your Apple is a pair of Game Controllers which are connected to cables which plug into the Game I/O Connector. The two rotary dials on the controllers are connected to two analog inputs on the connector; the two pushbuttons are connected to two of the one-bit inputs.

+5v	1	16	NC
PB0	2	15	AN0
PB1	3	14	AN1
PB2	4	13	AN2
$\overline{C040}$ STROBE	5	12	AN3
GC0	6	11	GC3
GC2	7	10	GC1
Gnd	8	9	NC

Figure 16.  
Game I/O Connector Pinouts

Table 29: Game I/O Connector Signal Descriptions		
Pin:	Name:	Description:
1	+5v	+5 volt power supply. Total current drain on this pin must be less than 100mA.
2-4	PB0-PB2	Single-bit (Pushbutton) inputs. These are standard 74LS series TTL inputs.
5	$\overline{C040}$ STROBE	A general-purpose strobe. This line, normally high, goes low during $\Phi 0$ of a read or write cycle to any address from SC040 through SC04F. This is a standard 74LS TTL output.
6,7,10,11	GC0-GC3	Game controller inputs. These should each be connected through a 150K Ohm variable resistor to +5v.
8	Gnd	System electrical ground.
12-15	AN0-AN3	Annunciator outputs. These are standard 74LS series TTL outputs and must be buffered if used to drive other than TTL inputs.
9,16	NC	No internal connection.

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### CASSETTE INTERFACE JACKS

The two female miniature phone jacks on the back of the Apple II can connect your Apple to a normal home cassette tape recorder.

#### Cassette Input Jack:

This jack designed to be connected to the "Earphone" or "Monitor" output jacks on most tape recorders. The input voltage should be 1 volt peak to peak (nominal). The input impedance is 12K ohms.

#### Cassette Output Jack:

This jack is designed to be connected to the "Microphone" input on most tape recorders. The output voltage is 25mv into a 100 Ohm impedance load.

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### VIDEO OUTPUT

#### RCA Jack:

On the back of the Apple board, near the right edge is a standard RCA phono jack. The sleeve on this jack is connected to the Apple's common ground and the tip is connected to the video output signal through a 200 ohm potentiometer. This potentiometer can adjust the voltage on this connector from 0 to 1 volt peak.

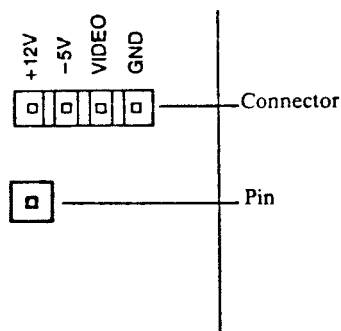
#### Auxiliary Video Connector:

On the right side of the Apple board near the back is a Molex KK100 series connector with four square pins, .25 inch on .10 inch centers. This connector supplies the composite video output and two power supply voltages. This connector is illustrated in figure 15 with a signal description in Table 28.

#### Auxiliary Video Pin:

This single metal wire-wrap pin below the Auxiliary Video Output Connector supplies the same video signal available on that connector. It is meant to be a connection point for Eurapple PAL/SECAM encoder boards.

Pin	Name	Description
1	GROUND	System common ground; 0 volts.
2	VIDEO	NTSC compatible positive composite video. Black level is about .75 volt, white level about 2.0 volt, sync tip level is 0 volts. Output level is not adjustable. This is not protected against short circuits.
3	+12v	+12 volt power supply.
4	-5v	-5 volt line from power supply.



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Figure 15. Auxiliary Video Output Connector and Pin.

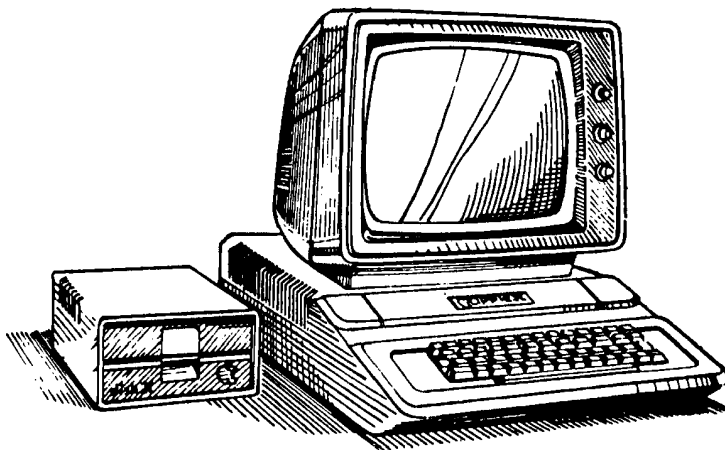


## Apple II Computer Technical Information

# APPLE II / APPLE II-PLUS LEVEL II SERVICE REFERENCE MANUAL

**Pre-Release Version**

## CHAPTER 6 OTHER INPUT / OUTPUT FEATURES



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1981**

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### "USER 1" JUMPER

There is an unlabeled pair of solder pads on the Apple board, to the left of slot 0, called the "User 1" jumper. This jumper is illustrated in Photo 8. If you connect a wire between these two pads, then the USER 1 line on each peripheral connector becomes active. If any peripheral card pulls this line low, all internal I/O decoding is disabled. The I/O SELECT and the DEVICE SELECT lines all go high and will remain high while USER 1 is low, regardless of the address on the address bus.

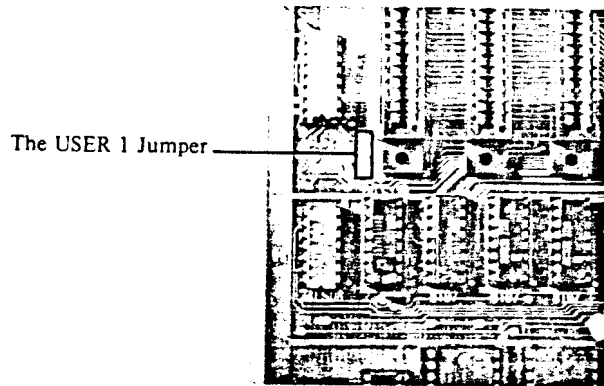


Photo 8. The USER 1 Jumper.

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## OTHER INPUT/OUTPUT FEATURES

Input:   Cassette Input  
          Three One-bit Digital Inputs  
          Four Analog Inputs  
OUTPUT:  Cassette Output  
          Built-In Speaker  
          Four "Annunciator" Outputs  
          Utility Strobe Output

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### The Cassette Interface

On the back edge of the Apple's main board, on the right side next to the VIDEO connector, are two small black packages labelled "IN" and "OUT". These are miniature phone jacks into which you can plug a cable which has a pair of miniature phono plugs on each end. The other end of this cable can be connected to a standard cassette tape recorder so that your Apple can save information on audio cassette tape and read it back again.

The connector marked "OUT" is wired to yet another soft switch on the Apple board. This is another toggle switch, like the speaker switch. The soft switch for the cassette out-put plug can be toggled by referencing memory location number 49184 (or the equivalent-16352 or hexadecimal \$C020). Referencing this location will make the voltage on the OUT connector swing from zero to 25 millivolts (one fortieth of a volt), or return from 25 millivolts back to zero. If the other end of the cable is plugged into the MICROPHONE input of a cassette tape recorder which is recording into a tape, this will produce a tiny "click" on the recording. By referencing the memory location associated with the cassette output soft switch repeatedly and frequently, a program can produce a tone on the recording. By varying the pitch and duration of this tone, information may be encoded on a tape and saved for later use.

Be forewarned that if you attempt to flip the soft switch for the cassette output by writing to its special location, you will actually generate two "clicks" on the recording. The reason for this is mentioned in the description of the speaker. You should only use "read" operations when toggling the cassette output soft switch.

The other connector, marked "IN", can be used to "listen" to a cassette tape recording. Its main purpose is to provide a means of listening to tones on the tape, decoding them into data, and storing them in memory. Thus, a program or data set which was stored on cassette tape may be read back in and used again.

The input circuit takes a 1 volt (peak-to-peak) signal from the cassette recorder's EARPHONE jack and converts it into a string of ones and zeroes. Each time the signal applied to the input circuit swings from positive to negative, or vice-versa, the input circuit changes state: if it was sending ones, it will start sending zeroes, and vice versa. A program can inspect the state of the cassette input circuit by looking at memory location number 49248 or the equivalents-16288 or hexadecimal \$C060. If the value which is read from this location is greater than or equal to 128, then the state is a "one", if the value in the memory location is less than 128, then the state

is a "zero". Although BASIC programs can read the state of the cassette input circuit, the speed of a BASIC program is usually much too slow to be able to make any sense out of what it reads. There is, however, a program in the System Monitor which will read the tones on a cassette tape and decode them.

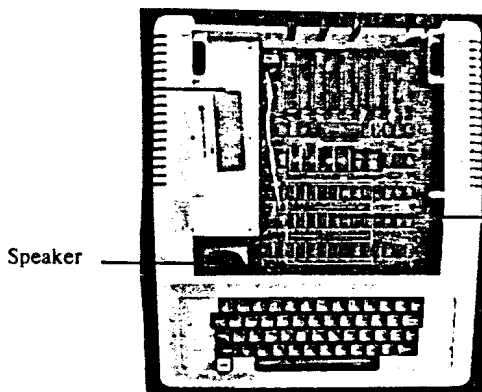
#### THE SPEAKER

Inside the Apple's case, on the left side under the keyboard, is a small 8 ohm speaker. It is connected to the internal electronics of the Apple so that a program can cause it to make various sounds.

The speaker is controlled by a soft switch. The switch can put the paper cone of the speaker in two positions: "in" and "out". This soft switch is not like the soft switches controlling the various video modes, but is instead a toggle switch. Each time a program references the memory address associated with the speaker switch, the speaker will change state: change from "in" to "out" or vice-versa. Each time the state is changed, the speaker produces a tiny "click". By referencing the address of the speaker switch frequently and continuously, a program can generate a steady tone from the speaker.

The soft switch for the speaker is associated with memory location number 49200. Any reference to this address (or the equivalent addresses-16336 or hexadecimal \$C030) will cause the speaker to emit a click.

A program can "reference" the address with memory location for the speaker by performing a "read" or "write" operation to that address. The data which are read or written are irrelevant, as it is the address which throws the switch. Note that a "write" operation on the Apple's 6502 microprocessor actually performs a "read" before the "write", so that if you use a "write" operation to flip and soft switch, you will actually throw that switch twice. For toggle-type soft switches, such as the speaker switch, this means that a "write" operation to the special location controlling the switch will leave the switch in the same state it was in before the operation was performed.



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### ANNUNCIATOR OUTPUTS

The four one-bit outputs are called "annunciators". Each annunciator output can be used as an input to some other electronic device, or the annunciator outputs can be connected to circuits to drive lamps, relays, speakers, etc.

Each annunciator is controlled by a soft switch. The addresses of the soft switches for the annunciators are arranged into four pairs, one pair for each annunciator. If you reference the second address in the pair, you turn the annunciator's output "on". When an annunciator is "off", the voltage on its pin on the Game I/O Connector is near 0 volts; when an annunciator is "on", the voltage is near 5 volts. There are no inherent means to determine the current setting of an annunciator bit. The annunciator soft switches are:

Table 9: Annunciator Special Locations				
Ann.	State	Address:		
		Decimal	Hex	
0	off	49240	-16296	SC058
	on	49241	-16295	SC059
1	off	49242	-16294	SC05A
	on	49243	-16293	SC05B
2	off	49244	-16292	SC05C
	on	49245	-16291	SC05D
3	off	49246	-16290	SC05E
	on	49247	-16289	SC05F

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### STROBE OUTPUT

There is an additional output, called C040 STROBE, which is normally +5 volts but will drop to zero volts for a duration of one-half microsecond under the control of a machine language or BASIC program. You can trigger this "strobe" by referring to location 49216 (-16320 or \$C040). Be aware that if you perform a "write" operation to this location, you will trigger the strobe twice.

### ONE-BIT INPUTS

The three one-bit inputs can each be connected to either another electronic device or to a pushbutton. You can read the state of any of the one-bit inputs from a machine language or BASIC program on the same manner as you read the Cassette input, above, the locations for the three one-bit inputs have the addresses 49249 through 49251 (-16287 through -16285 or hexadecimal \$C061 through \$C063).

### ANALOG INPUTS

The four analog inputs can be connected to 150k Ohm variable resistors or potentiometers. The variable resistance on an input varies, the timing characteristics of its corresponding timing circuit change accordingly. Machine language programs can sense the changes on the timing loops and obtain a numerical value corresponding to the position of the potentiometer.

Before a program can start to read the setting of a potentiometer, it must first reset the timing circuits. Location number 49264 (-16272 or

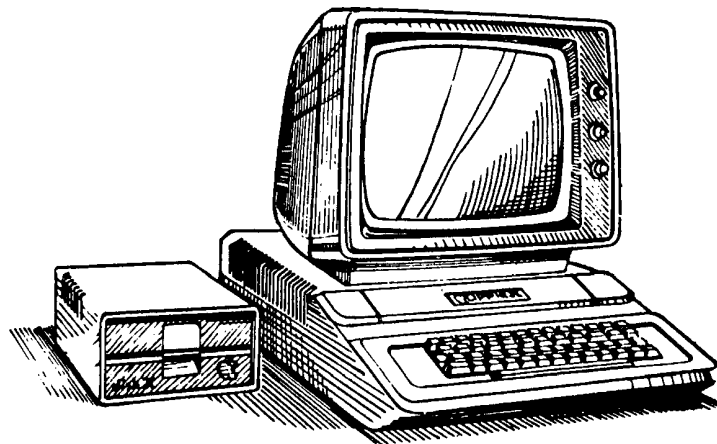


## Apple II Computer Technical Information

# APPLE II / APPLE II-PLUS LEVEL II SERVICE REFERENCE MANUAL

Pre-Release Version

## CHAPTER 7 MOTHERBOARD



Written by  
**Apple Computer, Inc. • Level II Service Center**  
**1981**

( This page is not part of the original service manual )

hexidecimal \$C070) does just this. When you reset the timing circuits, the values contained in the four locations 49252 through 49255 (-16284 through -16281 or \$C064 through \$C067) become greater than 128 (their high bits are set). Within 3,060 milliseconds, the values contained on these four locations should drop below 128. The exact time it takes for each location to drop in value is directly proportional to the setting of the game paddle associated with that location. If the potentiometers connected to the analog inputs have a greater resistance than 150k Ohms, or there are no potentiometers connected, then the values in the game controller locations may never drop to zero.

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## MAIN LOGIC BOARD

### THEORY OF OPERATION

The APPLE II's Main Logic Board represents the full range of integration from simple gates to highly dense microprocessor and memory chips. Much of the power of the APPLE II logic circuitry comes from the use of medium-scale (MSI) integrated circuits. These include multiplexers, shift registers, counters and decoders.

This Theory of Operation contains detailed descriptions of medium-scale ICs as they apply to the APPLE II design. It was written with the understanding that the reader has had exposure to simple gates and memory/microprocessor circuits. Since almost none of the APPLE II's use of medium-scale IC's is straightforward, each MSI package is described before detailing how it functions in the APPLE II. In cases where an MSI device is used in several sections of the circuit board, the functional description will be repeated. If you already know how a device functions you may want to pass over the device's functional description, and concentrate on how it fits into the APPLE II design.

This material is especially intended for the Service Technician, but it should also be helpful to individuals who need to interface hardware to the APPLE II.

There are three sections to this chapter:

1. The written part, which breaks the Main Logic Board into 11 sections verbally guides you through the APPLE II logic within each section, with appropriate overlapping between sections.
2. A block diagram and ten schematic drawings (Figures S1 - S11) which show the APPLE II logic circuits within each section.
3. A System Timing Diagram which graphically shows the timing signals within the Main Logic Board and includes a state diagram of the Sync Counters.

The goal of this chapter is to allow you to understand how the APPLE II works, using the schematics to refresh your memory when necessary. The written part is intended to help you through the schematics, and should be read WITH the schematics and System Timing Diagram.

As a practical note, the Service Technician will want to be able to get around on the Main Logic Board using a scope. It is suggested that an "open APPLE II" be created using a logic board, keyboard, power supply and monitor. As signals are described they can be observed as well, thus speeding up learning.

Effort has been made to keep each section complete unto itself at the risk of making this part of the manual redundant at times. This will allow you to read the sections in any order you want to. Please read SECTION 1: OVERVIEW first to get a general flavor.

One great asset to the the Service Technician is a working knowledge of the software contained in the APPLE II's F8 Monitor and the various APPLE II "soft switch" commands. The F8 Monitor is well documented in Chapter 9 and the

soft switches in Chapter 2.

Lastly, a few details:

ICs are identified on the Main Logic Board using an X-Y coordinate system. The X coordinate ranges from 1 to 14 with position 1 on the far left and position 14 on the far right as you face the keyboard. The Y coordinate ranges alphabetically from A (bottom row) to K (top row) as you face the keyboard. IC "B2", for example, locates the 74S86 in the second row and column from the lower left edge of the Main Logic Board. Pin numbers are indicated with a dash following the IC location. "B2-8" therefore locates pin 8 of the 74LS86 at B2.

Three types of TTL (Transistor-Transistor Logic) are used in the APPLE II. They are:

Standard TTL (example: "74166")... These parts are used only occasionally in the APPLE II and are electrically similar to Fairchild's 9000 series. APPLE part numbers of each type are prefixed with "301" so that the part number for "74166" becomes "301-0166", and the part number for "9334" becomes "301-9334".

Low-power Schottky TTL (example: "74LS195")... These ICs combine fast switching times with power needs similar to standard TTL. These chips are used in the high frequency System Timing section of APPLE II. The corresponding APPLE part numbers begin with "307" so that "74S195" becomes "307-0195".

ICs of the above types will be described once in each section using the full part name, and then will be abbreviated as follows:

"74175" becomes "175"

"74LS138" becomes "138"

"74166" becomes "166"

Signals which are active low are indicated with a single quote (') following the signal's mnemonic as in RAS (Row Address Strobe).

Numbers in base 16 (hexadecimal) are preceded with a "\$".

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## OVERVIEW

### SECTION 1

The Main Logic Board is one of a family of modules which make up the APPLE II product line. It is one of three "essential" modules which comprise a minimum APPLE II system. These essential modules are:

1. MAIN LOGIC BOARD. This is the large printed-circuit board which takes up most of the space inside the APPLE II's case. It is an integrated single board computer and video display terminal. With it we can display text or graphics through an external monitor, or using an inexpensive modulator, through an ordinary television set.
2. POWER SUPPLY. This square metal box sits on the upper left-hand corner as you face the keyboard. It supplies all the power requirements needed by the APPLE II.
3. KEYBOARD. The keyboard sends parallel ASCII characters to the Main Logic Board and allows programs or data to be manually entered.

In addition to these essential modules, peripheral devices may be connected to the APPLE II by installing printed-circuit cards into one of the eight connectors at the back of the Main Logic Board. These include disc drives, printers, etc. Circuits within the Main Logic Board allow control signals to be sent to each peripheral card under program control.

The Main Logic Board is the nucleus of the APPLE II computer. Figure S-1 is a Block Diagram of the logic board divided into 11 sections. Each section will be described briefly in this chapter.

The APPLE II Main Logic Board is both a computer and video display device; Random-Access Memory (RAM) is commonly shared by both. The computer end is controlled by a Synertek-MOS Technology 6502 microprocessor which generates 16-bit Addresses (via the System Address Bus) and one system control output, the R/W (Read-Write) line. The Address generated by the 6502 points to a memory or I/O (input-output) location, and the R/W line controls the direction of data over an eight-bit Data Bus. Some of the data flowing into the 6502 contains instructions, called opcodes, which direct the microprocessor to perform certain tasks.

The video circuits also generate an address to memory. All of the accesses to memory by the video circuits are memory reads which cause a byte of data to be sent to the Video Generator adds sync pulses and a color burst signal to the video data to produce composite video, available from an RCA jack behind the computer.

Making all of this possible are the System Timing circuits which coordinate the timing events of both the microprocessor and the video circuits.

Here's a quick guide to the topic of each remaining sections. The appropriate schematic will be the same as the section's number. For Section 4 (Sync Counters) for example, the appropriate schematic would be Figure S-4.

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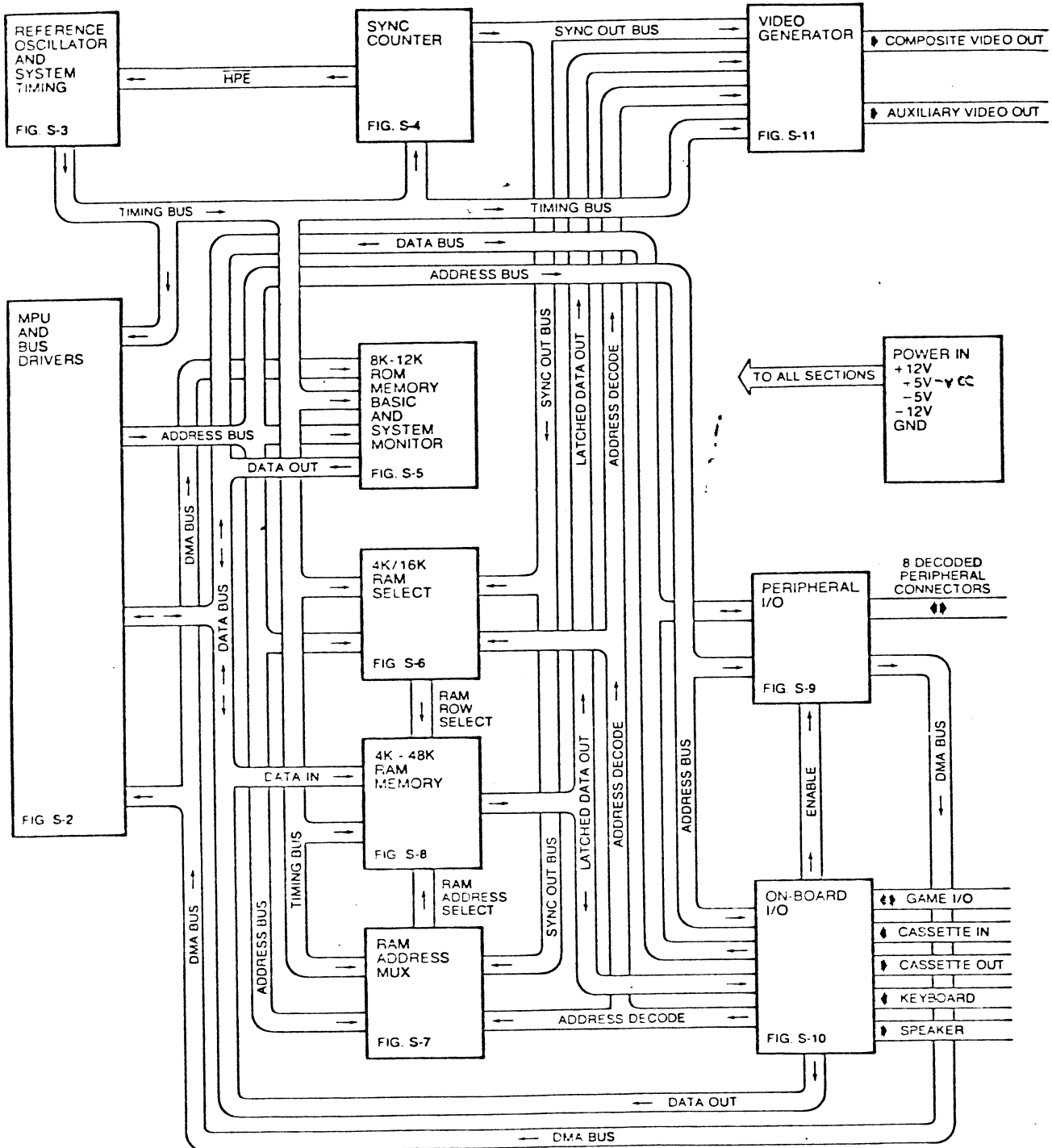


FIGURE S-1 APPLE II SYSTEM DIAGRAM

SECTION 2: MPU and System Bus. Signals to and from the 6502 microprocessor are isolated from the System Busses by bus drivers. These chips also create Direct Memory Access (DMA) capability. System Timing signal "PHASE ZERO" drives the microprocessor's clock input.

Section 3: Reference Oscillator and System Timing. Here a variety of timing signals are created.

One Mhz signals PHASE ZERO and PHASE ONE are used to select alternately between the microprocessor and the video bus cycles (memory accesses). These signals also enable circuits such as Peripheral I/O which use the System (buffered 6502) Busses. LDPS<sup>~</sup> advances the Sync Counters at one Mhz. LD194 controls when the Video Generator's graphics circuits load a new byte of data.

Two Mhz signals RAS<sup>~</sup> (Row Address Strobe) are timing signals to the APPLE II's dynamic RAM which receives an address in two steps (multiplexed). AX<sup>~</sup> controls when the RAM Address Mux circuits do the actual multiplexing. Q3 is available for general use.

Other System Timing signals include the 3.58 Mhz COLOR REF signal, 7M and 14M. These signals are used by the Video Generator.

SECTION 4: Sync Counters. Clocked by the one Mhz LDPS<sup>~</sup> signal, these four binary counters generate six horizontal and eight vertical timing signals. In the horizontal direction, signals H0 through H5 go through 65 states (40 microseconds of "live" characters and 25 microseconds of blanking). In vertical direction, signals VA, VB, VC, and V0 - V4 go through 262 state (192 "live" and 70 blanking). In text mode, VA, VB, and VC select one of the eight vertical scan lines within each character. Signals V0 - V4 point to a row of characters out of 245 possible rows.

SECTION 5: ROM Memory. The Apple II stores some programs permanently in 2K byte Read-Only Memory (ROM) ICs. Six ROMs may reside in the Main Logic Board for a total of 12K bytes of storage. Several different ROM variations are currently being offered, but every stock APPLE II offers and F8 (machine-language) Monitor and a high-level BASIC language in ROM.

SECTION 6: RAM Select. Random-Access Memory (RAM) is stored in three rows of 16K-bit RAMs for a total of 48K bytes of on-board R/W<sup>~</sup> memory. A given byte-wide row of RAM is selected when it receives the CAS<sup>~</sup> signal. This Section describes how that happens and describes how RAM address line A6 is driven.

SECTION 7: RAM Address Mux. This describes the circuits which allow both microprocessor and video circuits to access memory, and describes the function of some circuits which modify the Sync Counter outputs to create a Video Address.

SECTION 8: RAM Memory. The RAMs and their data latches are described here.

SECTION 9: Peripheral I/O. The Main Logic Board offers expansion capability via eight plug-in connectors. Three control signals, Device Select (DEV SEL<sup>~</sup>), I/O Select (I/O SEL<sup>~</sup>) and I/O Strobe (I/O STRB<sup>~</sup>) appear at each

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connector and make control over the peripheral device possible.

SECTION 10: On-Board I/O. The Apple II offers on-board I/O (Input/Output) circuits which include the keyboard, video display and the built-in loudspeaker.

SECTION 11. Video Generator. The Apple II displays text characters and also operates in two graphics modes. This section describes how video data is created for each mode.

It will be helpful to have the System Timing Diagram and the appropriate detailed schematic alongside when tracing through the logic. The detailed schematics are of the REV 0 board and as such do not accurately show the current APPLE II circuitry in all cases.

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## MPU AND SYSTEM BUS

### SECTION 2

The 6502 microprocessor is the heart of the APPLE II computer. The 6502 is an eight bit parallel, single chip processor with a repertoire of 56 instructions. Signals coming in and out of the 6502 divide into three groups of related signals, or "busses".

#### 1. ADDRESS BUS (A0 - A15)

These 16 lines point to  $2^{16}$ , or 65,536 unique locations in memory. The address lines coming from the 6502 cannot be placed into a high impedance or "floating" conditions. Also, they lack the drive capability to power both the on-board chips and peripheral cards which make use of them. 8T97 tristate buffers are then used to connect the 6502's address lines A0 - A15 to the System Address Bus. The Address Bus, as presented by the 6502, is valid about 200ns before the rising edge of the PHASE ZERO clock and is valid until after the PHASE ZERO clock falls. When PHASE ZERO is high, or its inverse, PHASE ONE, is low, a valid address is present on the Address Bus. For this reason, PHASE ZERO is used as a high-going enable, and PHASE ONE as a low going enable to ICs which use the System Address lines as inputs. These ICs include the motherboard 138s which are decoders for ROM and I/O space, and various chips on the peripheral cards.

The DMA' signal, normally pulled high through an on-board 1K ohm resistor, drives inverter input C11-13. If a peripheral device pulls this signal low, it causes the 8T97s to become high impedance, which released the Address Bus to the peripheral device.

#### 2. DATA BUS (D0 - D7)

The Data Bus allows eight bits of data to be transferred to or from the 6502. When the 6502 performs a READ operations, data flows from the DATA Bus into the 6502. When a WRITE operation occurs, data passes from the 6502 onto the Data Bus.

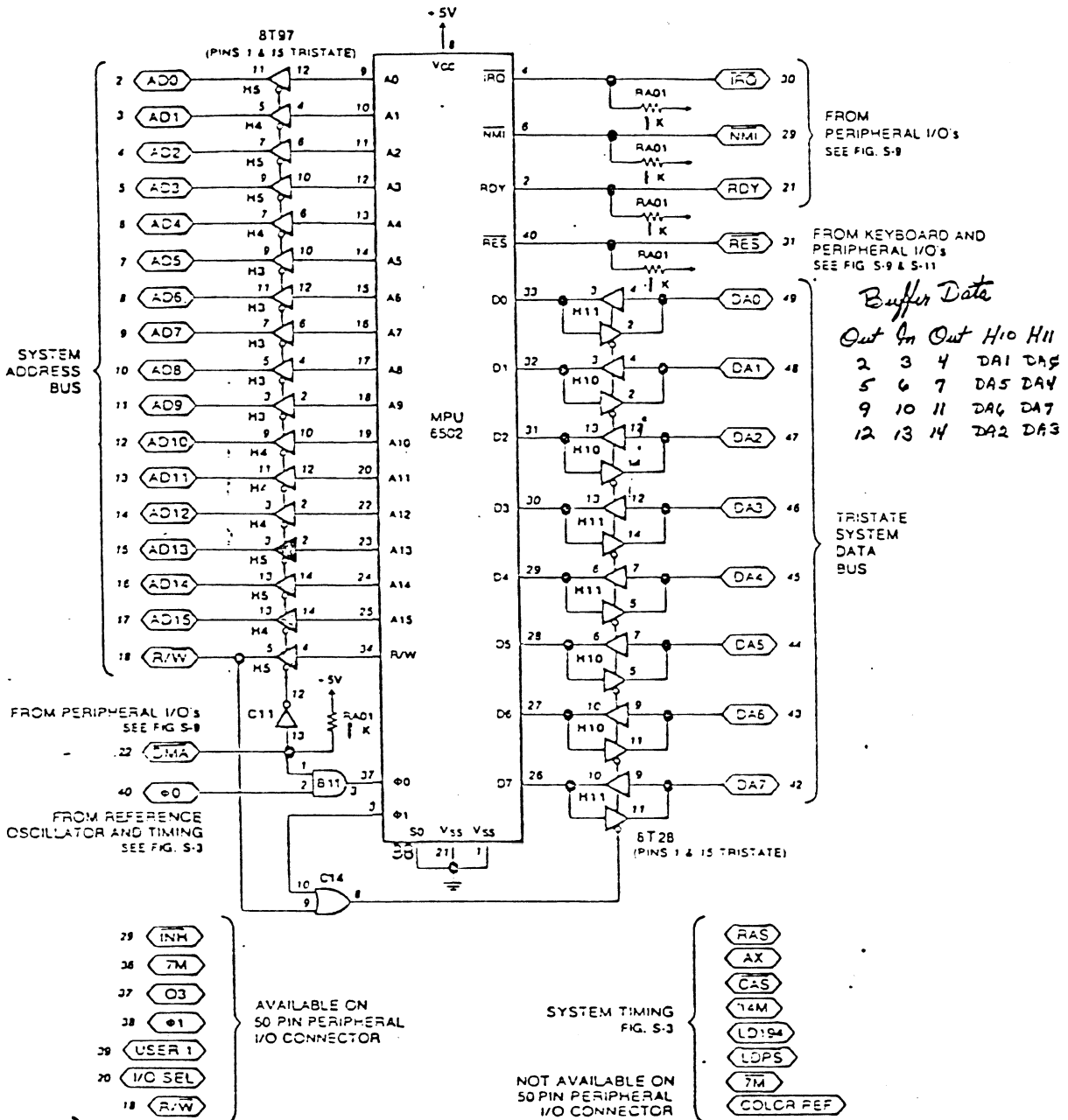
As in the case of the address lines, the 6502 data lines are also buffered - this time with 8T28 bus transceivers. Pins 1 and 15 of each 8T28 are tied together, and form a receive / transmit input. Driving this input is C14-8. This signal goes low only when R/W' and the 6502's internal PHASE ONE goes low. Data from the 6502 will then be gated onto the System Data Bus. The 6502's PHASE ONE is used instead of the PHASE ONE from System Timing because the flow of data across the Data Bus must closely follow the 6502's internal timing. The 6502's PHASE ONE clock is produced when it inverts the PHASE ZERO signal, as provided by B11-3, and lags the System Timing PHASE ONE by a few nanoseconds.

During a READ cycles, data to the 6502 must be valid at least 100ns prior to the falling edge of PHASE ZERO.

During a WRITE cycle, data from the 6502 is valid roughly 200ns before the falling edge of PHASE ZERO.

8T28 3-state quad Bus Transceiver  
 8T97 high speed hex 3-state inverters

Read cycle - valid at least 100ns prior to falling edge of phase 0 (Data to 6502)  
 Write cycle - valid ~ 200ns before falling edge of phase 0 (Data from 6502)



R/W (H5-5):  
 C14-9, C14-13  
 A2-4, I/O-18

FIGURE S-2 MPU AND SYSTEM BUS

Valid address on bus is indicated by Phase 0 high & Phase 1 low

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### 3. CONTROL BUS

This bus comprises six signals:

RES', NMI', IRQ', RDY, which connect directly to the processor.

R/W', which is buffered by one of the 8T97 gates.

DMA', which is implemented in hardware surrounding the 6502.

The RES' line is a "wake up" signal to the 6502 and causes it to begin executing code, starting at the address pointed to by locations \$FFFC and \$FFFD in memory. This signal goes low for about 150 milliseconds after system power-up and whenever the RESET key is pressed.

NMI' is a non-maskable (unconditional) interrupt input which causes the 6502 to save its current address and then jump to the address pointed to by locations \$FFFA and \$FFFB.

IRQ' is much like NMI except that the I flag internal to the 6502 must be at a logic "0" in order for this interrupt to be acknowledged by the CPU. The 6502 then jumps to the location pointed to by locations \$FFFE and \$FFFF.

RDY is an input intended to extend read cycles by 1 microsecond when the 6502 is connected to slow memory devices such as EPROM ICs. This input is sampled during PHASE ONE. If the RDY input is low (not-RDY) the CPU will then delay for one microsecond before reading the data.

All of the \$FFFA-\$FFFF locations point into the F8 MONITOR ROM which permanently stores these indirect addresses or "vectors". This allows the system to be able to handle any of these input signals immediately upon power-up.

The R-W' line controls the direction of data flow to and from the 6502. Like the Address Bus, it is also valid roughly 200ns before the rising edge of PHASE ZERO. Similarly, PHASE ZERO can be used as a negative-going enable and PHASE ONE as a positive-going enable for any IC using R/W as an input.

DMA', when held low, causes both the System Address Bus And the System Data Bus to tristate. An external device can pick up the busses and perform its own memory or I/O transfers. This signal should be brought low during I1.

When running a program, the 6502 first performs a fetch cycle by reading an opcode from memory. Then the 6502 executes the opcode, which could be a memory read or write instruction, an instruction to move data between two of the 6502's internal registers, etc. After this the 6502 then fetches another instructions and the pattern repeats. This fetch-execute pattern is called an instruction cycle. The time it takes for each instruction cycle varies from 2 to 6 microseconds with the APPLE II's Mhz clock.

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## REFERENCE OSCILLATOR AND SYSTEM TIMING

### SECTION 3

The Reference Oscillator consists of a differential amplifier made from discrete components, and a quartz crystal. The base of Q1 forms the different amp's inverting input and is held at AC ground (+5 V). The base of Q2 and the collector of Q1 form the amplifier's non-inverting input and output, respectively. The crystal electrically looks like a series L-R-C circuit with a resonant frequency of 14.31863 Mhz. It is tied from non-inverting input to non-inverting output creating a positive feedback loop. Above and below the crystal's resonant frequency, inductive and capacitive reactance, respectively, dominate and create a large voltage drop across the crystal causing very little voltage to appear at the base of Q2 (the non-inverting input). At the crystal's resonant frequency, inductive and capacitive reactance cancel allowing a large signal to appear at the base of Q2, and oscillations to take place.

The Exclusive-OR gate at B2 buffers and squares up the inverted output of the oscillator which appears across R3. The X-OR gate's output provides the 14M signal mainly to drive the System Timing circuits, but 14M is also used in the Video Generator section.

System Timing is generated by the tight interaction between three devices: the 195 at C2, the 153 at C1 and the 175 at B1. These three devices are operated synchronously - which means that all three chips are clocked together causing outputs to change together. Many of the outputs drive inputs on the same or another chip, getting ready for the next clocking. In addition, HPE' (Horizontal Parallel Enable) from the Sync Counters periodically causes most System Timing signals to be stretched slightly.

Eight basic signals are generated by System Timing:

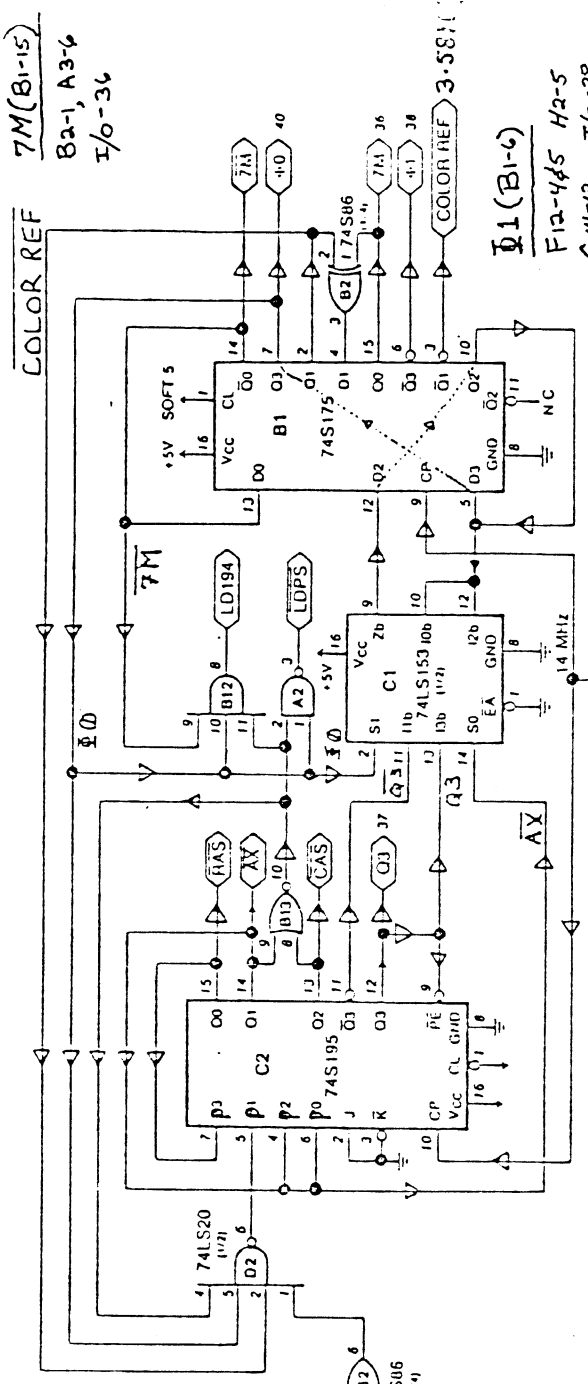
1. 7M - A seven Mhz general purpose timing signal.
2. COLOR REF - A 3.58 Mhz signal used by an external television receiver as a phase reference for color information, as sent by the APPLE II.
3. PHASE ZERO - A one Mhz signal used in both Microprocessor and Video timing. The term PHASE TWO is used in manufacturer's literature to describe the 6502 microprocessor's clock input (and output). PHASE ZERO supplies this input and is used with PHASE ONE for one Mhz timing needs.
4. PHASE ONE - The inverse of PHASE ZERO.
5. RAS' (Row Address Strobe) - This two Mhz signal is used to strobe a seven-bit row address into the 4116 dynamic RAM chips.
6. AX' (Address multipleX) - This two Mhz signal tells RAM hardware to switch from row to column address so that the seven-bit column address may be strobed into the RAMs.
7. CAS' (Column Address Strobe) - This signal, also two Mhz, tells a row of 16K dynamic RAM to select the memory cell at the intersection of the row and

74LS153 Dual 4-to-1 multiplexer  
 74LS175 Quad D flip-flops  
 74LS195 4-bit parallel access shift register (fully synchronous data transfer) ( $\div 7$  generates RAM timing)

AX (2 MHz):  
 C2-4, 6, 14  
 B13-9, C1-14  
 E11, 12, 13-2

CAS (CA-13)  
 B13-8, F2-1  
 F1-12-7

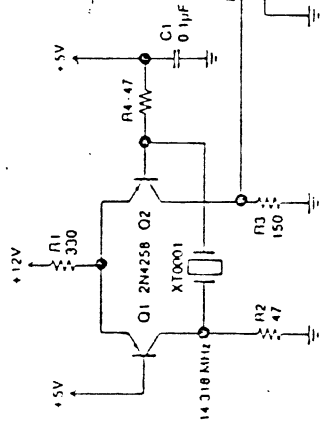
FROM SYNC COUNT FIG. S-4  
 FIPE (D13-12)  
 SOFT 5  
 A2-B



7M (B1-15)  
 B2-1, A3-6  
 I/O-36

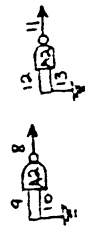
I1 (B1-6)  
 F12-4, 5 H2-5  
 C14-12 I/O-38

I0 (B1-7)  
 C1-2 A2-1 D2-5  
 J1-1 B12-10 B11-2  
 E11, 12 F13-14 F13-6  
 I/O-40



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FIGURE S-3 REPEAT OSCILLATOR AND SYSTEM TIMING



RAS & CAS - 2 MHz  
LOPS - 1 MHz

Soft 5 (A2-8)  
 C2-1, B2-4  
 A3-9, B1-1  
 B4-1, B5-1

Soft 5 (A2-11)  
 D11-1, D12-1, D13-1, 5  
 D14-1, 7, 10  
 B10-1, 4, 10 B9-1, 2  
 B8-1 A, E14-6  
 I/O-110-12, 11, F14-15

Oscillator from underside of board.

SYSTEM TIMING dashed line = 14M·J

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D2-6	HPE'	LDP S'	LD194	Q3	AS7	AS7	I1	I0	COLOR REF	7M
1	1	1	0	1	1	1	1	0	0	1
1	1	1	0	1	1	1	1	0	1	0
1	1	1	0	1	1	0	1	0	1	1
1	1	1	0	1	0	0	1	0	0	0
1	1	1	0	0	0	0	1	0	0	1
1	1	1	0	0	0	1	1	0	1	0
1	1	1	0	0	1	1	1	0	1	1
1	1	1	0	1	1	1	0	1	0	0
1	1	1	0	1	1	1	0	1	0	1
1	1	1	0	1	1	0	0	1	1	0
1	1	0	0	1	0	0	0	1	1	1
1	1	0	1	0	0	0	0	1	0	0
1	1	1	0	0	0	1	0	1	0	1
1	1	1	0	0	1	1	1	0	1	0
1	1	1	0	0	1	1	0	1	1	0
1	1	1	0	1	1	1	1	0	1	1
1	1	1	0	1	1	1	0	0	1	0
1	1	1	0	1	1	0	1	0	0	1
1	1	1	0	1	0	0	1	0	1	0
1	1	1	0	0	0	0	1	0	1	1
1	1	1	0	0	1	1	1	0	0	1
1	1	1	0	1	1	1	0	1	1	0
1	1	1	0	1	1	1	0	1	1	1
1	1	1	0	1	1	0	0	1	0	0
1	1	0	0	1	0	0	0	1	0	1
1	1	0	1	0	0	0	0	1	1	0
1	1	1	0	0	0	1	0	1	1	1
1	1	1	0	0	1	1	1	0	0	0

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D <sup>2</sup> -G	HPE'	LDP S'	LD194	Q3	CAS	RAS	I1	I0	COLOR REF	7M
1	1	1	0	0	1	1	1	0	0	1
1	1	1	0	1	1	1	0	1	1	0
1	1	1	0	1	1	1	0	1	1	1
1	1	1	0	1	1	0	0	1	0	0
1	1	0	0	1	0	0	0	1	0	1
1	1	0	1	0	0	0	0	1	1	0
1	0	1	0	0	0	1	0	1	1	1
1	0	1	0	0	1	1	1	1	0	0
1	0	1	0	1	1	1	1	0	0	1
1	0	1	0	1	1	1	0	0	1	0
1	0	1	0	1	1	0	0	1	1	1
1	0	1	0	1	1	1	1	0	0	0
1	0	1	0	1	1	1	0	1	0	1
1	0	1	0	1	1	0	0	1	1	0
1	0	0	0	1	0	0	0	1	1	1
0	0	0	1	0	0	0	0	1	0	0
0	0	0	0	0	0	0	0	1	0	1
1	0	0	1	0	0	0	0	1	1	0
1	1	1	0	0	0	1	0	1	1	1
1	1	1	0	0	1	1	1	0	0	0
1	1	1	0	1	1	1	1	0	0	1
1	1	1	0	1	1	1	0	0	1	0
1	1	1	0	1	1	0	0	1	1	1
1	1	1	0	1	1	1	1	0	1	0
1	1	1	0	1	1	0	0	0	1	0
1	1	1	0	1	0	0	1	0	0	1

column addresses, and perform either a read or write cycle.

8. Q3 - A general purpose two MHz waveform similar to the RAM timing signals.

Two other signals are generated by combining the basic signals. They are:

1. LD194 (LoaD 194s) - This signal is used in the Video Generator circuits and determines when the 194 Universal Shift Registers will parallel-load graphics data.
2. LDPS' (LoaD Parallel to Serial) - This signal forms the clock input to the 161 Sync Counters, and determines when the 166 Shift Register will parallel load one character row of data.

The Q3, COLOR REF and 7M signals also exist in their inverted form and are used occasionally in various sections of the Main Logic Board. These signals are produced as follows:

7M and COLOR REF are produced by dividing down 14M by two and then four; this is done in the 175.

RAM timing signals, RAS', AX' and CAS', are generated in the 195 by first parallel loading ones, then shifting in zeroes.

The Phase Clocks are produced by the interaction between all three chips. Using the 153, PHASE ZERO routes either Q3 or Q3' indirectly back into its D input at the 175, causing PHASE ZERO to change polarity twice each micro-second.

The 175 acts as a divide-by-two to produce 7M and 7M'. With the help of the EXCLUSIVE-OR gate at B2, 7M is divided by two to produce the 3.58 Mhz COLOR REF signal. (The actual frequency of 14M is 14.31818 Mhz; when divided down, 7M then has an actual frequency of 7.15909 Mhz, COLOR REF the required frequency of 3.579545 Mhz, and so on). Later on we will discuss how the 175 also helps generate the Phase Clocks.

The generation of 7M and 7M' is straightforward. The Q0' signal feeds its D0 Input to create a divide-by two. Less straightforward is the second divide-by-two which produces the 3.58 Mhz COLOR REF signal. Here the D1 Input is 7M exclusive-ORed with Q1. Here are the states:

7M	CURRENT: Q1	D1	NEXT: Q1
0	0	0	0
1	0	1	1
0	1	1	1
1	1	0	0
0	0	0	0
1	0	1	1

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Observe that Q1 half the frequency of 7M, which creates the 3.58 Mhz color burst signal.

The 195 Four-Bit Parallel-Access Shift Register acts as a divide-by-seven and generates the RAM timing signals: RAS', AX', and CAS'. The J and K' inputs, when tied together, form a D type input; this "D" input (pins 2 and 3 of the 195) is tied to ground. When the 195 is in SHIFT RIGHT mode, zeroes are continually shifted into to the Q0 position.

RAS', AX', CAS' and Q3 appear to be the same waveform shifted in time. This is true up until one 14M clock pulse after Q3 goes low. We also see that Q3 is connected to the PE' input of the 195. When Q3 goes, the operation mode changes from shift right mode to parallel load mode. This causes the 195 to behave as a group of D type latches where data at the P0 through P3 inputs appears at the Q0 through Q3 outputs at the next clocking.

Then, AX' goes high one clock pulse after Q3 goes low. This happens because AX's Parallel Input P1 is held high by the NAND gate at D2 pin 6.

RAS' and CAS' go high one clock pulse after AX' goes high. This is because AX' feeds their parallel enable inputs P0 and P2. Q3 goes high one clock pulse after RAS' goes high, because RAS' feeds the parallel enable input to Q3. At this point our cycle repeats for the 195's timing.

In detail, the generation of the phase clocks PHASE ZERO and PHASE ONE involves the interaction of all three System Timing chips. The 153 at C1 plays an important part.

Driving the Select Inputs to the 153 are:

PHASE ZERO, which drives the S1 Input and chooses between the I0b/I1b set of inputs and the I2b/I3b set.

AX', which drives the S0 input and chooses between the lower and higher numbered inputs within each set.

The phase clocks are generated using the 2 Mhz RAM signals which the 195 generates the unused latches on the 175 as a shift register and the 153 as a switch.

Of the phase clocks, only PHASE ZERO feeds back into the circuitry. Note the path that it takes within the 175 and how long each path takes:

From D2 to Q2, 70ns.

From D3 to Q3, 70ns.

Driving half of the inputs to the 153 (I0b and I2b) is the Q2 output. Since the 153's Z output drives the D2 input to the 175 while the 153 is selecting either the I0b or I2b inputs, the signal at Q2 then feeds back into itself.

The 153's S0 input is driven by AX', and the S1 input by PHASE ZERO. When AX' is low, the I0b and I2b inputs to the 153 are selected causing the Q2

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signal to recirculate.

The other two inputs to the 153, I1b and I3b, are driven by Q3 and Q3', respectively. When AX' is high, either Q3' or Q3 is selected depending on the current value of PHASE ZERO.

During the first 500ns of timing, AX' is high, then goes low, then goes high again. When AX' is low, the signal from Q2 of the 195 recirculates through the 153 Q2 can only change when AX' is high.

Q3' is low, and Q3 is high when AX' first goes high. This causes PHASE ZERO to select a value equal to itself to be routed to the D2 input of the 175. Why? If PHASE ZERO is low with AX' high, Q3 (which is low) is routed to the D2 input. That leaves us with the period when AX' is high for the second time, for PHASE ZERO to change. Q3' is now high and Q3 low, causing PHASE ZERO to select its opposite to be routed into D2 of the 175. Two 14M clockings later this signal at D2 becomes the new PHASE ZERO.

The HPE' signal from the SYNC COUNTERS, which occurs during the 65th character position of each line, feeds into the EXCLUSIVE-OR gate at B2 which acts as an inverter. This output drives pin 1 of the 74LS20 at D2. Four signals must be high in order for the 74LS20's output to go low. They are:

HPE' (inverted by the X-OR gate)

COLOR REF'

PHASE ZERO

B13 pin 10 (AX' and CAS' low)

This occurs just before the second falling of Q3 as indicated on the System Timing Diagram.

When Q3 goes from high to low the 195 is in Parallel Enable mode. Usually, AX' is loaded with a one on the next clock pulse, which then pulls RAS' and CAS' up on the clocking after that. With P1 at a zero level, RAS', CAS', Q3 and Phase zero are frozen because they all depend on AX' to go high in order to change. The only signal which feeds the LS20 that is not dependent on AX' to go high is the COLOR REF' signal. Therefore, System Timing stops until the clock pulse after COLOR REF goes low. This adds two 14M clockings or one-half COLOR REF cycle to each line and causes the COLOR REF signal to be inverted with respect to the video data after each line. This allows the non-interlaced color video output of the APPLE II to work properly with ordinary color display devices.

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## SYNC COUNTERS

### SECTION 4

During PHASE ZERO high, the 6502 microprocessor accesses memory. The 6502's Address Bus is valid about 200ns before the rising edge of PHASE ZERO, and is stable until after the falling edge of PHASE ZERO. During PHASE ONE high, the Video circuits access memory, fetching a byte of memory and routing it to the Video Generator. Ram Select (Figure S-6) and Ram Address Mux (Figure S-7) circuits switch between the 6502's Address Bus and the "Video Address Bus" begins life at the Sync Counters as seen in Figure S-4.

The Sync Counters consist of four 161 Four-Bit Binary Counters cascaded together. The counters are operated synchronously (all of the counters are clocked at the same time). When a carry is to be generated from one counter to the next, the counter generating the carry sets a flag, which indicates that the last count has been reached. This flag, called TC (Terminal Count), Enables the next counter stage to advance at the next clocking.

The Sync Counters provide both horizontal and vertical addresses, which point to a memory location containing the ASCII code for the current text character to be sent out. Six signals are used to define the current horizontal character position. They are H0 through H5 and HPE' (Horizontal Parallel Enable).

APPLE II uses 65 horizontal character positions per line. 40 of those are "live" while 25 are used for blanking. One count is used for Parallel Loading the 161's at D13 and D14. This causes HPE' to go from low to high while the remaining six signals, H0 through H5 stay low. 64 counts are used for these six signals H0 through H5 to go through a complete count sequence.

Besides Parallel Loading the 161's at D13 and D14, HPE' also affects System Timing by introducing a 140ns "freeze" on most of the System Timing signals. Refer to Section 3 for more details.

Each time a line of horizontal characters is displayed (the horizontal signals H0 through H5 and HPE' run through a complete 65-count sequence), the current vertical position is incremented so that the video circuits then begin fetching bytes of data from screen memory allocated for the next line. Eight signals are used to define the current vertical character position. They are VA, VB, VC, and V0 through V4.

VA, VB, and VC determine which row (of eight rows of dots) is to be displayed. In TEXT mode, these signals are used by the 2316 Character Generator ROM to select the correct row of dots to be shifted out. In LORES mode, VC selects between the two 194's - VA and VB are not used. In HIRES mode, these signals influence the memory addressing sequence so that data is fetched from a unique memory location for each character - wide row of dots to be displayed.

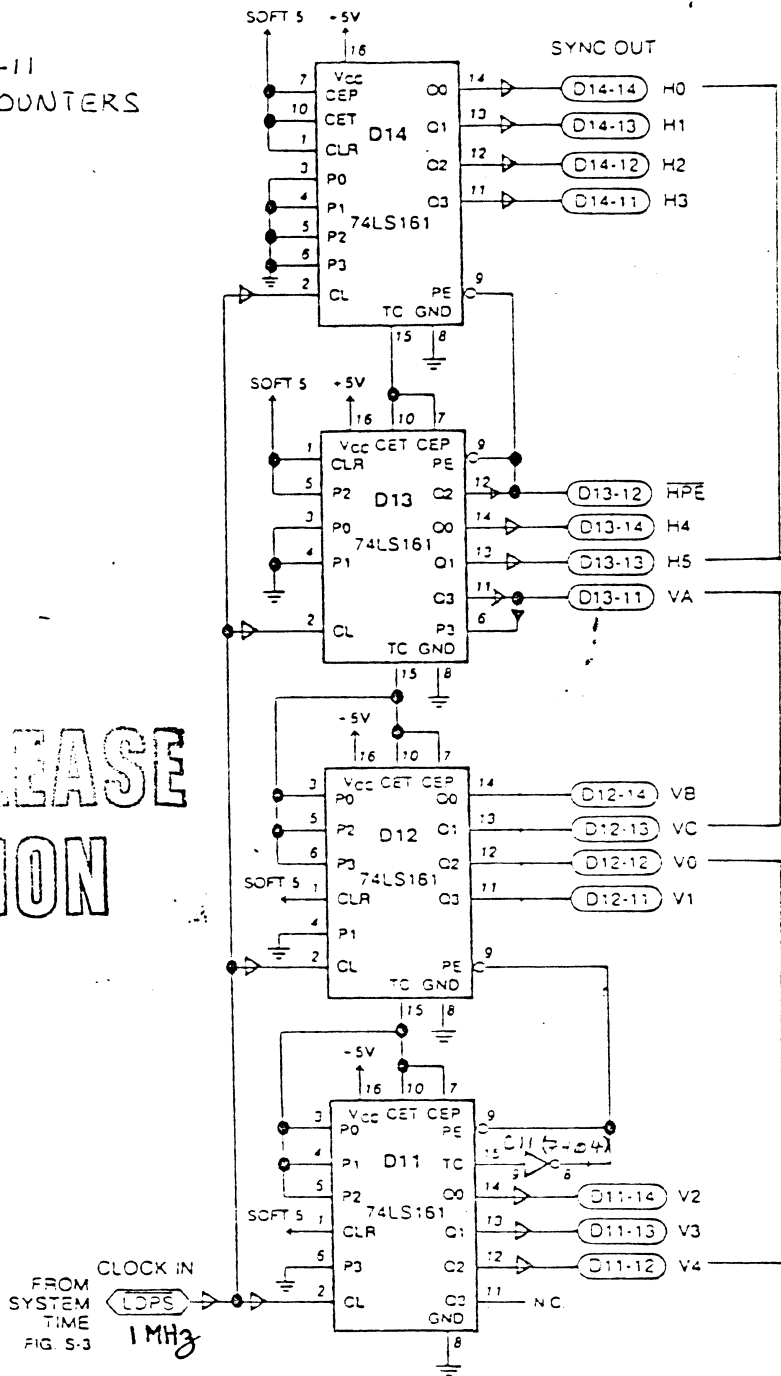
Looking at Figure S-4, we see that VA Feeds its own Parallel Enable input. This leaves VA undisturbed by the Parallel Load That occurs during HPE'. Each Parallel Load copies the current value of VA back into itself.

The Vertical scan time in the APPLE II design is divided into 192 scan lines of "live" video followed by 70 lines of blanking. Looking at the System Timing

74LS161 4-bit binary counter

SOFT 5 = A2-11  
ALL SYNC COUNTERS

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HORIZONTAL  
CHARACTER  
POSITION  
65 STATES,  
40µs ON-SCREEN  
25µs BLANKING

THESE SELECT  
ONE OF THE  
EIGHT VERTICAL  
SCAN LINES  
WITHIN A  
TEXT CHAR.

THESE SELECT  
WHICH ROW  
OF CHARS  
OUT OF 24  
ON-SCREEN

*Vertical*  
262 States  
- 192 Lines  
- 70 Blanking

FIGURE S-4 SYNC COUNTERS

V1 (D12-11): C11-3, E11-12  
VB (D12-14): C12-6, A5-15  
VC (D12-13): A8-5, A5-16  
C12-13, H1-13

Diagram, observe that the "live" vertical count and the first 64 counts of blanking are straightforward binary up-counting. Six extra counts are added to the blanking time with the following scheme:

At the 64th count of blanking, all of the counters are at an "all ones" condition. In addition D11-11 is high which means that all TC outputs including the TC output from the 161 at D11 are high. This causes the PE inputs of D11 and D12 to be held low by the inverter at C11 pin 8. On the next clocking, both D11 and D12 will Parallel Load data. (The 161's at D13 and D14 will again wrap around to all zeroes as usual.) This causes D11 and D12 to be set to a pattern six counts short of an all-ones condition.

However, D11-11 is pre-set to a zero, which means that on the seventh clocking after D11 and D12 Parallel Load, all counter outputs except D11-11 will wrap around to zero instead of Parallel Loading again. This happens because the unused output of D11 (pin 11) is at a logic zero and therefore the 161 at D11 cannot generate a TC signal until D11-11 goes high once again.

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## ROM MEMORY

### SECTION 5

Just below the microprocessor are six sockets which may be filled with from one to six slightly smaller integrated circuits. These ICs are the Read-Only Memory (ROM) "chips" for the Apple. They contain programs for the Apple which are available the moment you turn on the power. Many programs are available in ROM, including the Apple System Monitor, the Apple Autostart Monitor, Apple Integer BASIC and Applesoft II BASIC, and the Apple Programmer's Aid #1 utility subroutine package. The number and contents of your Apple's ROMs depend upon which type of Apple you have, and the accessories you have purchased.

The APPLE II's motherboard ROM memory is organized into six sections of 2K (2048) bytes each. The type "2316" ROMs are referred to by the memory locations into which they map. The D0 ROM occupies space from \$D000 - \$D7FF, the F8 ROM from \$F800 - \$FFFF, etc. On a standard APPLE II, locations \$E000 - \$FFFF contain ROM memory with an optional IC available for the \$D000 - \$D7FF memory space. An APPLE II PLUS contains ROM memory in the entire \$D000 - \$FFFF memory space.

The two low-going Chip Select Inputs for each ROM are provided by outputs from the 138 at F12. Looking at Figure S-5, we see that the two negative-going enable inputs to the 138 (E1' and E2') are driven by pin 6 of the AND gate at H1. In order for one of the 138's outputs to go low, all of the Enable Inputs must be satisfied. This happens only if:

1. A14 and A15 are high (\$C000 - \$FFFF memory space addressed.)
2. PHASE ONE is low (a valid address is on the Address Bus at this time.)

If the 138's Enable Inputs are not satisfied, all outputs Z0 through Z7 are high.

If the Enable Inputs are satisfied, the three Address Inputs to the 138 select one of the Z0 through Z7 outputs to go low. Since the Address Inputs to the 138 are driven by A11 through A13, each 138 output reflects a unique 2K byte memory space. These low-going outputs are routed to the two low-going Enable Inputs of the appropriate ROM chip. The selected ROM will then go from high-impedance to low-impedance mode. The ROM places a byte of code onto the Data Bus selected from the 2K bytes which are permanently stored (mask programmed) within it. The byte to be selected is determined by the 12 Address Inputs A0 through A11, which drive the appropriate inputs to the ROM.

At the rising edge of PHASE ONE, the low-going enable to the 138 is removed, forcing all of its outputs high and disabling ROM. The selected ROM returns to tristate mode at this time.

The high-going enable (CS2) to each ROM has a pullup resistor to +5 volts. This INH' signal is available on the bus to deselect ROM memory. Two current APPLE products, the ROM Card and the Language Card, use this signal to "bank switch" the motherboard ROMs out, so that memory on the peripheral card can be mapped into the same address space.

74LS138 1 of 8 decoder/demultiplexer

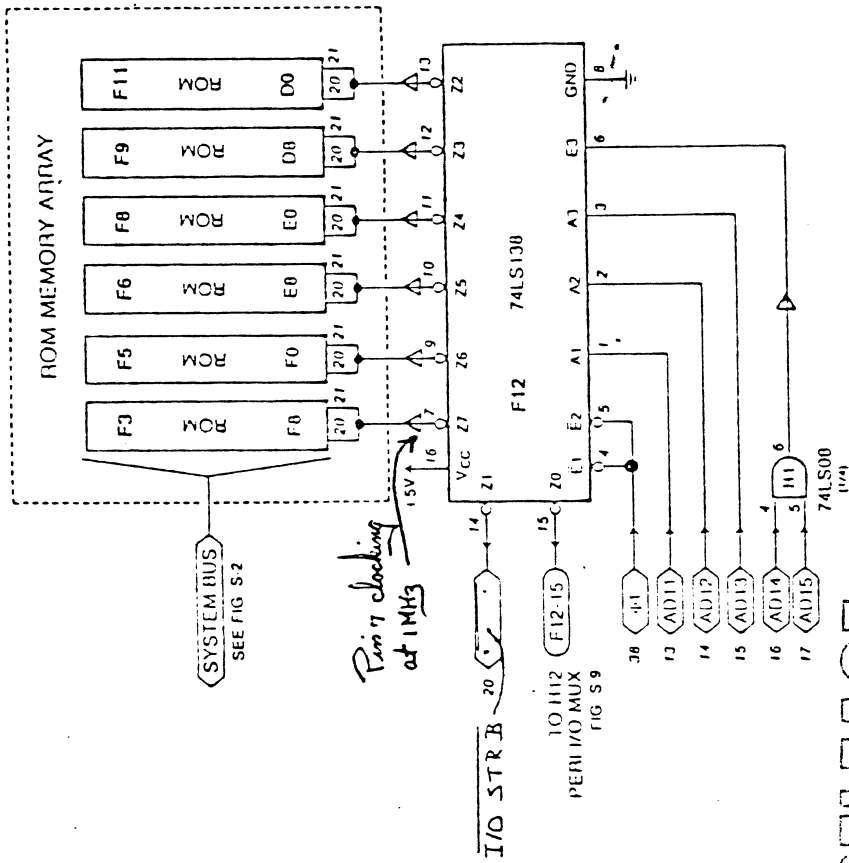
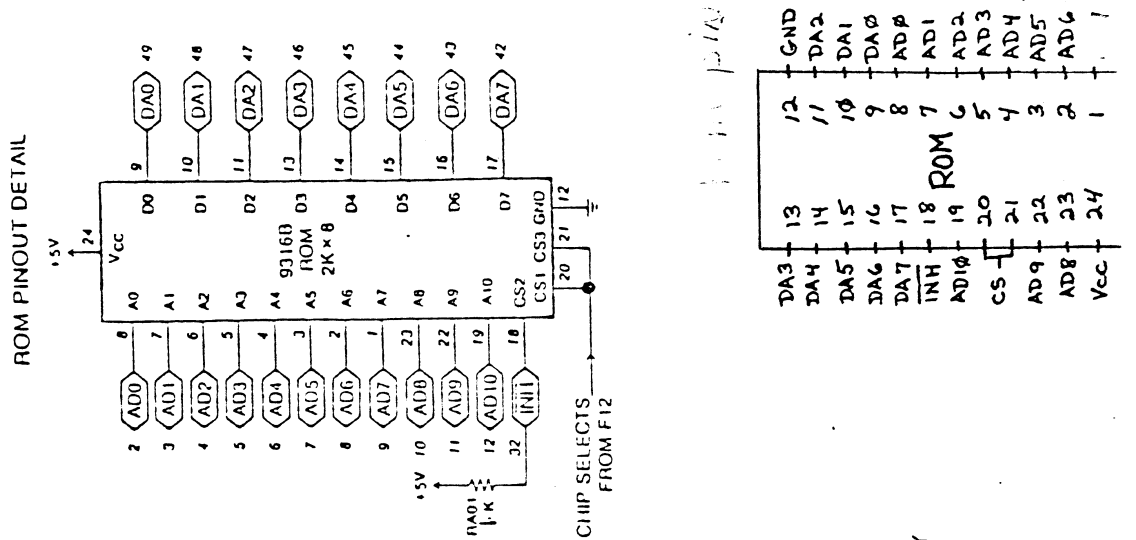


FIGURE S-5 ROM MEMORY

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## RAM SELECT

### SECTION 6

Right below the ROMs and the central mounting nut is an area marked by a white square on the board which encloses twenty-four sockets for integrated circuits. Some or all of these may be filled with ICs. These are the main Random Access Memory (RAM) "chips" for your Apple. An Apple can hold 4,096 to 49,152 bytes of RAM memory in these three rows of components.\* Each row can hold eight ICs of either the 4K or 16K variety. A row must hold eight of the same type of memory components, but the two types can both be used in various combinations on different rows to give nine different memory sizes.\*\* The RAM memory is used to hold all of the programs and data which you are using at any particular time. The information stored in RAM disappears when the power is turned off.

The 6502 microprocessor has 16 address lines, and therefore can address 2<sup>16</sup> or 64K bytes of memory. APPLE II memory space is divided into four 16K sections and takes advantage of 16K dynamic RAMs. The top two address lines, A14 and A15, select the 16K block to be addressed:

A15	A14	SELECTED MEMORY
0	0	ROW C RAM: \$0 TO \$3FFF
0	1	ROW D RAM: \$4000 TO \$7FFF
1	0	ROW E RAM: \$8000 TO \$BFFF
1	1	I/O SPACE: \$C000 TO \$CFFF
		ROM OR LANGUAGE CARD: \$D000 TO \$FFFF

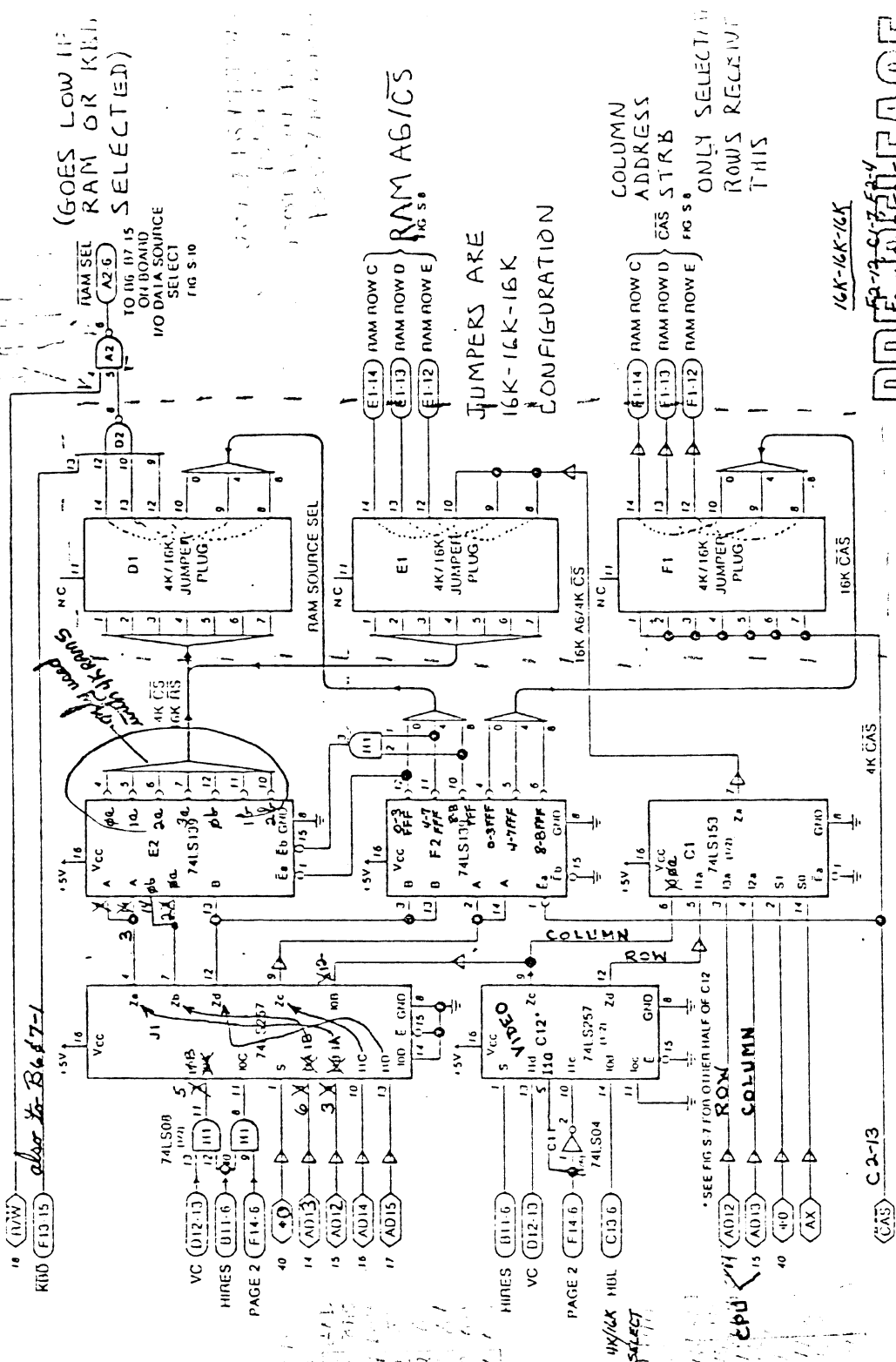
This leaves 14 address lines, A0 through A13, to select an individual byte within a row of RAM. (I/O and ROM / Language Card address space is discussed separately.)

The 16K "4116" Dynamic RAM has only 7 Address Inputs, A0 through A6. In order to send 14 address bits to the RAM, we send them in two groups of seven, a Row Address followed by a Column Address. We also send control signals which indicate when the Row and Column Addresses are valid. These control signals, RAS' (Row Address Strobe) and CAS' (Column Address Strobe) perform other important functions as well: RAS' refreshes data within the RAM, and when R/W is high and RAS' and CAS' are low, then the output of the RAM is enabled.

Looking at figure S-6 we see three sets of signals generated: RAM SEL', RAM A6, and RAM CAS'.

RAM SEL' goes low when there is a READ from RAM or the keyboard. This then places data from either RAM or the keyboard onto the System Data Bus, via the 257s at B6 and B7. RAM A6 sends two bits of address information to the RAM each time a READ or WRITE is performed.

74LS159 Dual 1 to 4 decoder / demultiplexer  
 74LS153 Dual 4 to 1 multiplexer  
 74LS257 Quad 2 to 1 3-state data selector / multiplexer

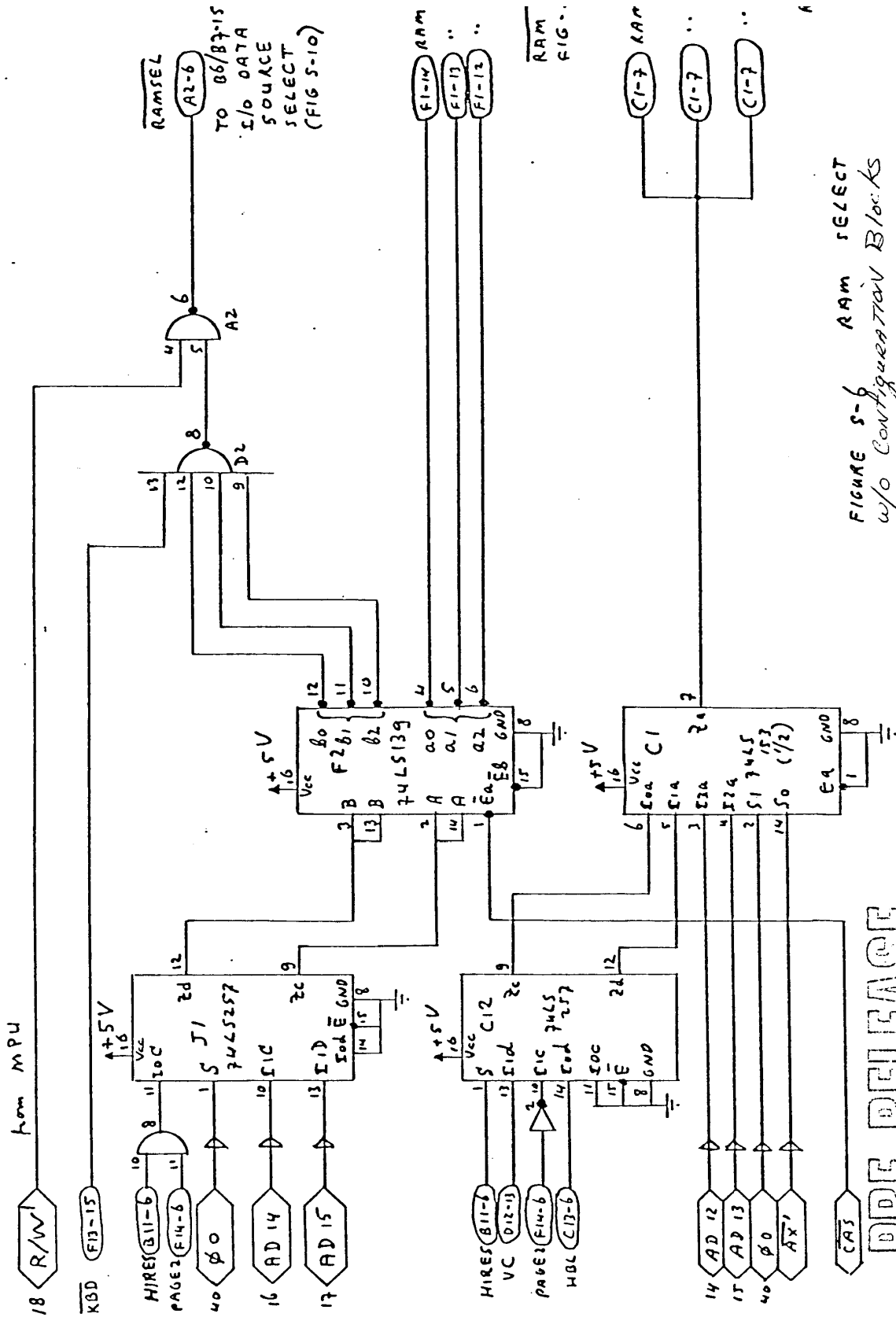


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FIGURE S-6 4K/16K RAM SELECT WITH CONFIGURATION Blocks

FIG 1:  
 4 Test  
 5 Mix  
 6 Page 2

Phase zero high - CPU  
 low - Video



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CAS' is the RAM chip select signal in 16K schemes. Only chips that receive CAS' actually go into a low-impedance mode when a READ from RAM happens. During a WRITE to RAM, only chips that receive CAS' actually change their data.

Referring to the System Timing Diagram, note that there are two memory accesses (bus cycles) each microsecond. The first one occurs when PHASE ZERO is low. This is the Video Cycle where a byte of data is fetched to be displayed on the screen.

The second memory access occurs when PHASE ZERO is high. This is the Microprocessor Cycle where a byte of data is read from or written to memory. There are three timing events within each cycle:

RAS'... When this signal goes low, the Row Address as it appears on RAM A0-A6 is strobed into memory.

AX' (Address multipleX)... This signal causes a switchover from Row to Column Address as seen on RAM A0-A6.

CAS'... This signal strobes in the now valid Column Address into RAM and selects a row of RAM.

Referring back to Figure S-6, we have two activities occurring:

1. The PHASE ZERO clock selects between Video (PHASE ZERO low) and Microprocessor (PHASE ZERO high) addresses.
2. AX' selects between Row Addresses (AX' high) and Column Addresses (AX' low) during each Video and Microprocessor Cycle.

Let's look at how the RAM A6 signal is produced. On systems with 16K RAMs, the RAM A6 signal is common to each RAM. The 153 at C1 produces both the Row A6 and Column A6 for each bus cycle (Video and Microprocessor).

Driving the Select Inputs to the 153 are:

PHASE ZERO - Drives the S1 input and chooses between the two Video Address Inputs (pins 5 and 6) and the two microprocessor inputs (pins 3 and 4).

AX' - Drives S0 input, and chooses between the two Video Address Inputs during PHASE ZERO low, and the two Microprocessor Inputs during PHASE ZERO high.

The Microprocessor Inputs to the 153 are straightforward - A12 and A13 from the microprocessor's Address Bus. The Video Inputs to the 153 are not as straightforward, however. They come from the 257 at C12.

Driving the Select Input to the 257 is the HIRES signal which is high during HIRES graphics and low otherwise. This is done because a different addressing scheme is required for HIRES as opposed to LORES and TEXT.

Now let's look at how RAM CAS' is produced. Recall that we want to only give the chips in a selected ROW of RAM the CAS' signal. During PHASE ZERO (microprocessor mode), the high-order address lines A14 and A15 Select between four blocks of 16K bytes each. At this time we use these high order address lines

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to point to a row of RAM to receive CAS'. During PHASE ONE (Video Mode), we use the Video Address signals to properly select a row of RAM.

RAM CAS' is produced at one of the outputs of the 139 only when CAS' goes low. At that time the values at the A and B inputs determine which row gets CAS'. The A and B inputs are determined by the 257 at J1.

Note in Figure S-6 that the other half of the 139 sends its outputs to a four input NAND gate at D2. This half of the 139 is configured much like the first half except that the Enable pin (pin 15) is grounded. This 139 half feeds the four input NAND gate at D2 with a low going signal any time RAM in the motherboard is selected. Also feeding this NAND gate is the KBD' signal from F13-5. The output of the NAND gate at pin 8 then goes high if either the keyboard or RAM is selected. DF2 pin 8 then drives one input of a two input NAND gate at A2. R/W', the microprocessor READ-WRITE line, drives the other input. The result is that RAM SEL' at A2 pin 6 goes low any time there is a READ from the keyboard or RAM. This gates keyboard or RAM data onto the System Data Bus (Figure S-10).

-----  
\* You can extend your RAM memory to 64K by purchasing the Apple Language Card, part of the Apple Language System (part #A2B0006).

\*\* Due to continuing cost reductions on 16K RAMs, current revisions of the Apple II will accept only 16K RAMs.

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## RAM ADDRESS MUX

### SECTION 7

Two bus cycles occur within an APPLE II each microsecond. One cycle occurs when PHASE ZERO is high and causes the address generated by the microprocessor to be presented to the RAM chips. The other cycle occurs when PHASE ONE is high and causes the Video Address generated by the Sync Counters to be switched in. Some of the Sync Counter Outputs are ready "as is" to be presented to RAM memory while others undergo further processing. Both the Microprocessor Address and the processed Video Address are, at alternate 500ns intervals, presented to the RAM ICs. The RAM chips expect an address to be presented in two steps. With 16K RAMs, a seven bit row address is first presented. The RAM stores this internally when RAS' goes low. Then, a seven bit column address is presented and CAS' is sent to a selected row of RAM which causes it and the seven other selected RAM chips in that row to transfer data to or from the System Data Bus.

We then have a four-way multiplexing scheme, because both the Microprocessor Address and the Video Address must be presented to RAM, each being sent in two stages: a Row Address followed by a Column Address.

Looking at Figure S-7 (Appendix A) we see that six of the seven RAM Address lines are generated using the 153's at E12 and E13. The seventh address line is covered in the RAM Select chapter.

As shown in Figure S-7, two signals drive the select inputs to each 153:

1. PHASE ZERO - Drives each S0 input. It is high during microprocessor access and low during video access.
2. AX' - Drives each S1 input. IT is high when the Row Address is being presented, and low when the Column Address is presented, to the RAMs.

Twice during each bus cycle, RAS' (Row Address Strobe) goes low, strobing the Row Address into the RAM chips (they internally latch the Row Address). Next, AX' goes from high to low causing the 153s to switch over to the Column Address. Only a selected Row of RAM receives CAS' (Column Address Strobe), which latches the Column Address, now valid at the RAM address lines, into the RAM chip and causes a READ or WRITE operation to take place.

The refresh scheme used with dynamic RAM requires each chip to receive the full 128 possible Row Addresses, followed by RAS', every two milliseconds. The Video Address, multiplexed in during PHASE ZERO low, meets this requirement, and thus provides a transparent refresh without the need for dedicated refresh hardware.

Looking at Figure S-7, we see 12 Microprocessor Address lines and 12 Video Address lines driving the 153 inputs. For each Microprocessor address line, a corresponding Video Address line exists. In some cases the correspondence is straightforward - H0, H1, and H2 correspond to A0, A1, and A2. In order to hold the screen memory size down to a minimum, however, an extra chip, the 283 Adder, was introduced. Here's why....

74LS153 Dec 4-to-1 multiplexer  
 74LS257 Quad 2-to-1 data selector/multiplexer (3-state)  
 74LS283 4-bit full adder with fast carry

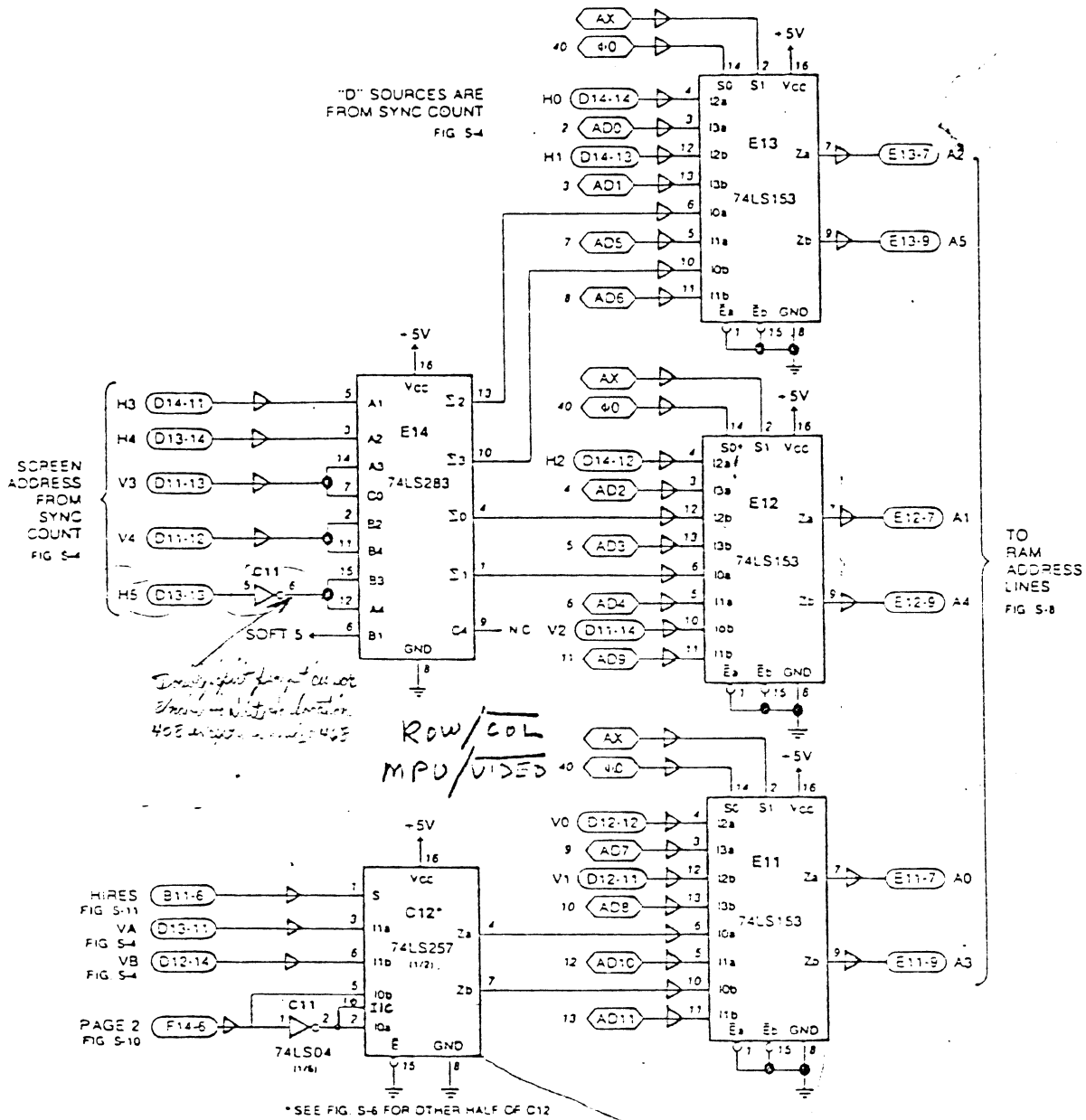


FIGURE S-7 RAM ADDRESS MUX & Refresh Count

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In TEXT mode, there are 24 lines of 40 characters each for a total of 960 "live" characters. To be able to address each character in memory we need only 10 address lines since  $2^{10}$  equals 1024, more than the 960 we need. Furthermore, we don't care what the Video Address looks like during blanking except to satisfy the RAM refresh requirements. We do want all of the RAM memory that contains video character to be in one continuous block, however. There are a total of 11 "video address" lines generated by the Sync Counters: H0 through H5, and V0 through V4. (In TEXT mode, VA, VB, and VC go only to the 2316 Character Generator and don't affect the Video Addressing). The 283 takes in 5 Video Address lines from the Sync Counters, and by adding them together a four bit sum is created. This reduces the count to ten lines resulting in 1024 memory locations used to map 960 "live" characters. (The 64 "wasted" characters are used by the Peripheral Cards. This is documented in the Hobby Card Manual).

The 283 adds the two four bit binary words, plus a carry bit. It produces a four bit result and a carry out. The carry out is not used in the APPLE II design. The following are the two four-bit word signals:

$$\begin{array}{r}
 \phantom{OP A:} \phantom{+} \phantom{V4} \phantom{H5'} \phantom{V3} \phantom{H4} \phantom{H3} \phantom{1} \phantom{(SOFT\ 5\ VOLTS)} \\
 OP A: \quad H5' \quad V3 \quad H4 \quad H3 \\
 OP B: \quad + \quad V4 \quad H5' \quad V4 \quad 1 \quad (SOFT\ 5\ VOLTS) \\
 \hline
 = \quad E3 \quad E2 \quad E1 \quad E0 \quad (TO\ 153's)
 \end{array}$$

The formula above accomplishes the compression from five signals to four. The circuit adds horizontal and vertical signals together, plus a constant, so that the address gaps created by horizontal and vertical blanking are removed. This scheme for generating addresses is responsible for the interweaving that takes place when a page of memory is filled with data from beginning to end consecutively. Adjacent lines are not stored in consecutive memory locations.

Another aspect of the Video Addressing not mentioned until now is the action of the 257 at C12. Looking at Figure S-7, we see that the 257 generates the upper two Address Bits of the Video Address. The Select Input of C12 is driven by the HIRES soft-switch output from the 9334 at B11. When S is low (TEXT/LORES mode) the PAGE 2 soft-switch output from the 9334 and its complement form the Video Address equivalents of A11 and A12, respectively. This circuit creates the \$400 or \$800 base address used when in TEXT/LORES modes. The high-order four bits are all at a logic zero when in TEST/LORES. The circuits which do this are discussed in the RAM SELECT chapter.

When the HIRES soft-switch output is high (HIRES mode) these two outputs reflect VA and VB from the Sync Counters. HIRES uses an eight K byte memory block and must toggle the equivalent of A12 to A0 in the process of scanning the full memory block. VC is used as the video equivalent of A12, and the base address of \$2000 (HIRES PAGE 1) or \$4000 (HIRES PAGE 2) is generated in circuits found in the Ram Select chapter. This causes the twelve-way interlace seen when filling a HIRES page with data, starting at the base address and moving upwards.

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## RAM MEMORY WITH DATA LATCH

### SECTION 8

The APPLE II design centers heavily on the use of Random Access Memory (RAM). Our explanations are limited to the use of type "4116" 16K dynamic RAM ICs.

The four corners of each RAM supply power to the IC:

PIN NUMBER	FUNCTION	VOLTAGE
1	Vbb	-5 V
8	Vdd	+12 V
9	Vcc	+5 V
16 (GROUND)	Vss	0 V

Seven pins are used for addressing:

PIN NUMBER	FUNCTION
5	A5
6	A4
7	A3
10	A0
11	A1
12	A2
13	A6

Since each address line is independent of the others, the address labels assigned to the seven address pins are purely arbitrary. For example, one could switch the trace going to pin 5 of a RAM chip with the trace going to pin 6 with no effect in performance. Data would be stored in and read from different cells within the RAM but there would be no change external to the RAM. Usually the signals driving the RAM address lines are routed to the RAM address inputs at the convenience of the printed circuit board designer.

Two pins are used for DATA:

DIN (Data IN) appears at pin 2. This pin is driven by one of the System Data Bus signals D0-D7.

DOU (Data OUT) appears at pin 14. This RAM signal drives the 174 RAM latches at B5 and B8.

74LS174 74LS174 D-type flip-flop (edge triggered, 8-bit, 100ns)

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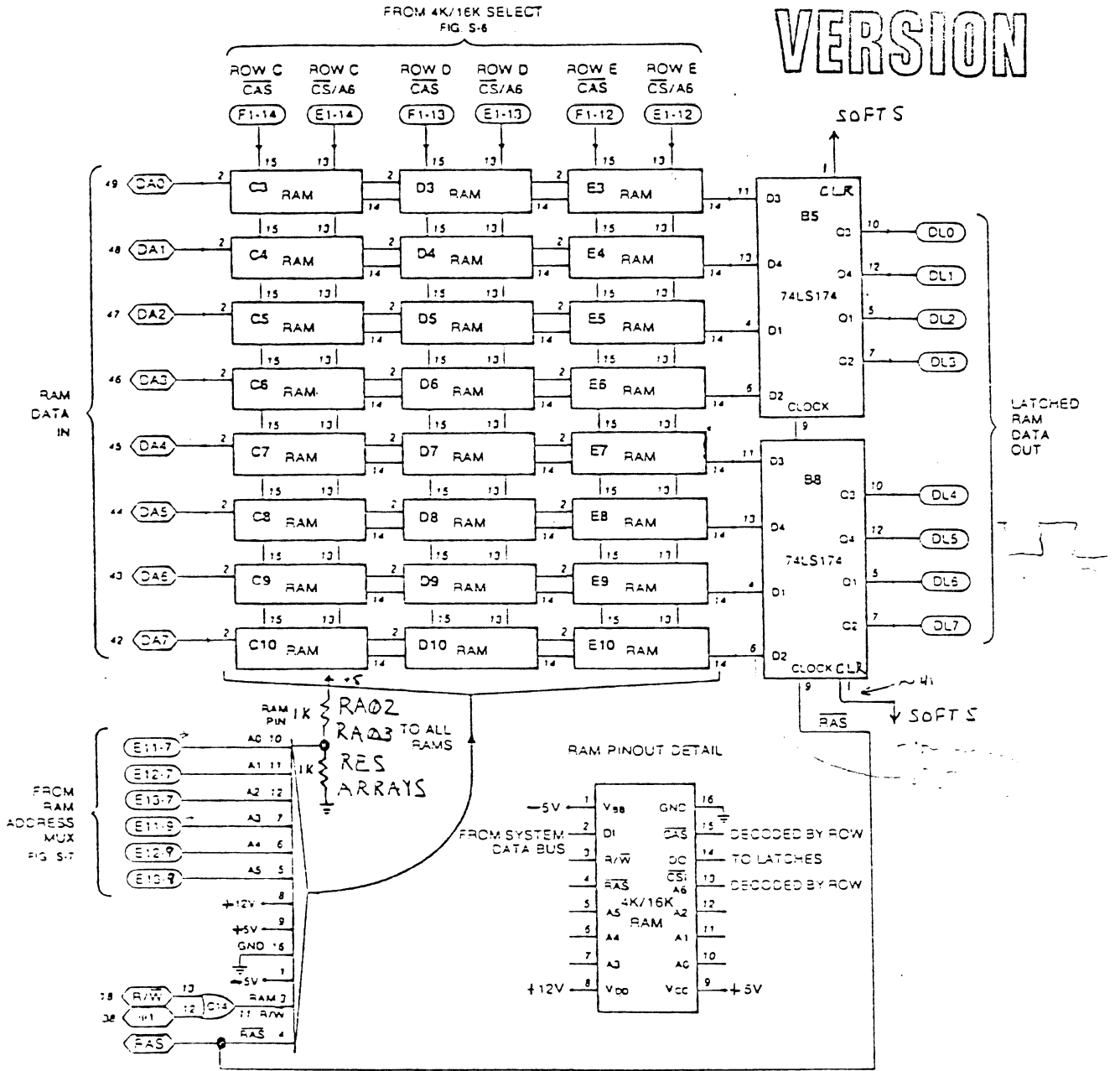
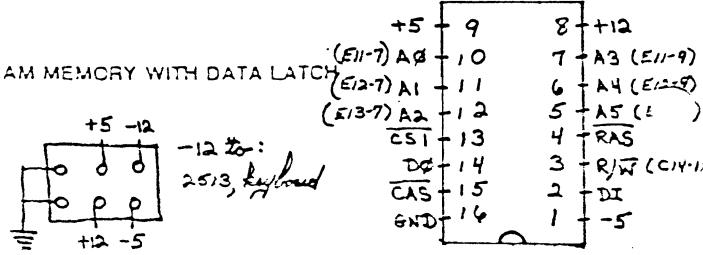


FIGURE S-8 4K TO 48K RAM MEMORY WITH DATA LATCH



There are three RAM control inputs:

WRITE' (READ/WRITE input). This input is driven by the System R/W' line and is Ored with the PHASE ONE clock before being presented to the RAM chips.

RAS' (Row Address Strobe). This signal latches the ROW address into each RAM and causes all cells in the indicated ROW to be refreshed.

CAS' (Column Address Strobe) Is applied only to selected rows of RAM and causes the unique bit cell indentified by the row and column address to be selected. If a write operation is indicated, the value which appears at the DIN input of the RAM cell is copied into the selected bit cell. If a read operation is indicated, the selected bit cell's contents is routed to the DOUT pin and latched by the 174's.

Looking at Figure S-8, we see that the RAM's WRITE' is driven by ORing the System R/W' with the PHASE ONE clock as described earlier. This is done to guarantee that a WRITE cycle only occurs during PHASE ZERO high (the micro-processor's turn to access memory) and never during PHASE ONE high (video's turn to access memory).

The 174s at B5 and B8 are each Quad "D" Latches with a positive-going Clock input. RAM data is latched so that the system can use RAM data while the next address is being set up. Looking at the System Timing Diagram, we see that the new ROW address is strobed into RAM 140ns after the data produced by the previous READ is latched into the 174s.

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## PERIPHERAL I/O

### SECTION 9

Three pins on each slot of the APPLE II motherboard are used to send control pulses to the circuit card installed in that slot position. They are:

CONN. PIN# PRONOUNCED:	SIGNAL NMEMONC
-----	-----
20 "I/O STROBE"	I/O STRB'
41 "DEVICE SELECT"	DEV SEL'
1 "I/O SELECT"	I/O SEL'

Each of these signals produces a low-going pulse for 500ns in response to an address generated by the 6502 microprocessor. Of the three signals, only one, I/O STRB', is common to all slots. The remaining two signals can be sent to a selected slot to the exclusion of all other slots. (I/O STRB' is detailed in the ROM Memory section).

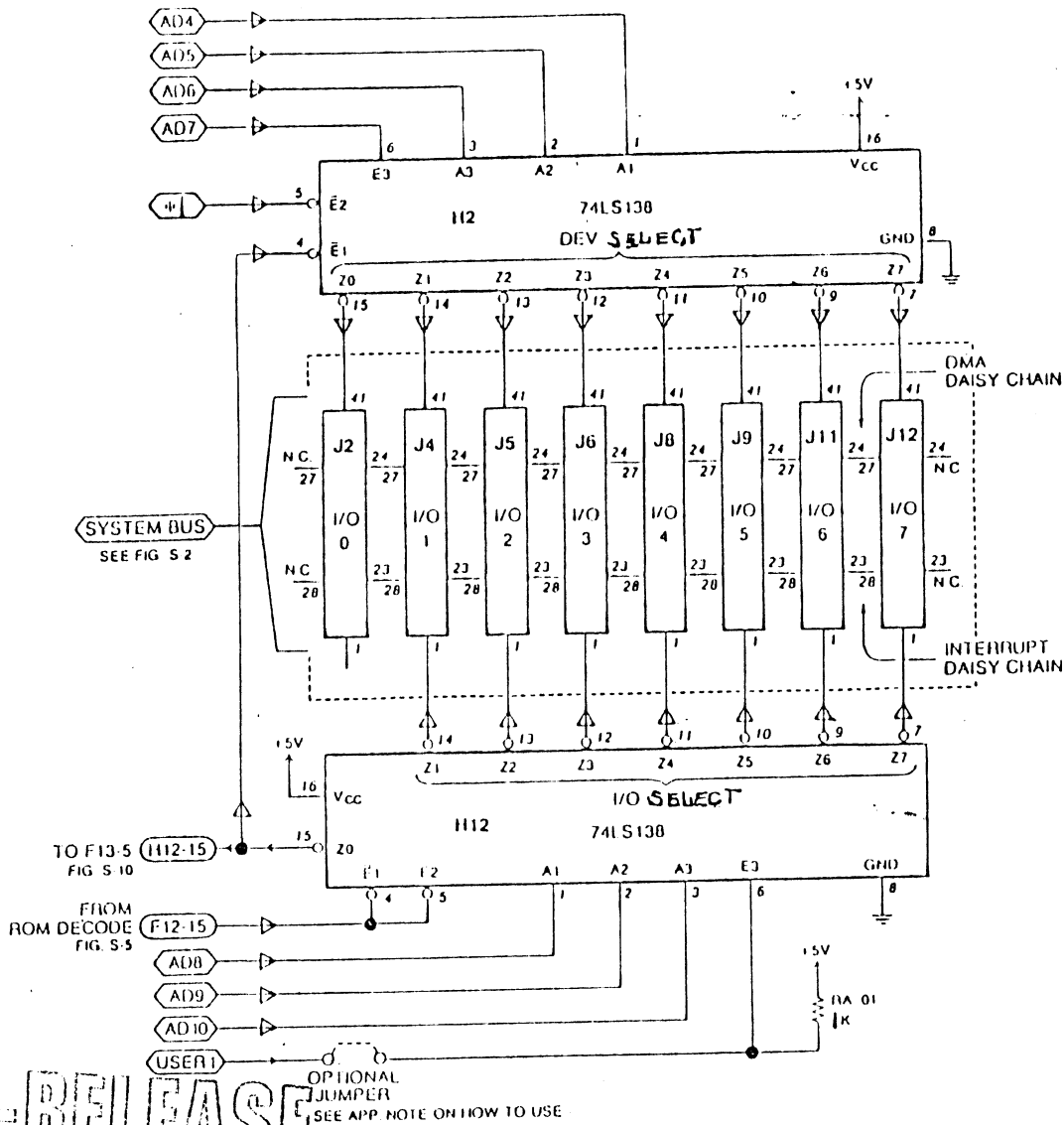
DEV SEL' and I/O SEL' are slot dependent signals. Each slot has a set of addresses which cause a pulse to be generated only at that particular slot. This eliminates the need to have the hardware in each peripheral card decide which signals are intended for it and which are not.

I/O SEL' signals are generated by the 138 at H2. Driving its active-low inputs is F12-15 (see ROM Decode section). This pin goes low anytime an address in the \$C000 to \$C7FF range is generated. Looking at Figure S-9, we see that A8, A9, and A10 drive the Address Inputs to the (H2) 138. This causes the various outputs of the chip to go low anytime a particular 256 byte memory area is addressed. The Z0 output of H12 responds to addresses in the \$C000 to \$C0FF range and is used to enable the keyboard, on-board I/O and soft-switch circuits when A7 is high (\$C080 to \$C0FF), then the 138 at H2 is enabled and DEV SEL' signals, to be detailed later, are generated.

The other seven outputs from the 138 at H12 are distributed among seven I/O slots (Slot 0 does not receive I/O SEL'). Since each slot receives I/O, SEL' over a 256 byte range, this signal is used to enable a small program in PROM which controls APPLE II'S communication with the card. As described in the ROM Decode section, the outputs of the 138 at F12 go low only during PHASE AERO high. The enable into pins 4 and 5 of the 138 at H12 will only go low during Phase zero High. Our I/O SEL' pulses will then be active only during the PHASE ZERO-high portion that the appropriate address is generated.

I/O SEL' provides slots 0 through 7 with a 256 byte memory area. The mapping for this is \$C <slot #> 00 to \$C <slot #> FF, with slot 0 having no I/O SEL' signal.

74LS138 1 of 8 decoder/demultiplexer



I/O CONNECTOR DETAIL

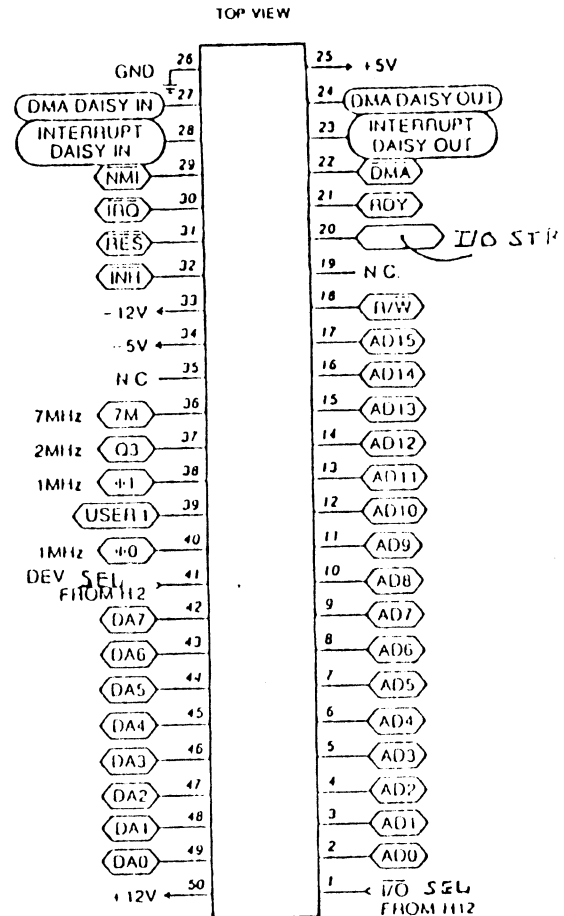


FIGURE S-9 PERIPHERIAL I/O CONNECTOR PINOUT AND CONTROL LOGIC

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Observe in Figure S-9 that the active-high enable to the 138 at H12 has a pull-up resistor, and an optional jumper to connect it to the USER1 pin at the I/O slot (Pin 39). If the jumper is shorted, then USER1 may be used to disable any I/O signals in the \$C800 memory range. This is done by bringing this pin to ground, which disables the 138's active high Enable Input.

DEV SEL' signals map into a tighter address space than the I/O SEL signals. Since the Z0 output of the 138 at H12 is used to enable the 138 at H2, the address space is limited to the \$C000 to \$C0FF space. Since A7 is also used as an enable to the 138 at H12, the address space is further limited to \$C080 to \$C0FF. This allows each peripheral connector a 16 byte address space since A4 to A7 Drive this 138's Address Inputs. Normally, address lines A0 to A3 Are used with the DEV SEL' signal to act as control signals for the peripheral card's hardware. The program to do this often resides in PROM, mapping into the peripheral card's I/O space. In summary:

I/O SEL' gives each peripheral slot, except Slot 0, 256 bytes of address space. Pin 1 of the selected slot will go low for one PHASE ZERO - high time period (500ns) each time one of the slot's 256 assigned addresses is generated by the 6502. This signal is used to enable a small PROM program on the peripheral card.

DEV SEL' gives each peripheral slot, including Slot 0, 16 bytes of address space. Pin 41 of the selected slot will go low for one PHASE ZERO - high time each time an address in the slot's DEV' address space is generated by the 6502. This signal is used to send control signals to the peripheral card.

Since the phase clocks are used to ENABLE the 138's, all signals generated by the 138's will LAG the phase clocks slightly. This means that that the DEV SEL' or I/O SEL' signal will be present until AFTER the falling edge of PHASE ZERO or the rising edge of PHASE ONE. These slot-dependent signals, along with I/O STRB', can be captured by sending the signal into the D input of a latch and clocking the latch with the rising edge of PHASE ONE.

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## ON-BOARD I/O

## SECTION 10

APPLE II offers on-board I/O (input/output) circuits which include the keyboard, video display and the built-in loudspeaker. Other on-board I/O capability includes cassette interface circuitry, Game Paddle (analog to digital conversion) circuits and some general purpose logic inputs and outputs.

Looking at Figure S-10, observe how address lines A0 - A13 distribute themselves between the four ICs at the left. The 138s at F12 and H12 provide enable signals to the ROMs and to the peripheral cards. This is mentioned in detail in the Rom Memory and Peripheral I/O chapters. It is important to note that the Z0 output from the 138 at H12 goes low when an address in the \$C000 - \$C0FF range is generated. You may recall from the Peripheral I/O chapter that the DEV SEL' signals are only enabled when A7 is high and the Z0 output just mentioned is low. The 138 at H12 also uses this Z0 output and A7 as enable signals but A7 is used as a low-going enable signal producing an address range of \$C000 - \$C07F for the 138 at F13 where an address range of \$C080 - \$C0FF exists for the DEV SEL' signals.

Driving the high going Enable Input of the 138 at F13 is the I/O signal from System Timing. This is done since the Address Bus is valid all the time that I/O is high. Address lines A4 to A6 drive this 138's Address Inputs. Since A0 to A3 do not connect with this device, each output will have a 16 byte memory space where any one of the 16 addresses present on the Address Bus will cause the selected output to go low.

Let's cover some F13's outputs and the memory locations into which they are mapped:

Z0 (\$C000 - \$C00F). A READ to any of these addresses causes an ASCII character from the keyboard to be placed onto the Data Bus via the 257s at B6 and B7.

Z1 (\$C010 - \$C01F). This is the Cassette Save signal which clocks the 74LS74 at K13 which is set up as a divide-by-two. This causes its output to toggle. R18 and R19 form a 120 to 1 voltage divider and reduce the four volt peak-to-peak signal from K13's Q2 output to under 40 millivolts peak-to-peak.

Z3 (\$C030 - \$C03F). This signal clocks the other 74LS74 at K13 which is also configured as a divide-by-two. The output of this LS74 is AC coupled to a single-package Darlington amplifier which drives the speaker through a 27 ohm current-limiting resistor.

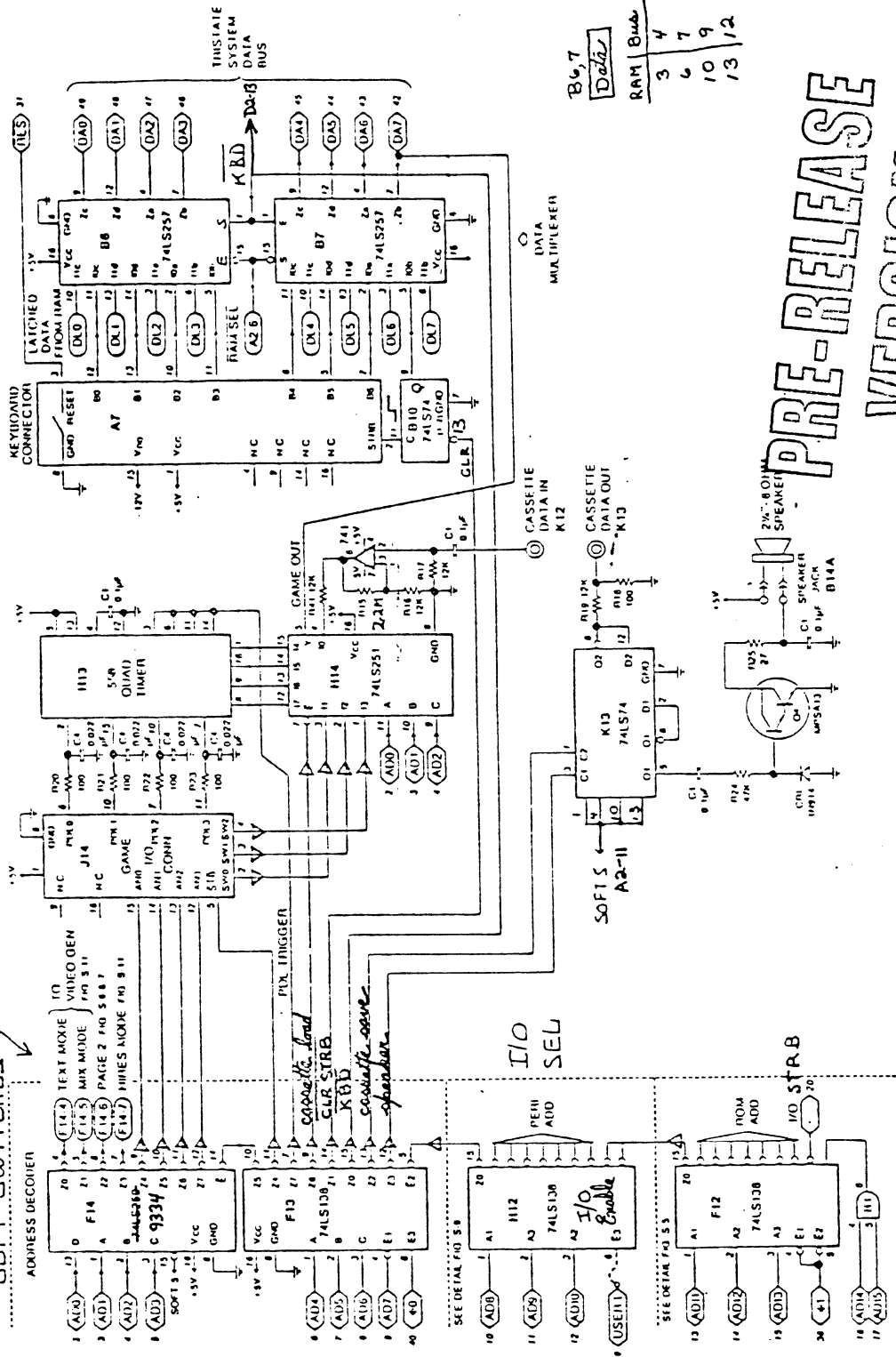
Z4 (\$C040 - \$C04F). This signal appears at pin 5 of the game I/O connector and is available for user applicaitons.

Z5 (\$C050 - \$C05F). This signal enables the 9334 at F14 which is responsible for the graphics "soft switches" and some software-controlled signals available at the Game I/O connector outputs.

Z6 (\$C060 - \$C06F). This signal enables the 251 at H14. The 251 chooses between the following inputs:

74LS74 Dual D-type flip flop  
 74LS251 8-input 3-state multiplexer  
 74LS257 Quad 2-to-1 data selector/multiplexer (3-state)  
 9334 Eight bit addressable latch

FN-6: H1-9, C12-5, C11-1  
 SOFT SWITCHES



B6,7	DATA
RAM	Bus
3	4
6	7
10	9
13	12

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FIGURE 5-10 ON-BOARD I/O

Action of F12 & H12 is to provide enable signals to ROMs & peripheral cards.

MUX INPUT NAME	INPUT IS
10	Cassette In
11	SW0
12	SW1
13	SW2
14	PDL0
15	PDL1
16	PDL2
17	PDL3

Since the 251's Select INputs are driven by A0-A2, these various inputs appear at Data bit 7 when reading to addresses \$C060 \$C067. The 251's Y output drives bit 7 of the Address Bus.

The Cassette In Signal to the 251 comes from the 741 Op-Amp at location K1.

The PDL signals to the 251 come from the 558 Quad Timer. The varying resistance of each paddle changes the R-C time constant; therefore, the time period for which the output remains high. This time period is converted into a number ranging from 0 to 255, in software.

Z7 (\$C070 - \$C07F). This output from the 138 resets all four of the 558's Timers.

The 257s at B6 and B7 buffer the keyboard and Latched RAM Data from the Data Bus.

The RAM SEL' signal drives the Enable Input to the 257, and goes low if RAM or the KBD is selected. When this happens, usually Latched RAM Data is selected. If our KBD' signal from the 138 at F13 is low, however, (READ from KBD) then the keyboard is selected.

The 9334 IC at F14 is an eight-bit Addressable Latch. The 9334's outputs perform two functions. The first one is to throw the soft switches which control the video modes. These switches are in the \$C050 to \$C057 address range. Note that A0 forms the D input to this 9334. This second function performed by the 9334 is to set the four Annunciator Outputs available at the Game I/O Connector. This general-purpose LSTTL outputs are available for user applications.

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## VIDEO GENERATOR

### SECTION 11

The Video Generator circuits convert bytes of data into serial video. Horizontal and vertical sync pulses are added to produce composite video. A color burst signal is also added when color graphics is displayed. The purpose of the Video Generator is then to:

1. Generate text or graphics serial video data.
2. Correctly route the video signal to the output jack.
3. Add horizontal and vertical sync pulses and, if required, a color burst signal.

There are three video modes:

1. TEXT. Data is displayed as alphanumeric characters in 24 lines of 40 columns each.
2. LORES (LOW RESolution) graphics. Data appears as colored squares within a 40 (h) by 48 (v) matrix with 16 available colors.
3. HIRES (HIGH RESolution) graphics. Data is shifted out as a 280 (h) by 192 (v) matrix with six colors available.

TEXT generation is the most straightforward of the three modes. Two principal ICs are involved - the \*2316 Character Generator and the 166 Shift Register. Referring to Figure S-11 we see that the 2316 is a special-purpose ROM with 9 Address Inputs and 5 Data Outputs. Let's describe what a character is supposed to look like on the screen:

A TEXT character appears as seven groups of five dots across. These groups of five dots are stacked vertically to produce a five (h) by seven (v) dot matrix. To the left and right of each character is a blank column used to separate characters horizontally. An eighth ROW of blank dots is produced by the Character Generator to separate characters vertically.

The Character Generator produces eight groups of five dots each which are shifted out as serial video. Looking at Figure S-11, we see that six of the Character Generator's inputs are from Latched RAM Data and represent the ASCII code of the character to be displayed. Three other inputs to the 2316 are VA, VB, and VC from the Sync Counters. These three signals go through 2<sup>3</sup> or eight different states, each state addressing a different row of dots within each character.

The 166 Shift Register accepts each five-dot row from the Character Generator, adds a blank dot in front of and behind the row, and shifts out the dots one at a time.

Three inputs from System Timing, 14M, 7M, and LDPS' (Load Parallel to Serial) control the action of the 166. During each shift, bits are shifted up alphabetically: G moves to H, F to G, E to F, etc. Note that both H and B inputs



are grounded; these create the blank dots to the left and right of each row which separate adjacent characters.

Our 166 mode diagram looks like this:

14M	7M	LDPS'	RESULT
X	1	X	HOLD CURENT POSITION
^	0	0	PARALLEL LOADS
^	0	1	SHIFTS UP ONE POSITION

NOTE: "~" represents a low-to-high transition. "X" means "can be any value."

The 166 is allowed to change only if 7M is high. This results in data being shifted out at 7 Mhz. Referring to the System Timing Diagram, we see that LDPS' occurs in the middle of PHASE ZERO once every microsecond, causing a new row of microsecond.

The Exclusive-OR gate, which QH feeds into, functions as a controlled inverter. Observe in Figure S-11 that Latched RAM Data bits six and seven feed into gates at B11 and B13, the output of which passes through the 194 at A10 via pins six and seven, to the other input of the Exclusive-OR gate. (The 194 at A10 functions as a latch.) The 555 Oscillator at B3 operates at about three hertz and also feeds into the gates at B11 and B13. As a result, when pin 12 of the EXCLUSIVE-OR is high, video will be displayed in inverse field, otherwise it passes through undisturbed. The effect of DL6 and DL7 on the serial video output is:

DL7	DL6	VIDEO MODE	
0	0	INVERSE	B13-4 IS HELD HIGH
0	1	FLASHING	B13-4 WILL BE HIGH (EXCEPT WHEN 555 IS HIGH)
1	0	NORMAL	B13-4 IS HELD LOW
1	1	NORMAL	B13-4 IS HELD LOW

The video output feeds into the 151 at A9. This chip acts as a master switch between TEXT, LORES, and HIRES modes. (will be discussed later)

Both LORES and HIRES GRAPHICS make use of the 194 Universal Shift Register. The complexity of this chip is due to the four operation modes which cause a Hold conditon, Shift Left and Right conditions, and a Parallel Load condition. For our purposes we can ignore one unused mode and describe the 194's operating modes as: (see top of next page)

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S1	S0	MODE	RESULT
0	0	HOLD	DATA STAYS THE SAME
1	0	SHIFT LEFT	DATA FROM Q3 SHIFTS TO Q2, Q2 TO Q1, ETC DSL INPUT SHIFTS INTO Q3
1	1	PAR. LOAD	DATA AT D0 - D3 APPEARS AT Q0 - Q3

NOTE: References made to "the twin 194s" refer to the two at B4 and B9. These two ICs are the nucleus of the LORES and HIRES circuits.

In both LORES and HIRES schemes Latched RAM Data is parallel-loaded into the Twin 194s and then shifted left for a one microsecond interval. The HIRES signal from F14 pin 7 drives the 257's Select Input. The 257 then chooses between Data Input Set 0 when in LORES mode or Data Input Set 1 when in HIRES mode. The effect that changing modes has on the Twin 194s is to:

1. Change the way data circulates within the 194's - they act as independent recirculating shift registers, or "spinners" when in LORES. In HIRES mode the Twin 194s connect in series to make one eight position shift register (only 7 are actually used).
2. Change the rate at which the 194s are shifted by effecting the S1 Mode Control input to the 194s.

The twin 194s have their S1 Inputs held high all the time when in LORES. Remember that Data Input Set 0 is selected (routed to the Z Outputs) when in LORES mode, and Data Input Set 1 is selected when in HIRES. Following the path back from the ZC output of the 257, we see that the 194s S1 inputs connect to Soft 5 volts via the IOc Input of the 257. The S0 inputs of the 194s are "hardwired" to the LD194 signal from System Timing. In LORES then, the 194s are in one of two modes:

1. Parallel Load (LD194 is high)
2. Shift Left (LD194 is low) enter a Hold state
3. When LD194 is low and 7M' is high, then the 194s do an eight bit shift. The Q0 output of the 194 at B9 feeds the Data Shift Left Input of the 194 at B4.

The 151 at A9 serves as the master switch between TEXT, LORES and HIRES. It also switches between inputs in LORES mode. Looking at Figure S11, we see that the C Input to the 151 is driven by pin 2 of the 174 at B8. This signal serves to switch between TEXT and graphics. When the C Input is low, one of the Data Inputs D0 through D3 are candidates to become the output. Select inputs A and B choose between the four inputs. All four inputs D0 through D3 are, however, driven by the video text signal. Therefore, we are in TEXT mode regardless of the values of the A and B inputs when C Input is low.

When the C input is high, one of the data inputs D4 through D7 are selected to become the output signal. Here the final selection process is more involved.

The Zb and Zd outputs of the 257 pass through the 194 at A10 which acts as a latch. The Q0 and Q1 outputs of the 194 which reflect the levels of the Zb and Zd outputs from the 257, drive the A and B inputs, selecting either Data Input D4, D5, D6, or D7. The selected input becomes the final output.

In LORES mode, Data Input set 0 is selected. H0 and VC from the Sync Counters are now routed to the A and B inputs, respectively, of the 151. This causes two effects:

1. When VC is low, the 194 at B4 is selected. When VC is high, the 194 at B9 is selected.
2. On even numbered columns, data is tapped from each 194 at its Q0 output. On odd numbered columns, data is tapped from each 194 at its Q2 output. This allows for continuous LORES patterns to be generated across the screen. This happens because each 194 is two clockings out of phase after 14 clockings (14 MOD four is two). The "tap" is moved two places to corrector for this.

VC, from the Sync Counters, changes polarity every time four horizontal lines are generated. Switching between the Twin 194s every four horizontal lines causes a byte of Latched RAM Data to appear as two LORES squares stacked on top of one another.

In HIRES mode, the A and B inputs to the 151 are both low. This causes only the Q0 output of the 194 at B4 to be selected.

In summary for mode switching:

1. In TEXT mode the C input to the 151 at A9 is low. Any values for the A and B inputs to the 151 selected TEXT video. In either graphics mode, the C input is high.
2. In LORES mode, H0 and VC from the Sync Counters drive the A and B inputs to the 151, causing a byte of Latched Ram Data to appear as two LORES squares, stacked one on top of another.
3. In HIRES mode, only Q0 of the 194 at B4 is selected as video data.

At the bottom of Figure S-11 are two soft switch outputs, TEXT and MIX, two soft Sync Counter outputs V2 and V4, and RAS' from System Timing. These signals combine in the gates at B12 and B13. The resulting signal, delayed by 1.5 microseconds by the cascaded latches at B5 and B8 drives the C input to the 151 switching between TEXT (C input high). These gates allow for MIX mode which has four text lines at the bottom of the screen. The HIRES ENABLE signal is produced by ANDing the HIRES signal with latch output B8-2, and is used to alter the addressing scheme when in HIRES mode.

In either GRAPHICS mode, brightness and color information is contained in the bit patterns that are shifted out. Brightness, or luminance is based on the ratio of the number of dots set high to the total number of dots sent out within a given screen area.

Color information is based on the phase relationship between the 3.58 Mhz

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COLOR BURST signal, which is sent for a brief time following the rising edge of the horizontal Sync pulse, and the serial video data.

As explained in the new APPLE II Reference Manual, the most significant bit from Latched RAM Data serves as a control bit in REV 1 or higher boards. This creates an additional 70ns delay to the serial video when the high-order bit from Latched RAM Data is set. We get green, violet, white and black when the "control bit" is 0 and orange, blue, white, and black when the control bit is 1.

The gates in the upper right corner of Figure S-11 produce the horizontal and vertical sync pulses that allow a television set to "lock in" to the APPLE II video signal. APPLE II generates composite video (all video information is contained in one signal); sync pulses are mixed in with the video data via R6. Looking at the System Timing Diagram, we see that horizontal blanking occurs during the first 25 counts of the Sync Counters. Note also that vertical blanking occurs whenever V3 and V4 from the Sync Counters are both high. Within each horizontal and vertical blanking period, a corresponding sync pulse is generated.

Circuits disable the 151 during blanking, thus forcing its output to a logic 0. Looking at Figure S-11, we can trace back from the STRB Input of the 151 (pin 7) through the 194 at A10 to pin 6 of the OR gate at C14. Since the STRB Input to the 151 is active low, we want the OR gate to go high only during horizontal or vertical blanking. Driving pin 5 of the OR gate is the HBL (Horizontal BLanking) signal produced by pin 6 of the LS51 - this signal is high during the first four counts of the Sync Counters. Driving pin 4 of the OR gate is V3 ANDed with V4, which is the Vertical Blanking signal. The sync pulses are produced by ANDing the blanking signals with a few more timing signals to narrow them down within the blanking periods. For the horizontal sync pulse we AND HBL with V3. For the vertical sync pulse we AND VBL with V2 And V1'. This is done with the lower LS51 in Figure S-11. This LS51 ORs the horizontal and vertical sync pulses and inverts the result so our sync pulses will be low-going. The final result is mixed into the output via R8.

Rev 1 or later boards have a modified version of the sync circuit, which corrects for some timing problems encountered when interfacing the APPLE II to certain television set models.

COLOR BURST occurs during HBL when H4 is high and H2 is low. Looking at the System Timing Diagram, we see that this starts right after the horizontal sync pulse and continues until H2 goes high (4 microseconds total time).

The COLOR BURST signal is shaped by R5, L1, C2, C3. This network is a tank circuit which is tuned to the COLOR BURST frequency of 3.58 Mhz.

Adjusting C3 causes a slight phase shift to the COLOR BURST signal with reference to the video data and has the effect of shifting the colors on the screen. This provides a "fine tuning" color adjustment on the APPLE II to supplement controls found on the television set.

\*Early revision boards used a 2513 Character Generator.

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VIDEO STATE DIAGRAM

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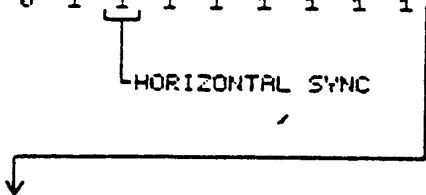
HORIZONTAL CHARACTER POSITIONS: 25 STATES OF BLANKING, 40 STATES OF "LIVE" VIDEO.  
 EACH STATE (ONE CHARACTER WIDE) LASTS 1 MICROSECOND (CLOCKED BY LDPS)

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	HBL					LIVE				
H0	0	X	X	X	X	X	X	X	X	X
H1	0	X	X	X	X	X	X	X	X	X
H2	0	X	X	X	X	X	X	X	X	X
H3	0	0	1	0	1	0	1	0	1	0
H4	0	0	0	1	1	0	0	1	1	1
H5	0	0	0	0	0	1	1	1	1	1
HPE'	0	1	1	1	1	1	1	1	1	1

65 HORIZONTAL CHARACTER  
 POSITIONS PER LINE OF TEXT

VERTICAL SYNC COUNTERS  
 INCREMENT HERE



	192 LIVE VERTICAL SCAN LINES: 24 CHARACTER POSITIONS WITH 8 SCAN LINES PER ROW.																								70 BLANKED SCAN LINES (VBL)								
A	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	1	0	1	0	1
B	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	1	0	0	1	1
C	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	0	1	1	1	1	
D	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	1	1	1	1	1	
1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	1	1	1	1	1	1	
2	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
3	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
4	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
5-11	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0

8 SCAN LINES  
 PER ROW OF  
 CHARACTERS

24 CHARACTER  
 ROWS

VERTICAL SYNC

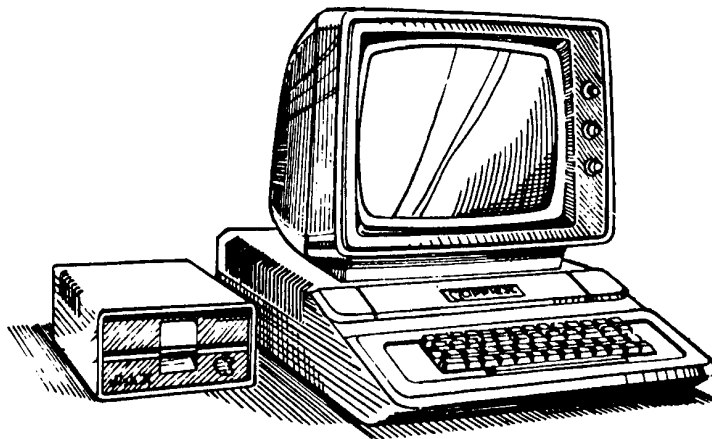


## Apple II Computer Technical Information

# APPLE II / APPLE II-PLUS LEVEL II SERVICE REFERENCE MANUAL

Pre-Release Version

## CHAPTER 8 MORE MEMORY



Written by  
Apple Computer, Inc. • Level II Service Center  
1981

( This page is not part of the original service manual )

MORE MEMORY

The Apple's 6502 microprocessor can directly reference a total of 65,536 distinct memory locations. You can think of the Apple's memory as a book with 256 "pages", with 256 memory locations on each page. For example, "page \$30" is the 256 memory locations beginning at location #3000 and ending at location \$30FF. Since the 6502 uses two eight-bit bytes to form the address of any memory location, you can think of the bytes as the page number and other as the location within the page.

The Apple's 256 pages of memory fall into three categories: Random Access Memory (RAM), Read-Only Memory (ROM), and Input/Output locations (I/O). Different areas of memory are dedicated to different functions. The Apple's basic memory map looks like this:

System Memory Map		
Page Number:		
Decimal	Hex	
0	S00	RAM (4K)
1	S01	
2	S02	
.	.	
.	.	
190	SBE	I/O (2K)
191	SBF	
192	SC0	
193	SC1	
.	.	
198	SC6	I/O ROM (2K)
199	SC7	
200	SC8	
201	SC9	
.	.	
206	SCE	ROM (12K)
207	SCF	
208	SD0	
209	SD1	
.	.	
254	SFE	
255	SFF	

Figure 5. System Memory Map

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## RAM STORAGE

The area in the Apple's memory map which is allocated for RAM memory begins at the bottom of Page Zero and extends up to the end of Page 191. The Apple has the capacity to house from 4K (4,096 bytes) of RAM on its main circuit board, (only early revisions with RAM configuration blocks). In addition, you can expand the RAM memory of your Apple all the way up to 64K (65,536 bytes) by installing an Apple Language Card. This extra 16K of RAM takes the place of the Apple's ROM memory, with two 4K segments of RAM sharing the 4K range from \$D000 to \$DFFF.

Most of your Apple's RAM memory is available to you for the storage of programs and data. The Apple, however, does reserve some locations in RAM for use of the System Monitor, various languages, and other system functions. Here is a map of the available areas in RAM memory:

Page Number:		Used For:
Decimal	Hex	
0	\$00	System Programs
1	\$01	System Stack
2	\$02	GETLN Input Buffer
3	\$03	Monitor Vector Locations
4	\$04	Text and Lo-Res Graphics Primary Page Storage
5	\$05	
6	\$06	
7	\$07	
8	\$08	Text and Lo-Res Graphics Secondary Page Storage
9	\$09	
10	\$0A	
11	\$0B	
12 through 31	\$0C  \$1F	FREE
32 through 63	\$20  \$3F	Hi-Res Graphics Primary Page Storage
64 through 95	\$40  \$5F	
96 through 191	\$60  \$BF	

## ZERO PAGE MEMORY MAPS

**Table 18: Monitor Zero Page Usage**

Decimal	Hex	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
		\$0	\$1	\$2	\$3	\$4	\$5	\$6	\$7	\$8	\$9	\$A	\$B	\$C	\$D	\$E	\$F
0	\$00																
16	\$10																
32	\$20	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
48	\$30	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
64	\$40	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
80	\$50	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
96	\$60																
112	\$70																
128	\$80																
144	\$90																
160	\$A0																
176	\$B0																
192	\$C0																
208	\$D0																
224	\$E0																
240	\$F0																

**Table 19: Applesoft II BASIC Zero Page Usage**

Decimal	Hex	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
		\$0	\$1	\$2	\$3	\$4	\$5	\$6	\$7	\$8	\$9	\$A	\$B	\$C	\$D	\$E	\$F
0	\$00	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
16	\$10	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
32	\$20																
48	\$30																
64	\$40																
80	\$50	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
96	\$60	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
112	\$70	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
128	\$80	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
144	\$90	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
160	\$A0	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
176	\$B0	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
192	\$C0	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
208	\$D0	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
224	\$E0	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
240	\$F0	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•

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Following is a breakdown of which ranges are assigned to which functions:

**Zero page:** Due to the construction of the Apple's 6502 microprocessor, the lowermost page in the Apple's memory is prime real estate for machine language programs. The System Monitor uses about 20 locations on Page Zero; Apple Integer BASIC uses a few more; and Applesoft II BASIC and Apple Disk Operating System use the rest. Tables 18, 19, 20, and 21 show the locations on zero page which are used by these system functions.

**Page one:** The Apple's 6502 microprocessor reserves all 256 bytes of Page 1 for use as a "stack". Even though the Apple usually uses less than half of this page at any one time, it is not easy to determine just what is being used and what is lying fallow, so you shouldn't try to use Page 1 to store any data.

**Page two:** The GETLN subroutine, which is used to get input lines by most programs and languages, uses Page 2 as its input buffer. If you're sure that you won't be typing any long input lines, then you can (somewhat) safely store temporary data in the upper regions of Page 2.

**Page three:** The Apple's Monitor ROM (both the Autostart and the original) use the upper sixteen locations in Page Three, from location \$3F0 to \$3FF (decimal 1008 to 1023). The Monitor's use of these locations is outlined on Table 14.

**Pages four through seven.** This 1,024-byte range of memory locations is used for the Text and Low-Resolution Graphics Primary Page display, and is therefore unusable for storage purposes. There are 64 locations in this range which are not displayed on the screen. These 64 locations are reserved for use by the peripheral cards.

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**Table 20: Apple DOS 3.2 Zero Page Usage**

Decimal	Hex	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
		\$0	\$1	\$2	\$3	\$4	\$5	\$6	\$7	\$8	\$9	\$A	\$B	\$C	\$D	\$E	\$F
0	\$00																
16	\$10																
32	\$20																
48	\$30																
64	\$40																
80	\$50																
96	\$60																
112	\$70																
128	\$80																
144	\$90																
160	\$A0																
176	\$B0																
192	\$C0																
208	\$D0																
224	\$E0																
240	\$F0																

**Table 21: Integer BASIC Zero Page Usage**

Decimal	Hex	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
		\$0	\$1	\$2	\$3	\$4	\$5	\$6	\$7	\$8	\$9	\$A	\$B	\$C	\$D	\$E	\$F
0	\$00																
16	\$10																
32	\$20																
48	\$30																
64	\$40																
80	\$50																
96	\$60																
112	\$70																
128	\$80																
144	\$90																
160	\$A0																
176	\$B0																
192	\$C0																
208	\$D0																
224	\$E0																
240	\$F0																

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### RAM CONFIGURATION BLOCKS

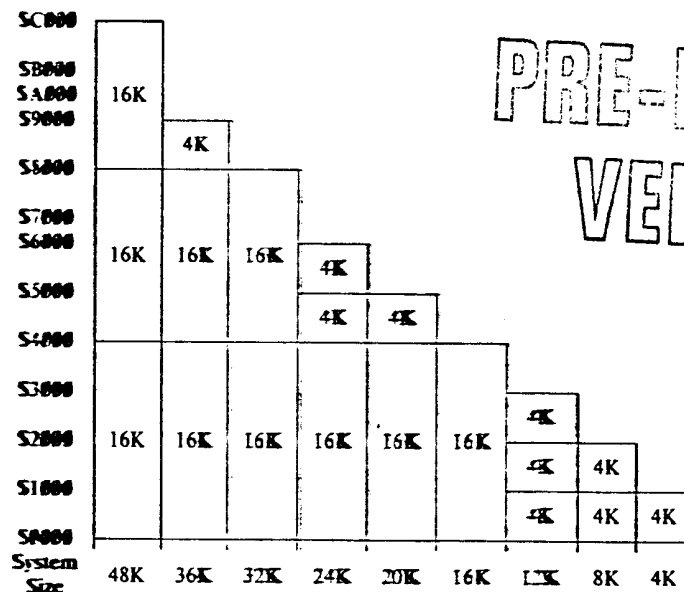
NOTE: RAM Configuration blocks are not included on Revision 7 and later Apple boards.

The Apple's RAM memory is composed of eight to 24 integrated circuits. These IC'S reside in three rows of sockets on the Apple board. Each row can hold eight chips of either the 4,096-bit (4-K) or 16,384-bit (16K) variety. The 4K RAM chips are of the Mostek "4096" family, and may be marked "MK4096" or "MCM6604". The 16K chips are of the "4116" type, and may have the denomination "MK4116" or "UPD4260". Each row must have eight of the same type of chip, although different rows may hold different types.

A row of eight 16K IC'S represents 16,384 eight-bit bytes of RAM. The leftmost IC in a row represents the lowermost (least significant) bit of every byte in that range, and the rightmost IC in a row represents the uppermost (most significant) bit of every byte. The row of RAM IC'S which is frontmost on the Apple board holds the RAM memory which begins at location 0 in the memory map; the next row back continues where the first left off.

You can tell the Apple how much memory it has, and of what type it is, by plugging Memory Configuration Blocks into three IC sockets on the left side of the Apple board. These configuration blocks are three 14-legged critters which look like big, boxy integrated circuits. But there are no chips inside of them; only three jumper wires in each. The jumper wires "strap" each row of RAM chips into a specific place on the Apple's memory map. All three configuration blocks should be strapped the same way. Apple supplies several types of standard configuration blocks for the most common system sizes.

There are nine different RAM memory configurations possible in your Apple. These nine memory sizes are made up from various combinations of 4K and 16K RAM chips in the three rows of sockets in the Apple. The nine memory configurations are:



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Of the fourteen "legs" on each controller block, the three in the upper-right corner represents the three rows of RAM chips on the Apple's main board. There should be a wire jumper from each one of these pins to another pin in the configuration block. The "other pin" corresponds to a place in the Apple's memory map where you want the RAM chips in each row to reside. The pins on the configuration block are represented thus:

4K range \$0000-\$0FFF	1	C	14	Frontmost row ("C")
4K range \$1000-\$1FFF	2		13	Middle row ("D")
4K range \$2000-\$2FFF	3		12	Backmost row ("E")
4K range \$3000-\$3FFF	4		11	No connection.
4K range \$4000-\$4FFF	5		10	16K range \$4000-\$7FFF
4K range \$5000-\$5FFF	6		9	16K range \$5000-\$7FFF
4K range \$8000-\$BFFF	7		8	16K range \$8000-\$BFFF

Figure 7. Memory Configuration Block Pinouts

If a row contains eight chips the 16K variety, then you should connect a jumper wire from the pin corresponding to that row to a pin corresponding to a 16K range of memory. Similarly, if a row contains eight 4K chips, you should connect a jumper wire from the pin that row to a pin corresponding to a 4K range of memory. You should never put 4K chips in a row strapped for 16K, or vice versa. It is also not advisable to leave a row unstrapped, or to strap two rows into the same range of memory.

You should always make sure that there is some kind of memory beginning at location 0. Your Apple's memory should be in one contiguous block, but it does not need to be. For example, if you have only three sets of 4K chips, but you want to use the primary page for the High-Resolution Graphics mode, then you would strap one row of 4K chips to the beginning of memory (4K range \$0000 through \$0FFF), and strap the other two rows to the memory range used by the High-Resolution Graphics primary page (4K ranges \$2000 through \$2FFF and \$3000 through \$3FFF). This will give you 4K bytes of RAM memory to work with, and 8K bytes of RAM to be used as a picture buffer.

There is a problem in Apples with Revision 0 boards and 20K or 24K of RAM. In these systems, the 8K range of the memory map from \$400 to \$5FFF is duplicated in the memory range \$6000 to \$7FFF, regardless of whether it contains RAM or not. So systems with only 20K or 24K of RAM would appear to have 24K or 36K, but this extra RAM would be only imaginary. This has been changed in the Revision 1 Apple II boards.

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ROM STORAGE

The Apple, in its natural state, can hold from 2K (2,048 bytes) to 12K (12,288 bytes) of Read-Only memory on its main board. This ROM memory can include the System Monitor, a couple of dialects of the BASIC language, various system and utility programs, or pre-packaged subroutines such as are included in Apple's Programmer's Aid #1 ROM.

The Apple's ROM memory resides in the top 12K (48 pages) of the memory map, beginning at location \$D000. For proper operation of the Apple, there must be some kind of ROM in the uppermost locations of memory. When you turn on the Apple's power supply, the microprocessor must have some program to execute. It goes to the top locations in the memory map for the address of this program. In the Apple, this address is stored on ROM, and is the address of a program within the same ROM. This program initializes the Apple and lets you start to use it.

Here is a map of the Apple's ROM memory, and of the programs and packages that Apple currently supports in ROM:

Table 17: ROM Organization and Usage

Page Number:		Used By:	
Decimal	Hex		
208	SD0	Programmer's Aid #1	Applesoft II BASIC
212	SD4		
216	SD8		
220	SDC	Integer BASIC	
224	SE0		
228	SE4		
232	SE8		
236	SEC		
240	SF0		
244	SF4	Utility Subroutines	
248	SF8	Monitor ROM	Autostart ROM
252	SFC		

Six 24-pin sockets on the Apple's board hold the ROM integrated circuits. Each sockets can hold one of a type 9316B 2,048-byte by 8-bit Read-Only Memory. The leftmost ROM in the Apple's board holds the upper 2K of ROM in the Apple's memory map; the rightmost ROM IC holds the ROM memory beginning at page \$D0 in the memory map. If a Rom is not present in a given socket, then the values contained in the memory range corresponding to that socket will be unpredictable.

The Apple Firmware card can disable some or all of the ROMS on the Apple board, and substitute its own ROMs in their place. When you have an Apple Firmware card installed on any slot in the Apple's board, you can disable the Apple's on-board ROM'S by flipping the card's controller switch to its UP position and pressing and releasing the RESET button, or by referencing location \$C080 (decimal 49280 or -16256). To enable the Apple's on-board ROM'S again, flip the controller switch to the DOWN position and press RESET, or reference location \$C081 (decimal 49281 or -16255).

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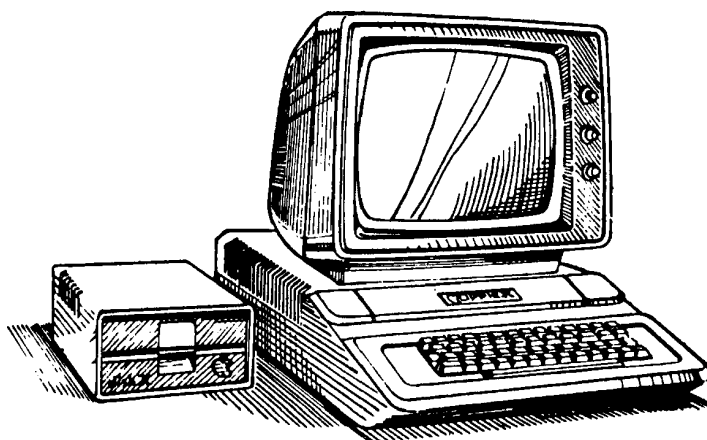


## Apple II Computer Technical Information

# APPLE II / APPLE II-PLUS LEVEL II SERVICE REFERENCE MANUAL

Pre-Release Version

## CHAPTER 9 SYSTEM MONITOR



Written by  
Apple Computer, Inc. • Level II Service Center  
1981

( This page is not part of the original service manual )

# PRE-RELEASE VERSION

## THE SYSTEM MONITOR

Buried deep within the recesses of the Apple's F8 ROM is a masterful program called the System Monitor. It acts as both a supervisor of the system and a slave to it; controls all programs and all programs use it. You can use the powerful features of the System Monitor to discover the hidden secrets in all 65,536 memory locations. From the Monitor, you may look at one, some, or all locations; you may change the contents of any location; you can write programs in Machine and Assembly languages to be executed directly by the Apple's microprocessor; you can save vast quantities of data and programs onto cassette tape and read them back in again; you can move and compare thousands of bytes of memory with a single command; and you can leave the Monitor and enter any other program or language on the Apple.

### ENTERING THE MONITOR

The Apple System Monitor program begins at location number \$FF69 (decimal 65385 or -151) in memory. To enter the Monitor, you or your BASIC program can CALL this location. The Monitor's prompt (an asterisk [\*]) will appear on the left edge of the screen, with a flashing cursor to its right. The Monitor accepts standard input lines just like any other system or language on the Apple. It will not take any action until you press RETURN. Your input lines to the Monitor may be up to 255 characters in length. When you have finished your stay in the Monitor, you can return to the language you were previously using by typing CTRL C <CR> (or, with the Apple DOS:

3DOG <CR> or RESET

### ADDRESSES AND DATA

Talking to the Monitor is somewhat like talking to any other program or language on the Apple: type a line on the keyboard, followed by a <CR>, and the Monitor will digest what you typed and act according to those instructions. You will be giving the Monitor three types of information: addresses, values, and commands. Addresses and values are given to the Monitor in hexadecimal notation uses the ten decimal digits (0-9) to represent themselves and the first six letters (A-F) to represent the numbers 10 through 15. A pair of hex digits can assume any value from 0 to 255, and a group of four hex digits can denote any number from 0 to 65,536. It so happens that any address in the Apple can be represented by four hex digits, and any value by two hex digits. This is how you tell the Monitor about addresses and values. When the Monitor is looking for an address, it will take any group of hex digits. If there are fewer than four digits in the group, it will prepend leading zeroes; if there are more than four hex digits, the Monitor will truncate the group and use only the last four hex digits. It follows the same procedure when looking for two-digit data values.

The Monitor recognizes 22 different command characters. Some of these are punctuation marks, others are upper-case letters or control characters. In the following sections, the full name of a command will appear in capital letters. The Monitor needs only the first letter of the command name. Some commands are invoked with control characters. You should note that although the Monitor recognizes and interprets these characters, a control character typed

on an input line will not appear on the screen.

The Monitor remembers the addresses of up to five locations. Two of these are special: they are the addresses of the last location whose value you inquired about, and the location which is next to have its value changed. These are called the last opened location and the next changeable location. The usefulness of these two addresses will be revealed shortly.

#### EXAMINING THE CONTENTS OF MEMORY

When you type the address of a location in memory alone on an input line to the Monitor, it will reply\* with the address you typed, a dash, a space, and the value\*\* contained in that location, thus:

```
*E000  
  
E000- 20  
*300  
  
0300- 99  
*
```

Each time the Monitor displays the value contained in a location, it remembers that location as the last opened location. For technical reasons, it also considers that location as the next changeable location.

\* In the example, your queries are in normal type and the Apple replies in BOLDFACE.

\*\* The values printed in these examples may differ from the values displayed by your Apple instructions.

#### EXAMINING SOME MORE MEMORY

If you type a period (.) on an input line to the Monitor, followed by an address, the Monitor will display a memory dump: the values contained in all locations from the last opened location to the location whose address you typed following the period. The Monitor then considers the last location displayed to be both the last opened location and the next changeable location.

```
*20  
  
0020- 00  
*.2B  
  
0021- 28 00 18 0F 0C 00 00  
0028- 18 06 D0 07  
*300  
  
0300- 99  
*.315  
  
0301- B9 00 08 0A 0A 0A 99
```

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```
0308- 00 08 C8 D0 F4 A6 2B A9
0310- 09 85 27 AD CC 03
*.32A
```

```
0316- 85 41
0318- 84 40 8A 4A 4A 4A 09
0320- C0 85 3F A9 5D 85 3E 20
0328- 43 03 20
*
```

You should notice several things about the format of a memory dump. First, the first line in the dump begins with the address of the location following the last opened location; second, all other lines begin with addresses which end alternately in zeroes and eights; and third, there are never more than eight values displayed on a single line in a memory dump. When the Monitor does a memory dump, it starts by displaying the address and value of the location following the last opened location. It then proceeds to the next successive location in memory. If the address of that location ends in an 8 or a 0, the Monitor will "cut" to a new line and display the address of that location and continue displaying values. After it has displayed the value of the location whose address you specified, it stops the memory dump and sets the address of both the last opened location, the Monitor will display the address and value of only the location following the last opened location.

You can combine the two commands (opening and dumping) into one operation by concatenating the second to the first; that is, type the first address, followed by a period and the second address. This two-addresses-separated-by-a-period form is called a memory range.

```
*300.32F
```

```
0300- 99 B9 00 09 0A 0A 0A 99
0308- 00 08 C8 D0 F4 A6 2B A9
0310- 09 85 27 AD CC 03 85 41
0318- 84 40 8A 4A 4A 4A 09
0320- C0 85 3F A9 5D 85 3E 20
0328- 43 03 20 46 03 A5 3D 4D
*30.40
```

```
0030- AA 00 FF AA 05 C2 05 C2
0038- 1B FD D0 03 3C 00 40 00
0040- 30
*E015.E025
```

```
E015- 4C ED ED
E018- A9 20 C5 24 B0 0C A9 8D
E020- A0 07 S0 ED FD A9
*
```

## EXAMINING STILL MORE MEMORY

A single press of the <CR> key will cause the Monitor to respond with one line of memory dump; that is, a memory dump from the location following the last

opened location to the next eight-location "cut". Once again, the last location displayed is considered the last opened and next changeable location.

\*5

0005- 00  
\*  
00 00  
\*  
0008- 00 00 00 00 00 00 00 00  
\*32

0032- FF  
\*  
AA 00 C2 05 C2  
\*  
0038- 1B FD D0 03 3C 00 3F 00  
\*

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#### CHANGING THE CONTENTS OF A LOCATION

You've heard all about the "next changeable location"; now you're going to use it. Type a colon followed by a value.

\*0

0000- 00  
\*:5F

Presto! The contents of the next changeable location have just been changed to the value you typed. Check this by examining that location again:

\*0

0000- 5F  
\*

You can also combine opening and changing into one operation:

\*302:42

\*302

0302- 42  
\*

When you change the contents of a location, the old value which was contained in that location disappears, never to be seen again. The new value will stick around until it is replaced by another hexadecimal value.

## CHANGING THE CONTENTS OF CONSECUTIVE LOCATIONS

You don't have to type an address, a colon, a value, and press <CR> for each and every location you wish to change. The Monitor will allow you to change the values of up to eighty-five locations at a time by typing only the initial address and colon, and then all the values separated by spaces. The Monitor will duly file the consecutive values in consecutive locations, starting at the next changeable location. After it has processed the string of values, it will assume that the location following the last changed location is the next changeable location. Thus, you can continue changing consecutive locations without breaking stride on the next input line by typing another colon and more values.

```
*300:69 01 20 ED FD 4C 0 3
```

```
*300
```

```
0300-69
```

```
*<CR>
```

```
01 20 ED FD 4C 00 03
```

```
*10:0 1 2 3
```

```
*:4 5 6 7
```

```
*10.17
```

```
0010- 00 01 02 03 04 05 06 07
```

```
*
```

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## MOVING A RANGE OF MEMORY

You can treat a range of memory (specified by two addresses separated by a period) as an entity unto itself and move it from one place to another in memory by using the Monitor's MOVE command. In order to move a range of memory from one place to another, the Monitor must be told both where the range is situated in memory and where it is to be moved. You give this information to the Monitor in three parts: the address of the destination of the range, the address of the first location in the range proper, and the address of the last location in the range. You specify the starting and ending addresses of the range in the normal fashion, by separating them with a period. You indicate that this range is to be placed somewhere else by separating the range and the destination address with a left caret (<). Finally, you tell the Monitor that you want to move the range to the destination by typing the letter M for "MOVE". The final command looks like this:

```
{destination} < {start}.{end} M
```

When you type this line to the Monitor, of course, the words in curly brackets should be replaced by hexadecimal address and the spaces should be omitted. Here are some real examples of memory moves:

```
*0.F
```

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0000- 5F 00 05 07 00 00 00 00  
0008- 00 00 00 00 00 00 00 00  
\*300:A9 8D 20 ED FD A9 45 20 DA FD 4C 00 03

\*300.30C

0300- A9 8D 20 ED FD A9 45 20  
0308- DA FD 4C 00 03  
\*<300.30CM

\*0.C

0000- A9 8D 20 ED FD A9 45 20  
0009- DA FD 4C 00 03  
\*310<8.AM

\*310.312

0310- DA FD 4C  
\*2<7.9M

0000- A9 8D 20 DA FD A9 45 20  
0008-DA FD 4C 00 03  
\*

The Monitor simply makes a copy of the indicated range and moves it to the specified destination. The original range is left undisturbed. The Monitor remembers the last location in the original range as the last opened location, and the first location in the original range as the next changeable location. If the second address in the range specification is less than the first, then only one value (that of the first location in the range) will be moved.

If the destination address of the MOVE command is inside the original range, then strange and (sometimes) wonderful things happen: the locations between the beginning of the range and the destination are treated as a sub-range and the values in this sub-range are replicated throughout the original range. See "Special Tricks", for an interesting application of this feature.

#### COMPARING TWO RANGES OF MEMORY

You can use the Monitor to compare two ranges of memory using much the same format as you use to move a range of memory from one place to another. In fact, the VERIFY command can be used immediately after a MOVE to make sure that the move was successful.

The VERIFY command, like the MOVE command, needs a range and a destination. In shorthand:

{destination} < {start}.{end} V

The Monitor compares the range specified with the range beginning at the destination address. If there is any discrepancy, the Monitor displays the address at which the difference was found and the two offending values.

```
*0:D7 F2 E9 F4 F4 E5 EE A0 E2 F9 A0 C3 C4 C5
```

```
*300<0.DM
```

```
*300<0.DV
```

```
*6:E4
```

```
*300<0.DV
```

```
0006-E4 (EE)
```

```
*
```

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Notice that if the VERIFY command finds a discrepancy, it displays the address of the location in the original range whose value differs from its counterpart in the destination range. If there is no discrepancy, VERIFY displays nothing. It leaves both ranges unchanged. The last opened and next changeable locations are set just as in the MOVE command. As before, if the ending address of the ranges will be compared. VERIFY also does unusual things if the destination is within the original range; see "Special Tricks".

#### SAVING A RANGE OF MEMORY ON TAPE

The Monitor has two special commands which allow you to save a range of memory onto cassette tape and recall it again for later use. The first of these two commands, WRITE, lets you save the contents of one to 65,536 memory locations on standard cassette tape.

To save a range of memory to tape, give the Monitor the starting and ending addresses of the range, followed by the letter W (for WRITE):

```
{start}.{end} W
```

To get an accurate recording, you should put the tape recorder in record mode before you press <CR> on the input line. Let the tape run a few seconds, then press <CR>. The Monitor will write a ten-second "leader" tone onto the tape, followed by the data. When the Monitor is finished, it will sound a 'beep!' and give you another prompt. You should then rewind the tape, and label the tape with something intelligible about the memory range that's on the the tape and what it's supposed to be.

```
*0:FF FF AD 30 C0 88 D0 04 C6 01 F0 08
```

```
*:CA D0 F6 A6 00 4C 02 00 60
```

```
*0.14
```

```
0000- FF FF AD 30 C0 88 D0 04
```

```
0008- C6 0A F0 08 CA D0 F6 A6
```

```
0010- 00 4C 02 00 60
```

```
*0.14W
```

```
*
```



CREATING AND RUNNING MACHINE LANGUAGE PROGRAMS

Machine language is certainly the most efficient language on the Apple, albeit the least pleasant in which to code. The Monitor has special facilities for those of you who are determined to use machine language to simplify creating, writing, and debugging machine language programs.

You can write a machine language program, take the hexadecimal values for the opcodes and operands, and store them in memory using the commands covered above. You can get a hexadecimal dump of your program, move it around in memory, or save it to tape and recall it again simply by using the commands you've already learned. The most important command, however, when dealing with machine language programs is the GO command. When you open a location from the Monitor and type the letter G, the Monitor will cause the 6502 microprocessor to start executing the machine language program which begins at the last opened location. The Monitor treats this program as a subroutine: when it's finished, all it need do is execute an RTS (return from subroutine) instruction and control will be transferred back to the Monitor.

Your machine language programs can call many subroutines in the Monitor to do various things. Here is an example of loading and running a machine language program to display the letters A through Z:

```
*300:A9 C1 20 ED FD 18 69 1 C9 DB D0 F6 60
*300.30C
0300- A9 C1 20 ED FD 18 69 01
0308- C9 DB D0 F6 60
*300G
ABCDEFGHIJKLMNQRSTUWXYZ
*
```

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(The instruction set of the Apple's 6502 microprocessor is listed in Appendix)

Now, straight hexadecimal code isn't the easiest thing in the world to read or debug. With this in mind, the creators of the Apple's Monitor neatly included a command to list machine language programs in assembly language form. This means that instead of having one, two, or three bytes of unformatted hexadecimal gibberish to comprehend for each instruction. The LIST command to start at the specified location and display a screenfull (20 lines) of instructions:

```
*300L
0300-  A9 C1          LDA    #SC1
0302-  20 ED FD      JSR    $$FDED
0305-  18            CLC
0306-  69 01         ADC    #01
0308-  C9 DB         CMP    #DB
030A-  D0 F6         BNE   $0302
030C-  60           RTS
030D-  00           BRK
030E-  00           BRK
```

```

030F- 00      BRK
0310- 00      BRK
0311- 00      BRK
0312- 00      BRK
0313- 00      BRK
0314- 00      BRK
0315- 00      BRK
0316- 00      BRK
0317- 00      BRK
0318- 00      BRK
0319- 00      BRK
*
```

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Recognize those first few lines? They're the assembly language form of the program you typed a page or so ago. The rest of the lines (the BRK instructions) are just there to fill up the screen. The address that you specify is remembered by the Monitor, but not in one of the ways explained before. It's put in the Program Counter, which is used solely to point to locations within programs. After a LIST command, the Program Counter is set to point to the location immediately following the last location displayed on the screen, so that if you do another LIST command it will continue with another screenfull of instructions, starting where the first screen left off.

#### THE MINI-ASSEMBLER

There is another program within the Monitor\* which allows you to type programs into the Apple in the same assembly format which the LIST command displays. This program is called the Apple Mini-Assembler. It is a "mini-assembler because it cannot understand symbolic labels, something that a full-blown assembler must do. To run the Mini-Assembler, type:

```
*F666G
```

```
!
```

You are now in the Mini-Assembler. The exclamation point (!) is the prompt character. During your stay in the Mini-Assembler, you can execute any Monitor command by preceding it with a dollar sign (\$). Aside from that, the Mini-Assembler has an instruction set and syntax all its own.

The Mini-Assembler remembers one address, that of the Program Counter. Before you start to enter a program, you must set the Program Counter to point to the location where you want your program to go. Do this by typing the address followed by a colon. Follow this with the mnemonic for the first instruction in your program, followed by a space. Now type the operand of the instruction (Formats for operands are listed on page 66). Now press <CR>. The Mini-Assembler converts the line you typed into hexadecimal, stores it in memory beginning at the location of the Program Counter, and then disassembles it again and displays the disassembled line on top of your input line. It then poses another prompt on the next line. Now it's ready to accept the second instruction in your program. To tell it that you want the next instruction to follow the first don't type and address or a colon, but only a space, followed by the next instruction's mnemonic and operand. Press <CR>. It assembles that line and

waits for another.

If the line you type has an error in it, the Mini-Assembler will beep loudly and display a circumflex (^) under or near the offending character in the input line. Most common errors are the result of typographical mistakes: misspelled mnemonics, missing parentheses, etc. The Mini-Assembler also will reject the input line if you forget the space before or after a mnemonic or include an extraneous character in a hexadecimal value or address. If the destination address of a branch instruction is out of the range of the brranch (more than 127 locations distant from the address of the instruction), the Mini-Assembler will also flag this as an error.

```

!300-LDX #02

0300-  A2 02          LDX    #$02
! LDA $0,X

0302-  B5 00          LDA    $00,X
! STA $10,X

0304-  95 10          STA    $10,X
! DEX

0306-  CA             DEX
! STA $D030

0307-  8D 30 C0       STA    $C030
! BPL $302

030A-  10 F6          BPL    $0302
! BRK

030C-  00             BRK
!
    
```

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To exit the Mini-Assembler and re:enter the Monitor, either press <CR> or type the Monitor command (preceded by a dollar sign) FF69G:

```
!$FF69G
```

\*

Your assembly language program is stored in memory. You can look at it again with the LIST command:

```

0300-  A2 02          LDX    #$02
0302-  B5 00          LDA    $00,X
0304-  95 10          STA    $10,X
0306-  CA             DEX
0307-  8D 30 C0       STA    $C030
030A-  10 F6          BPL    $0302
030C-  00             BRK
030D-  00             BRK
030E-  00             BRK
    
```

```

030F- 00          BRK
0310- 00          BRK
0311- 00          BRK
0312- 00          BRK
0313- 00          BRK
0314- 00          BRK
0315- 00          BRK
0316- 00          BRK
0317- 00          BRK
0318- 00          BRK
0319- 00          BRK
*
```

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-----  
\* The Mini-Assembler does not actually reside in the Monitor ROM, but is part of the Integer BASIC ROM set. Thus, it is not available on Apple II Plus systems or while Firmware Applesoft II is in use.

#### DEBUGGING PROGRAMS

As put so concisely by Lubarsky\*, "There's always one more bug." Don't worry, the Monitor provides facilities for stepping through ornery programs to find that one last bug. The Monitor's STEP\*\* command decodes, displays, and executes one instruction at a time, and the TRACE\*\* command steps quickly through a program, stopping when a BRK instruction is executed.

Each STEP command causes the Monitor to execute the instruction in memory pointed to by the Program Counter. The instruction is displayed in its disassembled form, then executed. The contents of the 6502's internal registers are displayed after the instruction is executed. After execution, the Program Counter is bumped up to point to the next instruction in the program.

Here's what happens when you STEP through the program you entered using the Mini-Assembler, above:

```

*300S
0300-  A2 02          LDX    #$02
      A=0A X=02 Y=D8 P=30 S=F8
*S
0302-  B5 00          LDA    $00,X
      A=0C X=02 Y=D8 P=30 S=F8
*S
0304-  95 10          STA    $10,X
      A=0C X=02 Y=D8 P=30 S=F8
*12
0012- 0C
*S
0306-  CA          DEX
      A=0C X=01 Y=D8 P=30 S=F8
```

```

*S
0307- 8D D0 C0      STA      $C030
      A=0C X=01 Y=D8 P=30 S=F8
*S
030A- 10 F6        BPL      $0302
      A=0C X=01 Y=D8 P=30 S=F8
*S
0302- B5 00        LDA      $00,X
      A=0B X=01 Y=D8 P=30 S=F8
*S
0304- 95 10        STA      $10,X
      A=0B X=01 Y=D8 P=30 S=F8
*

```

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Notice that after the third instruction was executed, we examined the contents of location 12. They were as we expected, and so we continued stepping. The Monitor keeps the Program Counter and the last opened address separate from one another, so that you can examine or change the contents of memory while you are stepping through your program.

The TRACE command is just an infinite STEPPER. It will stop TRACEing the execution of a program only when you push RESET or it encounters a BRK instruction in the program. If the TRACE encounters the end of a program which returns to the Monitor via an RTS instruction, the TRACEing will run off into never-never land and must be stopped with the RESET button.

```

*T
0306- CA          DEX
      A=0B X=00 Y=D8 P=32 S=F8
0307- 8D 30 C0    STA      $C030
      A=0B X=00 Y=D8 P=32 S=F8
030A- 10 F6        BPL      $0302
      A=0B X=00 Y=D8 P=32 S=F8
0302- B5 00        LDA      $00,X
      A=0A X=00 Y=D8 P=32 S=F8
0304- 95 10        STA      $10,X
      A=02 X=00 Y=D8 P=32 S=F8
0306- CA          DEX
      A=0A X=FF Y=D8 P=B0 S=F8
0307 8D 30 C0    STA      $C030
      A=0A X=FF Y=D8 P=B0 S=F8
030A- 10 F6        BPL      $0302

```

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```
A=0A X=FF Y=D8 P=B0 S=F8
030C- 00 BRK
030C- A=0A X=FF Y=D8 P=B0 S=F8
*
```

\* In Murphy's Law, and Other Reasons why Things Go Wrong, edited by Arthur Bloch. Price/Stern/Sloane 197/.

\*\* The STEP and TRACE commands are not available on Apples with the Autostart ROM.

#### EXAMINING AND CHANGING REGISTERS

As you saw above, the STEP and TRACE commands displayed the contents of the 6502's internal registers after each instruction. You can examine these registers at will or pre-set them when you TRACE, STEP, or GO a machine language program.

The Monitor reserves five locations in memory for the five 6502 registers: A,X, Y,P (processor status register), and S (stack pointer). The Monitor's EXAMINE command, invoked by a <CE), tells the Monitor to display the contents of these locations on the screen, and lets the location which holds the 6502's A-register be the next changeable location. If you want to change the values in these locations, just type a colon and the values separated by spaces. Next time you give the Monitor a GO, STEP, or TRACE command, the Monitor will load these five locations into their proper registers inside the 64502 before it executes the first instruction in your program.

\*CTRL E

```
A=0A X=FF Y=D8 P=B0 S=F8
*:BO 02
```

\*CTRL E

```
A=B0 X=02 Y=D8 P=B0 S=F8
*306S
```

```
0306- CA DEX
A=B0 X=0A Y=D8 P=30 S=F8
*S
```

```
030/- 8D 30 C0 STA $C030
A=B0 X=01 Y=D8 P=30 S=F8
*S
```

```
030A- 10 F6 BPL $0302
A=B0 X=01 Y=D8 P=30 S=F8
```

\*

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## MISCELLANEOUS MONITOR COMMANDS

You can control the setting of the Inverse/Normal location used by the COUT subroutine (see ~~Chapter 3~~ <sup>Chapter 3</sup>) from the Monitor so that all of the Monitor's output will be in Inverse video. The INVERSE command does this nicely. Input lines are still displayed in Normal mode, however. To return the Monitor's output to Normal mode, use the NORMAL command.

\*O.F

```
0000- 0A 0B 0C 0D 0E 0F D0 04
0008- C6 01 F0 08 CA D0 F6 A6
*1
```

\*O.F

```
0000- 0A 0B 0C 0D 0E 0F D0 04
0008- C6 01 F0 08 CA D0 F6 A6
*N
```

\*O.F

```
0000- 0A 0B 0C 0D 0E 0F D0 04
0008- C6 01 F0 08 CA D0 F6 A6
*
```

The BASIC command, invoked by a CTRL B, lets you leave the Monitor and enter the language installed in ROM on your Apple, usually either Apple Integer or Applesoft II BASIC. Any program or variables that you had previously in BASIC will be lost. If you've left BASIC for the Monitor and you want to re-enter BASIC with your program and variables intact, use the CTRL C (CONTINUE BASIC) command. If you have the Apple Disk Operating System (DOS) active, the ^3DOG command will return you to the language you were using, with your program and variables intact.

The PRINTER command, activated by a CTRL P, diverts all output normally destined for the screen to an Apple Intelligent Interface in a given slot in the Apple's backplane. The slot number should be from 1 to 7, and there should be an interface card in the given slot, or you will lose control of your Apple and your program and variables may be lost. The format for the command is:

```
{slot number} CTRL P
```

A PRINTER command to slot number 0 will reset the flow of printed output back to the Apple's video screen.

The KEYBOARD command similarly substitutes the device in a given backplane slot for the Apple's keyboard. For details on how these commands and their BASIC counterparts PR# and IN# work, please refer to "CSW and KSW Switches". The format for the KEYBOARD command is:

```
{slot number} CTRL K
```

The Monitor will also perform simple hexadecimal addition and subtraction.  
Just type a line in the format:

```
{value} + {value}
{value} - {value}
```

The Apple will perform the arithmetic and display the result:

```
*20+13
=33
*4A-C
=3E
*FF+4
=03
*3-4
=FF
*
```

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#### SPECIAL TRICKS WITH THE MONITOR

You can put as many Monitor commands on a single line as you like, as long as you separate them with spaces and the total number of characters in the line is less than 254. You can intermix any and all commands freely, except the STORE (:) command. Since the Monitor takes all values following a colon and places them in consecutive memory locations, the last value in a STORE must be followed by a letter command before another address is encountered. The NORMAL command makes a good separator; it usually has no effect and can be used anywhere.

```
*300.307 300:18 69 1 N 300.302 300S S
0300- 00 00 00 00 00 00 00 00
0300- 18 69 01
0300- 18 CLC
A=04 X=01 Y=D8 P=30 S=F8
0301- 69 01 ADC #$01
A=05 X=01 Y=D8 P=30 S=F8
*
```

Single-letter commands such as LCS,I, and N need not be separated by spaces.

If the Monitor encounters a character in the input line which it does not recognize as either a hexadecimal digit or a valid command character, it will execute all commands on the input line up to that character, and then grind to a halt with a noisy beep, ignoring the remainder of the input line.

The MOVE command can be used to replicate a pattern of values throughout a range in memory.

To do this, first store the pattern in its first position in the range:

```
*300:11 22 33
*
```

Remember the number of values in the pattern: in this case, 3. Then use this special arrangement of the MOVE command:

```
{start + number} < {start} . {end - number} M
```

This MOVE command will first replicate the pattern at the locations immediately following the original pattern, then re-replicate that pattern following itself and so on until it fills the entire range.

```
*303<300.32DM
```

```
*300.32F
```

```
0300- 11 22 33 11 22 33 11 22
0308- 33 11 22 33 11 22 33 11
0310- 22 33 11 22 33 11 22 33
0318- 11 22 33 11 22 33 11 22
0320- 33 11 22 33 11 22 33 11
0328- 22 33 11 22 33 11 22 33
*
```

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A similiar trick can be done with the VERIFY command to check whether a pattern repeats itself through memory. This is especially useful to verify that a given range of memory locations all contain the same value:

```
*300:0
```

```
*301<300.31FM
```

```
*301<300.31FV
```

```
*304:02
```

```
*301<300.31FV
```

```
0303-00 (02)
```

```
0304-02 (00)
```

```
*
```

You can create a command line which will repeat all or part of itself indefinitely by beginning the part of the command line which is to be repeated with a letter command, such as N, and ending it with the sequence 34:n, where n is a hexadecimal number specifying the character position of the command which begins the loop; for the first character in the line, n=0. The value for n must be followed with a space in order for the loop to work properly.

```
*N 300 302 34:0
```

```
0300- 11
0302- 33
0300- 11
0302- 33
0300- 11
```

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```
0302- 33
0300- 11
0302- 33
0300- 11
0302- 33
0300- 11
0302- 33
030
*
```

The only way to stop a loop like this is to press RESET.

#### CREATING YOUR OWN COMMANDS

The USER (CTRL Y) command, when encountered in the input line, forces the Monitor to jump to location number \$3F8 in memory. You can put your own JMP instruction in this location which will jump to your own program. Your program can then either examine the Monitor's registers and pointers or the input line itself. For example, here is a program which will make the CTRL Y command act as a "comment" indicator: everything on the input line following the CTRL Y will be displayed and ignored.

```
*F666G

!300:LDY $34

0300-  A4 34          LDY    #34
! LDA 200,Y

0302-  B9 00 02      LDA    $0200,Y
! JSR FDED

0305-  20 ED FD      JSR    $FDED
! INY

0308-  C8            INY
! CMP #$8D

0309-  C9 8D          CMP    #$8D
! BNE 302

030B-  D0 F5          BNE    $0302
! JMP $FF69

030D-  4C 69 FF      JMP    $FF69
!3F8:JMP $300

03F8-  4C 00 03      JMP    $0300
!$FF69G

*CTRL Y THIS IS A TEST.
THIS IS A TEST.
```

SPECIAL TRICKS WITH THE MONITOR

You can put as many Monitor commands on a single line as you like, as long as you separate them with spaces and the total number of characters in the line is less than 254. You can intermix any and all commands freely, except the STORE (:) command. Since the Monitor takes all values following a colon and places them in consecutive memory locations, the last value in a STORE must be followed by a letter command before another address is encountered. The NORMAL command makes a good separator; it usually has no effect and can be used anywhere.

```
*300.307 300:18 69 1 N 300.302 300S S
0300- 00 00 00 00 00 00 00 00
0300- 18 69 01
0300- 18 CLC
A=04 X=01 Y=D8 P=30 S=F8
0301- 69 01 ADC #01
A=05 X=01 Y=D8 P=30 S=F8
*
```

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Single-letter commands such as LCS,I, and N need not be separated by spaces.

If the Monitor encounters a character in the input line which it does not recognize as either a hexadecimal digit or a valid command character, it will execute all commands on the input line up to that character, and then grind to a halt with a noisy beep, ignoring the remainder of the input line.

The MOVE command can be used to replicate a pattern of values throughout a range in memory.

To do this, first store the pattern in its first position in the range:

```
*300:11 22 33
*
```

Remember the number of values in the pattern: in this case, 3. Then use this special arrangement of the MOVE command:

```
{start + number} < {start} . {end - number} M
```

This MOVE command will first replicate the pattern at the locations immediately following the original pattern, then re-replicate that pattern following itself and so on until it fills the entire range.

```
*303<300.32DM
*300.32F
0300- 11 22 33 11 22 33 11 22
0308- 33 11 22 33 11 22 33 11
0310- 22 33 11 22 33 11 22 33
0318- 11 22 33 11 22 33 11 22
```

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```
0320- 33 11 22 33 11 22 33 11
0328- 22 33 11 22 33 11 22 33
*
```

A similar trick can be done with the VERIFY command to check whether a pattern repeats itself through memory. This is especially useful to verify that a given range of memory locations all contain the same value:

```
*300:0
*301<300.31FM
*301<300.31FV
*304:02
*301<300.31FV
0303-00 (02)
0304-02 (00)
*
```

You can create a command line which will repeat all or part of itself indefinitely by beginning the part of the command line which is to be repeated with a letter command, such as N, and ending it with the sequence 34:n, where n is a hexadecimal number specifying the character position of the command which begins the loop; for the first character in the line, n=0. The value for n must be followed with a space in order for the loop to work properly.

```
*N 300 302 34:0
0300- 11
0302- 33
0300- 11
0302- 33
0300- 11
0302- 33
0300- 11
0302- 33
0300- 11
0302- 33
0300- 11
0302- 33
0300- 11
0302- 33
030
*
```

The only way to stop a loop like this is to press RESET.

## CREATING YOUR OWN COMMANDS

The USER (CTRL Y) command, when encountered in the input line, forces the Monitor to jump to location number \$3F8 in memory. You can put your own JMP instruction in this location which will jump to your own program. Your pro-

gram can then either examine the Monitor's registers and pointers or the input line itself. For example, here is a program which will make the CTRL Y command act as a "comment" indicator: everything on the input line following the CTRL Y will be displayed and ignored.

\*F666G

!300:LDY \$34

0300- A4 34 LDY #34  
! LDA 200,Y

0302- B9 00 02 LDA \$0200,Y  
! JSR FDED

0305- 20 ED FD JSR \$FDED  
! INY

0308- C8 INY  
! CMP #\$8D

0309- C9 8D CMP #\$8D  
! BNE 302

030B- D0 F5 BNE \$0302  
! JMP \$FF69

030D- 4C 69 FF JMP \$FF69  
!3F8:JMP \$300

03F8- 4C 00 03 JMP \$0300  
!\$FF69G

\*CTRL Y THIS IS A TEST.  
THIS IS A TEST.

\*

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## SUMMARY OF MONITOR COMMANDS

### Summary of Monitor Commands.

#### Examining Memory.

{adrs}	Examines the value contained in one location.
{adrs1}.{adrs2}	Displays the values contained in all locations between {adrs1} and {adrs2}.
<b>RETURN</b>	Displays the values in up to eight locations following the last opened location.

#### Changing the Contents of Memory.

{adrs}:{val} {val} ...	Stores the values in consecutive memory locations starting at {adrs}.
:{val} {val} ...	Stores values in memory starting at the next changeable location.

#### Moving and Comparing.

{dest}<{start}.{end}M	Copies the values in the range {start}.{end} into the range beginning at {dest}.
{dest}<{start}.{end}V	Compares the values in the range {start}.{end} to those in the range beginning at {dest}.

#### Saving and Loading via Tape.

{start}.{end}W	Writes the values in the memory range {start}.{end} onto tape, preceded by a ten-second leader.
{start}.{end}R	Reads values from tape, storing them in memory beginning at {start} and stopping at {end}. Prints "ERR" if an error occurs.

#### Running and Listing Programs.

{adrs}G	Transfers control to the machine language program beginning at {adrs}.
{adrs}L	Disassembles and displays 20 instructions, starting at {adrs}. Subsequent L's will display 20 more instructions each.

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Summary of Monitor Commands.

The Mini-Assembler

**^666G** Invoke the Mini-Assembler.\*

**S{command}** Execute a Monitor command from the Mini-Assembler.

**^FF69G** Leave the Mini-Assembler.

**{adr} S** Disassemble, display, and execute the instruction at {adr}, and display the contents of the 6502's internal registers. Subsequent S's will display and execute successive instructions.\*\*

**{adr} T** Step infinitely. The TRACE command stops only when it executes a BRK instruction or when you press **[RESET]**.\*

**[CTRL E]** Display the contents of the 6502's registers.

Miscellaneous.

**I** Set Inverse display mode.

**N** Set Normal display mode.

**[CTRL B]** Enter the language currently installed in the Apple's ROM.

**[CTRL C]** Reenter the language currently installed in the Apple's ROM.

**{val} + {val}** Add the two values and print the result.

**{val} - {val}** Subtract the second value from the first and print the result.

**{slot} [CTRL P]** Divert output to the device whose interface card is in slot number {slot}. If {slot}=0, then route output to the Apple's screen.

**{slot} [CTRL K]** Accept input from the device whose interface card is in slot number {slot}. If {slot}=0, then accept input from the Apple's keyboard.

**[CTRL Y]** Jump to the machine language subroutine at location \$3F8.

\* Not available in the Apple II Plus.  
 \*\* Not available in the Autostart ROM.

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## SOME USEFUL MONITOR SUBROUTINES

Here is a list of some useful subroutines in the Apple's Monitor and Autostart ROMs. To use these subroutines from machine language programs, load the proper memory locations or 6502 registers as required by the subroutine and execute a JSR to the subroutine's starting address. It will perform the function and return with the 6502's registers set as described.

**\$FDED COUT Output a character**

COUT is the standard character output subroutine. The character to be output should be in the accumulator. COUT calls the current character output subroutine whose address is stored in CSW (locations \$36 and \$37), usually COUT1 (see below).

**\$FDF0 COUT1 Output to screen**

COUT1 displays the character in the accumulator on the Apple's screen at the current output cursor position and advances the output cursor. It places the character using the setting of the Normal/Inverse location. It handles the control characters RETURN, linefeed, and bell. It returns with all registers intact.

**\$FE80 SETINV Set Inverse mode**

Sets Inverse video mode for COUT1. All output characters will be displayed as black dots on a white background. The Y register is set to \$3F, all others are unchanged.

**\$FE84 SETNORM Set Normal mode**

Sets Normal video mode for COUT1. All output characters will be displayed as white dots on a black background. The Y register is set to \$FF, all others are unchanged.

**\$FD8E CROUT Generate a RETURN**

CROUT sends a RETURN character to the current output device.

**\$FD8B CROUT1 RETURN with clear**

CROUT1 clears the screen from the current cursor position to the edge of the text window, then calls CROUT.

**\$FD8A PRBYTE Print a hexadecimal byte**

This subroutine outputs the contents of the accumulator in hexadecimal on the current output device. The contents of the accumulator are scrambled.

**\$FDE3 PRHEX Print a hexadecimal digit**

This subroutine outputs the lower nybble of the accumulator as a single hexadecimal digit. The contents of the accumulator are scrambled.

**\$F941 PRNTAX Print A and X in hexadecimal**

This outputs the contents of the A and X registers as a four-digit hexadecimal value. The accumulator contains the first byte output, the X register contains the second. The contents of the

accumulator are usually scrambled.

**SF948 PRBLNK Print 3 spaces**

Outputs three blank spaces to the standard output device. Upon exit, the accumulator usually contains SA0, the X register contains 0.

**SF94A PRBL2 Print many blank spaces**

This subroutine outputs from 1 to 256 blanks to the standard output device. Upon entry, the X register should contain the number of blanks to be output. If X=500, then PRBL2 will output 256 blanks.

**SFF3A BELL Output a "bell" character**

This subroutine sends a bell (CTRL G) character to the current output device. It leaves the accumulator holding \$87.

**SFBDD BELL1 Beep the Apple's speaker**

This subroutine beeps the Apple's speaker for .1 second at 1KHZ. It scrambles the A and X registers.

**SFD#C RDKEY Get an input character**

This is the standard character input subroutine. It places a flashing input cursor on the screen at the position of the output cursor and jumps to the current input subroutine whose address is stored in KSW (locations \$38 and \$39), usually KEYIN (see below).

**SFD35 RDCHAR Get an input character or ESC code**

RDCHAR is an alternate input subroutine which gets characters from the standard input, but also interprets the eleven escape codes (see page 34).

**SFD1B KEYIN Read the Apple's keyboard**

This is the keyboard input subroutine. It reads the Apple's keyboard, waits for a keypress, and randomizes the random number seed (see page 32). When it gets a keypress, it removes the flashing cursor and returns with the keycode in the accumulator.

**SFD6A GETLN Get an input line with prompt**

GETLN is the subroutine which gathers input lines (see page 33). Your programs can call GETLN with the proper prompt character in location \$33; GETLN will return with the input line in the input buffer (beginning at location \$200) and the X register holding the length of the input line.

**SFD67 GETLNZ Get an input line**

GETLNZ is an alternate entry point for GETLN which issues a carriage return to the standard output before falling into GETLN (see above).

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**SFD6F GETLN1 Get an input line, no prompt**

GETLN1 is an alternate entry point for GETLN which does not issue a prompt before it gathers the input line. If, however, the user cancels the input line, either with too many backspaces or with a **CTRL X**, then GETLN1 will issue the contents of location \$33 as a prompt when it gets another line.

**SFCA8 WAIT Delay**

This subroutine delays for a specific amount of time, then returns to the program which called it. The amount of delay is specified by the contents of the accumulator. With A the contents of the accumulator, the delay is  $\frac{1}{2}(26+27A+5A^2)$  microseconds. WAIT returns with the A register zeroed and the X and Y registers undisturbed.

**SF864 SETCOL Set Low-Res Graphics color**

This subroutine sets the color used for plotting on the Low-Res screen to the color passed in the accumulator. See page 17 for a table of Low-Res colors.

**SF85F NEXTCOL Increment color by 3**

This adds 3 to the current color used for Low-Res Graphics.

**SF800 PLOT Plot a block on the Low-Res screen**

This subroutine plots a single block on the Low-Res screen of the prespecified color. The block's vertical position is passed in the accumulator, its horizontal position in the Y register. PLOT returns with the accumulator scrambled, but X and Y unmolested.

**SF819 HLINE Draw a horizontal line of blocks**

This subroutine draws a horizontal line of blocks of the predetermined color on the Low-Res screen. You should call HLINE with the vertical coordinate of the line in the accumulator, the leftmost horizontal coordinate in the Y register, and the rightmost horizontal coordinate in location \$2C. HLINE returns with A and Y scrambled, X intact.

**SF828 VLINE Draw a vertical line of blocks**

This subroutine draws a vertical line of blocks of the predetermined color on the Low-Res screen. You should call VLINE with the horizontal coordinate of the line in the Y register, the top vertical coordinate in the accumulator, and the bottom vertical coordinate in location \$2D. VLINE will return with the accumulator scrambled.

**SF832 CLRSCR Clear the entire Low-Res screen**

CLRSCR clears the entire Low-resolution Graphics screen. If you call CLRSCR while the video display is in Text mode, it will fill the screen with inverse-mode "@" characters. CLRSCR destroys the contents of A and Y.

**SF836 CLRTOP Clear the top of the Low-Res screen**

CLRTOP is the same as CLRSCR (above), except that it clears only the top 40 rows of the screen.

**SF871      SCRN      Read the Low-Res screen**

This subroutine returns the color of a single block on the Low-Res screen. Call it as you would call PLOT (above). The color of the block will be returned in the accumulator. No other registers are changed.

**SFB1E      PREAD      Read a Game Controller**

PREAD will return a number which represents the position of a game controller. You should pass the number of the game controller (0 to 3) in the X register. If this number is not valid, strange things may happen. PREAD returns with a number from \$00 to \$FF in the Y register. The accumulator is scrambled.

**SFF2D      PRERR      Print "ERR"**

Sends the word "ERR", followed by a bell character, to the standard output device. The accumulator is scrambled.

**SFF4A      IOSAVE      Save all registers**

The contents of the 6502's internal registers are saved in locations \$45 through \$49 in the order A-X-Y-P-S. The contents of A and X are changed; the decimal mode is cleared.

**SFF3F      IOREST      Restore all registers**

The contents of the 6502's internal registers are loaded from locations \$45 through \$49.

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## MONITOR SPECIAL LOCATIONS

**Table 14: Page Three Monitor Locations**

Address:		Use:	
Decimal	Hex	Monitor ROM	Autostart ROM
1008	\$3F0	None.	Holds the address of the subroutine which handles machine language "BRK" requests (normally \$FA59).
1009	\$3F1		
1010	\$3F2	None.	Soft Entry Vector.
1011	\$3F3		
1012	\$3F4	None.	Power-up Byte.
1013	\$3F5	Holds a "JuMP" instruction to the subroutine which handles Applesoft II "&" commands.* Normally \$4C \$58 \$FF.	
1014	\$3F6		
1015	\$3F7		
1016	\$3F8	Holds a "JuMP" instruction to the subroutine which handles "USER" (CTRL.Y) commands.	
1017	\$3F9		
1018	\$3FA		
1019	\$3FB	Holds a "JuMP" instruction to the subroutine which handles Non-Maskable Interrupts.	
1020	\$3FC		
1021	\$3FD		
1022	\$3FE	Holds the address of the subroutine which handles Interrupt ReQuests.	
1023	\$3FF		

\* See page 123 in the Applesoft II BASIC Reference Manual.

## MINI-ASSEMBLER INSTRUCTION FORMATS

The Apple Mini-Assembler recognizes 56 mnemonics and 13 addressing formats used in 6502 Assembly language programming. The mnemonics are standard, as used in the MOS Technology/Synertek 6500 Programming Manual (Apple part number A2L0003), but the addressing formats are different. Here are the Apple standard address mode formats for 6502 Assembly Language:

Mode:	Format:
Accumulator	None.
Immediate	#S{value}
Absolute	S{address}
Zero Page	S{address}
Indexed Zero Page	S{address},X S{address},Y
Indexed Absolute	S{address},X S{address},Y
Implied	None.
Relative	S{address}
Indexed Indirect	(S{address}),X
Indirect Indexed	(S{address}),Y
Absolute Indirect	(S{address})

An {address} consists of one or more hexadecimal digits. The Mini-Assembler interprets addresses in the same manner that the Monitor does: if an address has fewer than four digits, it adds leading zeroes; if it has more than four digits, then it uses only the last four.

All dollar signs (\$), signifying that the addresses are in hexadecimal notation, are ignored by the Mini-Assembler and may be omitted.

There is no syntactical distinction between the Absolute and Zero Page addressing modes. If you give an instruction to the Mini-Assembler which can be used in both Absolute and Zero-Page mode, then the Mini-Assembler will assemble that instruction in Absolute mode if the operand for that instruction is greater than \$FF, and it will assemble that instruction in Zero Page mode if the operand for that instruction is less than \$0100.

Instructions with the Accumulator and Implied addressing modes need no operand.

Branch instructions, which use the Relative addressing mode, require the *target address* of the branch. The Mini-Assembler will automatically figure out the relative distance to use in the instruction. If the target address is more than 127 locations distant from the instruction, then the Mini-Assembler will sound a "beep", place a circumflex (^) under the target address, and ignore the line.

If you give the Mini-Assembler the mnemonic for an instruction and an operand, and the addressing mode of the operand cannot be used with the instruction you entered, then the Mini-Assembler will not accept the line.

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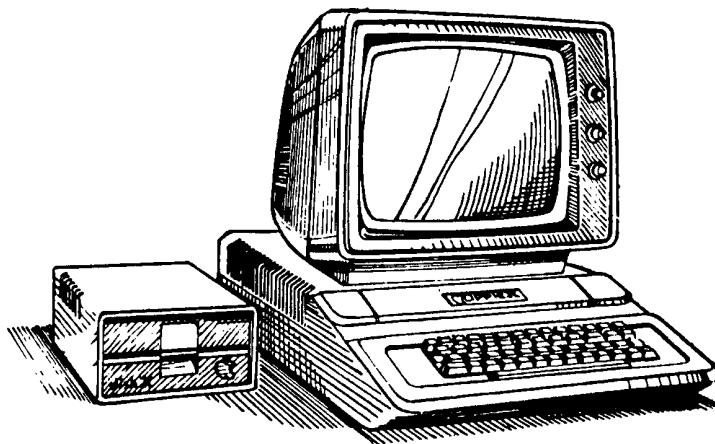


## Apple II Computer Technical Information

# APPLE II / APPLE II-PLUS LEVEL II SERVICE REFERENCE MANUAL

**Pre-Release Version**

## CHAPTER 10 TROUBLESHOOTING GUIDE



**Written by  
Apple Computer, Inc. • Level II Service Center  
1981**

( This page is not part of the original service manual )

# PRE-RELEASE VERSION

## TROUBLESHOOTING GUIDE

### General Troubleshooting Tips:

On both a hardware and a software level, APPLE II is highly interactive. The first step in repairing an APPLE II system is to isolate the problem to a particular module. With the Modular Exchange Program, this is done at the Dealer level. When a Main Logic Board is received, it should be connected up to a known-good Power Supply, Keyboard and Disk II so that any failures observed are the fault of the board under repair. When a unit is received as a complete APPLE II having its own Power Supply and Keyboard, the case must be removed from the unit so the the board may be completely exposed. You may also wish to remove the board, and connect it to a known-good Keyboard and Power Supply.

Most board failures are due to IC failure. In this case, the problem can usually be narrowed down to an area on the board, and parts substitution will identify the bad component.

If the problem is mechanical in nature, (open or shorted trace, bad socket) no amount of chip-swapping will solve the problem. In this case, the bad signal must be found with an oscilloscope to repair the board.

When an IC fails, often one of its outputs will fail to toggle even though the inputs to the chips are good. Sometimes an IC'S input will, due to an internal short, hang up a healthy IC'S output. This can be difficult to locate when the signal goes to many places on the board.

Mechanical failures on the board generally cause either dead shorts or opens, which can be positively identified with a VOM or continuity tester. Mechanical intermittents should be aggravated by flexing the board to bring out the failure.

Board contaminants (spilled liquids, etc.) can be removed from the bottom side of the board by scrubbing the board with a small brush soaked in alcohol. This is much more difficult to do on the component side of the board, and requires that the plastic carrier for each socket in the affected area be removed, and the board area carefully cleaned as above.

With intermittent boards, special attention is required. A 24 or 48 hour burn-in period will show whether a repair on an intermittent unit was successful or not. In cases where a unit dies completely after a period of time, a simple Monitor command such as:

```
N E000LLL 34:0 <SP> <RET>
```

will generate repeating screen action, indicating whether the machine is functioning or not. Often a Heat Gun and a can of Cold Spray will speed things up.

Here are some suggestions:

Each technician should have their own personal known-good Main Logic Board to use as a source of components when substituting parts into

the board under repair. This serves two purposes. First, we have confidence in the parts which are being placed into the bad unit. Second, the empty sockets in the known good board provide a record of what parts were replaced; this helps when filling out the paperwork.

It sometimes helps to scope out a known-good board when troubleshooting. This helps us get acquainted with what the proper signals should look like. After a while this won't be necessary.

The Main Logic Board Theory of Operation describes what the logic should be doing. It is especially important to spend time familiarizing yourself with the Medium-Scale (MSI) chips present on the board. Consult this material when in doubt.

Learn to use the F8 Monitor's software commands. (A tutorial on switching between video modes and testing video operation from the keyboard is given in the Section entitled "Using the Montor to Verify Video Failure"). It also helps to know 6502 Assembly Language programming (information on using the Dis-assembler and Mini-assembler can be found in the APPLE II Reference Manual, APPLE product number A2L0001A).

Temperature-related problems can be fixed by using a heat-gun and cold-spray to isolate the bad component. Heat the unit up until it fails, and then chill suspected ICS on the board using the thin plastic tube that comes with the cold-spray. The board will usually begin functioning correctly when the temperature-sensitive part is cooled.

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SERVICE PROCEDURES

Motherboard:

I. Test Set-Up:

A. Equipment Needed:

1. A "known good, in spec" 48k system complete with all Apple peripherals.
2. Oscilloscope
3. I C Puller
4. 48K RAM
5. Disk Interface Card
6. Diagnostics Diskette
7. Non Conductive Foam Pad
8. Heat Gun

B. Set up Procedure:

1. Place mother board to be tested in position on non-conductive foam pad.
2. With power supply switch OFF, plug power supply and video cable into motherboard. (no RAM should yet be installed!)

C. Visual Inspection:

1. Look for obvious damage- burned chips, scratches, drink strains, burn marks, drops of solder, etc.
2. Make sure that there are no missing chips.
3. Make sure that all chips are what they're supposed to be.
4. Make sure all chips are firmly seated.
5. Make sure that all chips are installed correctly pin 1 to hole 1.
6. Make sure that no pins are bent under.

II. Start-up

A. Video Problem:

1. Turn ON power supply.
2. If you have a video failure, look for symptom and possible fix in the section entitled "Motherboard Video Failures/Symptoms".
3. Repair video problem first and you may find that it will also fix a no reset problem if there is one.

III. Troubleshooting

A. Running Diagnostics:

1. When you have a good video pattern, continue the following procedures.
2. Assure power supply is OFF and insert only 16K of RAM (c-row only), plug in speaker and keyboard (Do not insert Disk Interface Card yet).
3. Turn ON power supply at which time determine whether you have a good cold-start reset (beep, prompt and cursor)-- if you have an Autoboot ROM at F8 you may also get some data locations listed on screen along with prompt and cursor).
4. If you have a good cold start, turn OFF power supply, install full 48K RAM, insert Disk Interface Card, insert Diagnostics Diskette in drive and continue testing (most motherboard problems from this point may be found in the section entitled "Motherboard Miscellaneous Failures/

Symtoms). IF YOU DO NOT HAVE A GOOD COLD START RESET (making sure all three: beep, prompt and cursor, are present), then refer to the section entitled "Motherboard Reset Failures/Symtoms".

5. When you have accomplished the fix and have a good cold start reset, turn OFF power supply and continue as stated in paragraph directly above.

V. Testing:

Once diagnostics have been completed error free, then it is suggested you final test system by running a continuous loop possibly similar to the following:

```
10 for X = 1 TO 39
20 TAB X (HTAB X for Applesoft)
30 PRINT X
40 FOR I = 1 TO 100:NEXT I
50 NEXT X
60 GOTO 10
RUN
```

While this loop is running you might run a heat gun over the board for a short period, then tap chips with the plastic end of a screw-drive. In justifying this seemingly unorthodox procedure, a sufficient number of problems are found at this point that would otherwise have found their wayback to the dealer/customer. Remember that our objective at this point is to create a potential hidden failure if one indeed exists. If there is no failure after a couple of passes with the heat gun and one pass shocking the ICS, pat yourself on the back and ship it (if you have any doubts put it on the burn-in rack overnight).

Of course, once these procedures above are exhausted, it becomes a matter of technical expertise finding opens, shorts, incorrect values, etc. Some test points for various system signals are provided in the section entitled "Scope and Meter".

It is suggested that as you repair a failure you might make note of the system and the fix action to provide a means of evaluation and ready, handy reference. This trouble shooting guide by no means provides all systems or fix actions.

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### USING THE MONITOR TO VERIFY VIDEO FAILURE

First, we need to get into the Monitor. On systems with the F8 Monitor ROM this is easy: just turn on the power and press the Reset button a couple of times. An asterisk prompt (\*) will be displayed in the lower left-hand corner of the screen. Newer circuit boards don't require you to press the Reset button at all, but it won't hurt to do so.

On systems with the newer Autostart Monitor (APPLE part number 341-0020) the system will boot up your disk drive if it finds a disc controller card in one of the motherboard slots 1 through 7. If no card is present it will go into BASIC, which is indicated with a greater-than (>) prompt in the lower left-hand corner of the screen. To enter the Monitor type CALL-151 followed by a Return.

To fill the screen with TEXT characters, type in the command L (for list). This invokes the disassembler which interprets memory locations as a series of machine language instructions and displays the opcodes for you. To look at the contents of the F8 ROM you type: F800 L. Each L command following causes the next locations in memory to be displayed.

Now suppose we wish to check out the LORES graphics mode. We do this by typing a series of soft-switch commands which causes the system to shift from TEXT mode into LORES mode. These commands are:

```
C050 C056
```

Now entering L causes the text displayed to appear as LORES characters. If we want a TEXT-window at the bottom to see what we are doing, we type:

```
C053
```

To make the TEXT-window disappear we type:

```
C052
```

These commands will tell you whether or not LORES graphics is ok or not.

For HIRES graphics, we can't alter the contents of screen memory just by entering L. This is because the HIRES screen memory area is mapped into locations \$2000 to \$3FFE instead of \$400 to \$800 as is the case with TEXT and LORES modes. In order to use the monitor to alter the HIRES screen memory we must do a "block move" into memory. Here's an example:

Fill the Hires main display page with the value \$55 (Since the monitor already speaks on hex, the dollar sign is not required.)

This is done with the command:

```
2000:55 2001<2000.3FFEM
```

To see the results use the soft-switch commands:

```
C050 C053 C057
```

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This will display vertical bars of green and purple on the HIRES screen. Do the block move using AA instead of 55:

2000:AA 2001<2000.3FFEM

This will produce orange and blue vertical bars on the HIRES screen. (On REV 0 boards you will still get the colors green and purple but the positions of the vertical bars will be reversed.)

The soft-switch command:

C055

Causes the APPLE II to jump into PAGE 2 of whatever graphics mode you are in. The screen locations for these secondary pages are:

Secondary page of TEXT/LORES: \$800 to \$BFF

Secondary page of HIRES: \$4000 to \$5FFF

To check out the secondary page of TEXT/LORES, try the following scheme:

C053 C055 (Page 1 with TEXT window)

800<400.7FFM (Loads data from primary to secondary page)

C055 (Switches into secondary page)

For LORES display type:

C056

To load into secondary HIRES page:

To display it type:

C050 C053 C055 C057

If you get lost, type:

C051 C054

Which will return you back to the primary TEXT page so you can see the last 20 or so commands typed in.

Now you have a way to verify each graphics mode and the machine's ability to switch between modes correctly. Again, practice switching modes and block-moving data on a known-good APPLE II system. Then on any machine with good Reset you will be able to verify a video problem without special equipment.

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MOTHERBOARD VIDEO FAILURE/SYMTOMS

No video at all (dark rather than light screen): With scope grounded, first scope (B2-74S86 pin 10) for 14MHz signal from crystal. Replace crystal if no oscillator signal or if signal is questionable and if this does not correct oscillation then replace Q1 and Q2 (2N4258's) below crystal. If signal at B2 pins 10 & 8 are good then swap the following ICs: (Note:swap 2 or 3 ICs at a time leaving replacements in until you have video. Then remove replacements in the same manner reinserting original ICs and turning system on after replacing 2 or 3 to assure no more than the one chip you replaced is bad).

REMEMBER TURN POWER OFF BEFORE SWAPPING CHIPS!

Most likely cause replace these four first:

B1-74LS175  
 B2-74S86  
 C1-74LS153  
 C2-74LS195

Turn power back on ----if still no video try these:

A2-74LS00	B10-74LS74	C13-74LS51	D2-74LS20	F14-9334
A9-74LS151	B11-74LS08	C14-74LS32	D11-74LS04	
A10-74LS194			D13-74LS161	

If you still have no video, refer to the Section entitled "Scope and Meter".

The following are various types of video failures/symptoms you may encounter and possible fixes. Be aware that the fix given may not be the only problem areas, they are only the most likely, giving you a starting point.

SYMPTOM	CAUSE
Blank white screen	F14-9334 6502 A3-74166 B5,8-74LS174
Screen goes blank when disk boots	B9-74LS194
Will get into diagnostics menu but screen goes all white during RAM test	B2-74S86 C11-74LS04 D11-74LS161 D12-74LS161 D13-74LS161 D14-74LS161
Video wavers	
Pulsating data with corresponding speaker static	H1-74LS08
Video distortion but reset OK	D2-74LS20
Top of video missing/distorted	B14-74LS02
Video pushed down & to the right	C13-74LS02
Can't write into upper left of screen	A9-74LS151

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Top three lines of HIRES missing  
Rolling(not scrolling) video

Full vertical screen of question  
marks scrolling (not rolling) up  
Entire screen inverse & prompt  
not flashing  
Inverse/incorrect prompt at CTRL  
B/C  
Split video with four corners

Split location of prompt/cursor

No prompt/cursor

No flashing cursor

Horizontal lines & garbage chars.

Color bar test has horizontal  
lines  
Color bars come up in text mode

Distorted color bars  
Vertical bars at cold start

Vertical bars in HIRES  
Left margin has vertical white  
column  
Graphic color bars broken up

No page 2  
Black squares with left to right  
moving characters

Smaller chars. & vertical bars  
Constantly active characters at  
row 9, column 39&40 also writes  
garbage into rows 3/4;11/12;19/20  
at reset  
Random chars. upon keyboard reset

Part graphics & part text  
Entire screen background of  
exclamation marks  
Garbage chars after warmup

Full video & reset but video  
is pushed down a couple of inches  
from top  
Distorted, diagonal breaks in video

A11-74LS74  
B14-74LS32  
C11-74LS04

E11-74LS153

B2-74LS86

F8 ROM  
B1-74LS174  
C1-74LS153  
C11-74LS04  
E14-74LS283

B3-555 timer  
open from C1 pin 3 to H2 pin 14  
B3-555 timer  
0.1uf capacitor just above B3  
B5-74LS174  
B11-74LS08

B4-74LS194  
B5-74LS174  
B8-74LS174  
A12-74LS02  
F14-9334  
A5-2513  
A9-74LS151  
C12-74LS257  
D12-74LS161  
B4-74LS194

A3-74LS166  
B4-74LS194  
B9-74LS194  
open B11 pin 6 to H1 pin 10

B12-74LS11  
B13-74LS02  
B2-74LS86

C11-74LS04  
B11-74LS08  
F1-(no F1 on boards Rev 7 and up).  
A11-74LS74

A5-2513  
27 microhenry choke at end of  
H-row

B14-74LS02  
C1-74LS153

Right half of text char. missing  
Video shows only top halves of letters,  
you get two tops instead of a top &  
bottom

A3-74LS166

Mis-shaped question marks/char

H1-74LS08  
A5-2513(VC line to pin 13 held low

No graphics but text ok

A3-74LS166  
A5-2513  
A9-74LS151  
B2-74LS86  
B10-74LS74  
B4-74LS194  
B9-74LS194  
A8-74LS257  
A9-74LS151  
A9-74LS151  
E11-74LS153  
A9-74LS151  
A10-74LS194

LORES/HIRES, only one works  
Double row of prompt, cursor & text  
No video but will reset & boot disk

All white screen with black blinking  
cursor square  
All white screen rolling upward &  
will produce a horizontal bar at each  
reset & may or may not reset continuously  
Vertical roll in LORES (color bars)  
but ok in text & can be corrected  
momentarily by tweaking video pot

A3-74LS166

A12-74LS02

replace video pot

PRE-RELEASE  
VERSION

# PRE-RELEASE VERSION

## MOTHERBOARD RESET FAILURES/SYMTOMS

For a no reset condition where there is no cursor, no prompt, and no speaker beep as obvious symptoms, with scope grounded, check pin 40 of the 6502 for a high to low transition when the reset key is pressed. If no transition occurs, check the following:

REMEMBER TURN POWER OFF WHEN REPLACING ICS!

A13-555  
Q5-(2N3904 near A13)  
capacitor below Q5 (.1uf)

Usually if you have a good reset from the keyboard, but are unable to get a cold start reset , Q5 is good and change the capacitor.  
IF YOU HAVE A GOOD TRANSITION WITH HIGH LEVEL AT +5V and still no reset swap the following ICS: NOTE: swap 2 or 3 at a time leaving replacements in until you have a good reset then remove replacement ICS in the same manner reinserting original ICS and turning system on after replacing 2 or 3 to assure no more than the one chip you replaced is bad.

Swap chips in the following order as they are arranged according to most common failures and will save you some time: Remove all ROM and the 6502, insert known good 6502 and the F8 ROM leaving all other ROMS out. Then proceed with the chips at the following locations.

B6-74LS257	H10-8T28	H3-8T97	C14-74LS32	D2-74LS20
B7-74LS257	H11-8T28	H4-8T97	A2-74LS00	E11-74LS153
		H5-8T97	B11-74LS08	E12-74LS153
				E13-74LS153

C1-74LS153	F12-74LS138	F14-9334	H1-74LS08
B5-74LS174	F13-74LS138	F2-74LS139	H12-74LS138
B8-74LS174	C11-74LS04	J1-74LS74	H14-74LS251

At this point, if you still have no reset, assure that your 16K of RAM has not gone bad by replacing the row. If a bad reset condition still remains refer to the Section entitled Scope and Meter. This may assist you in getting started in the right direction.

The following are various types of reset failures/symtoms you may encounter and possible fixes. Be aware that the fix given may not be the only problem areas.

No reset & intermittent oscillator failure	Short-pins 5&6
No reset & random char. generation from keyboard reset	D2-74LS20    F1-jumper block E12-74LS153    F2-74LS139
Intermittent reset both at cold start & from keyboard reset	C14-74LS32
Intermittent reset,inputs random data & will not access drive	A2-74LS00 E8-ROM
Random chars. at keyboard reset	B11-74LS08

Constantly active chars. at Row 9,  
column 39&40 & writes random data  
into rows 3/4, 11/12, 19/20 at reset  
Repetitive/continuous reset without  
load at cold start  
Good at 16K, no reset above 16K  
Good at 16K, intermittent reset over  
16K & will not complete RAM test  
Reset OK but no speaker output (no beep)  
Good speaker output but no reset, prompt  
or cursor

No prompt or cursor

Split location of prompt/cursor  
No reset with ROM card in and  
switch in up position, OK with switch  
down (determined not to be a ROM card  
fault)  
No reset with Disk Interface Card,  
OK without

At cold start, reset may be intermittent,  
random data input & will not complete RAM  
test

F1-jumper block

C11-74LS04

B7-74LS257  
RAM short (RA02 or RA03)

F2-74LS139  
J13-74LS74

C13-74LS51  
F14-9334  
E11-74LS153  
E12-74LS153  
E14-74LS153  
H1-74LS08

B3-555  
cap. just above B3  
C11-74LS04

RA01

H2-74LS138  
H12-74LS138

RAM short

PRE-RELEASE  
VERSION

# PRE-RELEASE VERSION

## MISCELLANEOUS MOTHERBOARD SYMTOMS/FAILURES

Following are various types of miscellaneous motherboard failures/symtoms and possible fixes. Be aware that the fix given may not be the only problem areas, they are only the most likely, giving you a starting point.

Unable to access drive:	B5-74LS174 B6-74LS257	
Will not boot disk, drive LED on, prompt switches back and forth from Monitor to a mis-shaped rounded Basic:	B5-74LS174 H2-74LS138 H3-74LS8T97 H12-74LS138	C1-74LS153 B6-74LS257 B7-74LS257
Will not boot disk:		
Prompt but no cursor and will not access disk:	B3-555	
Disk boots then screen goes blank:	B9-74LS194	
Goes into monitor, program stops after warmup:	RAM E11-74LS153 E12-74LS153 E13-74LS153 E14-74LS153 Slot 0 50-pin connector	C1-74LS153 B6-74LS257 B7-74LS257 ROM Card in slot 0
Keyboard input failures but keyboard is good:	B6-74LS257 B7-74LS257 B10-74LS74 anything in keyboard strobe line	C11-74LS04 F13-74LS138
Will not run D-row RAM & has static output to speaker & screen during diagnostics:	H1-74LS08 J1-74LS257 D2-74LS20	
Will not run E-row RAM & has static output to speaker & screen during diagnostics:	D2-74LS20 H1-74LS08 J1-74LS257	
Will not run E-row RAM (no static output at speaker):	D1-jumper block D-row RAM F1-not on rev. 7 or later boards.	
Cursor moves by itself through diagnostics menu, sometimes will not move when ESC pressed & will boot intermittently:		I/O select not grounded
Will not go to Basic from Monitor with CTRL B/C:	B6-74LS257	
Double row of prompt, cursor, & chars.:	E11-74LS153	

SCOPE AND METER

NO RESET

A no reset condition is where there is no cursor, no prompt, and no speaker. Check pin 40 of the 6502 for a high to low transition when the reset key is pressed. If no transition occurs check the following: Q5 (2N3904 near A13, and the capacitor below Q5(.1 microfarad). Usually if Q5 is bad the APPLE will keyboard reset (but will not power on reset). If a transition occurs check the following points with an oscilloscope:

Data Lines D0-D7 (pins 49-42 on I/O slots),  
 Address Lines A0 to A15 (pins 2-17 on I/O slots),  
 Read/Write (the write signal is active low) at pin 34 of the 6502,  
 pin 5 of H5(8T97),  
 pin 9(R/W in) of C14,  
 pin 8(R/W out) at C14.

Look for low logic levels and missing (except AD7 and AD9 which are normally low) signals. The following IC'S could be at fault:

SYMPTOMS	PROBABLE CAUSE	
Low Data Levels	B6-74LS257	H10-8T28
	B7-74LS257	H11-8T28
	Bad ROM'S	
Bad Address levels	H3-8T97	Bad ROM'S
	H4-8T97	6502
	H5-8T97	
No R/W signal	H5-8T97	A2-74LS00
	C14-74LS32	
	6502	

With an osilloscope check for the 1 MHz clock on pin 37 of the 6502. Also check B11 pin 1 (74LS08) for the 1 Mhz clock. Check B11 pin 1 for +5 volt level. C11 pin 13 (74LS04) for a +5 volt level, and C11 pin 12 for a low level. See schematic for futher details. Check the following IC'S.

SYMPTOMS	PROBABLE CAUSE
No 1 MHz at 6502	C11-74LS04 B11-74LS08 RA01 (resistor pak)

PRE-RELEASE  
VERSION

## SCOPE AND METER

## RA01 (resistor pak)

Check the following signals to make sure there is proper RAM addressing. Check the CAS bar signals at pin 15 of the RAM. The CAS bar signal at pins 4 (\$0-3FFF), 5 (\$4000-\$7FFF), 6 (\$8000-\$BFFF) from F2 (74LS139). Check the CS bar signal at pins 13 of the RAM and pin 7 of C1 (74LS153). Check RAM SEL bar at pin 4 of the RAM, pin 6 of A2 (74LS00). Check inputs and outputs of D2 (74LS20) and pins 10 (\$8000-\$BFFF), 11 (\$4000-\$7FFF), and pin 12 (\$0-\$3FFF). See the schematic for complete detail and check the inputs and outputs of the following IC'S.

J1-74LS257	H1-74LS08	F2-74LS139
C1-74LS153	C12-74LS257	D2-74LS20
C11-74LS04	C14-74LS32	A2-74LS00

Also check the Memory Select headers for continuity (except Rev 7 and above boards)

Check RAM pins 5,6,7, and 10,11,12 for RA0 (pin10), RA1 (pin 11), RA2 (pin 12), RA3 (pin 7), RA4 (pin 6), and RA5 (pin 5). These are the RAM refresh, video addressing signals. Also check pins 7 and 9 of E11,12, and 13 (74LS153's). Check the address and sync inputs to the 74LS153's (see schematic for pinouts).

If the system works with 16k RAM but not with 32K or 48K check RA02 and RA03 resistor paks. These located between E10 and E11 and D10 and D11. Check these with an ohm meter from pins 7 and 9 of E11,12,13 between ground and +5 volts. There should be a reading of about 500 ohms between pin 7 of E11 and ground. Also, it should read the same for pin 7 of E11 and +5 volt buss (about 500 ohms). The readings should be the same for each for them (see schematic for more details).

PRE-RELEASE  
VERSION

# SERVICE PROCEDURE

## New style keyboards(two part)

<u>Symptoms</u>	<u>Cause</u>
No keyboard output	Encoder(331-0931)
No Data Strobe(no keybd output)	B3(74LS00) B4(74LS00) C6(.1 microfarad cap)
Incorrect data out	Encode B5(74LS04) B3(74LS00)
No output	Cable
P, Return, and : keys repeat resistor. See Apple Service Bulletin #15	Change R10 to 3.0K ohm 1/4 watt

PRE-RELEASE  
VERSION

*APPLE*  
P.S. TEST PROCEDURE

*Original - 1981  
#A20001*

1. DISASSEMBLE

- (A) REMOVE RIVETS AND SHEETMETAL SCREWS THAT HOLD LID TO HOUSING.
- (B) REMOVE PCB HOLD-DOWN SCREWS AND WASHERS.
- (C) REMOVE PCB FROM HOUSING.
- (D) FIND THE TWO RIVETS.

2. VISUAL CHECK

- (A) DETERMINE LEVEL OF SUPPLY, UPDATE AS NECESSARY.  
C6 C7 C16 10UF, 25V ; R17 R20 39 OHM, 1/4W.
- (B) CHECK FOR BAD DATE CODE OF CR1, IF "7841" CHANGE.
- (C) CHECK FOR MOST COMMON FAILURES.
  - (1) RESISTANCE ACROSS CR16 220 OHM, IF LESS CR15 OR CR16 BAD.
  - (2) IF FUSE BLOWN CR3 MAY BE SHORTED OR Q1 & Q2 MAY BE BAD.
  - (3) IF R1 IS OPEN CR1 PROBABLY BAD.
- (D) CHECK FOR BURNT RESISTORS AND BAD SOLDER CONNECTIONS.

3. LOAD TEST

- (A) HOOK-UP P.S. TO TEST FIXTURE. CHECK FOR FAILURE.
- (B) TAKE IN CIRCUIT RESISTANCE READINGS TO FIND CAUSE OF FAILURE.  
HAVING A KNOWN GOOD P.S. TO COMPARE WITH WOULD BE HELPFUL.
- (C) MAKE NECESSARY REPAIRS.
- (D) TEST AT ALL S/W SETTINGS.
- (E) VIBRATION TEST, WITH POWER APPLIED TO P.S. ,  
TAP PCB WITH THE HANDLE OF A SCREWDRIVER.  
NO FLUCTUATION IN OUTPUT SHOULD OCCUR.

4. FINAL TEST

- (A) SECURE PCB IN HOUSING, REPLACE LID.
- (B) VERIFY OPERATION.
- (C) BURN-IN FOR 3-6 HOURS.  
COMMON THERMAL PROBLEMS AR1, CR17, CR18, OR CR19.
- (D) VERIFY OPERATION.
- (E) REPLACE SHEETMETAL SCREWS & RIVETS.

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APPLE ORIGINAL FILE  
P.S. PROBLEMS #A81001

"BAD" MEANS COMPONENT COULD BE OPEN, SHORTED, MISSING, WRONG VALUE, PHYSICALLY DAMAGED, HEAT SENSITIVE, OR HAVE A POOR SOLDER CONNECTION.

SYMPTOM ON TESTER	PROBABLE CAUSE IN ORDER OF OCCURRENCE
FAILS CROWBAR TEST	(1) Q5 BAD
@107 HI LOAD NO OUTPUT	(1) FUSE BLOWN - CHECK CR3 (2) R1 OPEN - CHECK CR1 (3) BAD S/W (4) CR15 OR CR16 BAD (5) CR1 BAD
@107 HI LOAD ALL VOLTAGES LO WON'T ADJUST	(1) AR1 BAD (2) C6 OR C7 BAD (3) Q1 OR Q2 BAD (4) CR9, CR18 OR CR19 BAD
@107 HI LOAD OSCILLATING MAKES CLICKING SOUND	(1) AR1 BAD (2) C6 OR C7 BAD (3) Q1 OR Q2 BAD (4) CR5, CR9 OR CR11 BAD
@115 1A LOAD +12V DROPS BELOW 11.25V	(1) CR17, CR18 OR CR19 BAD
@120 HLOO LOAD EXCESSIVE RIPPLE OR MAKES CLICKING SOUND	(1) AR1 BAD (2) R17 BAD (3) C11, C12 OR C18 BAD (4) CR9 OR CR19 BAD
@120 LHOO LOAD EXCESSIVE RIPPLE OR MAKES CLICKING SOUND	(1) CR17, CR18 OR CR19 BAD
@137 LO LOAD EXCESSIVE RIPPLE OR MAKES CLICKING SOUND	(1) C6 OR C7 BAD (2) CR5, CR6, CR9 OR CR11 BAD
VIBRATION PROBLEM	(1) SOLDER CONNECTION OF SINGLE ENDED CAPACITORS (2) HEAT SINK TO PCB SOLDER CONNECTION (3) R16 BAD - REPLACE

PRE-RELEASE  
VERSION

August 1981

REPAIR MANUAL FOR ASTEC POWER SUPPLY AA1040

PRE-RELEASE  
VERSION

Section I: Test Set-up

A. Equipment Needed

1. Isolation Transformer (minimum of 500 VA rating)  
Dangerously high voltages are present in this power supply. For the safety of the individual doing the testing, please use an isolation transformer. The 599 VA rating is needed to keep the AC wave form from being clipped off at the peaks. These power supplies have peak charging capacitors and draw full power at the peak of the AC wave form.
2. 0-140V Variable Transformer (Variac)  
Used to vary input voltage. Recommend 10 Amp. 1.4 DVA rating, minimum
3. Voltage meter - Needed to measure DC voltages to 50VDC and AC voltages to 200VAC. Recommend 2 digital Multi Meters.
4. Oscilloscope - Need X10 and X100 probes.
5. Load board with connectors  
See table I for values of loads required. The entry on the table for safe load power is the minimum power ratings for the load resistors used.
6. Ohm meter.

B. Set-up Procedure

Set-up as shown in Figure 1. Monitor the input voltage and the output voltage of the regulated bus, which is the +5 output, with DVM's. Also monitor the +5 output with the oscilloscope using 50mv/div sensitivity. The DVM monitoring the +5 output can also be used to check the other outputs. See text of section III for test points within power supply.

Section II

A. Visual Inspection:

Check power supply for any broken, burned, or obviously damaged components. Visually check fuse; if any question, check with Ohm meter.

- B. Load power supply with minimum load as specified in Table I. Bring power up slowly with variable Transformer while monitoring +5 output with scope and DVM. Supply should start with approximately 40-60 VAC applied and should regulate when 104 VAC is reached. If output has reached 5 volts, do a performance test as shown in Section VI. If there is no output refer to Section III.

PRE-RELEASE  
VERSION

### Section III - No Output

#### General

With the AC input applied to the L & N connections and the power does not produce an output, and power switch on one or more components have failed. A no output fault condition is most likely caused by a shorted or opened component on the primary side but may also be caused by a short on the secondary. To determine this follow the steps below.

- A. Check Fuse:  
If fuse is blown, replace but do not apply power until cause of failure is found.
- B. Preliminary Check on Major Primary Components:  
Check Diode Bridge (DB1), Power Transistor (Q2) and check diode (D3) for shorted junctions. If a component is found shorted, replace it.
- C. Primary Check on Major Secondary Components:  
Using Ohm meter from output common to each output, with output loads disconnected, check for shorted rectifiers or capacitors. If the +12V output is shorted also check crowbar: SCR (SCR1), +12V.
- D. Check B+ with the fuse intact:  
Set power supply and attach X100 scope probe ground to the anode of (D1). Slowly turn up power and check for B+ Cathode of D3 (near the transformer T1). With input at 107VAC, this point should be between 260-270 VDC. If this is not correct check R1 and DB1.  
  
If R8 is open, it was most likely caused by a shorted component that is fed power by T1. Check the following components for proper operation, (Q2, Q1, D3).
- E. Check Q4 Waveforms:  
Use X100 probe on Heat Sink of Q2, check collector waveform. Transistor should be switching, correct waveform is shown in Figure 2. If this is not present check for open junctions on Q2. If Q2 is OK, check to see if base voltage is being supplied to Q2; it should be .7V. If it is not present, check components, (C6, Q1, D1, and R3).

### Section IV - Low Outputs

- A. All outputs are low  
If all outputs are low at the same time, check to insure that the voltage selection jumper is in the proper position.
- B. +5V output  
The power supply is regulated off the +5V DC output. If this output is low, it could cause the others to be low, If so, adjust +5V by changing R20. If adjustment to correct voltage is not possible, check Q3 and Q4.
- C. If any one output is not present, first check the rectifier associated with that output and then the rest of the components in the circuit and

the solder joints on the PCB. Check respective choke for output in question (ie. L2, L3, L4, L5).

Section V - Crowbar

If the crowbar is not operating, check Z1 and SCR1. If the crowbar is not triggering within the specified limits, change Z1 and check that any adjustment resistor in series with Z1 has not changed value from its color code value.

Section VI - Performance Test

Each of these test conditions should be set-up and noted to be within the limits specified in Table II.

STEP	INPUT	+5V LOAD	+12V	-12V	-5V
1.	107 VAC	Max	Max	Max	Max
2.	132	Max	Max	Max	Max
3.	120	Max	Min	Min	Min
4.	120	Min	Min	Max	Min
5.	132	Min	Min	Min	Min
6.	Test Crowbar Limits				

If the power supply does not pass the above test, refer to Section IV and V.

PRE-RELEASE  
VERSION

Table I: Load Board Values

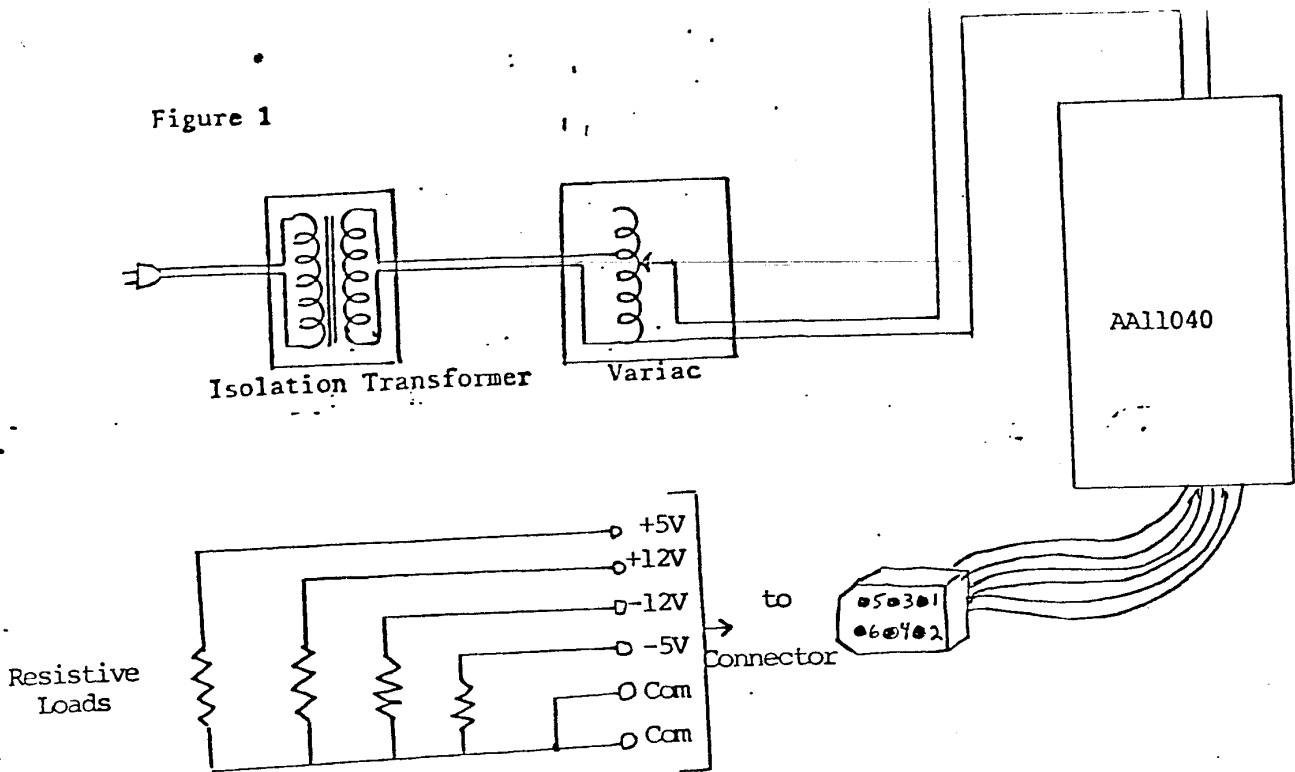
OUTPUT	MIN LOAD	LOAD RESISTANCE	SAFE LOAD POWER	MAX LOAD	LOAD RESISTANCE	SAFE LOAD POWER
+5V	1.0A	5.0 ohms	10 watts	2.5A	2.0 ohms	25 watts
+12V	0.25A	48 ohms	6 watts	2.5A	4.8 ohms	60 watts
-12V	0.05A	240 ohms	1 watt	0.25A	48 ohms	6 watts
-5V	0.10A	50 ohms	1 watt	0.25A	20 ohms	2.5 watts

Table II: Voltage and Ripple Specifications

OUTPUT	MIN	MAX	RIPPLE (MAX RP)
+ 5V	4.90V	5.10V	45MV
+ 12V	11.10V	12.50V	100MV
-12V	-10.80V	-13.20V	100MV
-5V	-4.70V	-5.70V	45MV

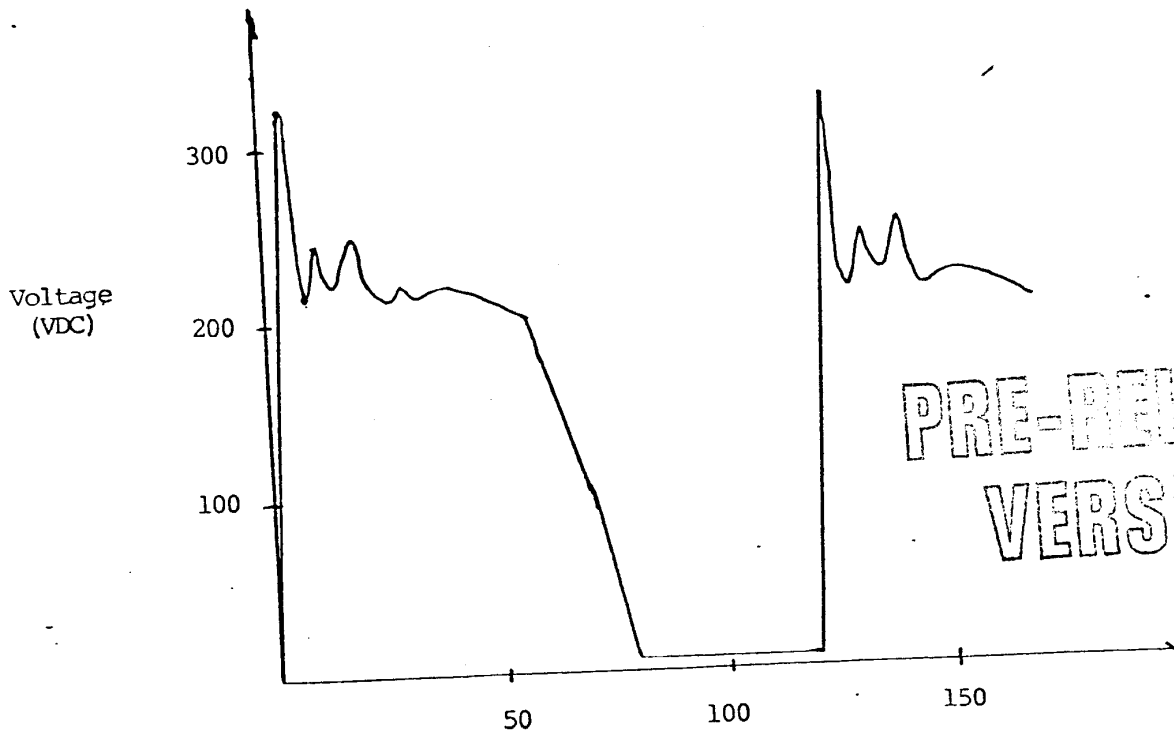
PRE-RELEASE  
VERSION

Figure 1



Pin No.	Output
1	Common
2	Common
3	+5V
4	+12V
5	-12V
6	-5V

Figure 2



# PRE-RELEASE VERSION

June 1981

## REPAIR MANUAL FOR ASTEC POWER SUPPLY AA11040(B)

### Section I: Test Set-up

#### A. Equipment Needed

1. Isolation Transformer (minimum of 500 VA rating)  
Dangerously high voltages are present in this power supply. So for the safety of the individual doing the testing please use an isolation transformer. The 500 VA rating is needed to keep the AC wave form from being clipped off at the peaks. These power supplies have peak charging capacitors and draw full power at the peak of the AC wave form.
2. 0-140V Variable Transformer (Variac)  
Used to vary input voltage. Recommend 10 Amp. 1.4 KVA rating, minimum.
3. Voltage meter - Needed to measure DC voltages to 50VDC and AC voltages to 200VAC. Recommend 2 digital Multi Meters.
4. Oscilloscope - Need X10 and X100 probes.
5. Load board with connectors-  
See table one for values of loads required. The entry on the table for safe load power is the minimum power ratings for the load resistors used.
6. Ohm meter.

#### B. Set-up Procedure

Set-up as shown in Figure 1. You will want to monitor the input voltage and the output voltage of the regulated buss, which is the +5 output, with DVM's. Also monitor the 5 output with the oscilloscope using 50mv/div sensitivity. The DVM monitoring the +5 output can also be used to check the other outputs. See text of section III for test points within power supply.

Section II

PRE-RELEASE  
VERSION

A. Visual Inspection:

Check power supply for any broken, burned, or ~~obviously damaged~~ components. Visually check fuse, if any question check with Ohm meter.

B. Start-up

Load power supply with minimum load as specified in Table I. Bring power up slowly with variable Transformer while monitoring +5 output with scope and DVM. Supply should start with approx. 40-60 VAC applied and should regulate when 95 VAC is reached. If output has reached 5 volts, do a performance test as shown in Section VI. If there is no output refer to Section III.

Section III - No Output

General

With the AC input applied to the L & N connections and the power does not produce an output, and power switch on, one or more components have failed. A no output fault condition is most likely caused by a shorted/open component on the primary side but may also be caused by a short on the secondary. To determine this follow the steps below.

A. Check Fuse:

If fuse is blown, replace but do not apply power until cause of failure is found.

B. Preliminary Check on Major Primary Components:

Check Diode Bridge (DB1), Power Transistor (Q2) and catch diode (D3) for shorted junctions. If any component is found shorted, replace.

C. Primary Check on Major Secondary Components:

Using Ohm meter from output common to each output, with output loads disconnected, check for shorted rectifiers or capacitors. If +12V output is shorted also check crowbar; SCR (SCR1), +12V.

D. Check B with the fuse intact:

Set power supply and attach X100 scope probe ground to the anode of (D1). Slowly turn up power and check for B+ on end of (R28) nearest the transformer. With input at 95VAC, this point should be between 260-270 VDC. If this is not correct check resistor and DB1.

If R5 is open it was most likely caused by a shorted component that is fed power by R28. Check the following components for proper operation, (Q2, Q1, D1)

E. Check Q4 Waveforms:

Using X100 probe on Heat Sink of Q4, check collector waveform. Transistor should be switching, correct waveform is shown in Figure 2.

-3-

*PRESENT*  
 If this is not ~~present~~ check for open junctions on Q2. If Q2 is ok, check to see if base voltage is being supplied to Q2, it should be .7V. If it is not present, check components, (L3, Q1, D1 and R3).

#### Section IV - Low Outputs

- A. All outputs are low.  
 If all outputs are low all at the same time, check to insure that the voltage selection jumper is in the proper position.
- B. +5V output.  
 The power supply regulates off of the +5V DC output. If this output is low, it could cause the others to be low. If so, adjust +5V by changing R25.
- C. If any one output is not present, first check the rectifier associated with that output and then the rest of the components in the circuit and the solder joints on the PCB.

#### Section V - Crowbar

If the crowbar is not operating, check Z1, Q4, and SCR1. If the crowbar is not triggering within the specified limits change Z1 and check that R26 and R27 are of the proper resistance.

#### Section VI Performance Test

Each of these test conditions should be set-up and noted to be within the limits specified in Table II.

STEP	INPUT	+5V LOAD	+12V	-12V	-5V
1.	90 VAC	Max	Max	Max	Max
2.	132	Max	Max	Max	Max
3.	120	Max	Min	Min	Min
4.	120	Min	Min	Max	Min
5.	132	Min	Min	Min	Min
6.	Test Crowbar Limits.				

If the power supply does not pass the above tests, refer to Section IV and V.

PRE-RELEASE  
 VERSION

-4-

Table I: Load Board Values

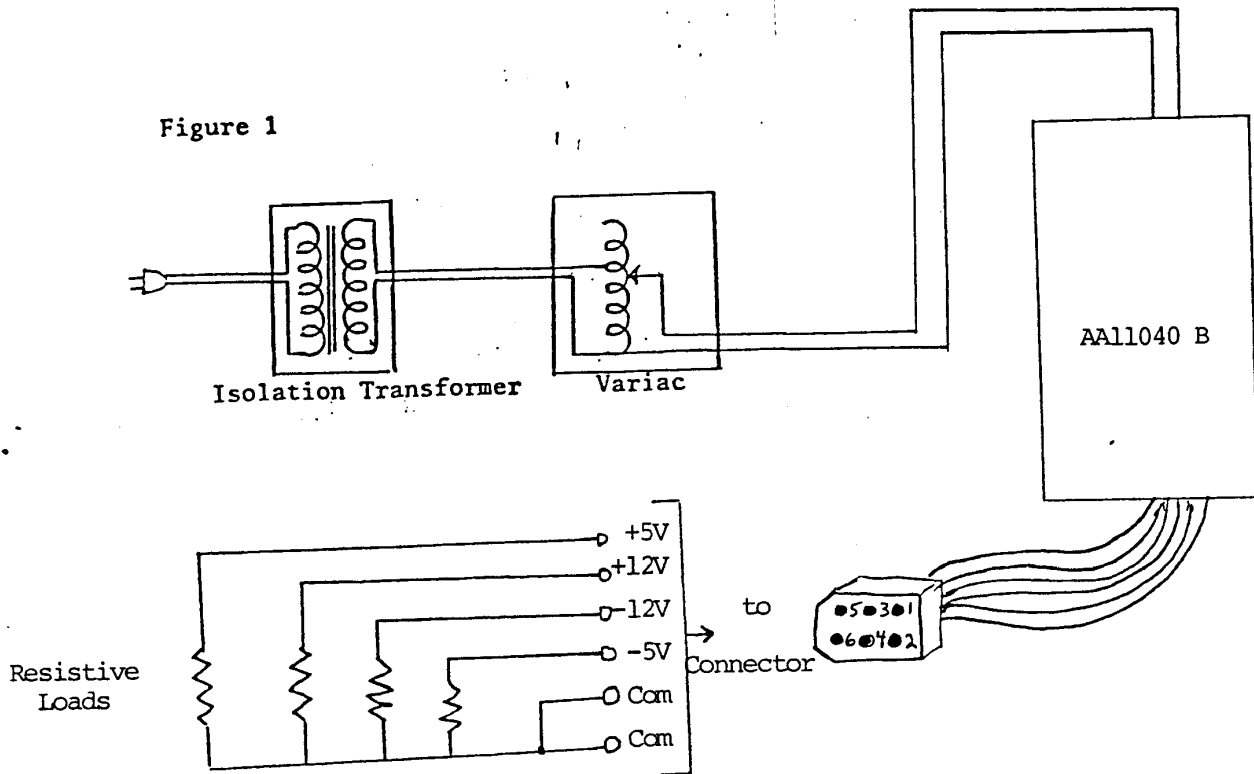
OUTPUT	MIN LOAD	LOAD RESISTANCE	SAFE LOAD POWER	MAX LOAD	LOAD RESISTANCE	SAFE LOAD POWER
+5V	1.0A	5.0 ohms	10 watts	2.5A	2.0 ohms	25 watts
+12V	0.25A	48 ohms	6 watts	2.5A	4.8 ohms	60 watts
-12V	0.05A	240 ohms	1 watt	0.25A	48 ohms	6 watts
-5V	0.10A	50 ohms	1 watt	0.25A	20 ohms	2.5 watts

Table II: Voltage and Ripple Specifications

OUTPUT	MIN	MAX	RIPPLE (MAX RP)
+ 5V	4.90V	5.10V	45MV
+ 12V	11.10V	12.50V	100MV
-12V	-10.80V	-13.20V	100MV
-5V	-4.70V	-5.70V	45MV

PRE-RELEASE  
VERSION

Figure 1



Pin No.

Output

1

Common

2

Common

3

+5V

4

+12V

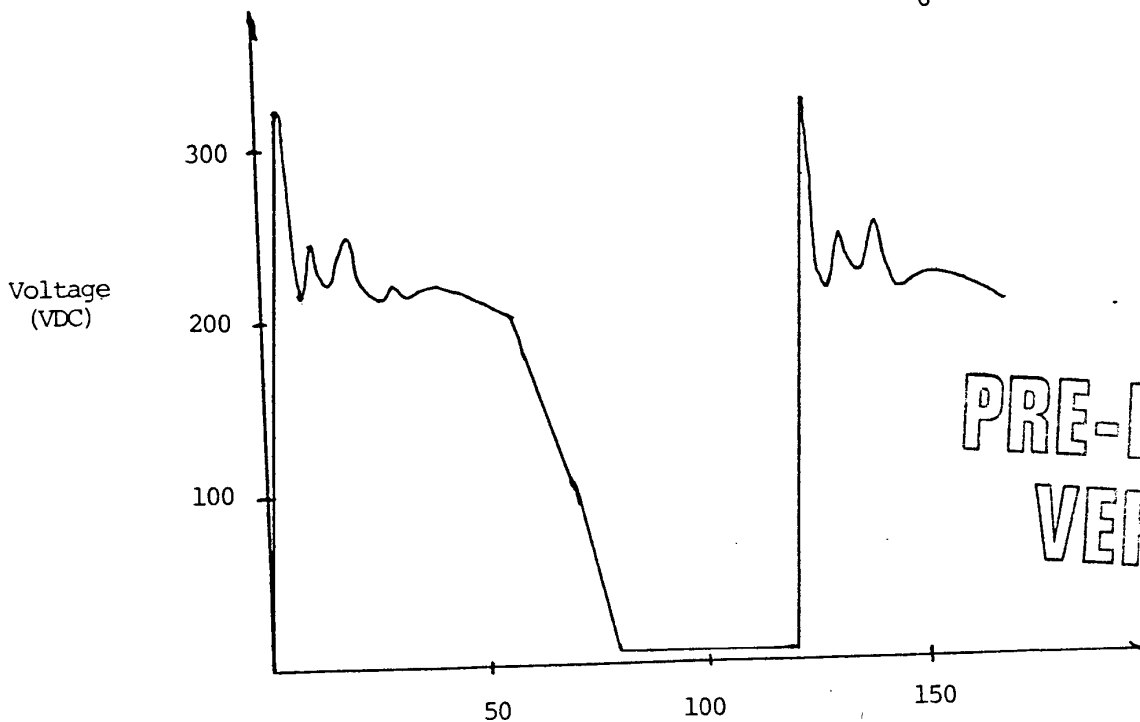
5

-12V

6

-5V

Figure 2



## SCOPE AND METER

### Introduction:

The following scope & meter points of reference and procedures are provided only as a guideline for tech's in training status. Tech's should eventually develop their own methods/procedures with which they feel most comfortable.

When metering RAM, ROM or I/O slots for continuity the following will not zero out:

RAM: Row- pin 2 will read approximately 19 to 20 and pin 14 will read open.

Column- pin 15 will read open.

ROM: Pins 20 & 21 will read open.

I/O slots: The following pins will read open --1,19,23,27,28,35,41.

PRE-RELEASE  
VERSION

SECTION 5: REFERENCE GUIDE TO SIGNALS

A. SYSTEM TIMING

SIGNAL MNEMONIC	LOCATION
14M	B2-8
7M	B1-15
7M'	B1-14
COLOR REF	B1-3
COLOR REF'	B1-2
.....	
PHASE ZERO	B1-7
PHASE ONE	B1-6
.....	
RAS'	C2-15
AX'	C2-14
CAS'	C2-13
Q3	C2-12
Q3'	C2-11
.....	
LD194	B12-8
LDPS'	A2-3

PRE-RELEASE  
VERSION

B. VIDEO

SIGNAL MNEMONIC	LOCATION
H0	D14-14
H1	D14-13
H2	D14-12
H3	D14-11
H4	D13-14
H5	D13-13
HPE'	D13-12
HBL	C13-6
.....	
VA	D13-11
VB	D12-14
VC	D12-13
V0	D12-12
V1	D12-11
V2	D11-14
V3	D11-13
V4	D11-12
VBL	B11-8
.....	
SYNC	C13-8
TEXT VIDEO	B2-11

C. MPU

SIGNAL MNEMONIC	LOCATION
-----------------	----------

A0	H5-11
A1	H4-5
A2	H5-7
A3	H5-9
A4	H4-7
A5	H3-9
A6	H3-11
A7	H3-7
A8	H3-5
A9	H3-3
A10	H4-9
A11	H4-11
A12	H4-3
A13	H5-3
A14	H5-13
A15	H4-13

.....  
R/W                    H5-5

.....

D0	H11-2
D1	H10-2
D2	H10-14
D3	H11-14
D4	H11-5
D5	H10-5
D6	H10-11
D7	H11-11

PRE-RELEASE  
VERSION

D. ROM

SIGNAL	MNEMONIC	LOCATION
CS'	D0	F12-13
	D8	F12-12
	E0	F12-11
	E8	F12-10
	F0	F12-9
	F8	F12-7

E. RAM

SIGNAL	MNEMONIC	LOCATION
+12		PIN 8
+5		PIN 9
GND		PIN 16
-5		PIN 1
.....		
A0		PIN 10
A1		PIN 11
A2		PIN 12
A3		PIN 7
A4		PIN 6

A5	PIN 5
A6	PIN 13
.....	
RAS'	C2-15
.....	
CAS' : ROW C	F2-4
ROW D	F2-5
ROW E	F2-6
.....	
RAM R/W	C14-11
.....	
RAM SEL'	A2-6

F. ON-BOARD I/O

SIGNAL MNEMONIC	LOCATION
KBD	F13-15
KBDSTRB	F13-14
CASSETTE CLK	F13-13
CASSETTE OUT	K13-8
SPEAKER CLK	F13-12
SPEAKER OUT	K13-5
GAME I/O STRB	F13-11
9334 EN'	F13-10
251 EN'	F13-9
PDL TRIG	F13-7

G. PERIPHERAL I/O

SIGNAL MNEMONIC	LOCATION
DEV' : SLOT 0	H2-15
SLOT 1	H2-14
SLOT 2	H2-13
SLOT 3	H2-12
SLOT 4	H2-11
SLOT 5	H2-10
SLOT 6	H2-9
SLOT 7	H2-7
.....	
I/O SEL : SLOT 1	H12-14
SLOT 2	H12-13
SLOT 3	H12-12
SLOT 4	H12-11
SLOT 5	H12-10
SLOT 6	H12-9
SLOT 7	H12-7
.....	
I/O STRB'	F12-14

PRE-RELEASE  
VERSION

NOTE: Each location given represents the signal's point of origin (furthest upstream location). The schematic diagrams should be used to follow the signal downstream if necessary.

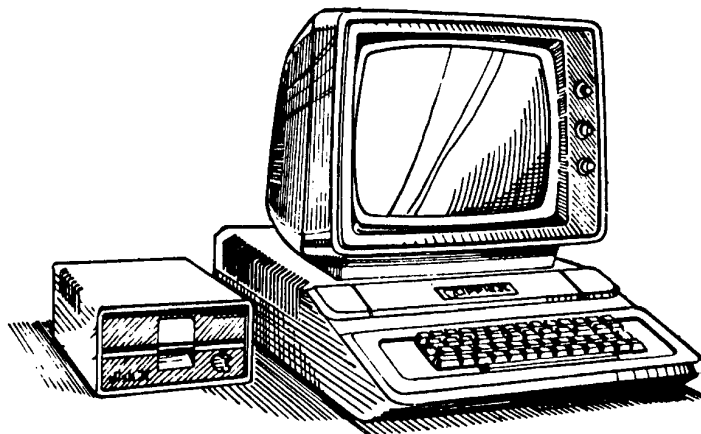


## Apple II Computer Technical Information

# APPLE II / APPLE II-PLUS LEVEL II SERVICE REFERENCE MANUAL

**Pre-Release Version**

**APPENDIX A  
IC CHIP MAPS • IC SPECIFICATIONS  
6502 INSTRUCTIONS • ROM LISTINGS**



**Written by  
Apple Computer, Inc. • Level II Service Center  
1981**

( This page is not part of the original service manual )

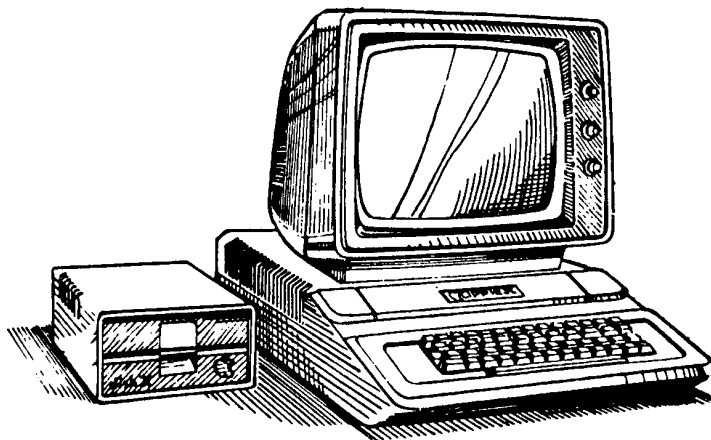


## Apple II Computer Technical Information

# APPLE II / APPLE II-PLUS LEVEL II SERVICE REFERENCE MANUAL

**Pre-Release Version**

## APPENDIX A IC CHIP MAPS

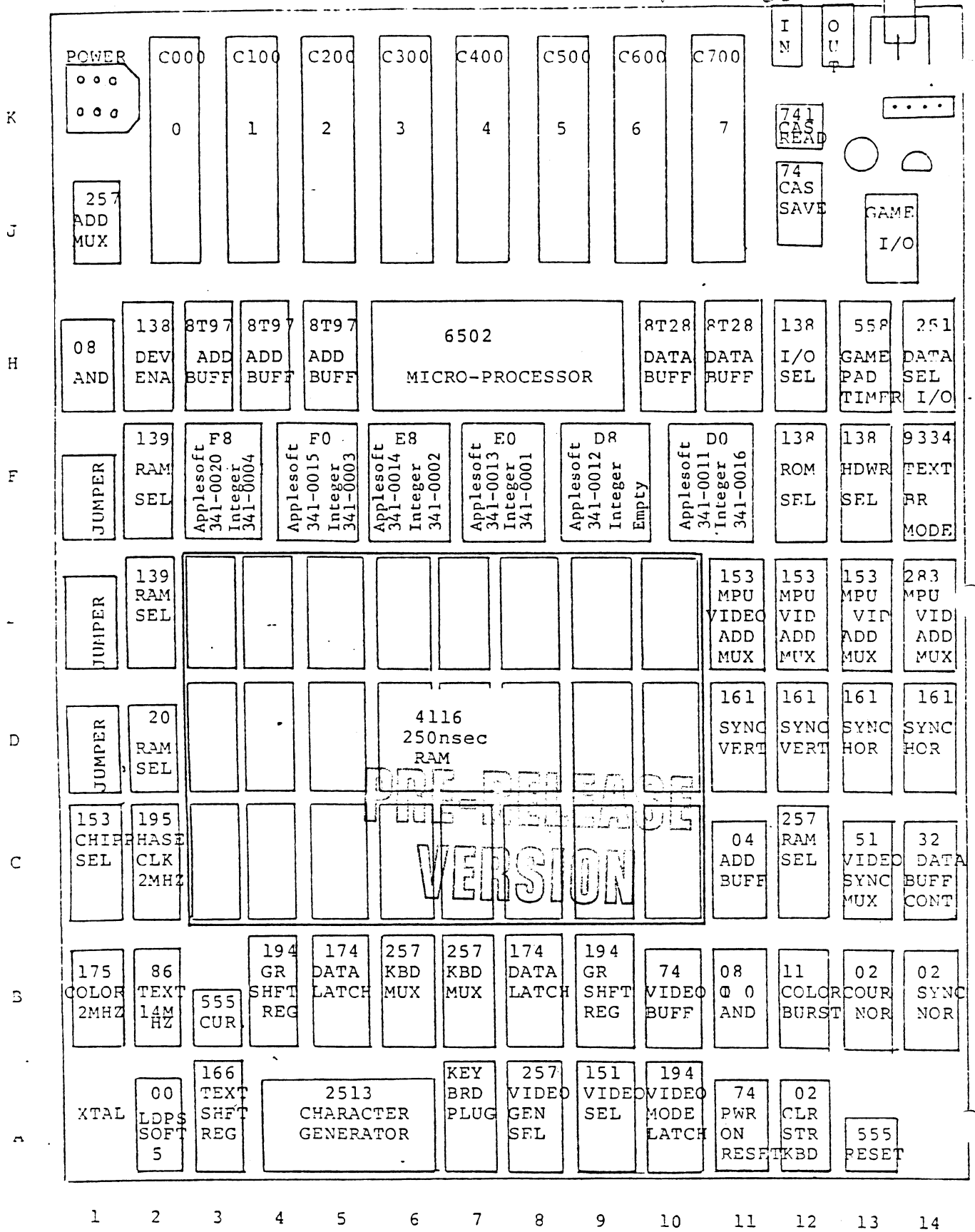


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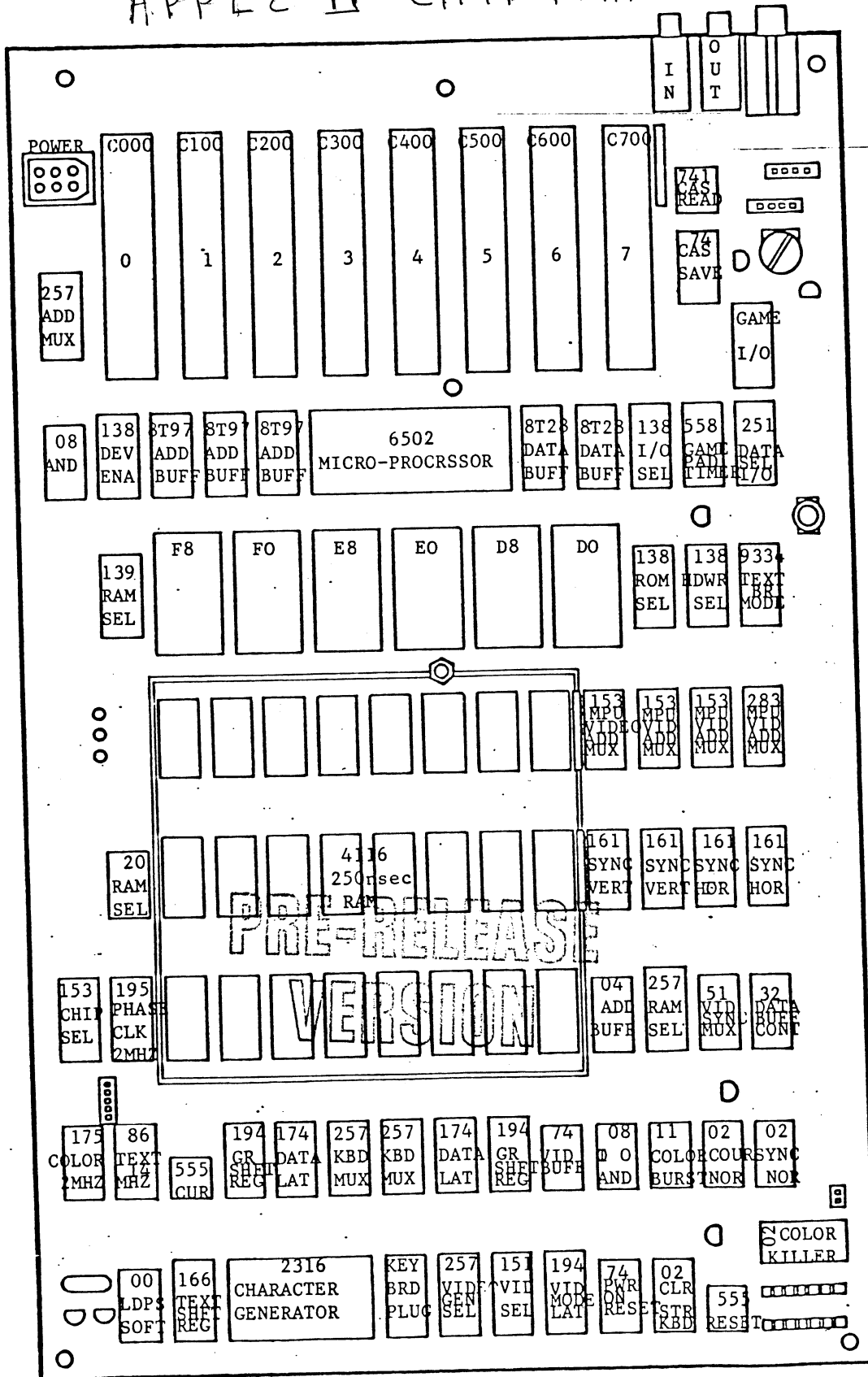
APPLE II CHIP MAP

*200 CC*



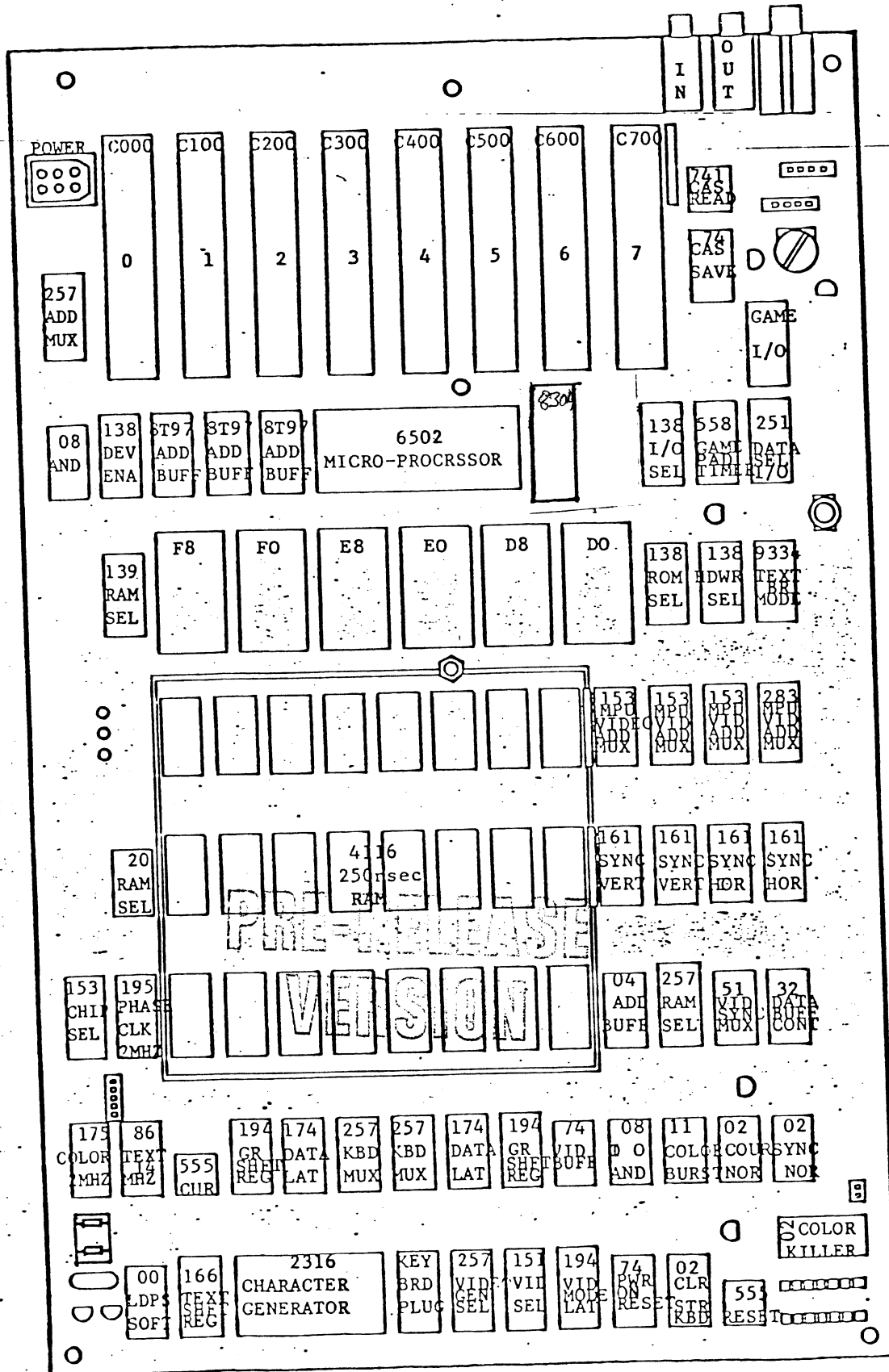
# APPLE II CHIP MAP

REV 7



820-0044

Rev B



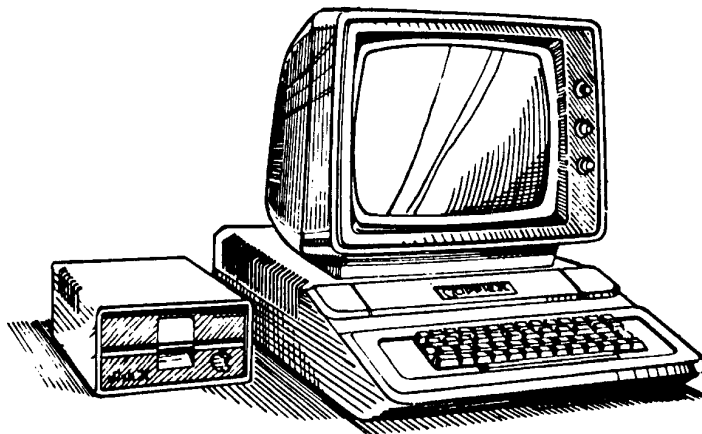


## Apple II Computer Technical Information

# APPLE II / APPLE II-PLUS LEVEL II SERVICE REFERENCE MANUAL

**Pre-Release Version**

## APPENDIX A IC SPECIFICATIONS



**Written by  
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1981**

( This page is not part of the original service manual )



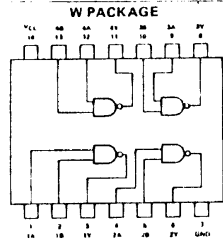
# QUADRUPLE 2-INPUT POSITIVE NAND GATE

S54S00/S03-A,F,W • N74S00/S03-A,F

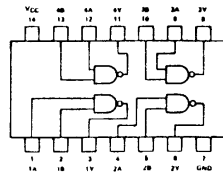
DIGITAL 54/74 TTL SERIES

S54S00  
N74S00  
N74S03

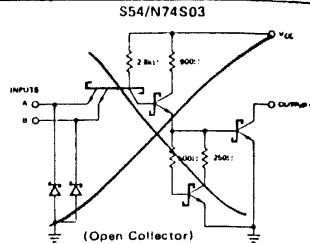
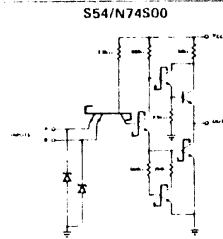
FIGURATIONS



A,F PACKAGE



TIC (each gate)



NOTE:  
Component values shown are nominal

ENDED OPERATING CONDITIONS

PARAMETER	S54S00			N74S00		
	MIN	NOM	MAX	MIN	NOM	MAX
Supply Voltage, V <sub>CC</sub>	4.5	5	5.5	4.75	5	5.25
Load Capacitance, C <sub>L</sub> (from each Output, N: High logic level)			20			20
Load Capacitance, C <sub>L</sub> (from each Output, N: Low logic level)			10			10
Free-Air Temperature, T <sub>A</sub>	-55		125	0		70

AL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted) (74S00)

PARAMETER	TEST CONDITIONS *	MIN	TYP **	MAX
High level input voltage			2	
Low level input voltage				0.8
Input clamp voltage	V <sub>CC</sub> = MIN, I <sub>I</sub> = -18mA			-12
High level output voltage	V <sub>CC</sub> = MIN, V <sub>IL</sub> = 0.8V, Series 54S I <sub>OH</sub> = -1mA, Series 74S	2.5	3.4	
Low level output voltage	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2V, I <sub>OL</sub> = 20mA			0.5
Input current at maximum input voltage	V <sub>CC</sub> = MAX, V <sub>I</sub> = 5.5V			1
High level input current (each input)	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7V			50
Low level input current (each input)	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.5V			-2
Short-circuit output current †	V <sub>CC</sub> = MAX	-40		-100
Supply current, high level output (average per gate)	V <sub>CC</sub> = MAX, All inputs at 0V		2.5	4
Supply current, low level output	V <sub>CC</sub> = MAX, All inputs at 5V		5	8

AGNETICS QUADRUPLE 2-INPUT POSITIVE NAND GATE ■ S54S00, S54S03, N74S00,

CHARACTERISTICS, V<sub>CC</sub> = 5V, T<sub>A</sub> = 25°C, N = 10 (74S00)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX
Propagation delay time, low-to-high level output	C <sub>L</sub> = 15pF, R <sub>L</sub> = 280Ω	2	3	4.5
Propagation delay time, high-to-low level output	C <sub>L</sub> = 15pF, R <sub>L</sub> = 280Ω	2	3	5
High level output voltage	C <sub>L</sub> = 50pF, R <sub>L</sub> = 280Ω		4.5	
Low level output voltage	C <sub>L</sub> = 50pF, R <sub>L</sub> = 280Ω		0.5	

NOTE 1

CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP **	MAX
High level input voltage		2		
Low level input voltage				0.8
Input clamp voltage	V <sub>CC</sub> = MIN, I <sub>I</sub> = -18mA			-12
High level output voltage	V <sub>CC</sub> = MIN, V <sub>IL</sub> = 0.8V, V <sub>OH</sub> = 5.5V, I <sub>OH</sub> = -1mA	2.5	3.4	
Low level output voltage	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2V, I <sub>OL</sub> = 20mA			0.5
Input current at maximum input voltage	V <sub>CC</sub> = MAX, V <sub>I</sub> = 5.5V			1
High level input current (each input)	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7V			50
Low level input current (each input)	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.5V			-2
Short-circuit output current †	V <sub>CC</sub> = MAX, All inputs at 0V	-40		-100
Supply current, high level output (average per gate)	V <sub>CC</sub> = MAX, All inputs at 0V		2.5	4
Supply current, low level output (average per gate)	V <sub>CC</sub> = MAX, All inputs at 5V		5	8

CHARACTERISTICS, V<sub>CC</sub> = 5V, T<sub>A</sub> = 25°C, N = 10

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX
Propagation delay time, low-to-high level output	C <sub>L</sub> = 15pF, R <sub>L</sub> = 280Ω	2	5	5ns
Propagation delay time, high-to-low level output	C <sub>L</sub> = 15pF, R <sub>L</sub> = 280Ω	2	4.5	7
High level output voltage	C <sub>L</sub> = 50pF, R <sub>L</sub> = 280Ω		4.5	
Low level output voltage	C <sub>L</sub> = 50pF, R <sub>L</sub> = 280Ω		0.5	

Values shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the device.  
 \* Test conditions are at V<sub>CC</sub> = 5V, T<sub>A</sub> = 25°C.  
 † For more than one output should be shorted at a time, and duration of the short-circuit test should not exceed one second.  
 Waveform examples are shown on page 2-293

PRE-RELEASE  
VERSION



QUADRUPLE 2-INPUT  
POSITIVE NOR GATE

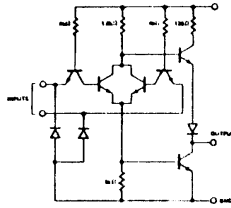
S5402  
N7402

S5402-A,F,W • N7402-A,F

DIGITAL 54/74 TTL SERIES

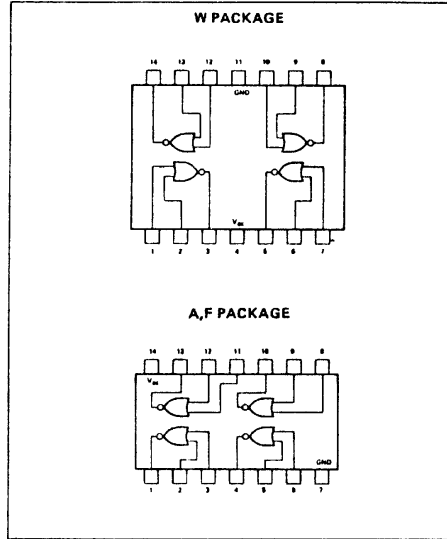
SIGNETICS QUADRUPLE 2-INPUT POSITIVE NOR GATE • S5402

FIG. 1 Schematic (each gate)



NOTE: Component values shown are nominal.

FIG. 2 PIN CONFIGURATIONS



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MIN	NOM	MAX	UNIT
Supply Voltage $V_{CC}$ : S5402 Circuits	4.5	5	5.5	V
N7402 Circuits	4.75	5	5.25	V
Normalized Fan-Out from each Output, $N$			10	
Operating Free-Air Temperature Range, $T_A$ : S5402 Circuits	-55	25	125	°C
N7402 Circuits	0	25	70	°C

STATIC CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER	TEST CONDITIONS*	MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at either input terminal to ensure logical 0 level at output	$V_{CC} = \text{MIN}$	2		V
$V_{in(0)}$	Logical 0 input voltage required at both input terminals to ensure logical 1 level at output	$V_{CC} = \text{MIN}$		0.8	V
$V_{out(1)}$	Logical 1 output voltage	$V_{CC} = \text{MIN}$ , $I_{load} = -400\mu\text{A}$	$V_{in} = 0.8\text{V}$	2.4 3.3	V
$V_{out(0)}$	Logical 0 output voltage	$V_{CC} = \text{MIN}$ , $I_{sink} = 16\text{mA}$	$V_{in} = 2\text{V}$	0.22 0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	$V_{CC} = \text{MAX}$ ,	$V_{in} = 0.4\text{V}$	-1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	$V_{CC} = \text{MAX}$ ,	$V_{in} = 2.4\text{V}$	40	$\mu\text{A}$
		$V_{CC} = \text{MAX}$ ,	$V_{in} = 5.5\text{V}$	1	
$I_{OS}$	Short circuit output	$V_{CC} = \text{MAX}$	S5402 N7402	-20 10	-55 55 mA

ELECTRICAL CHARACTERISTICS (Cont'd)

PARAMETER	TEST CONDITIONS*	MIN	TYP	MAX
$I_{CC(0)}$	Logical 0 level supply current	$V_{CC} = \text{MAX}$ , $V_{in} = 5\text{V}$	14	27
$I_{CC(1)}$	Logical 1 level supply current	$V_{CC} = \text{MAX}$ , $V_{in} = 0$	8	16

SWITCHING CHARACTERISTICS,  $V_{CC} = 5\text{V}$ ,  $T_A = 25^\circ\text{C}$ ,  $N = 10$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX
$t_{pd0}$	Propagation delay time to logical 0 level	$C_L = 15\text{pF}$ , $R_L = 400\Omega$	8	15
$t_{pd1}$	Propagation delay time to logical 1 level	$C_L = 15\text{pF}$ , $R_L = 400\Omega$	12	22

\* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the device type.  
\*\* All typical values are at  $V_{CC} = 5\text{V}$ ,  $T_A = 25^\circ\text{C}$ .  
† Not more than one output should be shorted at a time.

PRE-RELEASE  
VERSION

**SIGNETICS HEX INVERTER ■** S54S05, N74S05

SWITCHING CHARACTERISTICS,  $V_{CC} = 5V$ ,  $T_A = 25^\circ C$ ,  $N = 10$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX
$t_{PH}$	Propagation delay time, low-to-high level output	$C_L = 15 pF$ , $R_L = 280 \Omega$	2	3
		$C_L = 50 pF$ , $R_L = 280 \Omega$	NOTE 1	4.5
$t_{PL}$	Propagation delay time, high-to-low-level output	$C_L = 15 pF$ , $R_L = 280 \Omega$	2	3
		$C_L = 50 pF$ , $R_L = 280 \Omega$		5

**DC ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)**

PARAMETER	TEST CONDITIONS*	MIN	TYP**	MAX
$V_{IH}$	High-level input voltage			0.8
$V_{IL}$	Low-level input voltage			-1.2
$V_I$	Input clamp voltage	$V_{CC} = MIN$ , $I_I = -18mA$ , $V_{IL} = 0.8V$ ,		250
$I_{OH}$	High-level output current	$V_{OH} = 5.5V$ , $V_{CC} = MIN$ , $I_{OL} = 20mA$		0.5
$I_{OL}$	Low-level output current	$V_{CC} = MAX$ , $V_I = 5.5V$		1
$I_I$	Input current at maximum input voltage	$V_I = 2.7V$ , $V_{CC} = MAX$ ,		50
$I_{IH}$	High-level input current (each input)	$V_I = 0.5V$ , $V_{CC} = MAX$ ,		-2
$I_{IL}$	Low-level input current (each input)	All inputs at 0V		3.3
$I_{CCH}$	Supply current, high-level output (average per gate)		1.5	5
$I_{CCL}$	Supply current, low-level output (average per gate)		5	9

SWITCHING CHARACTERISTICS,  $V_{CC} = 5V$ ,  $T_A = 25^\circ C$ ,  $N = 10$

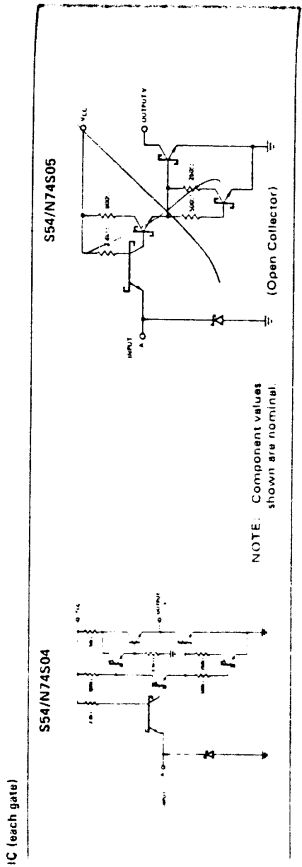
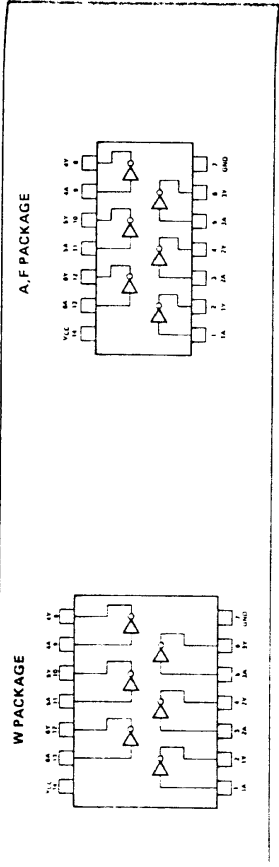
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX
$t_{PH}$	Propagation delay time, low-to-high level output	$C_L = 280pF$ , $R_L = 280\Omega$	2	5
		$C_L = 50pF$ , $R_L = 280\Omega$	NOTE	4.3
$t_{PL}$	Propagation delay time, high-to-low-level output	$C_L = 15pF$ , $R_L = 280\Omega$	2	4.5
		$C_L = 50pF$ , $R_L = 280\Omega$	1	7

\* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for device type.  
 \*\* All typical values are at  $V_{CC} = 5V$ ,  $T_A = 25^\circ C$ .  
 † Not more than one output should be shorted at a time, and duration of the short-circuit test should not exceed one second.  
 ‡ The pulse generator has the following characteristics:  $V_{in(1)} = 3V$ ,  $V_{in(0)} = 0V$ ,  $t_1 = t_0 = 2.5ns$ ,  $PRR = 1 MHz$ , duty cycle = 50%.  
 §  $t_{PLH}$  not under test are at 2.7V.  
 ¶  $t_{PLH}$  includes probe and jig capacitance.  
 †† NOTE 1: Load circuit and waveforms are shown on page 2-293

**PRE-RELEASE  
VERSION**

**HEX INVERTER**  
S54S05  
N74S04

S54S04-A,F,W • S54S05-A,F,W • N74S04-A,F,W • N74S05-A,F,W  
DIGITAL 54/74 TTL SERIES



**PERMITTED OPERATING CONDITIONS**

PARAMETER	S54S04		N74S04		UNIT
	MIN	NOM	MIN	MAX	
Supply Voltage, $V_{CC}$	4.5	5	4.75	5.25	V
Load Fan Out from each Output, N			10	20	
Free Air Temperature, $T_A$	-55		0	70	$^\circ C$

**DC ELECTRICAL CHARACTERISTICS (over recommended operating free air temperature range unless otherwise noted) (74S04)**

PARAMETER	TEST CONDITIONS*	MIN	TYP**	MAX	UNIT
High level input voltage		2		0.8	V
Low level input voltage				-1.2	V
Input clamp voltage	$V_{CC} = MIN$ , $I_I = -18mA$ , $V_{IL} = 0.8V$ ,	2.5	3.4		V
High level output voltage	$V_{OH} = 5.5V$ , $V_{CC} = MIN$ , $I_{OL} = 20mA$	2.7	3.4		V
Low level output voltage	$V_{CC} = MAX$ , $V_I = 5.5V$			0.5	V
Input current at maximum input voltage	$V_I = 2.7V$ , $V_{CC} = MAX$ ,			1	mA
High level input current (each input)	$V_I = 0.5V$ , $V_{CC} = MAX$ ,			50	$\mu A$
Low level input current (each input)	All inputs at 0V			-2	mA
Short circuit output current <sup>†</sup>		-40		-100	mA
Supply current, high level output (average per gate)			2.5	4	mA
Supply current, low level output (average per gate)					mA



# QUADRUPLE 2-INPUT POSITIVE AND GATES

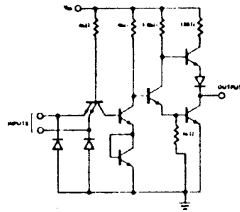
S5408  
N7408

S5408-A,F,W • N7408-A,F

DIGITAL 54/74 TTL SERIES

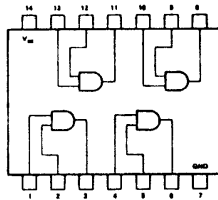
SIGNETICS QUADRUPLE 2-INPUT POSITIVE AND GATES ■ S

SCHEMATIC (each gate)

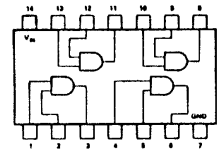


PIN CONFIGURATIONS

W PACKAGE



A PACKAGE



NOTE: Component values shown are nominal.

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply Voltage $V_{CC}$ : S5408 Circuits	4.5	5	5.5	V
N7408 Circuits	4.75	5	5.25	V
Normalized Fan-Out from Output, N			10	
Operating Free-Air Temperature Range, $T_A$ : S5408 Circuits	-55	25	125	°C
N7408 Circuits	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER	TEST CONDITIONS*	MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at both input terminals to ensure logical 1 level at output $V_{CC} = \text{MIN}$	2			V
$V_{in(0)}$	Logical 0 input voltage required at either input terminal to ensure logical 0 level at output $V_{CC} = \text{MIN}$			0.8	V
$V_{out(1)}$	Logical 1 output voltage $V_{CC} = \text{MIN}$ , $I_{load} = 800\mu\text{A}$	$V_{in} = 2.0\text{V}$ , 2.4	3.3		V
$V_{out(0)}$	Logical 0 output voltage $V_{CC} = \text{MIN}$ , $I_{sink} = 16\text{mA}$	$V_{in} = 0.8\text{V}$ , 0.22	0.4		V
$I_{in(0)}$	Logical 0 level input current (each input) $V_{CC} = \text{MAX}$	$V_{in} = 0.4\text{V}$		-1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input) $V_{CC} = \text{MAX}$ , $V_{CC} = \text{MAX}$	$V_{in} = 2.4\text{V}$ , $V_{in} = 5.5\text{V}$		40	$\mu\text{A}$ mA
$I_{OS}$	Open-circuit output current $V_{CC} = \text{MAX}$	S5408 N7408	-20 -18	-E -5b	mA

ELECTRICAL CHARACTERISTICS (Cont'd)

PARAMETER	TEST CONDITIONS*	MIN	TYP**
$I_{CC(1)}$	Logical 1 level supply current $V_{CC} = \text{MAX}$ , $V_{in} = 5\text{V}$		10
$I_{CC(0)}$	Logical 0 level supply current $V_{CC} = \text{MAX}$ , $V_{in} = 0$		18

SWITCHING CHARACTERISTICS,  $V_{CC} = 5\text{V}$ ,  $T_A = 25^\circ\text{C}$ ,  $N = 10$

PARAMETER	TEST CONDITIONS	MIN	TYP
$t_{pd0}$	Propagation delay time to logical 0 level $C_L = 15\text{pF}$ , $R_L = 400\Omega$		12
$t_{pd1}$	Propagation delay time to logical 1 level $C_L = 15\text{pF}$ , $R_L = 400\Omega$		17.5

\* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions device type.  
\*\* All typical values are at  $V_{CC} = 5\text{V}$ ,  $T_A = 25^\circ\text{C}$   
† Not more than one output should be shorted at a time.

PRE-RELEASE  
VERSION

# PRE-RELEASE VERSION

## TRIPLE 3-INPUT POSITIVE AND GATE

### DIGITAL 54/74 TTL SERIES

# N74S

# N74S1

**FEATURES**

**N74S11 ACTIVE PULL-UP**

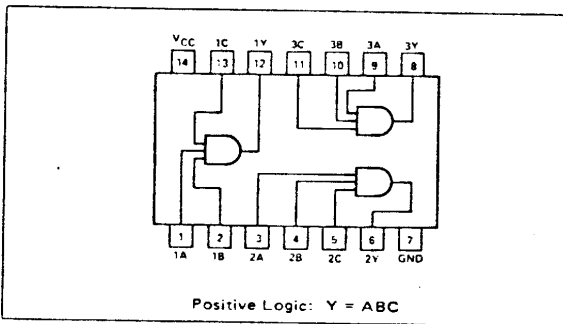
- TYPICAL PROPAGATION TIME
- TYPICAL POWER DISSIPATION AT 50% DUTY CYCLE

5 ns at  $C_L = 15$  pF  
32 mW PER GATE

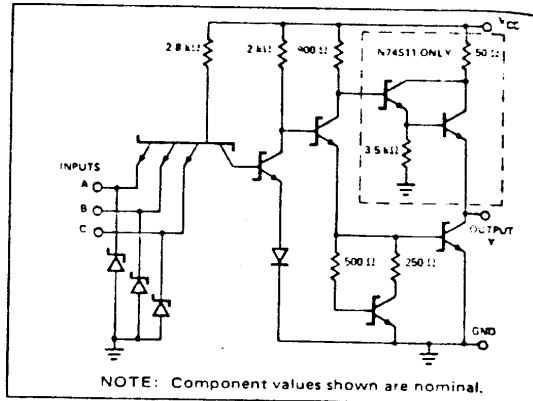
**N74S15 OPEN-COLLECTOR**

- TYPICAL PROPAGATION TIME
- TYPICAL POWER DISSIPATION AT 50% DUTY CYCLE

6 ns at  $C_L = 15$  pF  
29 mW PER GATE



**SCHEMATIC (each gate)**



**RECOMMENDED MAXIMUM FAN-OUT FROM EACH OUTPUT**

	N74S11	N74S15
Loads at a high logic level	20	10
Loads at a low logic level	10	10

**ELECTRICAL CHARACTERISTICS** (over operating free-air temperature range unless otherwise noted)

PARAMETER	TEST CONDITIONS*	N74S11			N74S15			UNIT
		MIN	TYP**	MAX	MIN	TYP**	MAX	
$V_{IH}$ High-level input voltage		2			2			V
$V_{IL}$ Low-level input voltage				0.8			0.8	V
$V_I$ Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.2			-1.2	V
$V_{OH}$ High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OH} = -1 \text{ mA}$	2.7	3.4					V
$I_{OH}$ High-level output current	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{OH} = 5.5 \text{ V}$						250	mA
$V_{OL}$ Low-level output voltage	$V_{CC} = \text{MIN}, V_{IL} = 0.8 \text{ V}, I_{OL} = 20 \text{ mA}$			0.5			0.5	V
$I_I$ Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1			1	mA
$I_{IH}$ High-level input current (each input)	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			50			50	μA
$I_{IL}$ Low-level input current (each input)	$V_{CC} = \text{MAX}, V_I = 0.5 \text{ V}$			-2			-2	mA
$I_{OS}$ Short-circuit output current †	$V_{CC} = \text{MAX}$	-40		-100				mA
$I_{CCH}$ Supply current, high-level output (average per gate)	$V_{CC} = \text{MAX}, \text{ All inputs at } 5 \text{ V}$	4.5	8		3.5	6.5		mA
$I_{CCL}$ Supply current, low-level output (Average per gate)	$V_{CC} = \text{MAX}, \text{ All inputs at } 0 \text{ V}$	8	14		8	14		mA

\*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable series on the second page of this section.

\*\*All typical values are at  $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$ .

†Not more than one output should be shorted at a time, and duration of the short-circuit test should not exceed one second.

**SWITCHING CHARACTERISTICS,  $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}, N = 10$**

PARAMETER	TEST CONDITIONS NOTE 1	N74S11			N74S15			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
$t_{PLH}$ Propagation delay time, low-to-high-level output	$C_L = 15 \text{ pF}, R_L = 280 \Omega$	2.5	4.5	7	2.5	5.5	8.5	ns
	$C_L = 50 \text{ pF}, R_L = 280 \Omega$		6			8.5		ns
$t_{PHL}$ Propagation delay time, high-to-low-level output	$C_L = 15 \text{ pF}, R_L = 280 \Omega$	2.5	5	7.5	2.5	6	9	ns
	$C_L = 50 \text{ pF}, R_L = 280 \Omega$		7.5			8		ns

NOTE 1: Load circuits and waveforms are shown on page 2-293

**PRE-RELEASE**

**DUAL 4-INPUT POSITIVE NAND GATE**

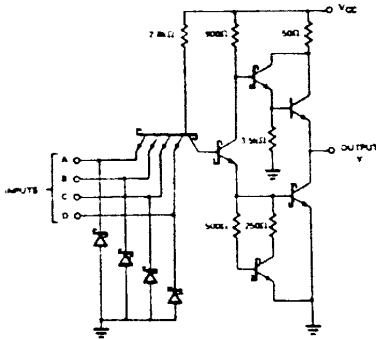
**S54S20**  
**N74S20**

S54S20-A,F,W • N74S20-A,F  
DIGITAL 54/74 TTL SERIES

**PRE-RELEASE**

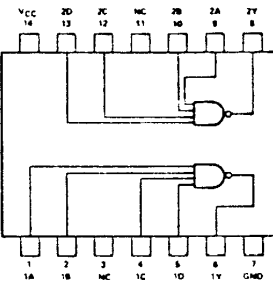
SCHEMATIC (each gate)

**VERSION**

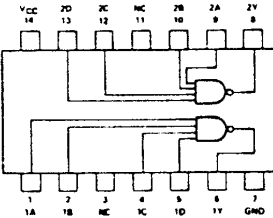


NOTE: Component values shown are nominal.

W PACKAGE



A,F PACKAGE



**RECOMMENDED OPERATING CONDITIONS**

PARAMETER	S54S20			N74S20			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage $V_{CC}$	4.5	5	5.5	4.75	5	5.25	V
Normalized Fan-Out from each Output, N:							
High logic level			20			20	
Low logic level			10			10	
Operating Free-Air Temperature, $T_A$	-55		125	0		70	°C

**ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)**

PARAMETER	TEST CONDITIONS*	MIN	TYP**	MAX	UNIT	
$V_{IH}$	High-level input voltage	2			V	
$V_{IL}$	Low-level input voltage			0.8	V	
$V_I$	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18\text{mA}$		-1.2	V	
$V_{OH}$	High-level output voltage	$V_{CC} = \text{MIN}, I_{OH} = -1\text{mA}$	2.5	3.4	V	
		$V_{CC} = \text{MIN}, V_{IH} = 2\text{V}, I_{OL} = 20\text{mA}$	2.7	3.4	V	
$V_{OL}$	Low-level output voltage			0.5	V	
$I_I$	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5\text{V}$		1	mA	
$I_{IH}$	High-level input current (each input)	$V_{CC} = \text{MAX}, V_I = 2.7\text{V}$		50	µA	
$I_{IL}$	Low-level input current (each input)	$V_{CC} = \text{MAX}, V_I = 0.5\text{V}$		-2	mA	
$I_{OS}$	Short-circuit output current †	$V_{CC} = \text{MAX}$	-40	-100	mA	
$I_{CCH}$	Supply current, high-level output (average per gate)	$V_{CC} = \text{MAX},$ All inputs at 0V		2.5	4	mA
$I_{CCL}$	Supply current, low-level output (average per gate)	$V_{CC} = \text{MAX},$ All inputs at 5V		5	9	mA

2-283



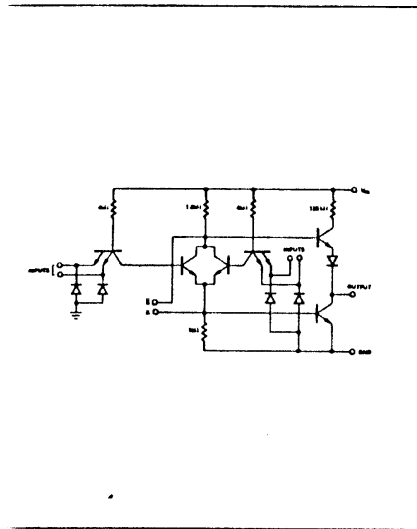
# EXPANDABLE DUAL 2-WIDE 2-INPUT AND-OR-INVERT GATES

S5450A,F,W • S5451-A,F,W • N7450-A,F • N7451-A,F

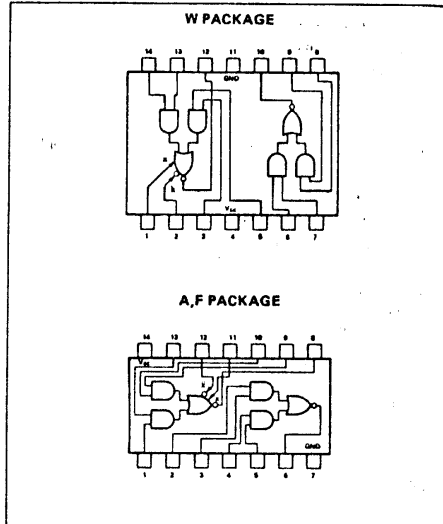
DIGITAL 54/74 TTL SERIES

S5450  
S5451  
N7450  
N7451

SCHEMATIC (each gate)



PIN CONFIGURATIONS



NOTES:  
1. Component values shown are nominal.  
2. Both expander inputs are used simultaneously for expanding.  
3. If expander is not used leave X and  $\bar{X}$  pins open.

- Make no external connection to X and  $\bar{X}$  pins of the S5451 and N7451.
- A total of four expander gates can be connected to the expander inputs.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MIN	NOM	MAX	UNIT
Supply Voltage $V_{CC}$ : S5450, S5451 Circuits	4.5	5	5.5	V
N7450, N7451 Circuits	4.75	5	5.25	V
Normalized Fan-Out from Output, N			10	
Operating Free-Air Temperature Range, $T_A$ : S5450, S5451 Circuits	-65	25	125	$^{\circ}$ C
N7450, N7451 Circuits	0	25	70	$^{\circ}$ C

CRITICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER	TEST CONDITIONS*	MIN	TYP**	MAX	UNIT
$V_{in(1)}$ Logical 1 input voltage required at both input terminals of either AND section to ensure logical 0 at output	$V_{CC} = \text{MIN}$	2			V
$V_{in(0)}$ Logical 0 input voltage required at one input terminal of each AND section to ensure logical 1 at output	$V_{CC} = \text{MIN}$			0.8	V
$V_{out(1)}$ Logical 1 output voltage	$V_{CC} = \text{MIN}$ , $I_{load} = -400\mu\text{A}$	2.4	3.3		V
$V_{out(0)}$ Logical 0 output voltage	$V_{CC} = \text{MIN}$ , $I_{sink} = 16\text{mA}$	0.22	0.4		V

SYNTHETICS EXPANDABLE DUAL 2-WIDE 2-INPUT AND-OR-INVERT GATES - S5450/S51, P

ELECTRICAL CHARACTERISTICS (Cont'd)

PARAMETER	TEST CONDITIONS*	MIN	TYP**	MAX
$I_{in(0)}$ Logical 0 level input current (each input)	$V_{CC} = \text{MAX}$ , $V_{in} = 0.4\text{V}$			-1.6
$I_{in(1)}$ Logical 1 level input current (each input)	$V_{CC} = \text{MAX}$ , $V_{in} = 2.4\text{V}$			40
$I_{sc}$ Short circuit output current†	$V_{CC} = \text{MAX}$		S5450, S5451 N7450, N7451	-20 -55
$I_{CC(0)}$ Logical 0 level supply current	$V_{CC} = \text{MAX}$ , $V_{in} = 5\text{V}$		7.4	14
$I_{CC(1)}$ Logical 1 level supply current	$V_{CC} = \text{MAX}$ , $V_{in} = 0$		4	8

ELECTRICAL CHARACTERISTICS (S5450 circuits) using expander inputs,  $V_{CC} = 4.5\text{V}$ ,  $T_A = -55^{\circ}\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP**	MAX
$I_E$ Expander current	$V_1 = 0.4\text{V}$ , $I_{sink} = 16\text{mA}$			2.9
$V_{BE(O)}$ Base-emitter voltage of output transistor (Q)	$I_{sink} = 16\text{mA}$ , $R_1 = 0$		0.41mA	1
$V_{out(1)}$ Logical 1 output voltage	$I_{load} = -400\mu\text{A}$ , $I_2 = -0.15\text{mA}$	2.4	3.3	
$V_{out(0)}$ Logical 0 output voltage	$I_{sink} = 16\text{mA}$ , $R_1 = 138\Omega$		0.3mA	0.4

ELECTRICAL CHARACTERISTICS (N7450 circuits) using expander inputs,  $V_{CC} = 4.75\text{V}$ ,  $T_A = 0^{\circ}\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP**	MAX
$I_E$ Expander current	$V_1 = 0.4\text{V}$ , $I_{sink} = 16\text{mA}$			3.1
$V_{BE(O)}$ Base-emitter voltage of output transistor (Q)	$I_{sink} = 16\text{mA}$ , $R_1 = 0$		0.62mA	1
$V_{out(1)}$ Logical 1 output voltage	$I_{load} = -400\mu\text{A}$ , $I_2 = -270\mu\text{A}$	2.4	3.3	
$V_{out(0)}$ Logical 0 output voltage	$I_{sink} = 16\text{mA}$ , $R_1 = 130\Omega$		0.43mA	0.4

CRITICAL CHARACTERISTICS,  $V_{CC} = 5\text{V}$ ,  $T_A = 25^{\circ}\text{C}$ , N = 10

PARAMETER	TEST CONDITIONS*	MIN	TYP	MAX
$t_{pd(0)}$ Propagation delay time to logical 0 level	$C_L = 15\text{pF}$ , $R_L = 400\Omega$		8	15
$t_{pd(1)}$ Propagation delay time to logical 1 level	$C_L = 15\text{pF}$ , $R_L = 400\Omega$		13	22

\*The conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the device. Both expander inputs X and  $\bar{X}$  are open.  
\*\*All typical values are at  $V_{CC} = 5\text{V}$ ,  $T_A = 25^{\circ}\text{C}$ .  
†This value is one output should be shorted at a time.

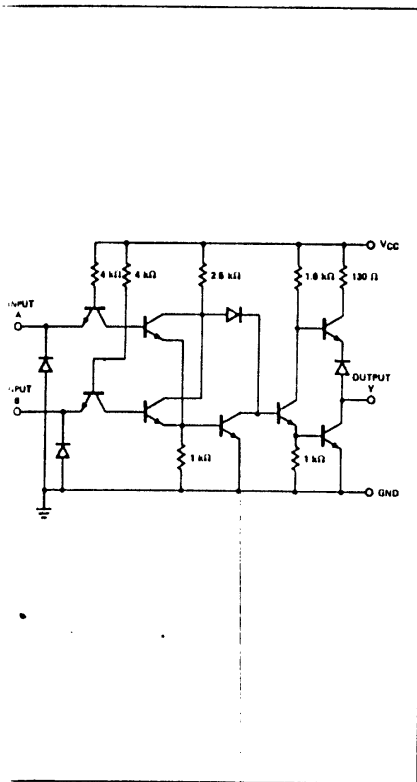
PRE-RELEASE  
VERSION

S5432F/W/A • N7432A/F  
DIGITAL 54/74 TTL SERIES

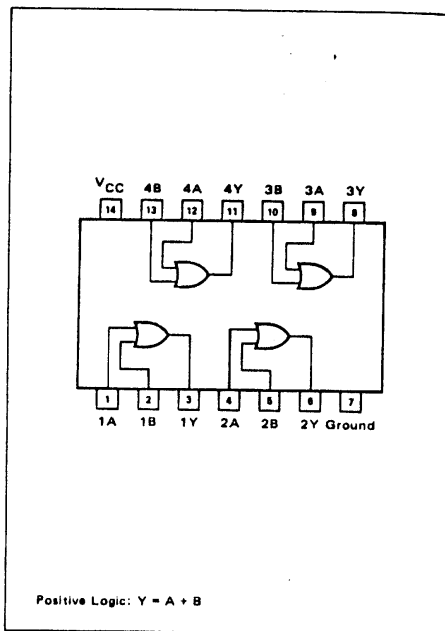
DESCRIPTION

The 54/7432 provides four 2 input or logic functions. Each gate may be used individually or connected serially to provide an equivalent five input or function.

SCHEMATIC (Each gate)



PIN CONFIGURATION (Top View) \*



\* Pin assignments for these circuits are the same for all packages.

ABSOLUTE MAXIMUM RATINGS

- Supply voltage,  $V_{CC}$  (see Note 1) . . . . . 7 V
- Input voltage . . . . . 5.5 V
- Operating free-air temperature range:
  - 5432 Circuits . . . . . -55°C to 125°C
  - 7432 Circuits . . . . . 0°C to 70°C
- Storage temperature range . . . . . -65°C to 150°C

NOTE:  
1. Voltage values are with respect to network ground terminal.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	5432			7432			UNIT
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
Supply voltage, $V_{CC}$	4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level		20	Low logic level		10	
	Low logic level		10	High logic level		20	
Operating free-air temperature, $T_A$	-55	25	125	0	25	70	°C

ELECTRICAL CHARACTERISTICS

PARAMETER	TEST CONDITIONS†	MIN.	TYP‡
$V_{IH}$	High-level input voltage	2	
$V_{IL}$	Low-level input voltage		
$V_I$	Input clamp voltage	$V_{CC} = \text{MAX.}$ $I_I = -12 \text{ mA}$	
$V_{OH}$	High-level output voltage	$V_{CC} = \text{MIN.}$ $V_{IH} = 2 \text{ V}$ , $I_{OH} = -800 \mu\text{A}$	2.4 3.3
$V_{OL}$	Low-level output voltage	$V_{CC} = \text{MIN.}$ $V_{IL} = 0.8 \text{ V}$ , $I_{OL} = 16 \text{ mA}$	0.22
$I_I$	Input current at maximum input voltage	$V_{CC} = \text{MAX.}$ $V_I = 5.5 \text{ V}$	
$I_{IH}$	High-level input current	$V_{CC} = \text{MAX.}$ $V_I = 2.4 \text{ V}$	
$I_{IL}$	Low-level input current	$V_{CC} = \text{MAX.}$ $V_I = 0.4 \text{ V}$	
$I_{OS}$	Short-circuit output current §	$V_{CC} = \text{MAX.}$	5432 -20
			7432 -18
$I_{CCH}$	Supply current, high-level output	$V_{CC} = \text{MAX.}$ See Note 2	15
$I_{CCL}$	Supply current, low-level output	$V_{CC} = \text{MAX.}$ See Note 3	23

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for type.

‡ All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ \text{C}$ .

§ Not more than one output should be shorted at a time.

NOTES: 2.  $I_{CCH}$  is measured with one input of each gate at 4.5 V, the remaining inputs grounded, and outputs open.

3.  $I_{CCL}$  is measured with both inputs of all gates grounded, and outputs open.

SWITCHING CHARACTERISTICS  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ \text{C}$ ,  $N = 10$

PARAMETER	TEST CONDITIONS	MIN.	T
$t_{PHL}$	Propagation delay time, high-to-low-level output	$C_L = 15 \text{ pF}$ , $R_L = 400 \Omega$	
$t_{PLH}$	Propagation delay time, low-to-high-level output		

PRE-RELEASE  
VERSION

**Signetics**

**PRE-RELEASE  
VERSION**

**DUAL D-TYPE  
EDGE-TRIGGERED FLIP-FLOPS**

**S54S74  
N74S74**

**DIGITAL 54/74 TTL SERIES**

**DESCRIPTION**

These monolithic dual edge-triggered flip-flops utilize Schottky TTL transistors to produce very high speed D-type flip-flops. Each flip-flop has individual clear and preset inputs, and also complementary Q and  $\bar{Q}$  outputs.

Information at input D is transferred to the Q output on the positive going edge of the clock pulse. Clock triggering occurs at a narrow level of the clock pulse and is not directly related to the duration time of the positive going pulse. When the clock input is at either the high or low level, the D-input signal has no effect.

These circuits are fully compatible for use with most TTL or DTL loads. A full fan-out to 10-normalized series 54S/74S loads is available from each of the outputs at low logic level. At a high logic level, a fan-out of 20 is available to facilitate tying unused inputs to high inputs. Maximum clock frequency is 75 megahertz, with a maximum power dissipation of 75 milliwatts per flip-flop.

The N74S74 is characterized for operation from 0°C to 70°C.

Typical Maximum Input Clock Frequency 90 MHz  
Typical Power Dissipation 75 mW per Flip-Flop

**TRUTH TABLE (Each Flip-Flop)**

INPUT	OUTPUT	
	Q	$\bar{Q}$
D	Q	$\bar{Q}$
L	L	H
H	H	L

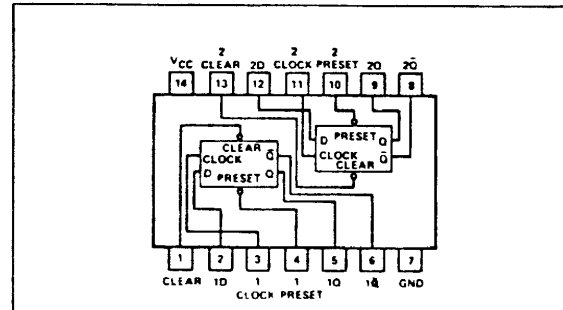
H = High level, L = Low level

NOTES: A.  $t_n$  = bit time before clock pulse  
B.  $t_{n+1}$  = bit time after clock pulse

**RECOMMENDED OPERATING CONDITIONS**

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, V <sub>CC</sub>	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level		20	
	Low logic level		10	
Clock frequency, f <sub>clock</sub>		70		MHz
Width of clock pulse, t <sub>w</sub> (clock)		7		ns
Width of preset pulse, t <sub>w</sub> (preset)		7		ns
Width of clear pulse, t <sub>w</sub> (clear)		7		ns
Input set-up time, t <sub>setup</sub>	High level data	10		ns
	Low level data	12		ns
Input hold time, t <sub>hold</sub>	0			ns
Operating free-air temperature, T <sub>A</sub>	0		70	°C

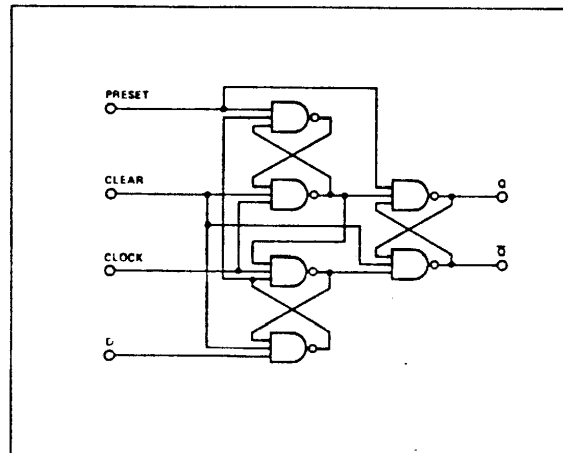
**PIN CONFIGURATION**



Positive Logic:

Low input to preset sets Q to high level  
Low input to clear resets Q to low level  
Preset and clear are independent of clock

**FUNCTIONAL BLOCK DIAGRAM (EACH FLIP-FLOP)**



**SIGNETICS DUAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS ■ S54S74,N74S74**

**ELECTRICAL CHARACTERISTICS**

PARAMETER		TEST CONDITIONS*	MIN	TYP**	MAX	UNIT
V <sub>IH</sub>	High level input voltage		2			V
V <sub>IL</sub>	Low level input voltage				0.8	V
V <sub>I</sub>	Input clamp voltage	V <sub>CC</sub> = MIN, I <sub>I</sub> = -18 mA			-1.2	V
V <sub>OH</sub>	High level output voltage	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V V <sub>IL</sub> = 0.8, I <sub>OL</sub> = 20 mA	2.7	3.4		V
V <sub>OL</sub>	Low level output voltage	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V V <sub>IL</sub> = 0.8, I <sub>OL</sub> = 20 mA			0.5	V
I <sub>I</sub>	Input current at maximum input voltage	V <sub>CC</sub> = MAX, V <sub>I</sub> = 5.5 V			1	mA
I <sub>IH</sub>	High level input current	V <sub>CC</sub> = MAX, D input			50	μA
		V <sub>I</sub> = 2.7 V, Clock or Preset			100	
		Clear			150	
I <sub>IL</sub>	Low level input current	V <sub>CC</sub> = MAX, D input			-2	mA
		V <sub>I</sub> = 0.5 V, Clock or Preset			-4	
		Clear			-6	
I <sub>OS</sub>	Short circuit output current †	V <sub>CC</sub> = MAX	-40		-100	mA
I <sub>CC</sub>	Supply Current	V <sub>CC</sub> = MAX, See Note 1		30		mA

\*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

\*\*All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

†Not more than one output should be shorted at a time, and duration of the short circuit test should not exceed one second.

**SWITCHING CHARACTERISTICS, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C, N = 10**

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f <sub>max</sub>	Maximum clock frequency	C <sub>L</sub> = 15 pF, R <sub>L</sub> = 280 Ω  NOTE 1		90		MHz
t <sub>PLH</sub>	Propagation delay time, low-to-high level output, from clear or preset			5		ns
t <sub>PHL</sub>	Propagation delay time, high-to-low level output, from clear or preset			8		ns
t <sub>PLH</sub>	Propagation delay time, low-to-high level output, from clock			7		ns
t <sub>PHL</sub>	Propagation delay time, high-to-low level output, from clock			7		ns

NOTE 1: Load circuit and test waveforms are shown on page 2-293

**PRE-RELEASE  
VERSION**

**signoties**

**QUAD EXCLUSIVE-OR, EXCLUSIVE-OR/  
NOR GATES**

**S54S86  
N74S86  
S54S135  
N74S135**

DIGITAL 54/74 TTL SERIES

PIN CONFIGURATION (Top View)\*

**FEATURES**

- FULLY COMPATIBLE WITH MOST TTL AND TTL MSI CIRCUITS
- FULLY SCHOTTKY CLAMPING REDUCES DELAY TIMES:
  - 7 ns Typical 54S86\*/74S86
  - 8 ns Typical 54S135\*/74S135
- 54S135\*, 74S135 CAN OPERATE AS EXCLUSIVE-OR GATE (C INPUT LOW) OR AS EXCLUSIVE-NOR GATE (C INPUT HIGH)

**ABSOLUTE MAXIMUM RATINGS**

Supply voltage (see Note 1) . . . . . 7 V  
 Input voltage . . . . . 5.5 V  
 Operating free-air temperature range:  
 54S86\*, 54S135\* Circuits . . . . . -55°C to 125°C  
 74S86, 74S135 Circuits . . . . . 0°C to 70°C  
 Storage temperature range . . . . . -65°C to 150°C

**NOTE:**

1 All voltage values are with respect to network ground terminal.

**FUNCTION TABLE 54S86\*, 74S86**

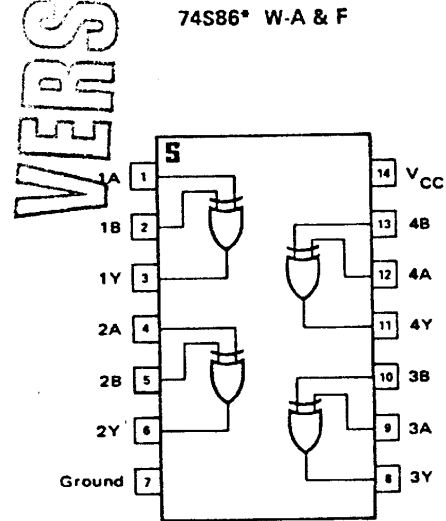
INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

\* H = High level, L = Low level

**FUNCTION TABLE 54S135\*, 74S135**

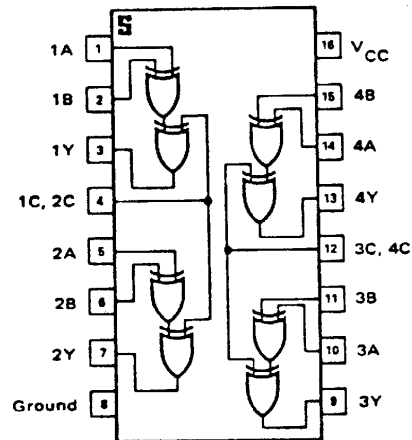
INPUTS			OUTPUT
A	B	C	Y
L	L	L	L
L	H	L	H
H	L	L	H
H	H	L	L
L	L	H	H
L	H	H	L
H	L	H	L
H	H	H	H

\* H = High level, L = Low level



Positive Logic:  $Y = A \oplus B = \bar{A}B + A\bar{B}$

**74S135\* W-B & F**



Positive Logic: With C low,  $Y = A \oplus B = \bar{A}B + A\bar{B}$   
 With C high,  $Y = A \oplus B = AB + \bar{A}\bar{B}$

\*Pin assignments same for all packages.

**SIGNETICS QUAD EXCLUSIVE-OR, EXCLUSIVE-OR/NOR GATES ■ S54/N74S86, S54/N74S135**

**ELECTRICAL CHARACTERISTICS** (Over recommended operating free-air temperature range. Unless otherwise noted.)

PARAMETER	TEST CONDITIONS*	MIN.	TYP.**	MAX.	UNIT
$V_{IH}$ High level input voltage		2			V
$V_{IL}$ Low-level input voltage				0.8	V
$V_I$ Input clamp voltage	$V_{CC} = \text{MIN.}, I_I = -18\text{mA}$			-1.2	V
$V_{OH}$ High-level output voltage	$V_{CC} = \text{MIN.}, I_I = -18\text{mA}$ Series 54S*	2.5	3.4		V
	$V_{IL} = 0.8\text{V}, I_{OH} = -1\text{mA}$ Series 74S*	2.7	3.4		
$V_{OL}$ Low-level output voltage	$V_{CC} = \text{MIN.}, V_{IH} = 2\text{V},$ $V_{IL} = 0.8\text{V}, I_{OL} = 20\text{mA}$			0.5	V
$I_I$ Input current at maximum input voltage	$V_{CC} = \text{MAX.}, V_I = 5.5\text{V}$			1	mA
$I_{IH}$ High-level input current	$V_{CC} = \text{MAX.}, V_I = 2.7\text{V}$			50	$\mu\text{A}$
$I_{IL}$ Low-level input current	$V_{CC} = \text{MAX.}, V_I = 0.5\text{V}$			-2	mA
$I_{OS}$ Short-circuit output current†	$V_{CC} = \text{MAX.}$	-40		-100	mA
$I_{CC}$ Supply current	$V_{CC} = \text{MAX.}$ See Note	54S86*			mA
		74S86			
		54S135*			
		74S135			

\* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

\*\* All typical values are  $V_{CC} = 5\text{V}, T_A = 25^\circ\text{C}$ .

† Not more than one output should be shorted at a time, and duration of the short-circuit test should not exceed one second.

NOTE:

$I_{CC}$  is measured with the inputs grounded and the outputs open.

**RECOMMENDED OPERATING CONDITIONS**

		54S86*	54S135*	74S86	74S135	UNIT		
		MIN.	NOM.	MAX.	MIN.		NOM.	MAX.
Supply voltage, $V_{CC}$		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			20			20	
	Low logic level			10			10	
Operating free-air temperature, $T_A$		-55		125	0		70	$^\circ\text{C}$

\* Full military version to be announced.

PRE-RELEASE  
VERSION

# Signetics 3-LINE-TO-8-LINE AND DUAL 2-LINE-TO-4-LINE DECODERS/DEMULTIPLEXERS

54/74S138  
54/74S139

DIGITAL 54/74 TTL SERIES

**DESCRIPTION**

These Schottky-clamped TTL MSI circuits are designed to be used in high-performance memory decoding or routing applications requiring very short propagation delays. In high-performance memory systems these decoders can be used to minimize the effects of system timing. When employed with high-speed memories requiring a fast-enable circuit the delay times of these decoders and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the Schottky-clamped system decoder is negligible.

The 54S138 and 74S138 decode one-of-eight lines dependent on the conditions at the three binary select inputs and the three enable inputs. Two active-low and one high enable inputs reduce the need for external gates and inverters when expanding. A 24-line decoder can be implemented without external inverters and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications. Typical delay time through the three-level address circuitry is 2.6 nanoseconds total or an average of 2.6 nanoseconds per level. Average power dissipation is typically 245 milliwatts or approximately 16 milliwatts each for the 15 output gates.

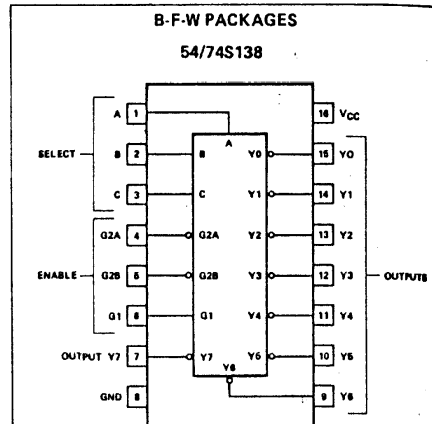
The 54S139 and 74S139 comprise two individual two-line-to-four-line decoders in a single package. The active-low enable input can be used as a data line in demultiplexing applications. Typical total delay time is 7.5 nanoseconds through the three-gate-level address circuitry. Power consumption is typically 300 milliwatts total.

These decoders/demultiplexers feature fully buffered outputs, each of which represents only one normalized Series 74S load to its driving circuit. All inputs are clamped to high-performance Schottky diodes to suppress ringing and simplify system design. The 54S138 and 74S138 are characterized for operation over the full military temperature range of -55°C to 125°C; the 74S138 and 74S139 are characterized for 0°C to 70°C industrial use.

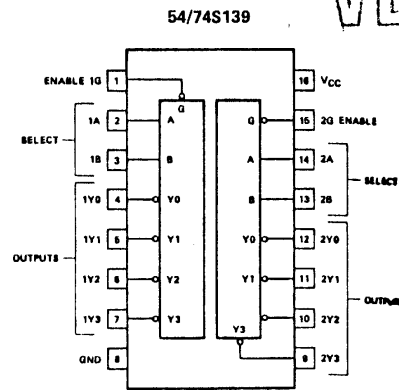
**Absolute Maximum Rating**

Supply Voltage, VCC (See Note 1)	7 V
Output Voltage	5.5 V
Operating Free-Air Temperature Range:	
54S138, 54S139 Circuits	-55°C to 125°C
74S138, 74S139 Circuits	0°C to 70°C

**PIN CONFIGURATIONS (Top View)**

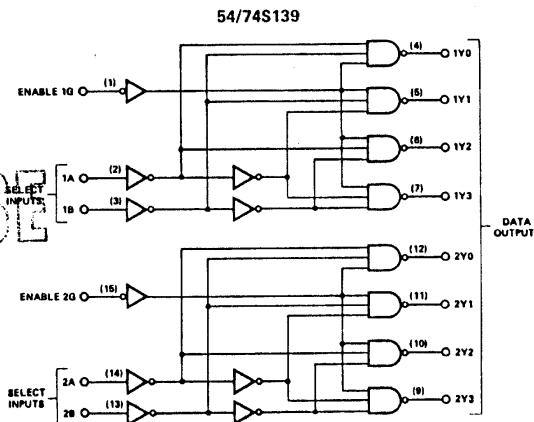
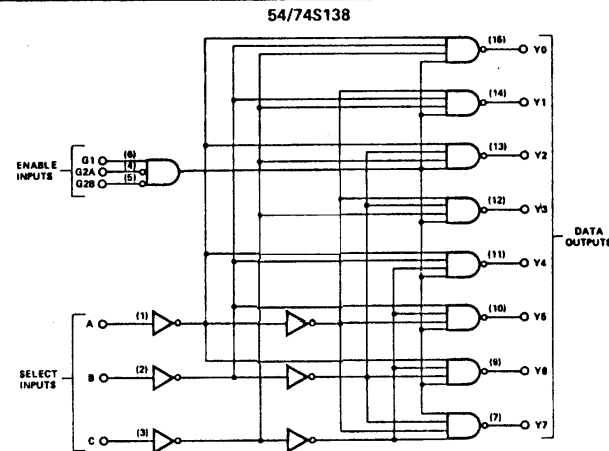


POSITIVE LOGIC: SEE FUNCTION TABLE



**BLOCK DIAGRAMS**

SIGNETICS DECODERS/DEMUL. LEXERS ■ 54/74S1:



54/74S138 FUNCTION TABLE

ENABLE		SELECT			OUTPUTS							
G1	G2 <sup>1</sup>	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
H	H	X	X	X	H	H	H	H	H	H	H	H
H	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	L	L	L	L	L	L
H	L	L	L	H	L	H	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	L	L	L	L
H	L	L	L	H	L	H	H	L	L	L	L	L
H	L	L	H	H	L	H	H	L	L	L	L	L
H	L	H	H	H	L	H	H	L	L	L	L	L
L	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
L	L	L	L	L	L	L	L	L	L	L	L	L
L	L	L	L	H	L	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	L	L	L	L
L	L	L	L	H	L	H	H	L	L	L	L	L
L	L	L	H	H	L	H	H	L	L	L	L	L
L	L	H	H	H	L	H	H	L	L	L	L	L

54/74S139 FUNCTION TABLE (EACH DECODER/DEMULTIPLE)

ENABLE		SELECT		OUTPUT	
G	B	A	Y0	Y1	
H	X	X	H	H	H
H	L	L	L	L	L
H	L	H	H	L	L
H	H	H	H	H	H

H = High level, L = Low level, X = Irrelevant

PRE-RELEASE  
VERSION

**SIGNETICS DECODERS/DEMULTIPLEXERS ■ 54/74S138, 54/74S139**

**RECOMMENDED OPERATING CONDITIONS**

PARAMETER		54S138 54S139			74S138 74S139			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V <sub>CC</sub>		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output N	High logic level			20			20	
	Low logic level			10			10	
Operating free-air temperature, T <sub>A</sub>		-55		125	0		70	°C

**RELEASE**

**VERSION**

**ELECTRICAL CHARACTERISTICS** (Over recommended operating free-air temperature range. Unless otherwise noted.)

PARAMETER	TEST CONDITIONS <sup>1</sup>	54S138 54S139			74S138 74S139			UNIT
		MIN	TYP <sup>2</sup>	MAX	MIN	TYP <sup>2</sup>	MAX	
V <sub>IH</sub> High-level input voltage		2			2			V
V <sub>IL</sub> Low-level input voltage				0.8			0.8	V
V <sub>I</sub> Input clamp voltage	V <sub>CC</sub> = MIN, I <sub>I</sub> = -18mA			-1.2			-1.2	V
V <sub>IH</sub> High-level output voltage	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2V, V <sub>IL</sub> = 0.8V, I <sub>OH</sub> = -1mA	Series 54S	2.5	3.4		2.5	3.4	V
		Series 74S	2.7	3.4		2.7	3.4	
V <sub>IL</sub> Low-level output voltage	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2V, V <sub>IL</sub> = 0.8V, I <sub>OL</sub> = 20mA			0.5			0.5	V
I <sub>I</sub> Input current at maximum input voltage	V <sub>CC</sub> = MAX, V <sub>I</sub> = 5.5V			1			1	mA
I <sub>IH</sub> High-level input current	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7V			50			50	μA
I <sub>IL</sub> Low-level input current	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.5V			-2			-2	mA
I <sub>OS</sub> Short-circuit output current <sup>3</sup>	V <sub>CC</sub> = MAX		-40		-100	-40		mA
I <sub>CC</sub> Supply current	V <sub>CC</sub> = MAX, Outputs enabled and open		49	74		60	90	mA

**NOTES:**

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
- All typical values are at V<sub>CC</sub> = 5V, T<sub>A</sub> = 25°C.
- Not more than one output should be shorted at a time, and duration of the short-circuit test should not exceed one second.

**SWITCHING CHARACTERISTICS** V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C, N = 10

PARAMETER <sup>1</sup>	FROM (INPUT)	TO (OUTPUT)	LEVELS OF DELAY	TEST CONDITIONS	54S138, 74S138			54S139 74S139			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
t <sub>PLH</sub>	Binary select	Any	2	C <sub>L</sub> = 15pF, R <sub>L</sub> = 280 Ω	4.5	7		5	7.5		ns
t <sub>PHL</sub>					7	10.5		6.5	10		
t <sub>PLH</sub>			3		7.5	12		7	12	ns	
t <sub>PHL</sub>					8	12		8	12		
t <sub>PLH</sub>	Enable	Any	2		5	8		5	8	ns	
t <sub>PHL</sub>					7	11		6.5	10		
t <sub>PLH</sub>			3		7	11				ns	
t <sub>PHL</sub>					7	11					

**NOTE:**

- t<sub>PLH</sub> ≡ propagation delay time, low-to-high-level output  
t<sub>PHL</sub> ≡ propagation delay time, high-to-low-level output



**8-INPUT DATA  
SELECTORS/MULTIPLEXERS**  
S54S151  
S54S251  
N74S151  
N74S251

**DIGITAL 54/74 TTL SERIES**

**DESCRIPTION**

The S54S151, S54S251, N74S151, and N74S251 Schottky-clamped, high-performance, eight-input data selectors/multiplexers are designed for use in very high-speed data routing applications. These multiplexers select one of eight data sources when so directed by the binary address inputs. Both true and complementary data are presented when the strobe input goes low.

**PRE-RELEASE  
VERSION**

The S54S151 and N74S151 are functionally and mechanically interchangeable with the S54151 and N74151 respectively, and in most TTL systems can be utilized to upgrade the performance of existing designs as delay times are typically half that of the S54151 or N74151.

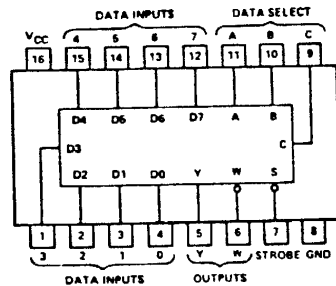
The S54S251 and N74S251 have three-state outputs which permit the outputs to be connected to a common bus. When the strobe input is high, both outputs are in a high-impedance state in which both the upper and lower transistors of each totem-pole output are off, and the output can neither drive nor load the bus. When the strobe input is low, the outputs are activated and operate as standard TTL totem-pole outputs.

Typical power dissipation is 225 milliwatts for the S54S151 or N74S151 and 275 milliwatts for the S54S251 and N74S251, or approximately 14 and 17 milliwatts respectively per equivalent gate. The S54S151 and S54S251 are characterized for operation over the military temperature range of -55°C to 125°C; the N74S151 and N74S251 are characterized for operation from 0°C to 70°C.

**RECOMMENDED OPERATING CONDITIONS**

PARAMETER	S54S151			S54S251			N74S151			N74S251			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V <sub>CC</sub>	4.5	5	5.5	4.5	5	5.5	4.75	5	5.25	4.75	5	5.25	V
Normalized fan-out from each output, N (at a low logic level)			10			10			10			10	
High-level output current, I <sub>OH</sub>			-1			-2			-1			-6.5	mA
Operating free-air temperature, T <sub>A</sub>	-55		125	-55		125	0		70	0		70	°C

**PIN CONFIGURATION**



Positive Logic: See function table.

**FEATURES**

- S54S151/N74S151 INTERCHANGEABLE WITH S54151/N74151 IN MOST SYSTEMS
- SCHOTTKY CLAMPED FOR SIGNIFICANT REDUCTION IN DELAY TIMES... 4.5 ns TYPICAL, DATA INPUT TO W OUTPUT
- HIGH-SPEED SELECTION FOR ONE OF EIGHT DATA SOURCES
- PERMITS MULTIPLEXING FROM N LINES TO ONE LINE
- S54S251 AND N74S251 HAVE TRI-STATE OUTPUTS
- FULLY COMPATIBLE WITH SERIES 54/74 AND OTHER TTL MSI CIRCUITS

**8-BIT B-INPUT DATA SELECTORS/MULTIPLEXERS ■ S54/N74S151, S54/N74S251**

**ALL CHARACTERISTICS** (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER	TEST CONDITIONS*	S54S151 N74S151		S54S251 N74S251		UNIT
		MIN	TYP**	MAX	MIN	
High-level input voltage		2		2		V
Low-level input voltage			0.8		0.8	V
Input clamp voltage	V <sub>CC</sub> = MIN, I <sub>I</sub> = -18 mA		-1.2		-1.2	V
High-level output voltage	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, Series 54S	2.5	3.4	2.4	3.2	V
	V <sub>IH</sub> = 0.8 V, I <sub>OH</sub> = MAX, Series 74S	2.7	3.4	2.4	3.2	
Low-level output voltage	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V,		0.5		0.5	V
	V <sub>IH</sub> = 0.8 V, I <sub>OL</sub> = 20 mA					
Off-state (high-impedance-state) output current	V <sub>CC</sub> = MAX, V <sub>O</sub> = 2.7 V				50	μA
Input current at maximum input voltage	V <sub>CC</sub> = MAX, V <sub>O</sub> = 0.4 V				-50	μA
High-level input current	V <sub>CC</sub> = MAX, V <sub>I</sub> = 5.5 V		1		1	mA
Low-level input current	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7 V		50		50	μA
Short-circuit output current†	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.5 V		-2		-2	mA
Supply current	V <sub>CC</sub> = MAX	-40	-100	-40	-100	mA
	V <sub>CC</sub> = MAX, All inputs at 4.5 V, All outputs open	45	70	55	85	mA

\*Conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the device type.  
 \*\*Typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.  
 †When one output should be shorted at a time, and duration of the short-circuit test should not exceed one second.

**LOGIC CHARACTERISTICS, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	S54S151, N74S151			S54S251, N74S251			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
Propagation delay time, low to high level output	A, B, or C (4 levels)	Y	C <sub>L</sub> = 15 pF, R <sub>L</sub> = 280 Ω, See Note 1	12	18		12	18	ns	
				12	18		13	19.5		
Propagation delay time, high to low level output	A, B, or C (3 levels)	W		10	15		10	15	ns	
				9	13.5		9	13.5		
Output enable time, high level	Any D	Y		8	12		8	12	ns	
				8	12		8	12		
Output enable time, low level	Any D	W		4.5	7		4.5	7	ns	
				4.5	7		4.5	7		
Output disable time from high level	Strobe	Y		11	16.5				ns	
				12	18					
Output disable time from low level	Strobe	W	9	13				ns		
			8.5	12						
Propagation delay time, low to high level output	Strobe	Y				13	19.5	ns		
						14	21			
Propagation delay time, high to low level output	Strobe	W				13	19.5	ns		
						14	21			
Output enable time, high level	Strobe	Y				6.5	8.5	ns		
						9	14			
Output enable time, low level	Strobe	W				5.5	8.5	ns		
						9	14			

†Propagation delay time, low to high level output  
 †Propagation delay time, high to low level output  
 †Output enable time, high level  
 †Output enable time, low level  
 †Output disable time from high level

**SIGNETICS 8-INPUT DATA SELECTORS/MULTIPLEXERS ■ S54/N74S151, S54/N74S251**

**FUNCTION TABLE**

SELECT			STROBE	INPUTS							OUTPUTS			
C	B	A		DATA							S54S151, N74S151	S54S251, N74S251	S54S251, N74S251	
			S	D0	D1	D2	D3	D4	D5	D6	D7	Y	W	Y
X	X	X	H	X	X	X	X	X	X	X	X	L	H	Z
L	L	L	L	L	X	X	X	X	X	X	X	L	H	L
L	L	L	L	H	X	X	X	X	X	X	X	H	L	H
L	L	H	L	X	L	X	X	X	X	X	X	L	H	L
L	L	H	L	X	H	X	X	X	X	X	X	H	L	H
L	H	L	L	X	X	L	X	X	X	X	X	L	H	L
L	H	L	L	X	X	H	X	X	X	X	X	H	L	H
L	H	H	L	X	X	X	L	X	X	X	X	L	H	L
L	H	H	L	X	X	X	H	X	X	X	X	H	L	H
H	L	L	L	X	X	X	X	L	X	X	X	L	H	L
H	L	L	L	X	X	X	X	H	X	X	X	H	L	H
H	L	H	L	X	X	X	X	X	L	X	X	L	H	L
H	L	H	L	X	X	X	X	X	H	X	X	H	L	H
H	H	L	L	X	X	X	X	X	X	L	X	L	H	L
H	H	L	L	X	X	X	X	X	X	H	X	H	L	H
H	H	H	L	X	X	X	X	X	X	X	L	L	H	L
H	H	H	L	X	X	X	X	X	X	X	H	H	L	H

H = high logic level, L = low logic level, Z = high impedance, X = irrelevant

PRE-RELEASE  
VERSION



DUAL 4-LINE TO 1-LINE  
DATA SELECTORS/MULTIPLEXERS

S54S  
N74S153

DIGITAL 54/74 TTL SERIES

DESCRIPTION

These are Schottky-barrier-diode-clamped TTL circuits that perform as data selectors/multiplexers which are significantly faster than standard TTL. As an example, the two-gate-level delay from the data inputs to the output is only 8.5 nanoseconds maximum for the N74S153. Overall, the guaranteed delay times for the S54S153 and N74S153 represent approximately a 100% improvement over standard TTL with only a 12% increase in maximum d-c power dissipation. In many cases, the S54S153 or N74S153 can plug into systems designed for S54153 or N74153.

These data selectors/multiplexers are fully compatible for use with standard, high-speed, and low-power TTL and DTL circuits. The Schottky-barrier-diode-clamped input represents only one normalized Series 54S/74S gate level, and full fan-out to 10 normalized Series 54S/74S gates is available from each of the outputs at low logic levels. A maximum of 10 normalized Series 54S/74S loads is provided at high logic levels to facilitate connection of unused inputs to used inputs. Maximum power dissipation is 225 milliwatts.

The S54S153 is characterized for operation over the full military temperature range of -55°C to 125°C; the N74S153 is characterized for operation from 0°C to 70°C.

These devices feature SCHOTTKY-BARRIER-DIODE CLAMPING FOR VERY FAST RISE AND FALL TIMES.

These devices are suitable for MULTIPLEXING FROM N LINES TO 1 LINE.

Pin assignments are the same as S54153 and N74153.

The ENABLE (EN) LINE PROVIDED FOR CASCADING IN MULTIPLE SECTIONS (10 n LINES).

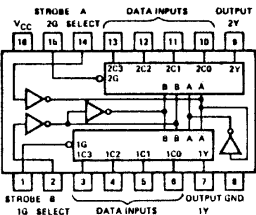
Typical AVERAGE PROPAGATION DELAY TIMES:  
 FROM DATA INPUT TO OUTPUT (2 GATE LEVELS) 6 ns  
 FROM STROBE INPUT TO OUTPUT (3 GATE LEVELS) 9.5 ns  
 FROM SELECT INPUT TO OUTPUT (4 GATE LEVELS) 12 ns

These devices feature LOW-IMPEDANCE TOTEM-POLE OUTPUTS.

These devices are COMPATIBLE WITH MOST TTL AND DTL CIRCUITS.

PIN CONFIGURATION

JORN DUAL-IN-LINE  
OR W FLAT PACKAGE (TOP VIEW)



LOGIC: SEE FUNCTION TABLE

FUNCTION TABLE

SELECT INPUTS	DATA INPUTS				STROBE	OUTPUT
B A	C0	C1	C2	C3	G	Y
X X	X	X	X	X	H	L
L L	L	X	X	X	L	L
L L	H	X	X	X	L	H
L H	X	L	X	X	L	L
L H	X	H	X	X	L	H
H L	X	X	L	X	L	L
H L	X	X	H	X	L	H
H H	X	X	X	L	L	L
H H	X	X	X	H	L	H

Address Inputs A and B are common to both sections.  
 H = High level, L = Low level, X = Irrelevant

SIGNETICS DUAL 4-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS = S54S153, N74S153

RECOMMENDED OPERATING CONDITIONS

PARAMETER	S54S153			N74S153		
	MIN	NOM	MAX	MIN	NOM	MAX
Supply voltage, V <sub>CC</sub>	4.5	5	5.5	4.75	5	6.25
Normalized fan-out from each output, N	High logic level	20		20		
	Low logic level	10		10		
Operating free-air temperature range, T <sub>A</sub>	-55		125	0		70

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER	TEST CONDITIONS*	MIN	TYP**	MAX	
V <sub>IH</sub>	High-level input voltage	2			
V <sub>IL</sub>	Low-level input voltage	2			
V <sub>I</sub>	Input clamp Voltage	0.8			
V <sub>OH</sub>	High-level output voltage	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = 0.8 V, I <sub>OH</sub> = -1 mA	Series 54S	2.5	3.4
V <sub>OL</sub>	Low-level output voltage	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = 0.8 V, I <sub>OL</sub> = 20 mA	Series 74S	2.7	3.4
I <sub>I</sub>	Input current at maximum input voltage	V <sub>CC</sub> = MAX, V <sub>I</sub> = 5.5 V	0.5		
I <sub>IH</sub>	High-level input current	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7 V	1		
I <sub>IL</sub>	Low-level input current	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.5 V	50		
I <sub>OS</sub>	Short-circuit output current ‡	V <sub>CC</sub> = MAX	-2		
I <sub>CC1</sub>	Supply current, low level output	V <sub>CC</sub> = MAX, See Note 1	-40	-100	
			45	70	

\* Conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.  
 \*\* Typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.  
 † More than one output should be shorted at a time.  
 ‡ Note: I<sub>CC1</sub> is measured with the outputs open and all inputs grounded.

PRE-RELEASE  
VERSION

LOADING CHARACTERISTICS, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C, N = 10

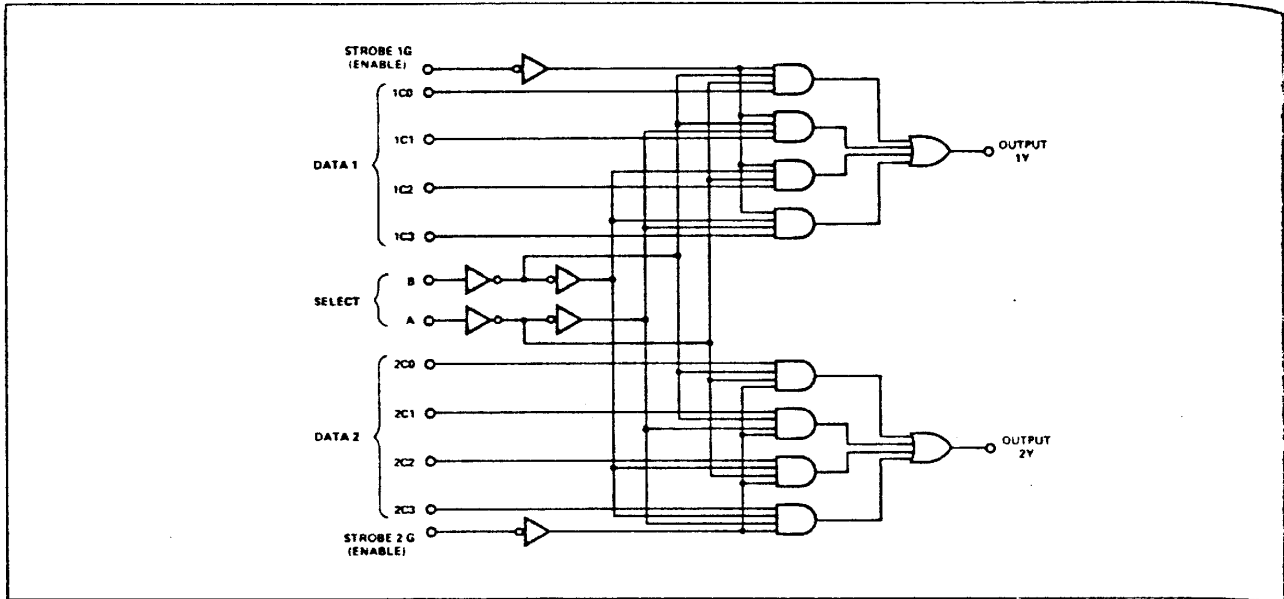
PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNI
t <sub>PLH</sub>	Data	Y	C <sub>L</sub> = 15 pF, R <sub>L</sub> = 280 Ω, See Note 2		6	9	ns
t <sub>PHL</sub>	Data	Y			6	9	ns
t <sub>PLH</sub>	Select	Y			11.5	18	ns
t <sub>PHL</sub>	Select	Y			12	18	ns
t <sub>PLH</sub>	Strobe	Y			10	15	ns
t <sub>PHL</sub>	Strobe	Y			9	13.5	ns

‡ Propagation delay time, low-to-high-level output.  
 ‡ Propagation delay time, high-to-low-level output.

Note 2: Load circuit and test waveforms are shown on page 2-293

SIGNETICS DUAL 4-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS ■ S54S153, N74S153

FUNCTIONAL BLOCK DIAGRAM



TEST TABLE FOR NOTE 2

INPUTS							OUTPUT Y WAVEFORM
B	A	C0	C1	C2	C3	G	
GND	GND	INPUT	X	X	X	GND	A
GND	4.5 V	X	INPUT	X	X	GND	A
4.5 V	GND	X	X	INPUT	X	GND	A
4.5 V	4.5 V	X	X	X	INPUT	GND	A
GND	INPUT	GND	4.5 V	X	X	GND	A
INPUT	GND	GND	X	4.5 V	X	GND	A
GND	GND	4.5 V	X	X	X	INPUT	B

X = Irrelevant    A=IN-PHASE OUTPUT  
 B=OUT-OF-PHASE

PRE-RELEASE  
 VERSION



SYNCHRONOUS 4-BIT COUNTER

S54160 N7  
 S54161 N74161  
 S54162 N74162  
 S54163 N74163

S54160-B,F,W • S54161-B,F,W • S54162-B,F,W • S54163-B,F,W  
 N74160-B,F • N74161-B,F • N74162-B,F • N74163-B,F

DIGITAL 54/74 TTL SERIES

DESCRIPTION

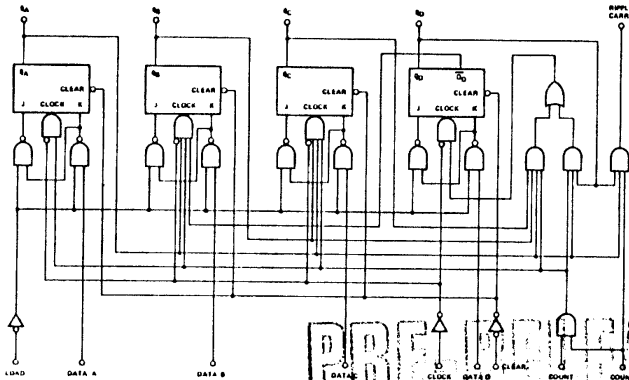
Synchronous, presettable counters feature an internal carry output for application in high-speed counting schemes. The S54162, N74160, and N74162 are decade counters and the S54163, N74161, and N74163 are 4-bit binary counters. Continuous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other as instructed by the count-enable inputs and internal clock. This mode of operation eliminates the output counting glitches normally associated with asynchronous (ripple) counters. A buffered clock input triggers the four J-K master-slaves on the rising (positive-going) edge of the clock input.

Inputs are diode-clamped to minimize transmission-line effects, simplifying system design. A full fan-out to ten normalized 74 loads is available from each of the outputs in the low-level state. A fan-out to 20 normalized Series 54/74 loads is provided in the high-level state to facilitate connection of unused inputs or outputs. Power dissipation is typically 325 milliwatts.

FUNCTIONAL DIAGRAM

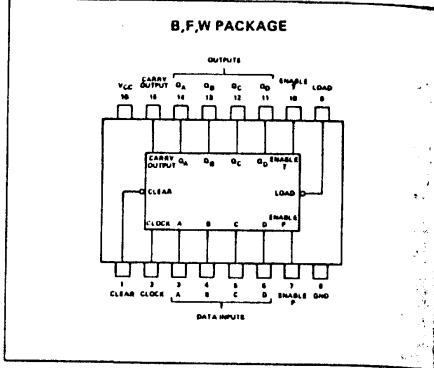
S54160/N74160 SYNCHRONOUS DECADE COUNTERS

(S54162/N74162 synchronous decade counters are similar; however the clear is asynchronous as shown for the S54163/N74163 binary counters).



PRE-RELEASE  
 VERSION

PIN CONFIGURATION

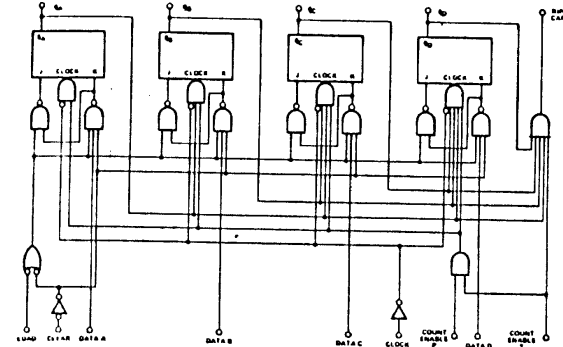


INTEGRATED CIRCUITS SYNCHRONOUS 4-BIT COUNTER ■ S54/N74160, S54/N74161, S54/N74162, S54/N74163

LOGIC DIAGRAM (Cont'd)

S54163/N74163 SYNCHRONOUS BINARY COUNTERS

S54161/N74161 synchronous binary counters are similar; however the clear is asynchronous as shown for the S54160/N74160 decade counters).



RECOMMENDED OPERATING CONDITIONS

PARAMETER	S54160, S54161 S54162, S54163			N74160, N74161 N74162, N74163		
	MIN	NOM	MAX	MIN	NOM	MAX
Supply Voltage V <sub>CC</sub>	4.5	5	5.5	4.75	5	5.25
Maximum Fan-Out from each Output, N:						
High logic level			20			20
Low logic level			10			10
Input Clock Frequency, f <sub>clock</sub>	0		25	0		25
Width of Clock Pulse, t <sub>w(clock)</sub>	25		25	25		25
Width of Clear Pulse, t <sub>w(clear)</sub>	20		20	20		20
Setup Time, t <sub>setup</sub> :						
Data Inputs, A, B, C, D	15		15	15		15
Enable P	20		20	20		20
Load	25		25	25		25
Clear	20		20	20		20
Hold Time at any Input, t <sub>hold</sub>	0		0	0		0
Operating Free Air Temperature, T <sub>A</sub>	-55	25	125	0	25	70

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise specified)

PARAMETER	TEST CONDITIONS*	S54160, S54161 S54162, S54163		N74160, N74161 N74162, N74163			UN
		MIN	TYP**	MAX	MIN	TYP**	
High-level input voltage		2					
Low-level input voltage	V <sub>CC</sub> = MAX,			0.8		2	
Input clamp voltage	V <sub>CC</sub> = MAX, V <sub>I</sub> = -12mA			-1.5		0.8	
High-level output voltage	V <sub>CC</sub> = MIN, V <sub>I</sub> L = 0.8V, I <sub>OH</sub> = -800μA	2.4			2.4		
Low-level output voltage	V <sub>CC</sub> = MIN, V <sub>I</sub> L = 0.8V, I <sub>OL</sub> = 16mA			0.4		0.4	
Input current at maximum input voltage	V <sub>CC</sub> = MAX, V <sub>I</sub> = 5.5V		1			1	
High-level Clock or enable T input current - Other inputs	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.4V		80			80	
Low-level Clock or enable T input current - Other inputs	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.4V		40			40	
Short-circuit output current†	V <sub>CC</sub> = MAX, V <sub>O</sub> = 0V		-3.2			-3.2	
Supply current, all outputs high	V <sub>CC</sub> = MAX, See Note 3		-1.6			-1.6	
			-20			-20	
			-57			-57	

# SIGNATICS

## HEX QUADRUPLE D-TYPE FLIP-FLOPS WITH CLEAR

S54S174  
S54S175  
N74S174  
DIGITAL 54/74 TTL SERIES N74S175

### DESCRIPTION

These high performance monolithic, positive-edge-triggered flip-flops utilize Schottky TTL technology to implement D-type flip-flops. All have a direct clear input, and the S54S175 and N74S175 feature complementary outputs from each flip-flop. Pin assignments for these Schottky flip-flops are identical to the standard TTL versions meaning that these Schottky versions can be used to upgrade existing system performance in most cases.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock signal. When the clock input is at either the high or low level, the D input signal has no effect at the output.

### FEATURES

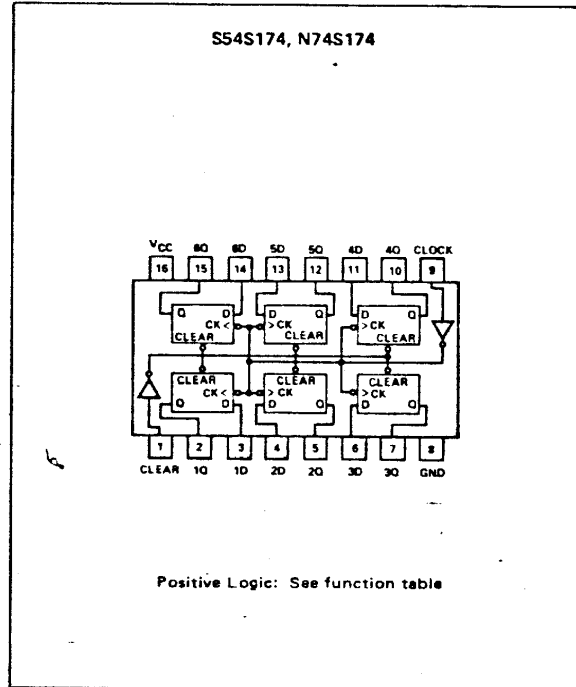
- FULL SCHOTTKY CLAMPING TO ACHIEVE TYPICAL MAXIMUM TOGGLE RATES OF 110 MHz
- FUNCTIONALLY AND MECHANICALLY IDENTICAL TO THE SERIES 54/74 COUNTERPARTS AND CAN BE USED TO UPGRADE EXISTING SYSTEMS WITH SIGNIFICANT IMPROVEMENT IN SPEED
- FULLY COMPATIBLE WITH OTHER TTL CIRCUITS
- S54S174 AND S54S175 OPERATE OVER FULL MILITARY TEMPERATURE RANGE OF -55°C TO 125°C
- FOR USE IN HIGH-PERFORMANCE:
  - BUFFER STORAGE REGISTERS
  - SHIFT REGISTERS
  - COUNTERS
  - PATTERN GENERATORS

### FUNCTION TABLE (EACH FLIP-FLOP)

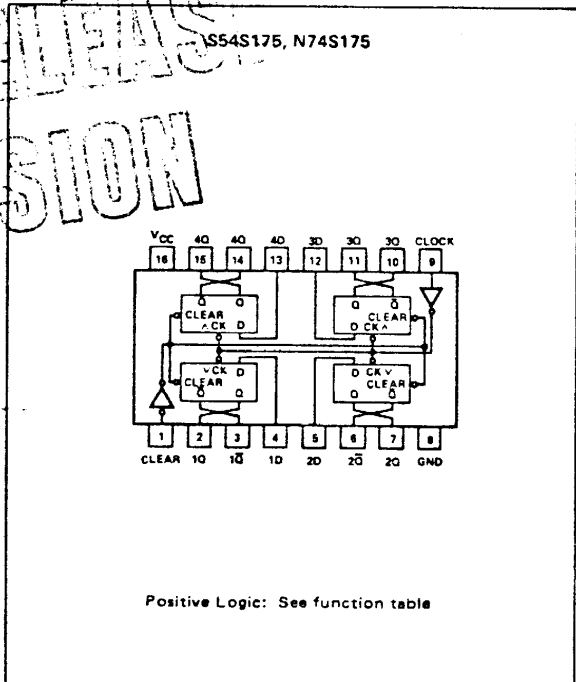
INPUTS			OUTPUTS	
CLEAR	CLOCK	D	Q	$\bar{Q}$ †
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q <sub>0</sub>	$\bar{Q}$ <sub>0</sub>

- High level (steady state)
- Low level (steady state)
- Irrelevant
- Transition from low to high level
- † The level of Q before the indicated steady-state input conditions were established
- S54S175 and N74S175 only

### PIN CONFIGURATION

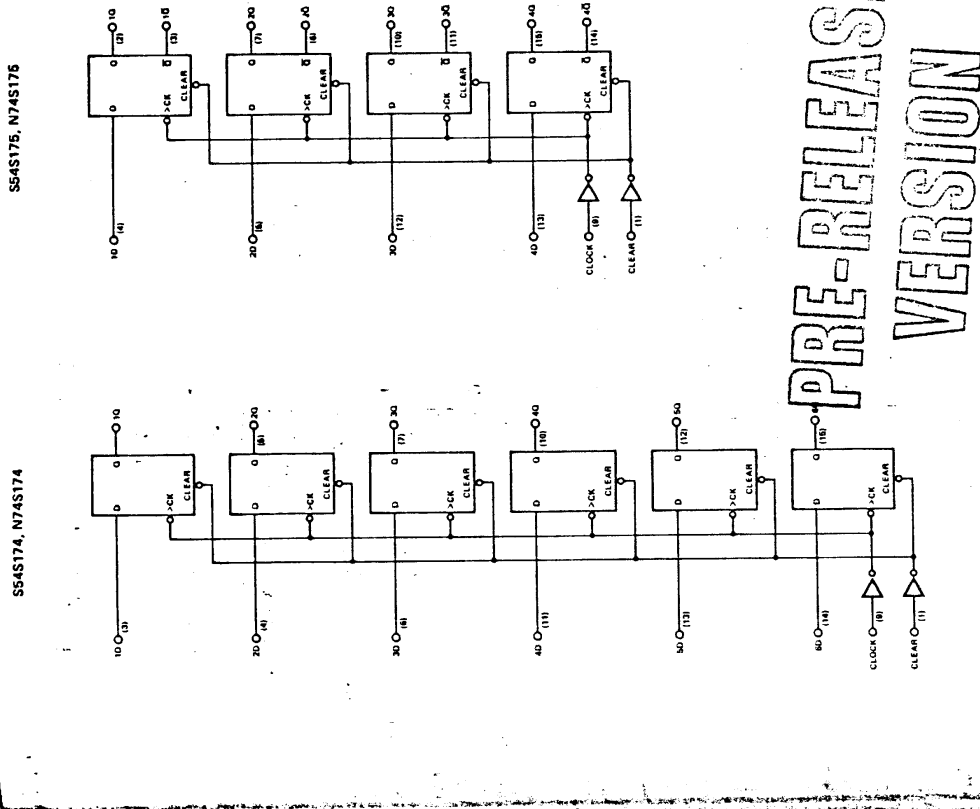


### PIN CONFIGURATION



PRE-RELEASE  
VERSION

SECTIONAL BLOCK DIAGRAMS



PRE-RELEASE  
VERSION

Dynamic input activated by a transition from a high level to a low level.

PARAMETER	S54S174, S54S175		N74S174, N74S175		UNIT		
	MIN	NOM	MAX	MIN		NOM	MAX
Supply voltage, $V_{CC}$	4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N			20			20	
Output clock frequency, f <sub>clock</sub>	0	75	0	12	75	75	MHz
Setup time, t <sub>setup</sub>	8		8	15			ns
Hold time, t <sub>hold</sub>	2		2				ns
Operating free-air temperature, T <sub>A</sub>	-55		125	0		70	°C

PARAMETER	TEST CONDITIONS*			UNIT
	MIN	TYP**	MAX	
High-level input voltage		2	0.8	V
Low-level input voltage			-1.2	V
Input clamp voltage	V <sub>CC</sub> = MIN, I <sub>I</sub> = -18 mA			
High-level output voltage	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, Series 54S			2.5
	V <sub>IH</sub> = 0.8 V, I <sub>OH</sub> = -1 mA, Series 74S			2.7
Low-level output voltage	V <sub>CC</sub> = MIN, V <sub>IL</sub> = 2 V			0.5
	V <sub>IL</sub> = 0.8 V, I <sub>OL</sub> = 20 mA			
Input current at maximum input voltage	V <sub>CC</sub> = MAX, V <sub>I</sub> = 5.5 V			1
High-level input current	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7 V			50
Low-level input current	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.5 V			-2
Short-circuit output current †	V <sub>CC</sub> = MAX			-100
Supply current	S54S174, N74S174			90
	S54S175, N74S175			60

\*Conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the device type.  
 †V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.  
 ‡The short-circuit current should be measured at a time, and duration of the short-circuit should not exceed one second.  
 \*With all outputs open and 4.5 V applied to all data and clear inputs, I<sub>CC</sub> is measured after a momentary ground, then 4.5 V is applied to clock.

PARAMETER	TEST CONDITIONS			UNIT
	MIN	TYP	MAX	
Maximum input clock frequency	75	110	20	MHz
Propagation delay time, low-to-high-level Q output from clear (S54S175, N74S175 only)		13		ns
Propagation delay time, high-to-low-level Q output from clear		13		ns
Propagation delay time, low-to-high-level output from clock		9		ns
Propagation time, high to low level output from clock		11		ns

\*Operating Characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C, N = 10



# 4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS

## S54S194 N74S194

DIGITAL 54/74 TTL SERIES

Performance bidirectional shift registers are functionally identical to the N54194 and S74194, however, the shift frequency of 110 megahertz the Schottky-clamped outputs can be used in very high speed systems, or can be used for the N54194/S74194 to upgrade the performance of existing systems. The universal shift register has four distinct modes of operation, namely:

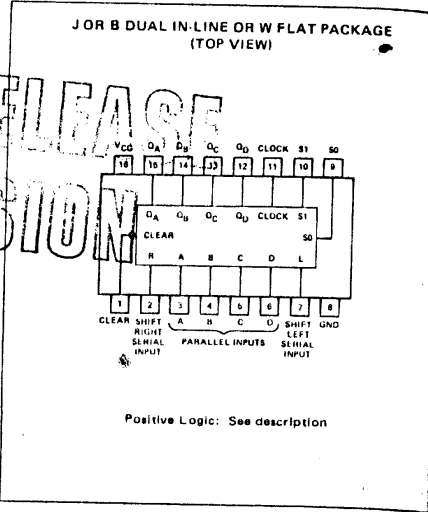
	MODE CONTROL	
	S1	S0
(clock) Load	H	H
(clock) Shift right (the direction $Q_A$ toward $Q_D$ )	L	H
(clock) Shift left (the direction $Q_D$ toward $Q_A$ )	H	L
(clock) Parallel data	L	L

In load mode, data is loaded into the associated flip-flop. In shift-right mode, the outputs after the positive transition of the clock loading, serial data flow is inhibited. Shift right is asynchronous with the rising edge of the clock pulse and S1 is low. Serial data for this mode is entered at data input. When S0 is low and S1 is high, data shifts right and new data is entered at the shift-left serial input. In shift-left mode, data is circulated when both mode control inputs are low. In parallel mode, the mode controls can be changed independently.

These shift registers are compatible with most other TTL families. All inputs are buffered to lower the drive requirements. The S54S194 is characterized for operation over the full military temperature range of -55°C to 125°C. The S74S194 is characterized for operation over the full commercial temperature range of 0°C to 70°C.

Characterized for operation over the full military temperature range of -55°C to 125°C. The S74S194 is characterized for operation over the full commercial temperature range of 0°C to 70°C.

### PIN CONFIGURATION



Positive Logic: See description

### FEATURES

- SCHOTTKY-CLAMPED TO ACHIEVE TYPICAL MAXIMUM SHIFT FREQUENCY OF 110 MHz
- FUNCTIONALLY AND MECHANICALLY IDENTICAL TO N54194, S74194 AND CAN BE USED TO UPGRADE EXISTING SYSTEMS WITH SIGNIFICANT IMPROVEMENT IN SPEED
- FULLY COMPATIBLE WITH MOST OTHER TTL AND DTL CIRCUITS
- N54S194 OPERATES OVER FULL MILITARY TEMPERATURE RANGE OF -55°C TO 125°C
- FOR USE IN HIGH-PERFORMANCE: ACCUMULATORS/PROCESSORS, SERIAL-TO-PARALLEL AND

### RECOMMENDED OPERATING CONDITIONS

PARAMETER	54S194			74S194			
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, $V_{CC}$	4.5	5	5.5	4.75	5	5.25	
High-level output current, $I_{OH}$			-1			-1	
Low-level output current, $I_{OL}$			20			20	
Clock frequency, $f_{clock}$	0		70	0		70	
Width of clock pulse, $t_w(\text{clock})$	7			7			
Width of clear pulse, $t_w(\text{clear})$	12			12			
Setup time, $t_{setup}$	PA	Mode control	8		8		
		Serial and parallel data	5		5		
		Clear inactive-state	9		9		
Hold time at any input, $t_{hold}$			3			3	
Operating free air temperature, $T_A$			-55	125		0	70

### ELECTRICAL CHARACTERISTICS over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS*	54S194			74S194		
		MIN	TYP**	MAX	MIN	TYP**	MAX
$V_{IH}$ High-level input voltage		2			2		
$V_{IL}$ Low-level input voltage				0.8			0.8
$V_{ICL}$ Input clamp voltage	$V_{CC} = \text{MIN}$ , $I_I = -18\text{mA}$			-1.5			-1.5
$V_{OH}$ High-level output voltage	$V_{CC} = \text{MIN}$ , $V_{IH} = 2\text{V}$ , $V_{IL} = 0.8\text{V}$ , $I_{OH} = -1\text{mA}$	2.5	3.4		2.7	3.4	
$V_{OL}$ Low-level output voltage	$V_{CC} = \text{MIN}$ , $V_{IH} = 2\text{V}$ , $V_{IL} = 0.8\text{V}$ , $I_{OL} = 20\text{mA}$			0.5			0.5
$I_{IH}$ Input current at maximum input voltage	$V_{CC} = \text{MAX}$ , $V_I = 5.5\text{V}$			1			1
$I_{IH}$ High-level input current	$V_{CC} = \text{MAX}$ , $V_I = 2.4\text{V}$			50			50
$I_{IL}$ Low-level input current	$V_{CC} = \text{MAX}$ , $V_I = 0.4\text{V}$			-2			-2
$I_{OS}$ Short-circuit output current†	$V_{CC} = \text{MAX}$	-40		-100	-40		-100
$I_{CC}$ Supply current	$V_{CC} = \text{MAX}$ , See Note 2		85	135		85	135
	$V_{CC} = \text{MAX}$ , $T_A = 125^\circ\text{C}$ , See Note 2			99			110
	SN54S194N SN54S194W						

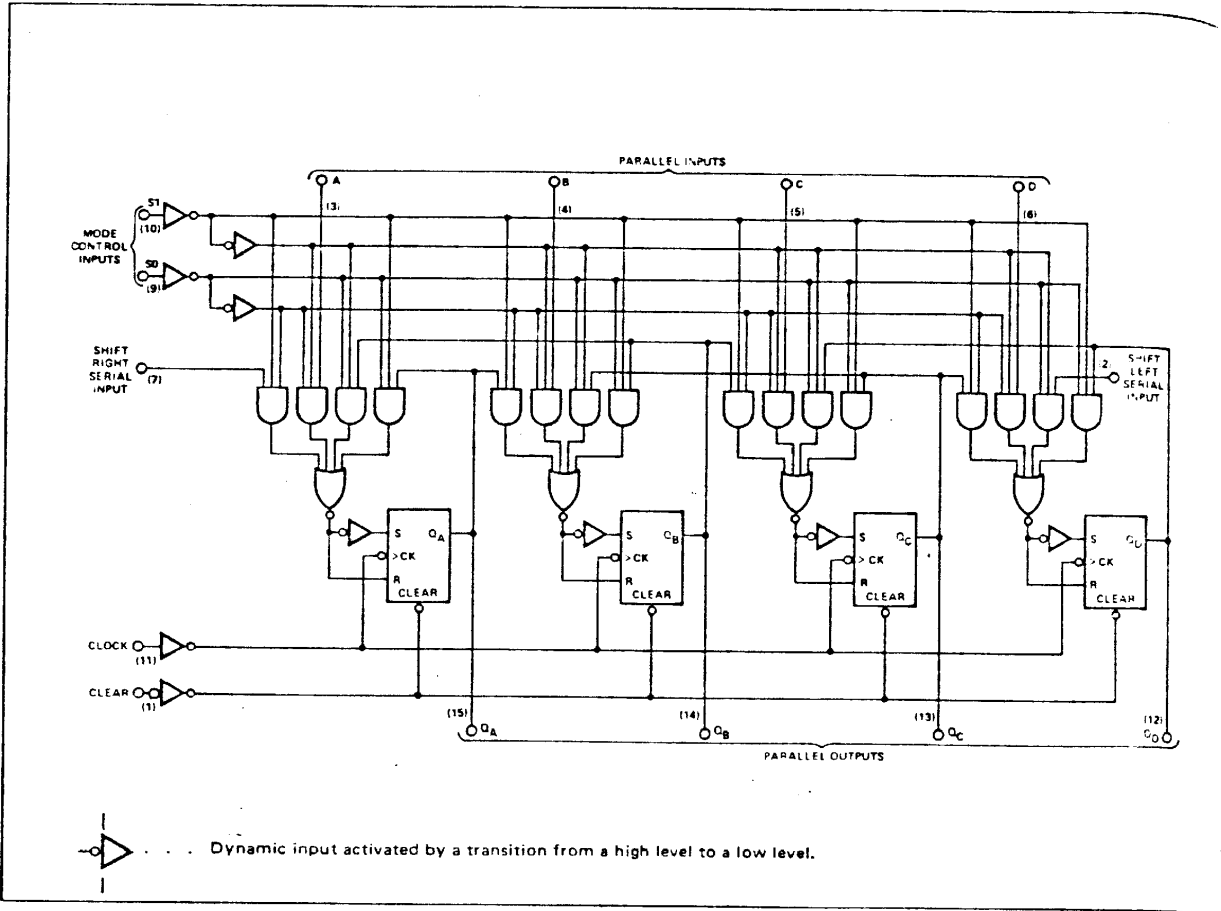
\* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.  
 \*\* Typical values are at  $V_{CC} = 5\text{V}$ ,  $T_A = 25^\circ\text{C}$ .  
 † Short more than one output should be shorted at a time, and duration of short-circuit should not exceed one second.  
 ‡ See Note 2.  
 § All outputs open, inputs A through D grounded, and 4.5V applied to S0, S1, clear, and the serial inputs.  $I_{CC}$  is measured with respect to GND, then 4.5V, applied to clock.

### SWITCHING CHARACTERISTICS $V_{CC} = 5\text{V}$ , $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX
Maximum clock frequency		70	105	
Propagation delay time, high-to-low-level output from clear	$C_L = 15\text{pF}$ , $R_L = 280\Omega$ , See Figure 1		12.5	18
Propagation delay time, low-to-high-level output from clock		4	8	1

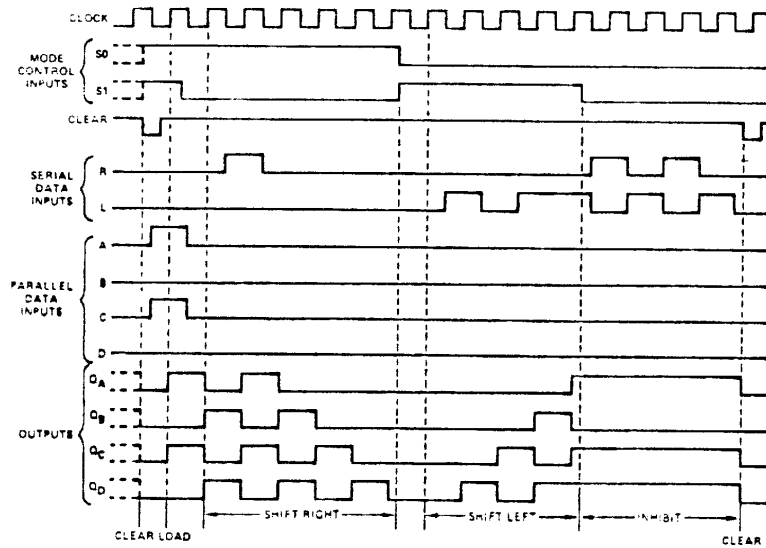
**SIGNETICS 4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS ■ S54S194, N74S194**

FUNCTIONAL BLOCK DIAGRAM

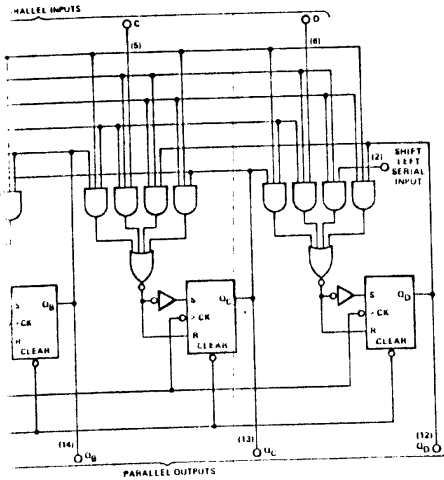


TYPICAL CLEAR, LOAD, HIGH-SHIFT, INHIBIT, AND CLEAR SEQUENCES

**PRE-RELEASE  
VERSION**

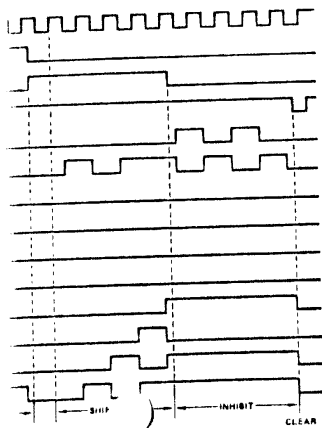


SHIFT REGISTER S54S194, N74S194



high level to a low level.

REFERENCES



4-BIT PARALLEL-ACCESS SHIFT REGISTERS

S54S195  
N74S195

DIGITAL 54/74 TTL SERIES

DESCRIPTION

These high-performance 4-bit registers feature a 110-megahertz typical maximum shift-frequency which makes them particularly attractive for very high-speed data processing systems. As the pin assignments are the same as the S54195 and N74195, existing systems can in most cases be upgraded merely by utilizing the Schottky-clamped versions. The registers have two modes of operation:

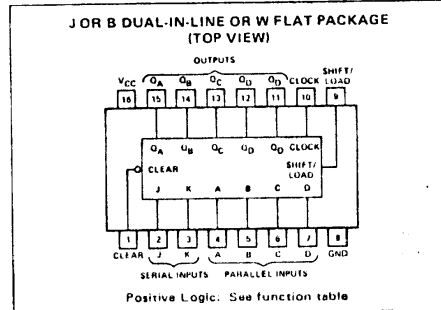
Parallel (Broadside) Load Shift (in the direction  $Q_A$  toward  $Q_D$ )

Parallel loading is accomplished by applying the four bits of data and taking the shift/load control input low. The data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shifting is accomplished synchronously when the shift/load control input is high. Serial data for this mode is entered at the J-K inputs. These inputs permit the first stage to perform as a J-K, D-, or T-type flip-flop as shown in the function table.

These shift registers are fully compatible with other TTL families. All inputs are buffered to lower the drive requirements to one maximum Series 54S/74S load, including the clock input. The S54S195 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ ; the N74S195 is characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

PIN CONFIGURATION



FEATURES

- SCHOTTKY-CLAMPED TO ACHIEVE TYPICAL MAXIMUM SHIFT FREQUENCY OF 110 MHz
- FUNCTIONALLY AND MECHANICALLY IDENTICAL TO S54195, S74195 AND CAN BE USED TO UPGRADE EXISTING DESIGNS WITH SIGNIFICANT IMPROVED SPEED
- FULLY COMPATIBLE WITH OTHER TTL CIRCUITS
- N54S195 OPERATES OVER FULL MILITARY TEMPERATURE RANGE OF  $-55^{\circ}\text{C}$  TO  $125^{\circ}\text{C}$
- USE IN HIGH-PERFORMANCE: ACCUMULATORS/PROCESSORS, SERIAL-TO-PARALLEL, PARALLEL-TO-SERIAL CONVERTERS

FUNCTION TABLE

CLEAR	SHIFT/LOAD	CLOCK	INPUTS				OUTPUTS						
			SERIAL		PARALLEL		$Q_A$	$Q_B$	$Q_C$	$Q_D$	$\bar{Q}_D$		
			J	$\bar{K}$	A	B	C	D					
L	X	X	X	X	X	X	X	X	L	L	L	L	H
H	L	↑	X	X	A	B	C	D	A	B	C	D	$\bar{Q}_D$
H	H	L	X	X	X	X	X	X	$Q_{A0}$	$Q_{B0}$	$Q_{C0}$	$Q_{D0}$	$\bar{Q}_{D0}$
H	H	↑	L	H	X	X	X	X	$Q_{A0}$	$Q_{B0}$	$Q_{C0}$	$Q_{D0}$	$\bar{Q}_{C0}$
H	H	↑	L	L	X	X	X	X	L	$Q_{A0}$	$Q_{B0}$	$Q_{C0}$	$\bar{Q}_{C0}$
H	H	↑	H	H	X	X	X	X	H	$Q_{A0}$	$Q_{B0}$	$Q_{C0}$	$\bar{Q}_{C0}$
H	H	↑	H	L	X	X	X	X	$Q_{A0}$	$Q_{A0}$	$Q_{B0}$	$Q_{B0}$	$\bar{Q}_{C0}$

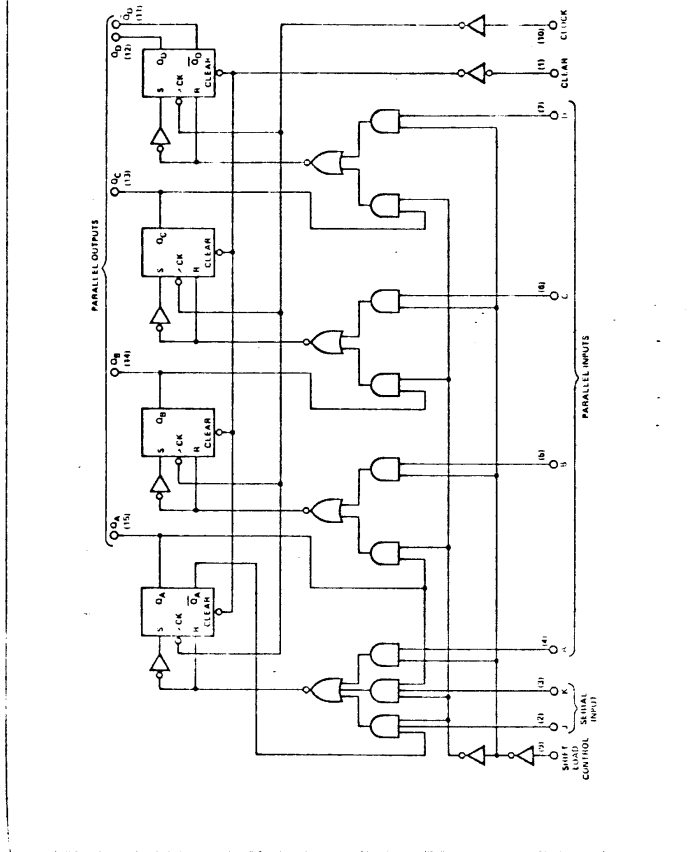
- High level (steady state)
- Low level (steady state)
- Irrelevant (any input, including transition)
- Transition from low to high level

74195  
74195 257

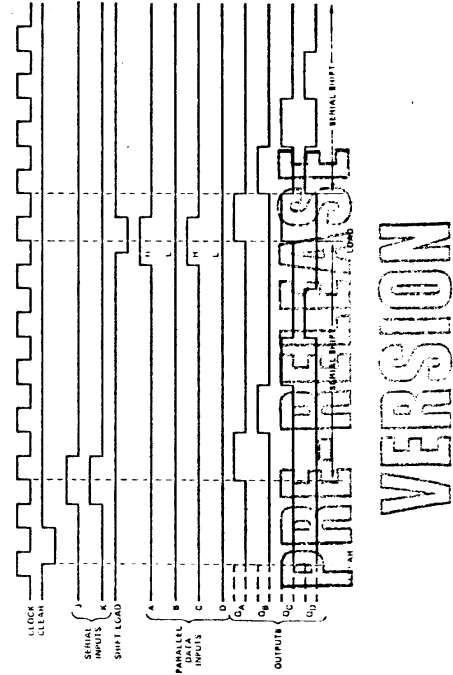
PRE-RELEASE  
VERSION

DIGITAL 54/74 TTL MINI SERIES ■ 5445195

FUNCTIONAL BLOCK DIAGRAM



TYPICAL CLEAR, SHIFT, AND LOAD SEQUENCES



PRELIMINARY  
VERSION

CONDITIONS	54195		74195		UNIT
	MIN	NOM	MAX	MAX	
voltage, $V_{CC}$	4.5	5	5.5	5	V
output current, $I_{OH}$	-800				mA
output current, $I_{OL}$	0	30	0	30	mA
clock input pulse, $t_w(\text{clock})$	16		16		nS
clear input pulse, $t_w(\text{clear})$	12		12		nS
setup time, $t_{setup}$ (see Figure 1)	25		25		nS
hold time, $t_{hold}$ (see Figure 1)	15		15		nS
release time, $t_{release}$ (see Figure 1)	25		25		nS
parallel data hold time, $t_{hold}$ (see Figure 1)	0		0		nS
free-air temperature, $T_A$	-55		125		°C

CHARACTERISTICS over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS*	MIN	TYP	MAX	UNIT
High-level input voltage		2		0.8	V
Low-level input voltage				-1.5	V
Input clamp voltage	$V_{CC} = \text{MIN.}, I_I = -17\text{mA}$ $V_{CC} = \text{MIN.}, V_{IH} = 4\text{V},$ $V_{IL} = 0.8\text{V}, I_{OH} = 900\mu\text{A}$	2.4		3.4	V
High-level output voltage	$V_{CC} = \text{MIN.}, V_{IH} = 4\text{V},$ $V_{IL} = 0.8\text{V}, I_{OL} = 5\text{mA}$	0.2		0.4	V
Low-level output voltage	$V_{CC} = \text{MAX.}, V_I = 2\text{V},$ $V_{CC} = \text{MAX.}, V_I = 0.2\text{V}$			1	mA
Input current at maximum input voltage				40	$\mu\text{A}$
High-level input current				-20	mA
Low-level input current				-18	mA
Short circuit output current†				39	mA
Supply current				63	mA

Conditions shown as MIN or MAX, use the appropriate value specified and recommended operating conditions for the applicable type.  
† Values are at  $V_{CC} = 5\text{V}, T_A = 25^\circ\text{C}$ .  
\* More than one output should be shorted at a time.

All outputs open, shift/load grounded, and 4.5V applied to the J, K, and data;  $V_{CC}$  is measured by applying a momentary load, followed by 4.5V, to clear and then applying a momentary ground, followed by 4.5V, to clock.

CHARACTERISTICS,  $V_{CC} = 5\text{V}, T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Maximum clock frequency		30		39	MHz
Propagation delay time, high-to-low-level output from clear	$C_L = 1$	19		30	nS
Propagation delay time, low-to-high-level output from clear	$R_L = 1$	6		14	nS
Propagation delay time, high-to-low-level output from clock		7		17	nS
Propagation delay time, low-to-high-level output from clock		7		17	nS



QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS S54S257, S54S258, N74S257, N74S258

DIGITAL 54/74 TTL SERIES

DESCRIPTION

Schottky clamped high-performance multiplexers feature four outputs which can interface directly with and drive data bus organized systems. With all but one of the common outputs disabled (at a high impedance state) the low impedance of the enabled output will drive the bus line to a high or low level.

The three-state output feature means that n-bit (paralleled) data buses with up to 258 sources can be implemented for data buses. This permits the use of standard TTL registers for data retention without the need for a separate output disable circuit.

Typical propagation delay times from data input to output are only 4.8 nanoseconds for the S54S257, N74S157 and only 4.5 nanoseconds for the S54S258, N74S258. Also, to minimize the delay that two outputs will attempt to take a common bus to different logic levels, the output enable circuitry is designed such that output disable times are shorter than the output enable times.

FEATURES

THREE-STATE OUTPUTS INTERFACE DIRECTLY WITH DATA BUS

SCHOTTKY CLAMPED FOR SIGNIFICANT IMPROVEMENT IN SWITCHING AND AC PERFORMANCE

FULLY COMPATIBLE WITH MOST TTL FUNCTIONS INCLUDING MSI

STANDARD PIN ASSIGNMENTS AS S54S157, N74S157 AND S54S158, N74S158

PROVIDES BUS INTERFACE FROM MULTIPLE SOURCES FOR HIGH-PERFORMANCE SYSTEMS

S54S257 AND N54S258 ARE GUARANTEED FOR OPERATION OVER THE FULL MILITARY TEMPERATURE RANGE OF -55°C TO 125°C

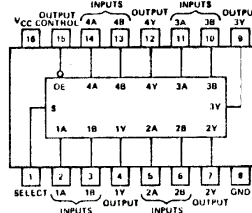
FUNCTION TABLE

OUTPUT CONTROL	INPUTS		OUTPUT Y	
	SELECT	A B	S54S257 S74S257	N54S258 N74S258
H	X	X X	Z	Z
L	L	L X	L	H
L	L	H X	H	L
L	H	X L	L	H
L	H	X H	H	L

PIN CONFIGURATION

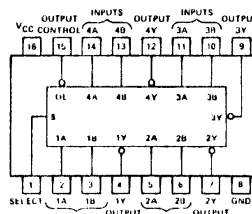
JORGAN B DUAL IN-LINE OR WFLAT PACKAGE (TOP VIEW)

S54S257, N74S257



Positive Logic: See function table

S54S258, N74S258



Positive Logic: See function table

SIGNETICS QUADRUPLE 2-LINE TO 1-LINE ■ S54S257, S54S258, N74S257, N74S258

RECOMMENDED OPERATING CONDITIONS

PARAMETER	S54S257, S54S258			N74S257, N74S258		
	MIN	NOM	MAX	MIN	NOM	MAX
Supply voltage, V <sub>CC</sub>	4.5	5	5.5	4.75	5	5.25
Normalized fan-out from each output, N	High logic level	40		10		
	Low logic level		10			
High-level output current, I <sub>OH</sub>			10			
Operating free-air temperature, T <sub>A</sub>	-55	125		0		70

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER	TEST CONDITIONS*	S54S257, S54S258		N74S257, N74S258		
		MIN	TYP**	MAX	MIN	TYP**
V <sub>IH</sub> High-level input voltage		2		2		
V <sub>IL</sub> Low-level input voltage						
V <sub>I</sub> Input clamp voltage	V <sub>CC</sub> = MIN, I <sub>I</sub> = -18 mA			0.8		
V <sub>OH</sub> High level output voltage	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, Series 54S V <sub>IL</sub> = 0.8 V, I <sub>OH</sub> = MAX, Series 74S	2.5	3.4	2.5	3.4	
V <sub>OL</sub> Low level output voltage	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = 0.8 V, I <sub>OL</sub> = 20 mA	2.4	3.2	2.4	3.2	
I <sub>O(off)</sub> Off state (high-impedance state) output current	V <sub>CC</sub> = MAX, V <sub>O</sub> = 2.4 V			50		
I <sub>I</sub> Input current at maximum input voltage	V <sub>CC</sub> = MAX, V <sub>I</sub> = 5.5 V			-50		
I <sub>IH</sub> High level input current	S input: V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7 V Any other			1	100	
I <sub>IL</sub> Low level input current	S input: V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.5 V Any other			50	-4	
I <sub>OS</sub> Short circuit output current†	V <sub>CC</sub> = MAX			-2		
I <sub>CC</sub> Supply current	All outputs high: V <sub>CC</sub> = MAX, See Note 1 All outputs low All outputs off	-40	-100	-40	-1	
		44	64	36		
		60	93	52		
		64	99	56		

\* Conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.  
\*\* Typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.  
† More than one output should be shorted at a time and duration of the short circuit test should not exceed one second.  
‡ I<sub>CC</sub> is measured with all outputs open and all possible inputs grounded while achieving the stated output conditions.

SWITCHING CHARACTERISTICS, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	S54S257, N74S257			S54S258, N74S258		
				MIN	TYP	MAX	MIN	TYP	MAX
t <sub>PLH</sub>	Data	Any	C <sub>L</sub> = 15 pF, R <sub>L</sub> = 280 Ω, See Note 4	5	7.5		4	6	
t <sub>PHL</sub>	Data	Any		4.5	6.5		4	6	
t <sub>PLH</sub>	Select	Any		8.5			8	12	
t <sub>ZH</sub>	Output	Any		8.5			7.5	12	
t <sub>ZL</sub>	Control	Any		13	19.5		13	19.5	
t <sub>HZ</sub>	Output	Any		14	21		14	21	
t <sub>LZ</sub>	Control	Any	5.5	8.5		5.5	8.5		

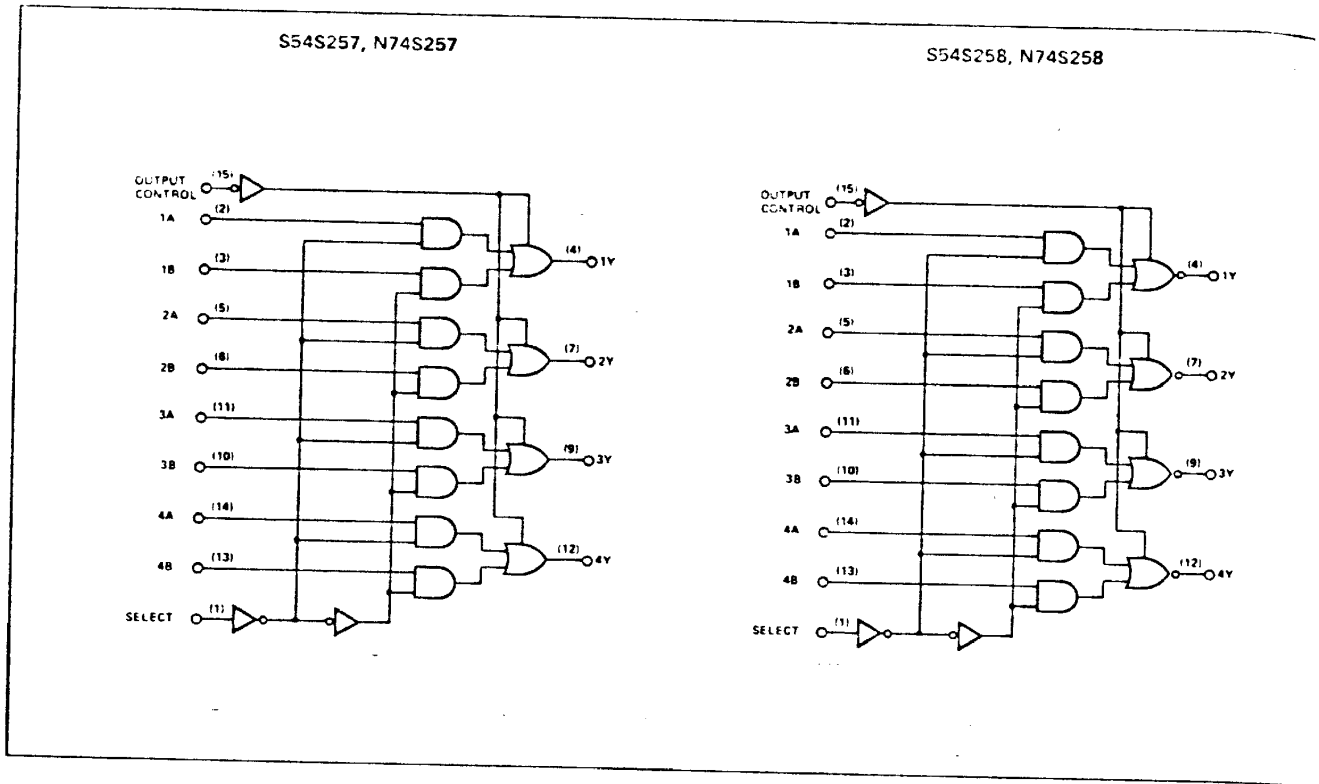
- \* Propagation delay time, low-to-high-level output
- \* Propagation delay time, high-to-low-level output
- \* Output enable time to high level
- \* Output enable time to low level
- \* Output disable time from high level
- \* Output disable time from low level

† Load circuit and waveforms are shown on page 2-293

PRE-RELEASE VERSION

SIGNETICS QUADRUPLE 2-LINE TO 1-LINE ■ S54S257, S54S258, N74S257, N74S258

FUNCTIONAL BLOCK DIAGRAMS



PRE-RELEASE  
VERSION

**TTL  
MSI**

**TYPES SN54283, SN74283  
4-BIT BINARY FULL ADDERS WITH FAST CARRY**

BULLETIN NO. DL-S 7211832, DECEMBER 1972

- Full-Carry Look-Ahead across the Four Bits
- Typical Add or Subtract Times:  
23 ns (Two 8-bit Words)  
43 ns (Two 16-bit Words)
- Systems Achieve Partial Look-Ahead Performance with the Economy of Ripple Carry
- Supply Voltage and Ground on Corner Pins to Simplify P-C Board Layout

**description**

The SN54283 and SN74283 adders are electrically and functionally identical to the SN5483A and SN7483A, respectively. Only the arrangement of the terminals has been changed in the SN54283 and SN74283.

These improved 4-bit full adders/subtractors feature full look-ahead across four bits to generate the carry term in typically 10 nanoseconds. This capability provides the system designer with partial look-ahead performance at the economy and reduced package count of a ripple-carry implementation.

These full adders are designed so that levels of the input and output, including the carry, are in their true form. Thus the end-around carry is accomplished without the need for level inversion.

Power dissipation is typically 310 mW. Delay times through the package are 10 ns and 16 ns respectively from carry-in to carry-out and data-in to data-out. The SN54283 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74283 is characterized for 0°C to 70°C operation.

**function table and schematics of inputs and outputs**

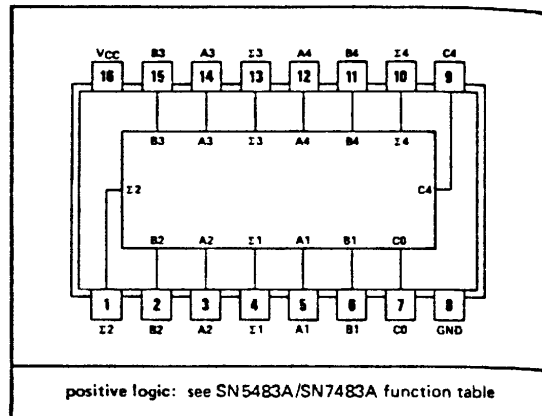
Same as SN5483A/SN7483A, see pages 198 and 199.

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)**

Supply voltage, V <sub>CC</sub> (see Note 1)	7 V
Input voltage	5.5 V
Interemitter voltage (see Note 2)	5.5 V
Operating free-air temperature range: SN54283	-55°C to 125°C
SN74283	0°C to 70°C
Storage temperature range	-65°C to 150°C

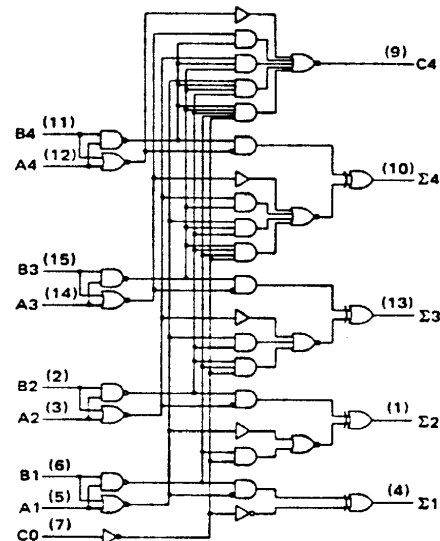
- NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.  
2. This is the voltage between two emitters of a multiple-emitter transistor. For this circuit, this rating applies between the following pairs: A1 and B1, A2 and B2, A3 and B3, A4 and B4.

J OR N DUAL-IN-LINE OR  
W FLAT PACKAGE (TOP VIEW)



positive logic: see SN5483A/SN7483A function table

**functional block diagram**



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PRE-RELEASE

VERSION

TYPES SN54283, SN74283

4-BIT BINARY FULL ADDERS WITH FAST CARRY

recommended operating conditions

	SN54283			SN74283			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage, V <sub>CC</sub>	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I <sub>OH</sub>	Any output except C4			-800			μA
	Output C4			-400			
Low-level output current, I <sub>OL</sub>	Any output except C4			16			mA
	Output C4			8			
Operating free-air temperature, T <sub>A</sub>	-55	125		0	70		°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54283			SN74283			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V <sub>IH</sub> High-level input voltage		2			2			V
V <sub>IL</sub> Low-level input voltage				0.8			0.8	V
V <sub>I</sub> Input clamp voltage	V <sub>CC</sub> = MIN, I <sub>I</sub> = -12 mA			-1.5			-1.5	V
V <sub>OH</sub> High-level output voltage	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = 0.8 V, I <sub>OH</sub> = MAX	2.4	3.6		2.4	3.6		V
V <sub>OL</sub> Low-level output voltage	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = 0.8 V, I <sub>OL</sub> = MAX		0.2	0.4		0.2	0.4	V
I <sub>I</sub> Input current at maximum input voltage	V <sub>CC</sub> = MAX, V <sub>I</sub> = 5.5 V			1			1	mA
I <sub>IH</sub> High-level input current	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.4 V			40			40	μA
I <sub>IL</sub> Low-level input current	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.4 V			-1.6			-1.6	mA
I <sub>OS</sub> Short-circuit output current§	Any output except C4			-20			-18	mA
	Output C4			-20			-18	
I <sub>CC</sub> Supply current	V <sub>CC</sub> = MAX, Outputs open	All B low, other inputs at 4.5 V		56			56	mA
		All inputs at 4.5 V		66	99		66	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡ All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

§ Only one output should be shorted at a time.

switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t <sub>PLH</sub>	C0	Any Σ	C <sub>L</sub> = 15 pF, R <sub>L</sub> = 400 Ω, See Note 3	14	21		ns
t <sub>PHL</sub>				12	21		
t <sub>PLH</sub>	A <sub>i</sub> or B <sub>i</sub>	Σ <sub>i</sub>		16	24		ns
t <sub>PHL</sub>				16	24		
t <sub>PLH</sub>	C0	C4	C <sub>L</sub> = 15 pF, R <sub>L</sub> = 780 Ω, See Note 3	9	14		ns
t <sub>PHL</sub>				11	16		
t <sub>PLH</sub>	A <sub>i</sub> or B <sub>i</sub>	C4		9	14		ns
t <sub>PHL</sub>				11	16		

† t<sub>PLH</sub> ≡ Propagation delay time, low-to-high-level output

t<sub>PHL</sub> ≡ Propagation delay time, high-to-low-level output

NOTE 3: Load circuit and voltage waveforms are shown on page 148.

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INSTRUMENTS RESERVES THE RIGHT TO MAKE CHANGES AT ANY TIME  
TO IMPROVE DESIGN AND TO SUPPLY THE BEST PRODUCT POSSIBLE.

**9334**  
**93L34**  
 8-BIT ADDRESSABLE LATCH

**PRE-RELEASE**  
**VERSION**

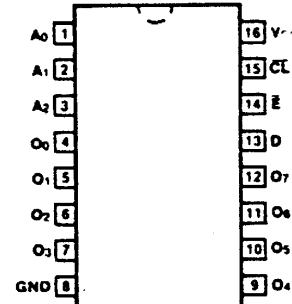
**DESCRIPTION** — The '34 is an 8-bit addressable latch designed for general purpose storage applications in digital systems. It is a multifunctional device capable of storing single line data in eight addressable latches, and being a one-of-eight decoder and demultiplexer with active level HIGH outputs. The device also incorporates an active LOW common clear for resetting all latches, as well as, an active LOW enable.

- SERIAL TO PARALLEL CAPABILITY
- EIGHT BITS OF STORAGE WITH OUTPUT OF EACH BIT AVAILABLE
- RANDOM (ADDRESSABLE) DATA ENTRY
- ACTIVE HIGH DEMULTIPLEXING OR DECODING CAPABILITY
- EASILY EXPANDABLE
- COMMON CONDITIONAL CLEAR

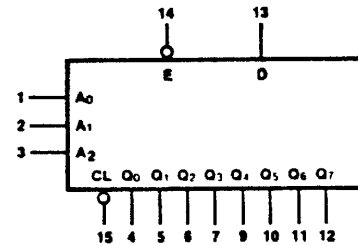
**ORDERING CODE:** See Section 9

3S	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V <sub>CC</sub> = +5.0 V ±5%, T <sub>A</sub> = 0°C to +70°C	V <sub>CC</sub> = +5.0 V ±10%, T <sub>A</sub> = -55°C to +125°C	
Plastic DIP (P)	A	9334PC, 93L34PC		9B
Ceramic DIP (D)	A	9334DC, 93L34DC	9334DM, 93L34DM	6B
Flatpak (F)	A	9334FC, 93L34FC	9334FM, 93L34FM	4L

**CONNECTION DIAGRAMS**  
**PINOUT A**



**LOGIC SYMBOL**



V<sub>CC</sub> = Pin 16  
 GND = Pin 8

**INPUT LOADING/FAN-OUT:** See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	93XX (U.L.) HIGH/LOW	93L (U.L.) HIGH/LOW
A <sub>0</sub> — A <sub>3</sub>	Address Inputs	1.0/1.0	0.5/0.25
D	Data Input	1.0/1.0	0.5/0.25
E	Enable Input (Active LOW)	1.5/1.5	0.75/0.38
CL	Clear Input (Active LOW)	1.0/1.0	0.5/0.25
O <sub>0</sub> — O <sub>7</sub>	Parallel Latch Outputs	18/6.0	10/5.0 (3.0)

34

**FUNCTIONAL DESCRIPTION** — The '34 has four modes of operation which are shown in the Mode Select Table. In the addressable latch mode, data on the data line (D) is written into the addressed latch. The addressed latch will follow the Data input with all non-addressed latches remaining in their previous states. In the memory mode, all latches remain in their previous state and are unaffected by the data or address inputs. To eliminate the possibility of entering erroneous data into the latches, the Enable should be held HIGH while the Address lines are changing. In the 1-of-8 decoding or demultiplexing mode, the addressed output will follow the state of the D input with all other outputs in the LOW state. In the clear mode all outputs are LOW and unaffected by the address and data inputs. When operating the '34 as an addressable latch, changing more than one bit of the address could impose a transient wrong address. Therefore, this should only be done while in the memory mode.

MODE SELECT TABLE

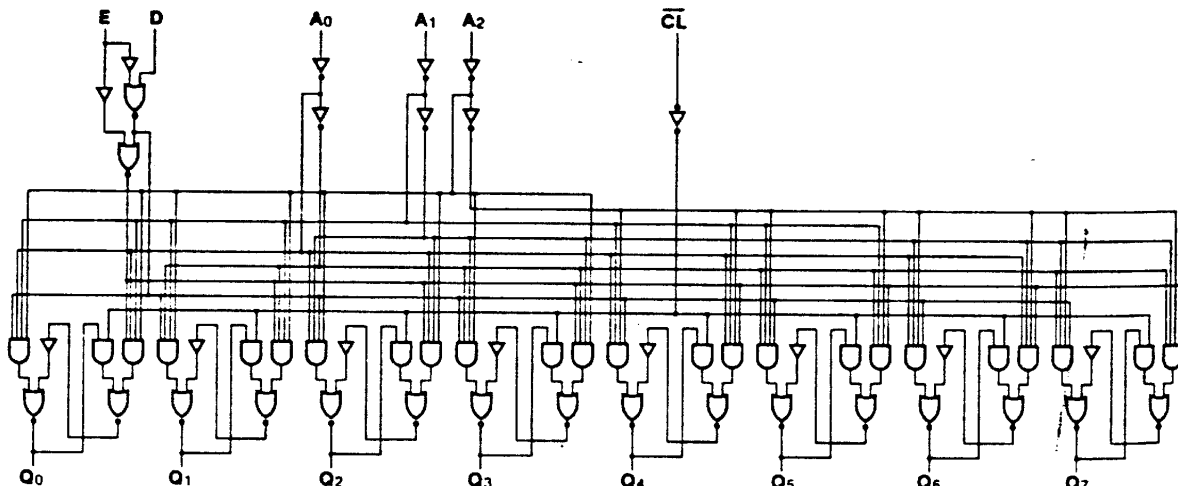
$\bar{E}$	$\bar{CL}$	MODE
L	H	Addressable Latch
H	H	Memory
L	L	Active HIGH 8-Channel Demultiplexer
H	L	Clear

TRUTH TABLE

INPUTS					OUTPUTS								MODE		
$\bar{CL}$	$\bar{E}$	A <sub>0</sub>	A <sub>1</sub>	A <sub>2</sub>	Q <sub>0</sub>	Q <sub>1</sub>	Q <sub>2</sub>	Q <sub>3</sub>	Q <sub>4</sub>	Q <sub>5</sub>	Q <sub>6</sub>	Q <sub>7</sub>			
L	H	X	X	X	L	L	L	L	L	L	L	L	L	Clear Demultiplex	
L	L	L	L	L	D	L	L	L	L	L	L	L	L		
L	L	H	L	L	L	D	L	L	L	L	L	L	L		
L	L	L	H	L	L	L	D	L	L	L	L	L	L		
L	L	L	L	H	L	L	L	D	L	L	L	L	L		
L	L	L	L	L	L	L	L	L	L	L	L	L	L	Memory	
L	L	H	H	H	L	L	L	L	L	L	L	L	D		
H	H	X	X	X	Q <sub>t-1</sub>	Q <sub>t-1</sub>	Q <sub>t-1</sub>	Q <sub>t-1</sub>	Q <sub>t-1</sub>	Q <sub>t-1</sub>	Q <sub>t-1</sub>	Q <sub>t-1</sub>	Q <sub>t-1</sub>		
H	L	L	L	L	D	Q <sub>t-1</sub>	Q <sub>t-1</sub>	Q <sub>t-1</sub>	Q <sub>t-1</sub>	Q <sub>t-1</sub>	Q <sub>t-1</sub>	Q <sub>t-1</sub>	Q <sub>t-1</sub>		Addressable Latch
H	L	H	L	L	Q <sub>t-1</sub>	D	Q <sub>t-1</sub>	Q <sub>t-1</sub>	Q <sub>t-1</sub>	Q <sub>t-1</sub>	Q <sub>t-1</sub>	Q <sub>t-1</sub>	Q <sub>t-1</sub>		
H	L	L	H	L	Q <sub>t-1</sub>	Q <sub>t-1</sub>	D	Q <sub>t-1</sub>	Q <sub>t-1</sub>	Q <sub>t-1</sub>	Q <sub>t-1</sub>	Q <sub>t-1</sub>	Q <sub>t-1</sub>		
H	L	L	L	H	Q <sub>t-1</sub>	Q <sub>t-1</sub>	Q <sub>t-1</sub>	D	Q <sub>t-1</sub>	Q <sub>t-1</sub>	Q <sub>t-1</sub>	Q <sub>t-1</sub>	Q <sub>t-1</sub>		
H	L	H	H	H	Q <sub>t-1</sub>	Q <sub>t-1</sub>	Q <sub>t-1</sub>	Q <sub>t-1</sub>	Q <sub>t-1</sub>	Q <sub>t-1</sub>	Q <sub>t-1</sub>	Q <sub>t-1</sub>	D		

H = HIGH Voltage Level      L = LOW Voltage Level      X = Immaterial      Q<sub>t-1</sub> = Previous Output State

LOGIC DIAGRAM



**DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)**

SYMBOL	PARAMETER	93XX		93L		UNITS	CONDITIONS
		Min	Max	Min	Max		
I <sub>CC</sub>	Power Supply Current	XM	86		21	mA	V <sub>CC</sub> = Max
		XC	86		26		

**AC CHARACTERISTICS: V<sub>CC</sub> = +5.0 V, T<sub>A</sub> = +25° C (See Section 3 for waveforms and load configurations)**

SYMBOL	PARAMETER	93XX		93L		UNITS	CONDITIONS
		C <sub>L</sub> = 15 pF		C <sub>L</sub> = 15 pF			
		Min	Max	Min	Max		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay E̅ to Q <sub>n</sub>	23	24	45	42	ns	Figs. 3-1, 3-9
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay D to Q <sub>n</sub>	28	24	65	45	ns	Figs. 3-1, 3-5
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay A <sub>n</sub> to Q <sub>n</sub>	35	35	66	66	ns	Figs. 3-1, 3-20
t <sub>PHL</sub>	Propagation Delay C̅ <sub>L</sub> to Q <sub>n</sub>	40		55		ns	Figs. 3-1, 3-10

**AC OPERATING REQUIREMENTS: V<sub>CC</sub> = +5.0 V, T<sub>A</sub> = +25° C**

SYMBOL	PARAMETER	93XX		93L		UNITS	CONDITIONS
		Min	Max	Min	Max		
t <sub>s</sub> (H)	Setup Time HIGH, D to E̅	20		45		ns	Fig. 3-13
t <sub>h</sub> (H)	Hold Time HIGH, D to E̅	0		-5.0		ns	
	Setup Time LOW, D to E̅	17		45		ns	
t <sub>h</sub> (L)	Hold Time LOW, D to E̅	0		-7.0		ns	
t <sub>s</sub> (H) t <sub>s</sub> (L)	Setup Time HIGH or LOW A <sub>n</sub> to E̅	5.0	5.0	10	10	ns	Fig. 3-21
t <sub>w</sub> (L)	E̅ Pulse Width LOW	17		26		ns	
t <sub>w</sub> (L)	C̅ <sub>L</sub> Pulse Width LOW			35		ns	Fig. 3-17

PRE-RELEASE  
VERSION

**DESCRIPTION**

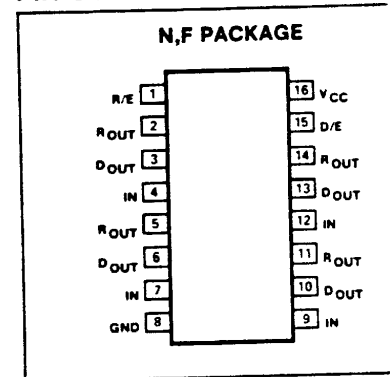
The 8T26A/28 consists of four pairs of 3-State logic elements configured as Quad Bus Drivers/Receivers along with separate buffered receiver enable and driver enable lines. This single IC Quad Transceiver design distinguishes the 8T26A/28 from conventional multi-IC implementations. In addition, the 8T26/28's ultra high speed while driving heavy bus capacitance (300pF) makes these devices particularly suitable for memory systems and bidirectional data buses.

Both the Driver and Receiver gates have 3-State outputs and low-current PNP inputs 3-State outputs provide the high switching speeds of totempole TTL circuits while offering the bus capability of open collector gates. PNP inputs reduce input loading to 200µA maximum.

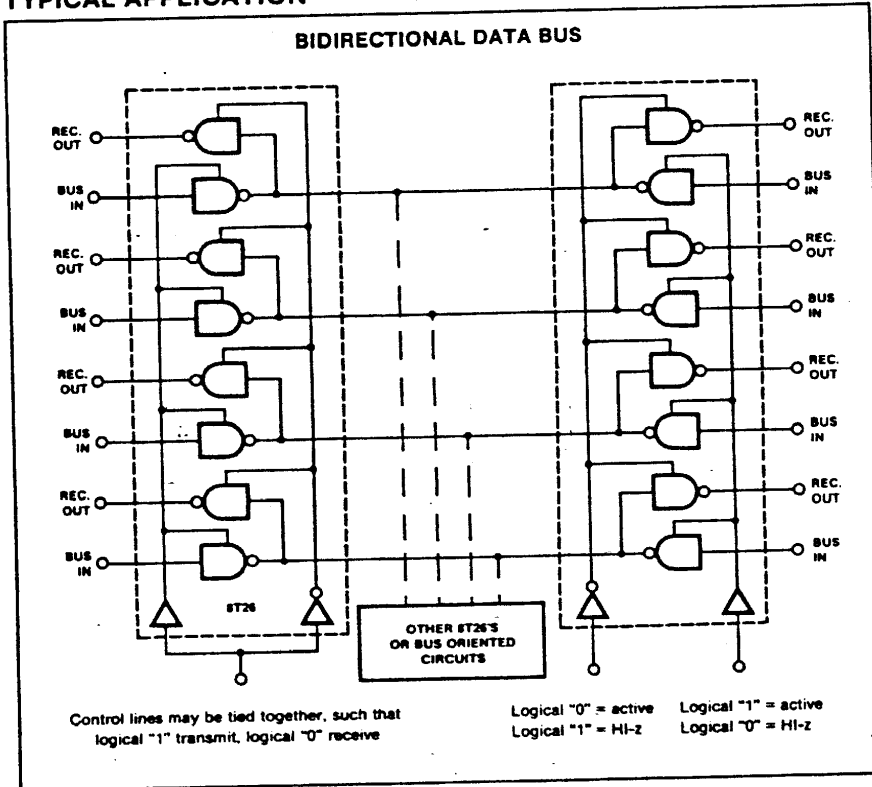
**APPLICATIONS**

- Half-duplex data transmission
- Memory interface buffers
- Data routing in bus oriented systems
- High current drivers
- MOS/CMOS-to-TTL interface

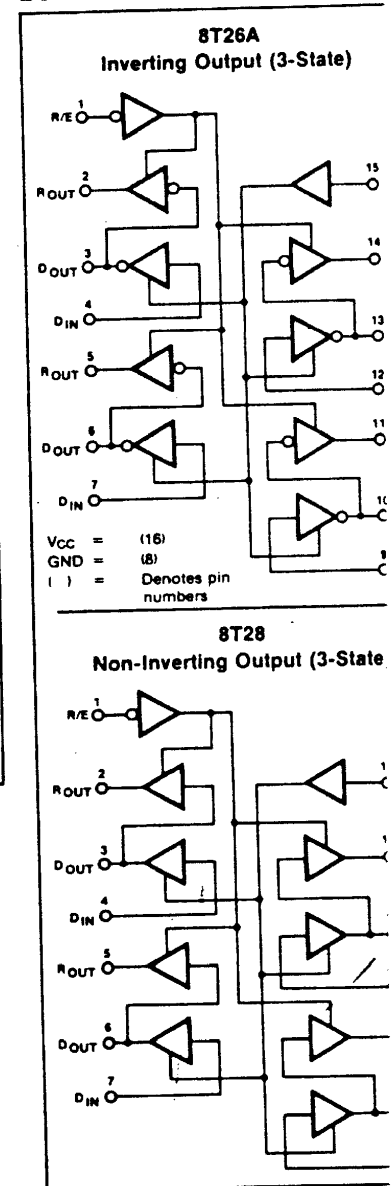
**PIN CONFIGURATION**



**TYPICAL APPLICATION**



**LOGIC DIAGRAM**



PRE-RELEASE  
VERSION

**DC ELECTRICAL CHARACTERISTICS**

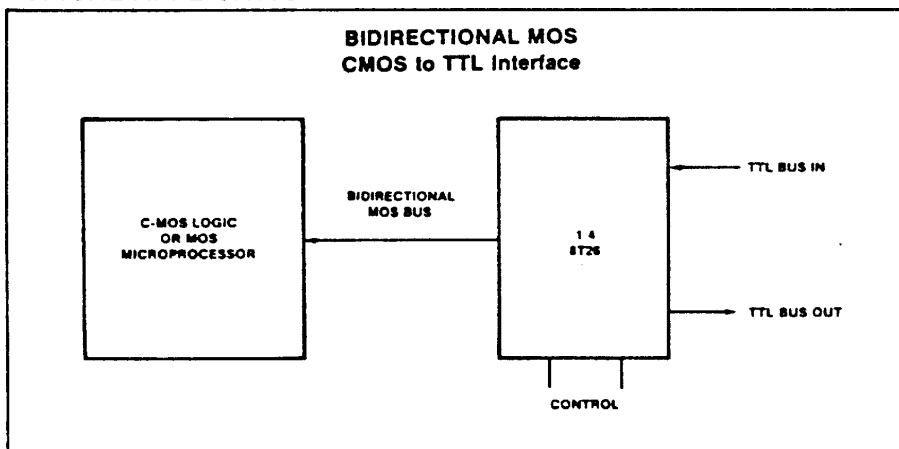
PARAMETER	TEST CONDITIONS	8T26A			8T28			UNIT
		Min	Typ	Max	Min	Typ	Max	
$V_{IL}$ $V_{IH}$ $V_{IC}$	Input voltage Low High Clamp		N/A N/A	-1.0		N/A N/A	-1.0	V
$V_{OL}$	Output voltage Low			0.5			0.5	V
	Drive			0.5			0.5	V
	Receive							V
$I_{IL}$	Input current Low Drive (low level) Disabled (low level) Receive			-200 -25 -200			-200 -25 -200	mA mA mA

NOTE  
Output sink current is supplied through a resistor to ground.

**AC ELECTRICAL CHARACTERISTICS**

PARAMETER	TO	FROM	TEST CONDITIONS	8T26A			8T28			UNIT
				Min	Typ	Max	Min	Typ	Max	
$t_{ON}$	Rout	Dout	$C_L = 30pF$			14			17	ns
	Dout	Din	$C_L = 300pF$			14			17	ns
$t_{OFF}$	Rout	Dout	$C_L = 30pF$			14			17	ns
	Dout	Din	$C_L = 300pF$			14			17	ns
	0	High Z	$C_L = 300pF$			25			28	ns
$t_{PZL}$	High Z	0				20			23	ns
	0	High Z	$C_L = 30pF$			20			23	ns
$t_{PLZ}$	High Z	0				15			18	ns

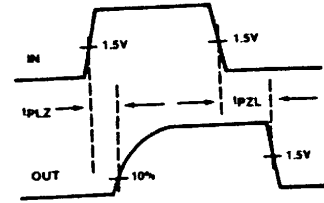
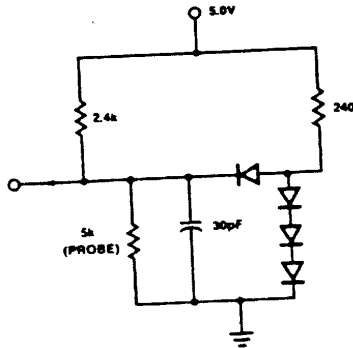
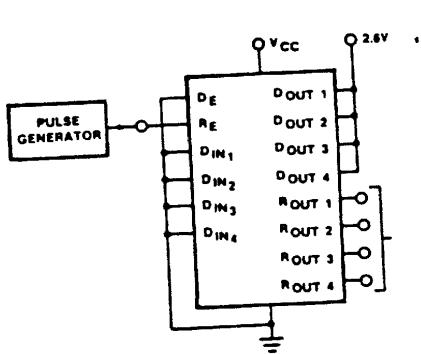
**TYPICAL APPLICATION**



PRE-RELEASE  
VERSION

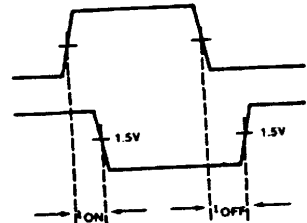
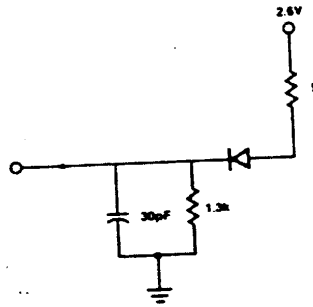
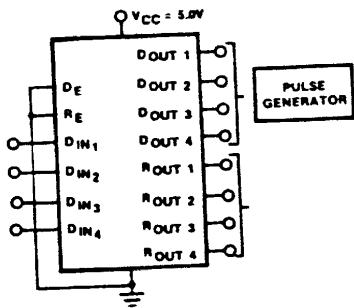
AC TEST CIRCUITS AND WAVEFORMS

PROPAGATION DELAY  
RECEIVE ENABLE TO RECEIVE OUTPUT



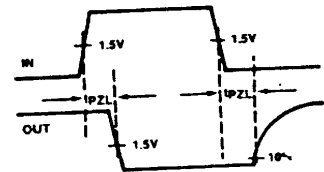
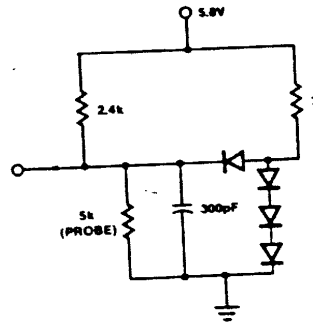
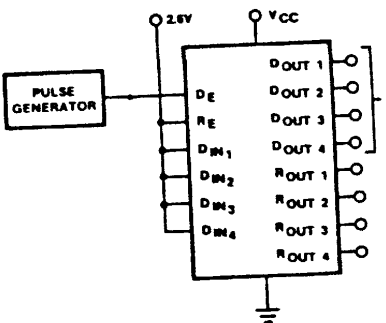
Input pulse:  
 $t_r = t_f = 5\text{ns}$  (10% to 90%)  
 freq = 5MHz (50% duty cycle)  
 Amplitude = 2.6V

DOUT TO ROUT



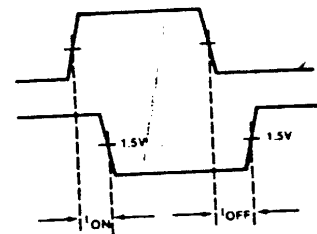
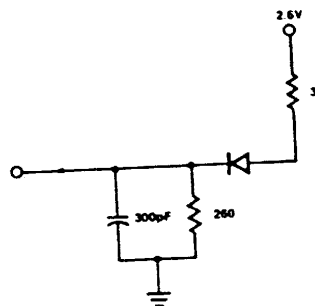
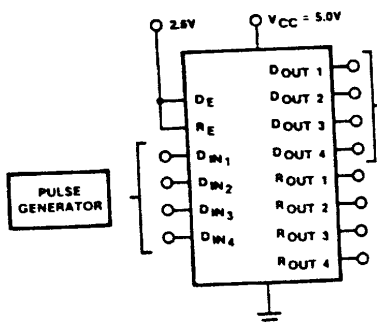
Input pulse:  
 $t_r = t_f = 5\text{ns}$  (10% to 90%)  
 freq = 10MHz (50% duty cycle)  
 Amplitude = 2.6V

DATA ENABLE TO DATA OUTPUT



Input pulse:  
 $t_r = t_f = 5\text{ns}$  (10% to 90%)  
 freq = 10MHz (50% duty cycle)  
 Amplitude = 2.6V

DIN TO DOUT





8T95  
8T96  
8T97  
8T98

FUNCTIONAL SPECIFICATION

DIGITAL 8T SERIES INTERFACE TTL/MSI

The Tri-State Bus Interface Elements described here have low current PNP inputs and is designed with high speed TTL technology for ultra high speed. The devices are designed to convert TTL/DTL or MOS/CMOS to tri-state bus levels. For maximum systems flexibility the 8T95 and 8T97 do so without logic inversion, whereas, the 8T96 and 8T98 provide the logical complement of the input. The 8T95 and 8T96 feature a common control line for all six outputs, whereas, the 8T97 and 8T98 have control lines for two outputs from one input and two from another input.

FEATURES

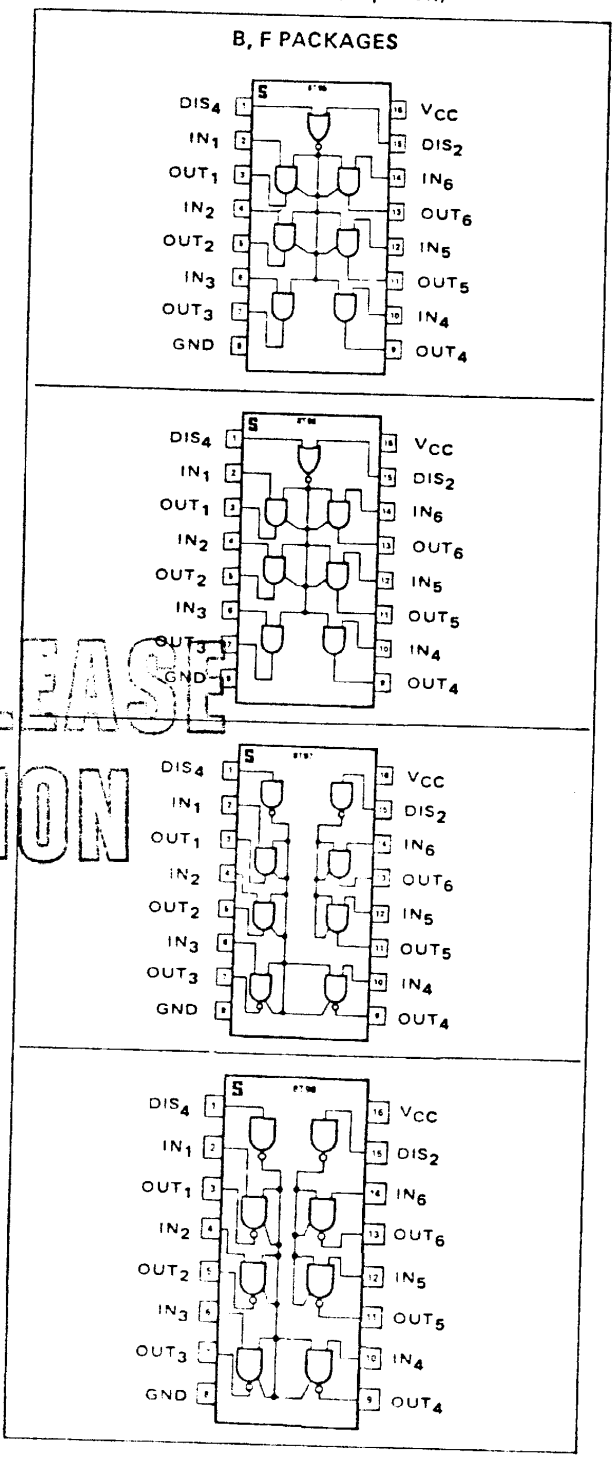
- LOW CURRENT PNP INPUTS (400µA)
- HIGH SPEED SHOTTKY TTL DESIGN (TYP. 8ns)
- TTL/DTL, MOS/CMOS COMPATIBLE
- LOW POWER DISSIPATION  
8T95/97 TYP. 325mW  
8T96/98 TYP. 295mW
- HIGH SPEED REPLACEMENTS FOR  
DM 8095 = 8T95  
DM 8096 = 8T96  
DM 8097 = 8T97  
DM 8098 = 8T98

PRE-RELEASE  
VERSION

8T95			
DISABLE DIS <sub>1</sub>	INPUT DIS <sub>2</sub>	INPUT	OUTPUT
0	0	0	0
0	0	1	1
0	1	x	H-z
1	0	x	H-z
1	1	x	H-z

8T96			
DISABLE DIS <sub>1</sub>	INPUT DIS <sub>2</sub>	INPUT	OUTPUT
0	0	0	1
0	0	1	0
0	1	x	H-z
1	0	x	H-z
1	1	x	H-z

(Top View)



HLS HIGH SPEED HLX TRI STATE BUFFERS/INVERTERS ■ 8T95/6/7/8

8T97

ENABLE	INPUT DIS <sub>2</sub>	INPUT	OUTPUT
0	0	0	0
0	0	1	1
x	1	x	H-Z*
1	x	x	H-Z**

8T98

DISABLE DIS <sub>4</sub>	INPUT DIS <sub>2</sub>	INPUT	OUTPUT
0	0	0	1
0	0	1	0
x	1	x	H-Z*
1	x	x	H-Z**

\*Output 5-6 only \*\*Output 1-4 only x = Irrelevant

Over Recommended Voltage and Temperature Range

CHARACTERISTIC	LIMITS				TEST CONDITIONS	NOTES
	MIN.	TYP.	MAX.	UNITS		
"1" Input Voltage	2.0			V	V <sub>CC</sub> = Min T <sub>A</sub> = 25°C	
"0" Input Voltage			0.8	V	V <sub>CC</sub> = Min T <sub>A</sub> = 25°C	
"1" Output Voltage	2.4			V	V <sub>CC</sub> = Min I <sub>0</sub> = -5.2 mA	6
"0" Output Voltage			0.5	V	I <sub>out</sub> = 48 mA	7
State Input Current			-40	μA	V <sub>CC</sub> = Max V <sub>in</sub> = 0.5V DIS = 2.0V	
State Output Current			40 -40	μA μA	V <sub>CC</sub> = Max V <sub>o</sub> = 2.4V V <sub>o</sub> = 0.5V	
"1" Input Current			40	μA	V <sub>CC</sub> = Max V <sub>in</sub> = 2.4V	
"0" Input Current			-400	μA	V <sub>CC</sub> = Max V <sub>IN</sub> = 0.5V DIS = 0.5V	
Short Circuit Current	-40	-80	-115	mA	V <sub>CC</sub> = Max V <sub>o</sub> = 0V	9, 10
Current (typical)			65 59	98mA 89mA	V <sub>CC</sub> = Max	
Current (max)					V <sub>CC</sub> = Max	
Voltage Rating	5.5			V	I <sub>in</sub> = 1 mA	
Clamp Voltage			-1.5	V	V <sub>CC</sub> = Min I <sub>in</sub> = -12 mA	
V <sub>CC</sub> Clamp Voltage			1.5	V	V <sub>CC</sub> = 0V I <sub>o</sub> = 12 mA	

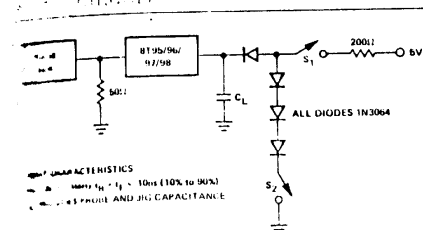
SIGNLETICS HIGH SPEED HLX TRI STATE BUFFERS/INVERTERS ■ 81

T<sub>A</sub> = 25°C and V<sub>CC</sub> = 5.0V

CHARACTERISTIC	LIMITS				TEST CONDITIONS	NOTE
	MIN.	TYP.	MAX.	UNITS		
Propagation Delays (All Devices)					See AC Test Figures	
Data Inputs to			5			
Data Outputs			6			
Logic "1" to High Z				t <sub>PIH</sub>		
Logic "0" to High Z				t <sub>POH</sub>		
High Z to Logic "1"				t <sub>PHI</sub>		
High Z to Logic "0"				t <sub>PHO</sub>		
			4	ns		
			6	ns		
			10	ns		
			12	ns		

6. Output source current is supplied through a resistor.  
7. Output sink current is supplied through a resistor.  
8. Refer to AC Test Figures and Test Table.  
9. V<sub>CC</sub> = 5.25V.  
10. Not more than one output should be shorted at a time.

PRE-RELEASE  
VERSION



	S <sub>1</sub>	S <sub>2</sub>
t <sub>on</sub>	Closed	Closed
t <sub>off</sub>	Closed	Closed
t <sub>OH</sub>	Closed	Closed
t <sub>1H</sub>	Closed	Closed
t <sub>HO</sub>	Closed	Open

# PRE-RELEASE TIMER 555

## VERSION LINEAR INTEGRATED CIRCUITS

### DESCRIPTION

The SE 555 monolithic timing circuit is a highly stable timer capable of producing accurate time delays, or oscillation. Additional terminals are provided for triggering and resetting if desired. In the time delay mode of operation, the time is precisely controlled by one external resistor and one capacitor. For a stable operation as an oscillator, the timing frequency and the duty cycle are both accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output structure can source or sink up to 200mA in active TTL circuits.

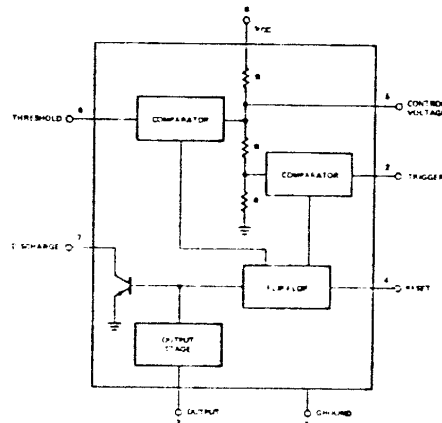
### FEATURES

- TIMING FROM MICROSECONDS THROUGH HOURS
- OPERATES IN BOTH ASTABLE AND MONOSTABLE MODES
- ADJUSTABLE DUTY CYCLE
- HIGH CURRENT OUTPUT CAN SOURCE OR SINK 200mA
- OUTPUT CAN DRIVE TTL
- TEMPERATURE STABILITY OF 0.005% PER °C
- NORMALLY ON AND NORMALLY OFF OUTPUT

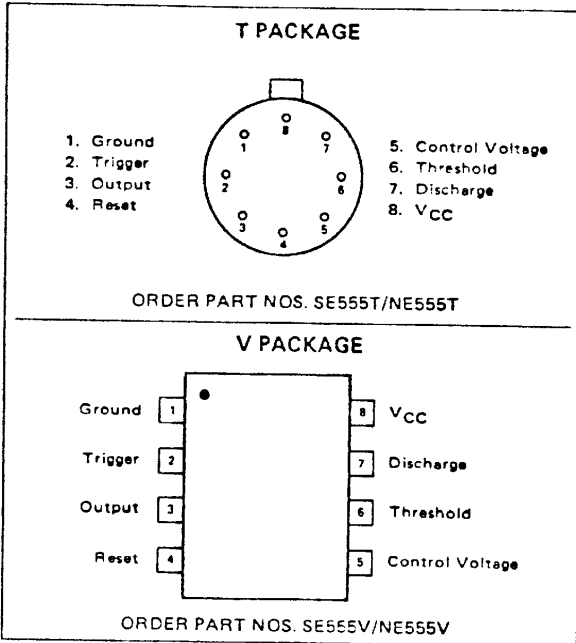
### APPLICATIONS

- PRECISION TIMING
- PULSE GENERATION
- SQUENTIAL TIMING
- TIME DELAY GENERATION
- PULSE WIDTH MODULATION
- PULSE POSITION MODULATION
- MISSING PULSE DETECTOR

### BLOCK DIAGRAM



### PIN CONFIGURATIONS (Top View)



### ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+18V
Power Dissipation	600 mW
Operating Temperature Range	
NE555	0°C to +70°C
SE555	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 60 seconds)	+300°C

NE 555 TIMER # 555

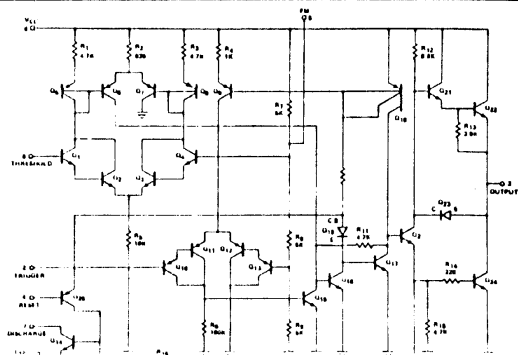
SIGNATURE 15

CHARACTERISTICS  $T_A = 25^\circ\text{C}$ ,  $V_{CC} = +5\text{V}$  to  $+15$  unless otherwise specified

PARAMETER	TEST CONDITIONS	SE 555			NE 555		
		MIN	TYP	MAX	MIN	TYP	MAX
Supply Voltage		4.5		18	4.5		16
Supply Current	$V_{CC} = 5\text{V}$ $R_L = \infty$ $V_{CC} = 15\text{V}$ $R_L = \infty$ Low State, Note 1		3 10	5 12		3 10	6 15
Timing Error (Monostable)	$R_A, R_B = 1\text{K}\Omega$ to $100\text{K}\Omega$ $C = 0.1\ \mu\text{F}$ Note 2						
Initial Accuracy			0.5	2		1	
Drift with Temperature			30	100		50	
Drift with Supply Voltage			0.05	0.2		0.1	
Threshold Voltage			2/3			2/3	
Trigger Voltage	$V_{CC} = 15\text{V}$	4.8	5	5.2		5	
Timing Error (Astable)	$V_{CC} = 5\text{V}$	1.45	1.67	1.9		1.67	
Trigger Current			0.5			0.5	
Reset Voltage		0.4	0.7	1.0	0.4	0.7	1.0
Reset Current			0.1			0.1	
Threshold Current	Note 3		0.1	.25		0.1	.25
Control Voltage Level	$V_{CC} = 15\text{V}$ $V_{CC} = 5\text{V}$ $V_{CC} = 15\text{V}$	9.6 2.9	10 3.33	10.4 3.8	9.0 2.6	10 3.33	11 4
Output Voltage (low)	$I_{SINK} = 10\text{mA}$ $I_{SINK} = 50\text{mA}$ $I_{SINK} = 100\text{mA}$ $I_{SINK} = 200\text{mA}$ $V_{CC} = 5\text{V}$ $I_{SINK} = 8\text{mA}$ $I_{SINK} = 5\text{mA}$		0.1 0.4 2.0 2.5	0.15 0.5 2.2	0.1 0.4 2.0 2.5	.75 .75 2.5 2.5	
Output Voltage Drop (low)	$I_{SOURCE} = 200\text{mA}$ $V_{CC} = 15\text{V}$ $I_{SOURCE} = 100\text{mA}$ $V_{CC} = 15\text{V}$ $V_{CC} = 5\text{V}$		12.5 3.0		12.5 2.75		.25 3.3
Rise Time of Output			100			100	
Fall Time of Output			100			100	

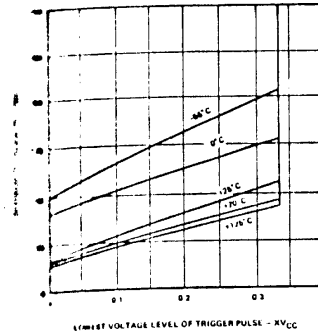
ES  
Supply Current when output high typically 1mA less.  
tested at  $V_{CC} = 5\text{V}$  and  $V_{CC} = 15\text{V}$   
This will determine the maximum value of  $R_A + R_B$ . For 15V operation, the max total R = 20 megohm.

UNIVALENT CIRCUIT (Shown for One Side Only)

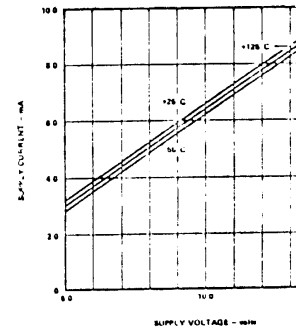


CHARACTERISTICS

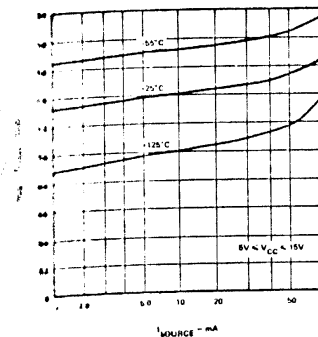
MINIMUM PULSE WIDTH REQUIRED FOR TRIGGERING



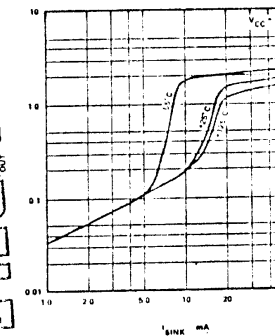
SUPPLY CURRENT vs SUPPLY VOLTAGE



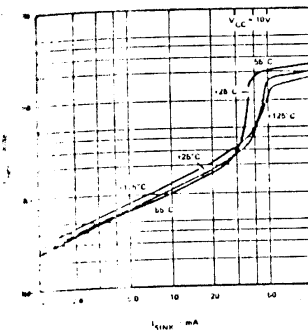
LOW OUTPUT VOLTAGE vs OUTPUT SINK CURRENT



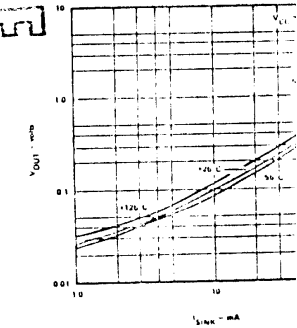
HIGH OUTPUT VOLTAGE vs OUTPUT SOURCE CURRENT



LOW OUTPUT VOLTAGE vs OUTPUT SINK CURRENT



LOW OUTPUT VOLTAGE vs OUTPUT SINK CURRENT



PRE-RELEASE VERSION

### DESCRIPTION

The SA/SE/NE558 and 559 Quad Timers are monolithic timing devices which can be used to produce four entirely independent timing functions. The 558 output sinks current whereas the 559 sources current. These highly stable, general purpose controllers can be used in a monostable mode to produce accurate time delays, from microseconds to hours. In the time delay mode of operation, the time is precisely controlled by one external resistor and one capacitor. Astable operation can be achieved by using two of the four timer sections.

The four timing sections in the 558 and 559 are edge triggered; therefore, when connected in tandem for sequential timing applications, no coupling capacitors are required. Output current capability of 100mA is provided in both devices.

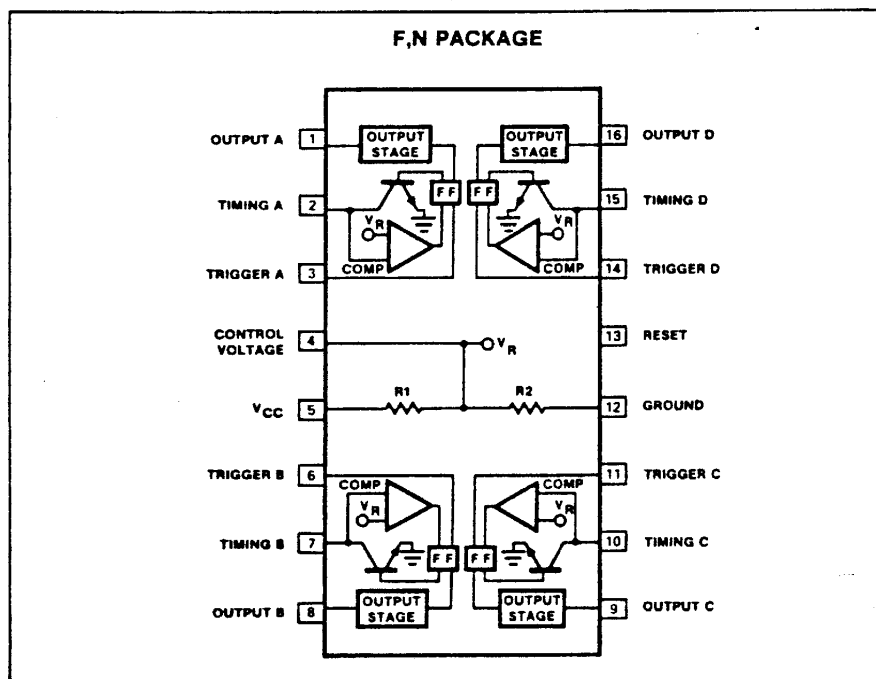
### FEATURES

- 100mA output current per section
- Edge triggered (no coupling capacitor)
- Output independent of trigger conditions
- Wide supply voltage range 4.5V to 18V
- Timer intervals from microseconds to hours
- Time period equals RC
- Military qualifications pending

### APPLICATIONS

- Sequential timing
- Time delay generation
- Precision timing
- Industrial controls
- Quad one-shot

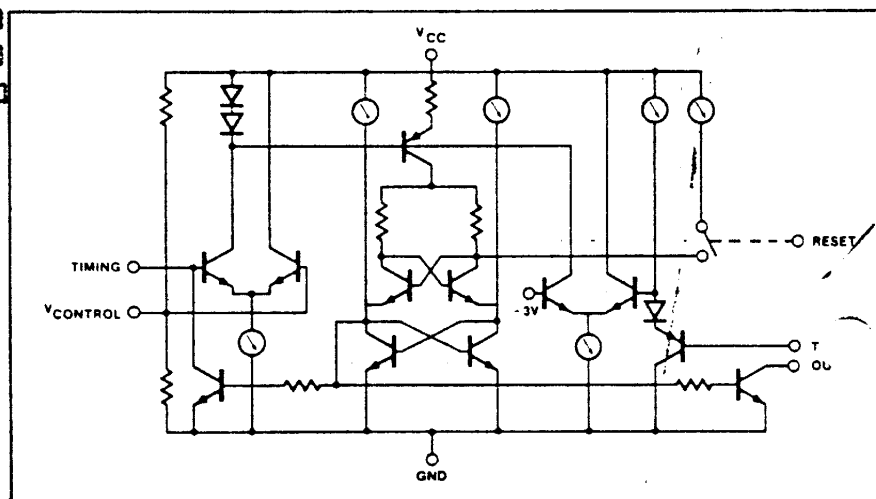
### PIN CONFIGURATION



### ABSOLUTE MAXIMUM RATINGS

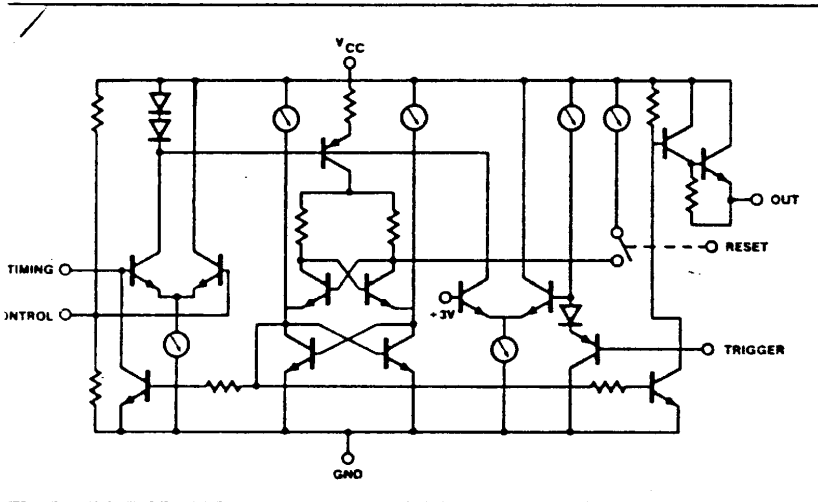
PARAMETER	RATING	UNIT
Supply voltage		
..SE558, SE559	+18	V
NE558, NE559	+16	V
SA558, SA559	+16	V
Power dissipation	1.25	W
Operating temperature range		
NE558, NE559	0 to +70	°C
SA558, SA559	-40 to +85	°C
SE558, SE559	-55 to +125	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering, 60sec)	+300	°C

### 558 EQUIVALENT CIRCUIT



RE-RELEASE  
VERSION

**EQUIVALENT CIRCUIT**



**PRE-RELEASE  
VERSION**

**CRITICAL CHARACTERISTICS**  $T_A = 25^\circ C$ ,  $V_{CC} = +5V$  to  $+15V$  unless otherwise specified.

PARAMETER	TEST CONDITIONS	SE558/SE559			NE558/NE559 SA558/SA559			UNIT
		Min	Typ	Max	Min	Typ	Max	
Supply voltage		4.5		18	4.5		16	V
Supply current (558) (559)	$V_{CC} = \text{Reset} = 15V$		21	32		27	36	mA
Timing accuracy ( $T = RC$ )	$V_{CC} = \text{Reset} = 15V$ $R = 2k\Omega$ to $100k\Omega$ $C = 1\mu F$		9	16		12	18	mA
Initial accuracy			1.0	3		2		%
Drift with temperature			150			150		ppm/ $^\circ C$
Drift with supply voltage			0.1			0.1		%/V
Trigger voltage <sup>1</sup>	$V_{CC} = 15V$	0.8	1.5	2.4	0.8	1.5	2.4	V
Trigger current	Trigger = 0V		5	30		5	100	$\mu A$
Reset voltage <sup>2</sup>		0.8	1.5	2.4	0.8	1.5	2.4	V
Reset current	Reset		50	300		50		$\mu A$
Threshold voltage			0.63			0.63		$\times V_{CC}$
Threshold leakage			15			15		nA
Output voltage (558) <sup>3</sup>	$I_L = 10mA$		0.1	0.2		0.1	0.4	V
	$I_L = 100mA$		0.7	1.5		1.0	2.0	V
Output voltage (559) <sup>4</sup>	$I_L = 10mA$	13	13.6		12.5	13.3		V
	$I_L = 100mA$	12.5	13.3		12.0	13.0		V
Output leakage			10			10		nA
Propagation delay(558)			1.0			1.0		$\mu s$
(559)			0.4			0.4		$\mu s$
Risetime of output	$I_L = 100mA$		100			100		ns
Falltime of output	$I_L = 100mA$		100			100		ns

<sup>1</sup> Trigger functions only on the falling edge of the trigger pulse only after previously being high. After reset the trigger must be brought high and then low to implement triggering.

<sup>2</sup> Reset below 0.8 volts, outputs set low and trigger inhibited. For reset above 2.4 volts, trigger enabled.

<sup>3</sup> 558 output structure is open collector which requires a pull up resistor to  $V_{CC}$  to source current. The output is normally low sinking current.

<sup>4</sup> 559 output structure is a darlington emitter follower which requires a pull down resistor to ground to source current. The output is normally low and sources current when switched high.

# PRE-RELEASE GENERAL PURPOSE OPERATIONAL AMPLIFIER $\mu$ A741

## VERSION LINEAR INTEGRATED CIRCUITS

### DESCRIPTION

The  $\mu$ A741 is a high performance operational amplifier with high open loop gain, internal compensation, high common mode range and exceptional temperature stability. The  $\mu$ A741 is short-circuit protected and allows for nulling of output voltage.

### FEATURES

- INTERNAL FREQUENCY COMPENSATION
- SHORT CIRCUIT PROTECTION
- OFFSET VOLTAGE NULL CAPABILITY
- EXCELLENT TEMPERATURE STABILITY
- HIGH INPUT VOLTAGE RANGE
- NO LATCH-UP

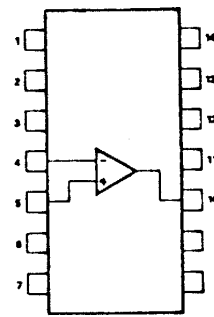
### ABSOLUTE MAXIMUM RATINGS

	$\mu$ A741C	$\mu$ A741
Supply Voltage	$\pm 18V$	$\pm 22V$
Output Power		
Load (Note 1)	500mW	500mW
Differential Input Voltage	$\pm 30V$	$\pm 30V$
Output Voltage (Note 2)	$\pm 15V$	$\pm 15V$
Voltage between Offset Null and $V^-$	$\pm 0.5V$	$\pm 0.5V$
Operating Temperature Range	$0^\circ C$ to $+70^\circ C$	$-55^\circ C$ to $+125^\circ C$
Storage Temperature Range	$-65^\circ C$ to $+150^\circ C$	$-65^\circ C$ to $+150^\circ C$
Lead Temperature (solder, 60 sec)	$300^\circ C$	$300^\circ C$
Output Short Circuit Duration (Note 3)	Indefinite	Indefinite

Rating applies for case temperatures to  $125^\circ C$ ; derate linearly at  $5 \text{ mW}/^\circ C$  for ambient temperatures above  $+75^\circ C$ .  
 For supply voltages less than  $\pm 15V$ , the absolute maximum input voltage is equal to the supply voltage.  
 Short circuit may be to ground or either supply. Rating applies to  $125^\circ C$  case temperature or  $+75^\circ C$  ambient temperature.

### PIN CONFIGURATIONS (TOP VIEW)

#### A PACKAGE

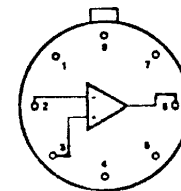


- 1. NC
- 2. NC
- 3. Offset Null
- 4. Inv. Input
- 5. Non-Inv. Input
- 6.  $V^-$
- 7. NC
- 8. NC
- 9. Offset Null
- 10. Output
- 11.  $V^+$
- 12. NC
- 13. NC
- 14. NC

ORDER PART NO.  $\mu$ A741CA

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#### T PACKAGE

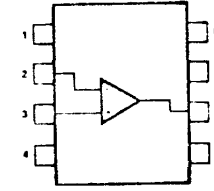


- 1. Offset Null
- 2. Inverting Input
- 3. Non-Inverting Input
- 4.  $V^-$
- 5. Offset Null
- 6. Output
- 7.  $V^+$
- 8. NC

ORDER PART NOS.  $\mu$ A741T/ $\mu$ A741CT

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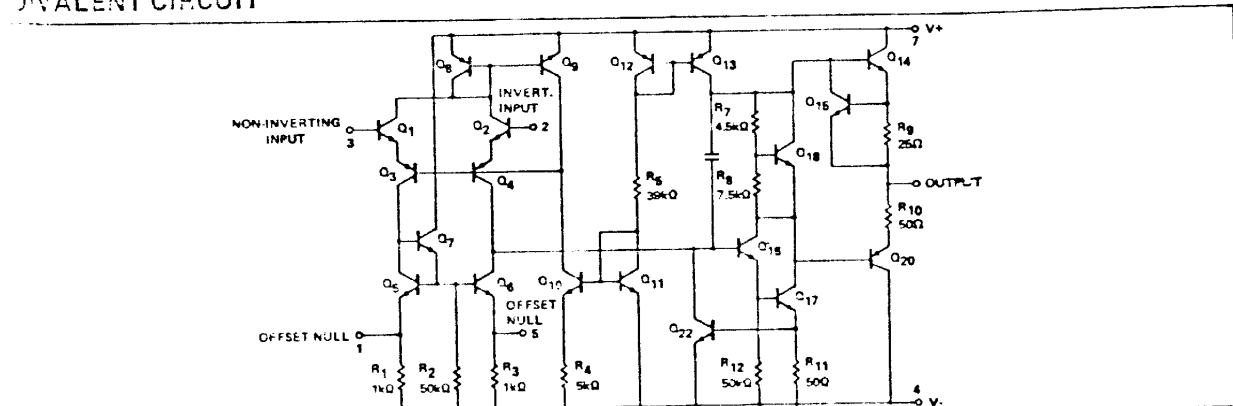
#### V PACKAGE



- 1. Offset Null
- 2. Inv. Input
- 3. Non-Inv. Input
- 4.  $V^-$
- 5. Offset Null
- 6. Output
- 7.  $V^+$
- 8. NC

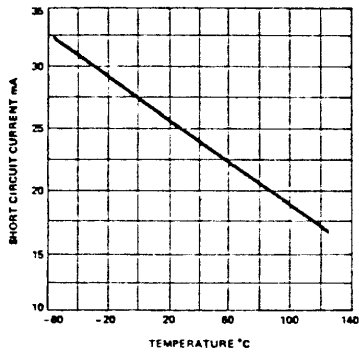
ORDER PART NO.  $\mu$ A741CV

### UNIVALENT CIRCUIT

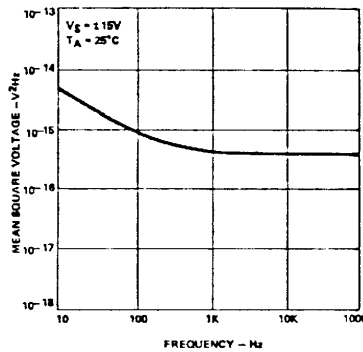


SIGNETICS GENERAL PURPOSE OPERATIONAL AMPLIFIER  $\mu$ A741

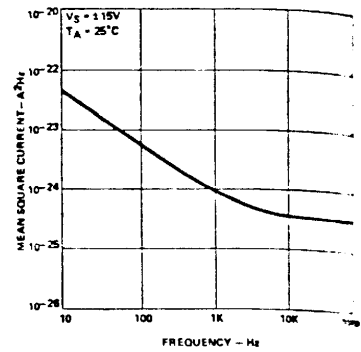
OUTPUT SHORT-CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



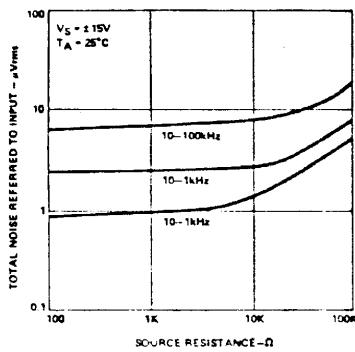
INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



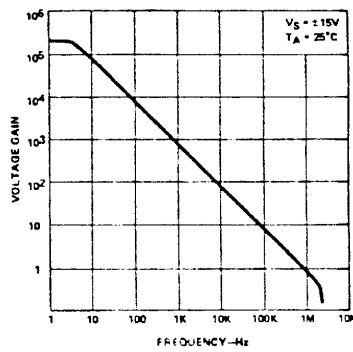
INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY



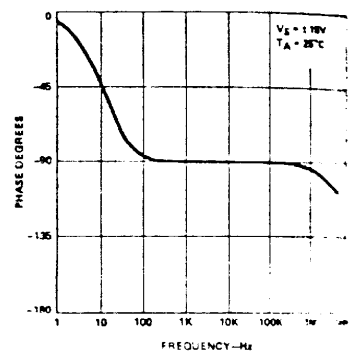
BROADBAND NOISE FOR VARIOUS BANDWIDTHS



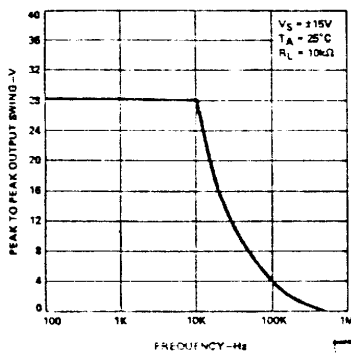
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



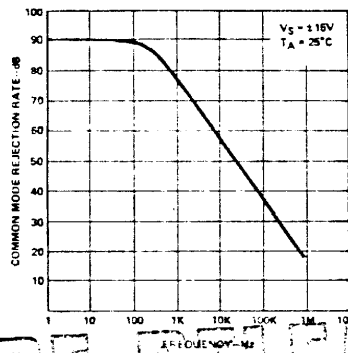
OPEN LOOP PHASE RESPONSE AS A FUNCTION OF FREQUENCY



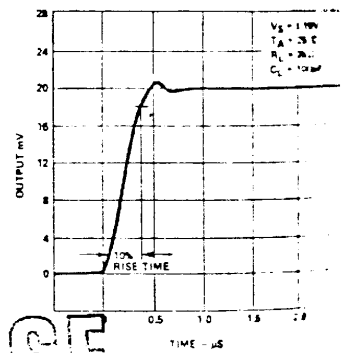
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



TRANSIENT RESPONSE



PRE-RELEASE  
VERSION

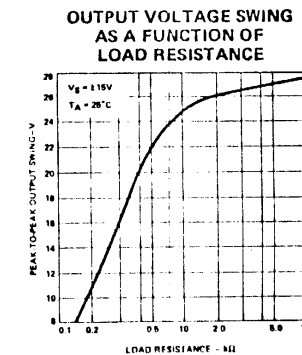
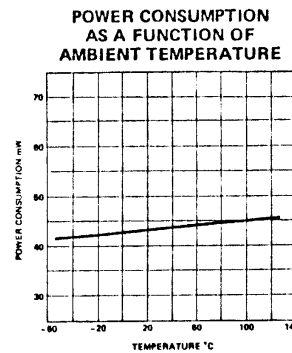
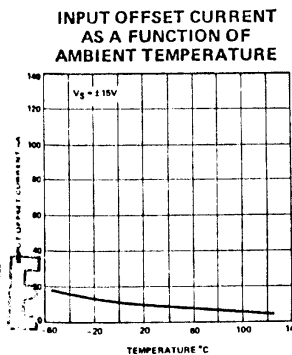
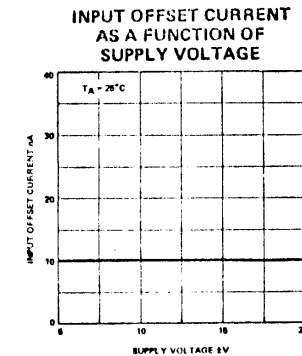
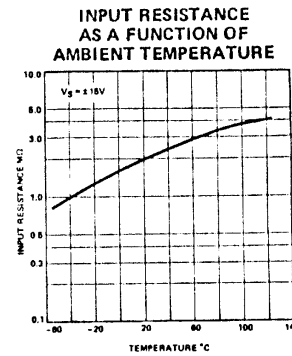
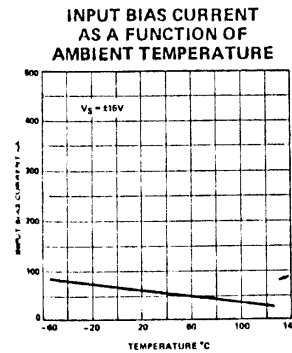
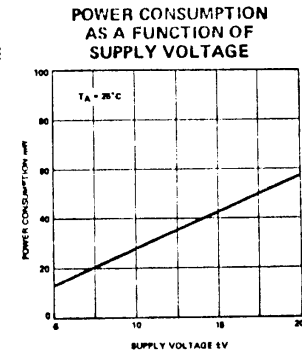
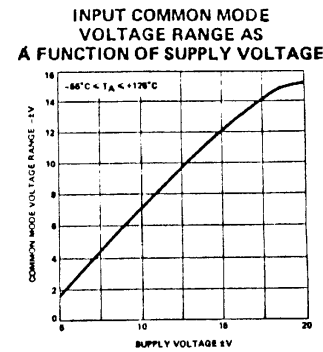
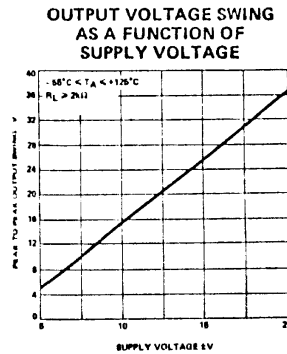
CHARACTERISTICS ( $V_S = \pm 15V$ ,  $T_A = 25^\circ C$  unless otherwise specified)

	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
<b><math>\mu A741C</math></b>					
Voltage	0.3	2.0	6.0	mV	$R_S < 10k\Omega$
		20	200	nA	
Gain		80	500	nA	$R_S < 10k\Omega$
		2.0		M $\Omega$	
Gain		1.4		pF	$R_S < 10k\Omega$
		$\pm 15$		mV	
Gain	$\pm 12$	$\pm 13$		V	$R_S < 10k\Omega$
	70	90		dB	
Gain		10	150	$\mu V/V$	$R_S < 10k\Omega$
		200,000		V	
Gain	20,000	$\pm 14$		V	$R_L > 2k\Omega, V_{out} = \pm 10V$
	$\pm 12$	$\pm 13$		V	
Gain	$\pm 10$	75		$\Omega$	$R_L > 2k\Omega$
		25		mA	
Gain		1.4	2.8	mA	$V_{in} = 20mV, R_L = 2k\Omega, C_L < 10\mu F$
		50	85	mW	
Gain		0.3		$\mu s$	$R_L > 2k\Omega$
		5.0		%	
Gain		0.5		V/ $\mu s$	$R_L > 2k\Omega$
			7.5	mV	
Gain			300	nA	$R_L > 2k\Omega, V_{out} = \pm 10V$
			800	nA	
Gain	15,000			V	$R_L > 2k\Omega$
	$\pm 10$	$\pm 13$		V	

	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
<b><math>\mu A741</math></b>					
Voltage	0.3	1.0	5.0	mV	$R_S < 10k\Omega$
		10	200	nA	
Gain		80	500	nA	$R_S < 10k\Omega$
		2.0		M $\Omega$	
Gain		1.4		pF	$R_S < 10k\Omega$
		$\pm 15$		mV	
Gain	50,000	$\pm 14$		V	$R_L > 2k\Omega, V_{out} = \pm 10V$
		$\pm 13$		V	
Gain		10	150	$\mu V/V$	$R_L > 2k\Omega$
		200,000		V	
Gain	25,000	$\pm 14$		V	$R_L > 2k\Omega, V_{out} = \pm 10V$
	$\pm 12$	$\pm 13$		V	
Gain	$\pm 10$	15	2.5	mA	$T_A = +125^\circ C$
		5.0	3.3	mA	
Gain		45	75	mW	$T_A = -55^\circ C$
		0.3	100	mW	
Gain		0.5		$\mu s$	$T_A = +125^\circ C$
		5.0		%	
Gain		0.5		V/ $\mu s$	$T_A = -55^\circ C$
			7.5	mV	
Gain			300	nA	$T_A = +125^\circ C$
			800	nA	
Gain	15,000			V	$T_A = -55^\circ C$
	$\pm 10$	$\pm 13$		V	

PRE-RELEASE  
VERSION

TYPICAL CHARACTERISTIC CURVES





# 64X8X5 CHARACTER GENERATOR

251

## SILICON GATE MOS 2500 SERIES

### DESCRIPTION

The Signetics 2513 is a high speed 2560-bit Static ROM organized as 64x8x5. A standard 7x5 dot matrix fits well in the 2513. The product uses +5V, -5V and -12V power supplies, TTL level interface signals and Tri-State Outputs for direct, low cost interfacing with TTL, DTL, CMOS and 2500 Series MOS.

### FEATURES

- 450 ns TYPICAL ACCESS TIME
- STATIC OPERATION
- TTL/DTL COMPATIBLE INPUTS
- +5, -5, -12V POWER SUPPLIES
- TRI-STATE OUTPUT CONTROLLED BY CHIP ENABLE FOR BUSSING CAPABILITY
- 2513/CM2140 ASCII FONT STANDARD (7 X 5)
- 24-PIN DIP
- P-MOS SILICON GATE TECHNOLOGY

### APPLICATIONS

RASTER SCAN CRT DISPLAYS (ROW OUTPUT)  
 PRINTER CHARACTER GENERATOR  
 PANEL DISPLAYS AND BILLBOARDS  
 MICRO-PROGRAMMING  
 CODE CONVERSION

### PROCESS TECHNOLOGY

The use of Signetics' P channel Silicon Gate Process allows the design and production of higher functional density and operating speed than other techniques.

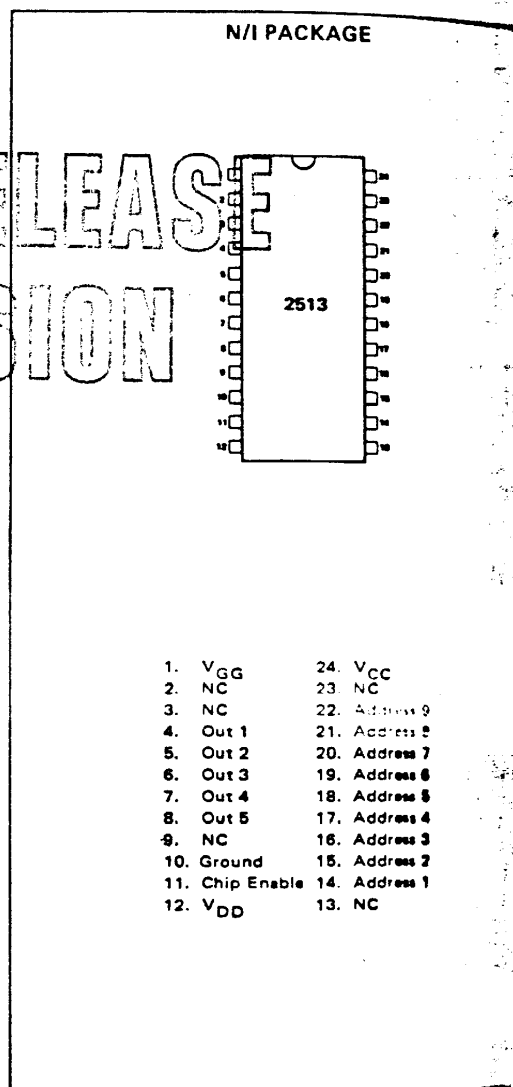
### SILICONE PACKAGING

Low cost silicone DIP packaging is implemented and reliability is assured by the use of Signetics unique silicon gate MOS process technology. Unlike the standard metal gate MOS process the silicon material over the gate oxide passivates the MOS transistors. In addition, Signetics proprietary surface passivation and silicone packaging techniques result in an MOS circuit with inherent high reliability, superior moisture resistance, and ionic contamination barriers.

### BIPOLAR COMPATIBILITY

All inputs of the 2513 can be driven directly by standard TTL voltage levels. The data output buffers are capable of sinking a minimum of 1.6 mA, sufficient to drive one standard TTL load.

### PIN CONFIGURATION (Top View)



- |                     |                     |
|---------------------|---------------------|
| 1. V <sub>GG</sub>  | 24. V <sub>CC</sub> |
| 2. NC               | 23. NC              |
| 3. NC               | 22. Address 9       |
| 4. Out 1            | 21. Address 8       |
| 5. Out 2            | 20. Address 7       |
| 6. Out 3            | 19. Address 6       |
| 7. Out 4            | 18. Address 5       |
| 8. Out 5            | 17. Address 4       |
| 9. NC               | 16. Address 3       |
| 10. Ground          | 15. Address 2       |
| 11. Chip Enable     | 14. Address 1       |
| 12. V <sub>DD</sub> | 13. NC              |

### PART IDENTIFICATION TABLE

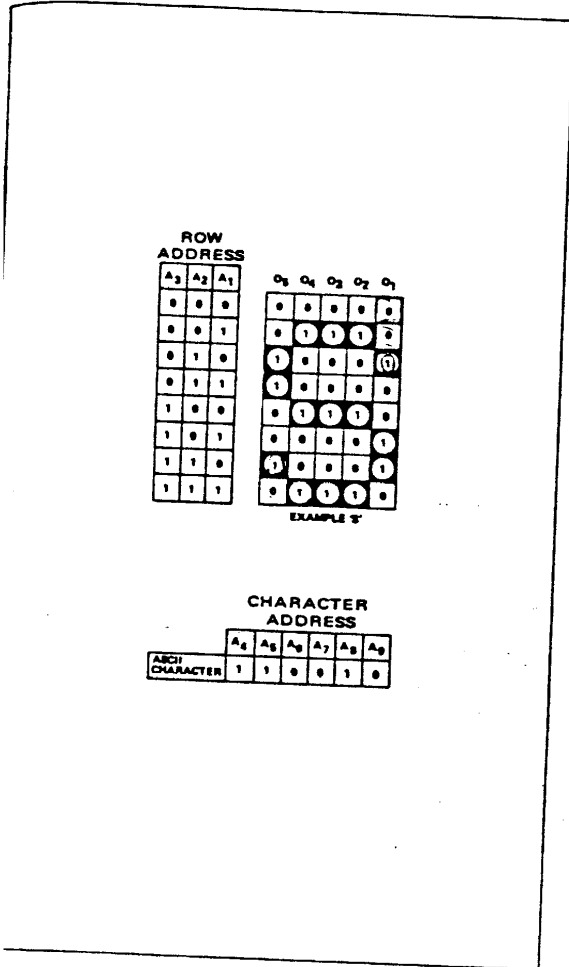
PART	ORGANIZATION	PROGRAMMING
2513N/I		
CM2140	64X8X5	ASCII Font
2513N/I	64X7X5	
CMXXXX	64X8X5	Custom

N PACKAGE = 24 PIN SILICONE DIP

I PACKAGE = 24 PIN CERAMIC DIP

SIGNETICS 64 X 8 X 5 CHARACTER GENERATOR ■ 2513

CHARACTER FORMAT



MAXIMUM GUARANTEED RATINGS(1)

Operating Ambient Temperature	0°C to 70°C
Storage Temperature	-65°C to +150°C
Package Power Dissipation(2) @T <sub>A</sub> 70°C	730mW
Input(3) and Supply Voltages with respect to V <sub>CC</sub>	+0.3 to -20V

PRE-RELEASE  
VERSION

NOTES

1. Stresses above those listed under "Maximum Guaranteed Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.
2. For operating at elevated temperatures the device must be derated based on a +150°C maximum junction temperature and a thermal resistance of 110°C/W junction to ambient.
3. All inputs are protected against static charge.
4. Parameters are valid over operating temperature range unless specified.
5. All voltage measurements are referenced to ground.
6. Manufacturer reserves the right to make design and process changes and improvements.
7. Typical values are at +25°C and nominal supply voltages.
8. Guaranteed input levels are stated for worst case conditions including a ±5% variation in V<sub>CC</sub> and a temperature variation of 0°C to +70°C. Actual input requirements with respect to V<sub>CC</sub> are V<sub>IH</sub> = V<sub>CC</sub> - 1.85V and V<sub>IL</sub> = V<sub>CC</sub> - 4.15V.

CHARACTERISTICS

= 0°C to +70°C; V<sub>CC</sub> = +5V ±5%; V<sub>DD</sub> = -5V ±5%; V<sub>GG</sub> = -12V ±5% unless otherwise noted. (Notes 4, 5, 6, 7)

SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
I <sub>LI</sub>	Input Load Current		10	500	nA	V <sub>IN</sub> = -5.5V T <sub>A</sub> = 25°C
I <sub>LO</sub>	Output Leakage Current		10	1000	nA	V <sub>OUT</sub> = -5.5V T <sub>A</sub> = 25°C V <sub>CE</sub> = V <sub>CC</sub>
I <sub>DD</sub>	V <sub>DD</sub> Power Supply Current		12	15	mA	Outputs Open
I <sub>GG</sub>	V <sub>GG</sub> Power Supply Current		10	15	mA	Outputs Open V <sub>CE</sub> = V <sub>CC</sub>
V <sub>IL</sub>	Input Logic "0"			+0.6	V	Note 8
V <sub>IH</sub>	Input Logic "1"	+3.4		5.3	V	Note 8

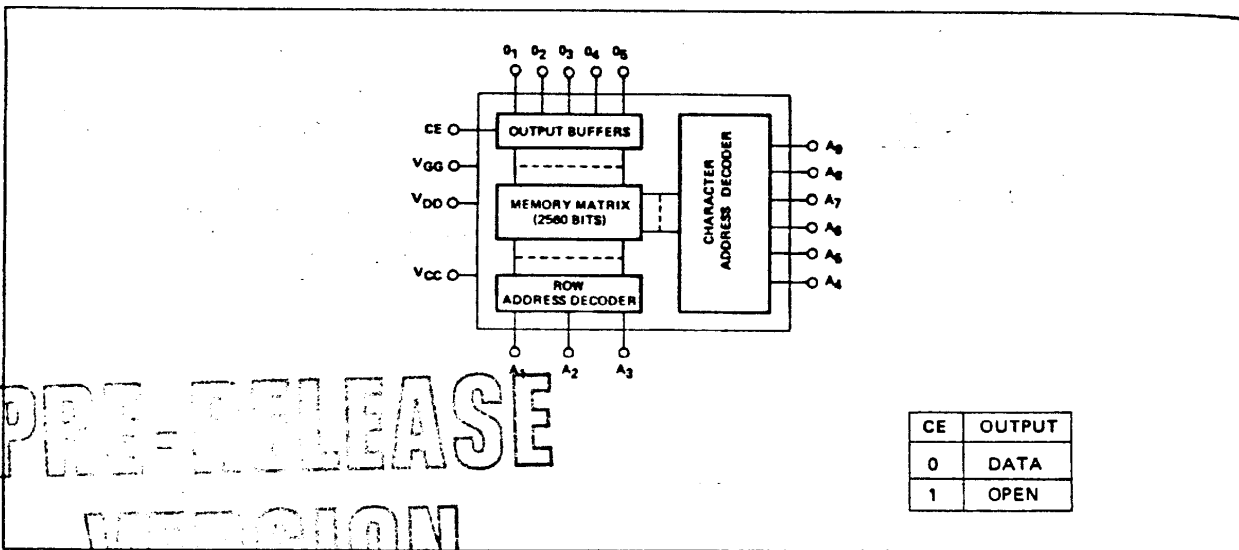
**SIGNETICS 64 X 8 X 5 CHARACTER GENERATOR ■ 2513**

**AC CHARACTERISTICS**

$T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ ;  $V_{CC} = 5\text{V} \pm 5\%$ ;  $V_{DD} = -5\text{V} \pm 5\%$ ;  $V_{GG} = -12\text{V} \pm 5\%$ ; unless otherwise noted.

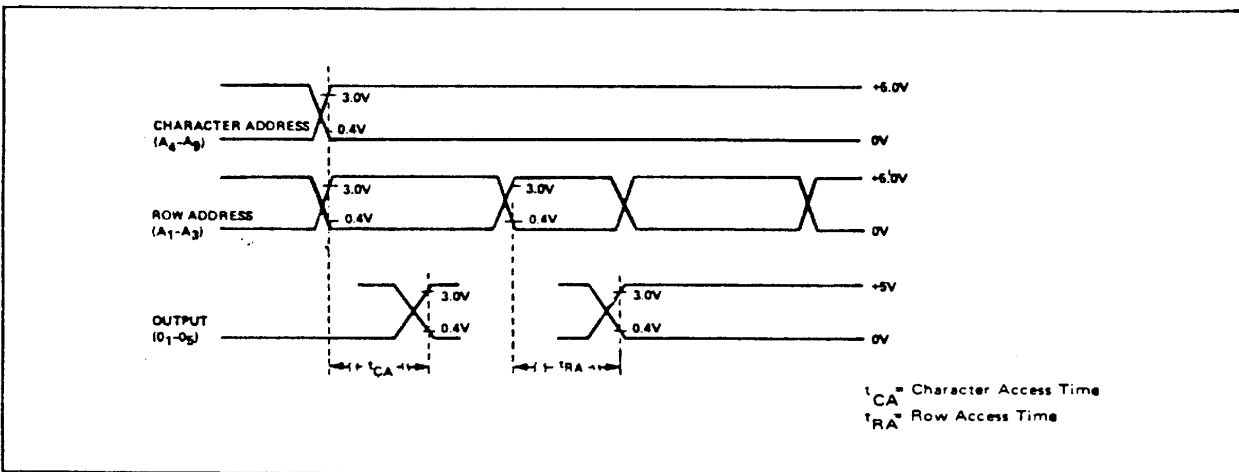
SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
$V_{OL}$	Output Logic "Zero"	-5		0.4	V	One TTL Load
$V_{OH}$	Output Logic "One"	3.0			V	One TTL Load
$t_{CA}(\text{CM2140})$	Character Access Time		500	600	ns	See AC Test Setup
$t_{RA}$	Row Access Time ( $A_1 - A_3$ )		450	500	ns	See AC Test Setup
$t_{CE}$	Chip Enable to Output		150		ns	
$C_{IN}$	Address Input Capacitance			10	pF	$f = 1\text{ MHz}$ , $V_{IH} = V_{CC}$ , $25\text{mV p-p}$

**BLOCK DIAGRAM**



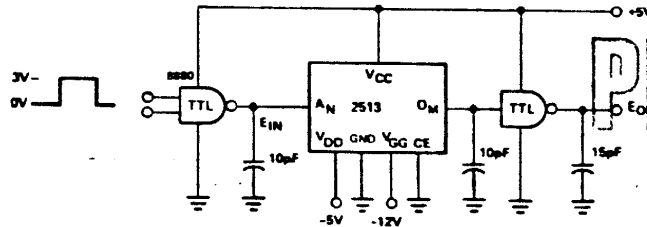
PRE-RELEASE  
VERSION

**TIMING DIAGRAM**



SIGNETICS 64 X 8 X 5 CHARACTER GENERATOR ■ 2513

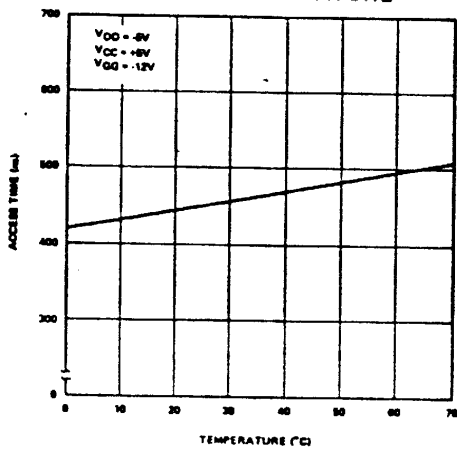
TEST SETUP



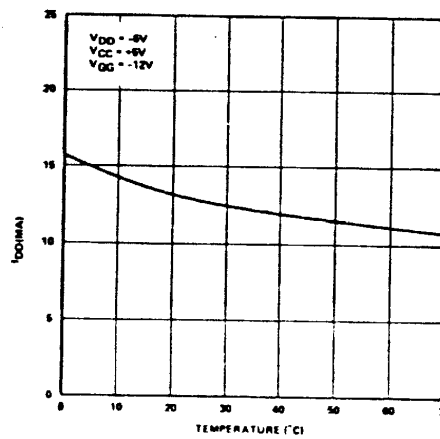
PRE-RELEASE  
VERSION

TYPICAL CHARACTERISTIC CURVES

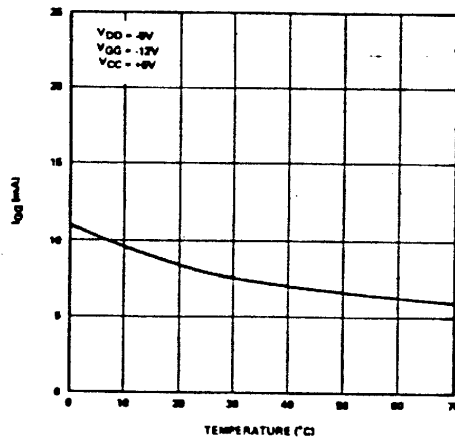
TYPICAL ACCESS TIME  
VERSUS TEMPERATURE



V<sub>DD</sub> POWER SUPPLY CURRENT  
VERSUS TEMPERATURE

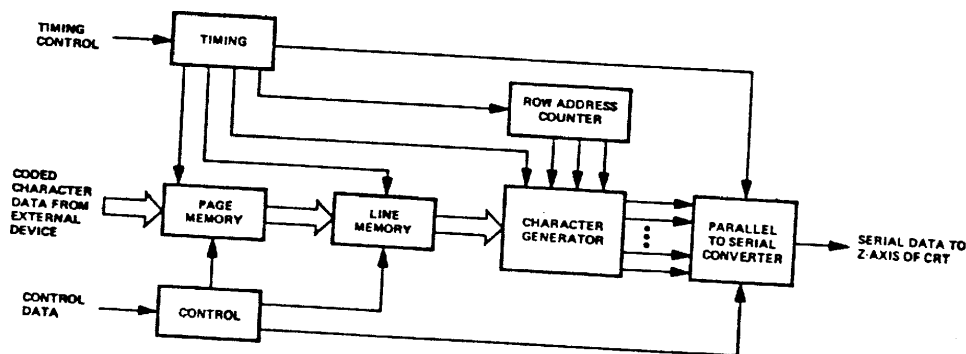


V<sub>GG</sub> POWER SUPPLY CURRENT  
VERSUS TEMPERATURE



# SIGNETICS 64 X 8 X 5 CHARACTER GENERATOR ■ 2513

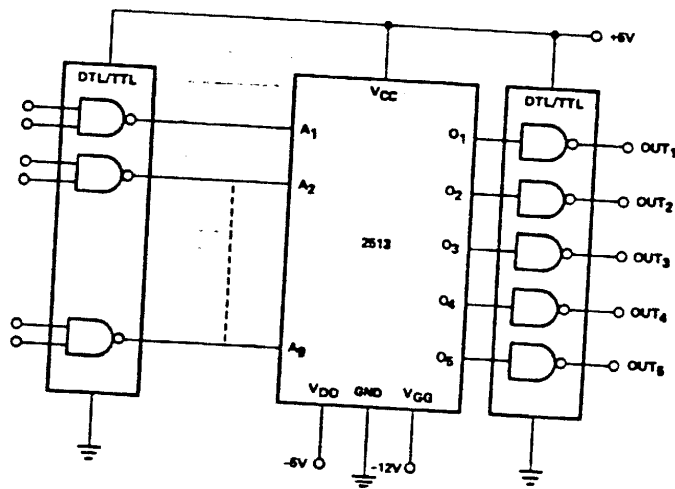
## APPLICATIONS INFORMATION



**APPLICATION INFORMATION**  
**CHARACTER GENERATOR:** The 2513 is designed to provide the information needed to convert the character codes into a dot matrix for display.  
**PAGE MEMORY:** THIS MEMORY CONTAINS CHARACTER CODES. TYPICALLY, IT CONTAINS THE SAME NUMBER OF CHARACTER CODES AS THE NUMBER OF CHARACTERS ON A FULL SCREEN.  
**LINE MEMORY:** THIS MEMORY CONTAINS THE CHARACTER CODES FOR ONE LINE OF THE CRT DISPLAY.

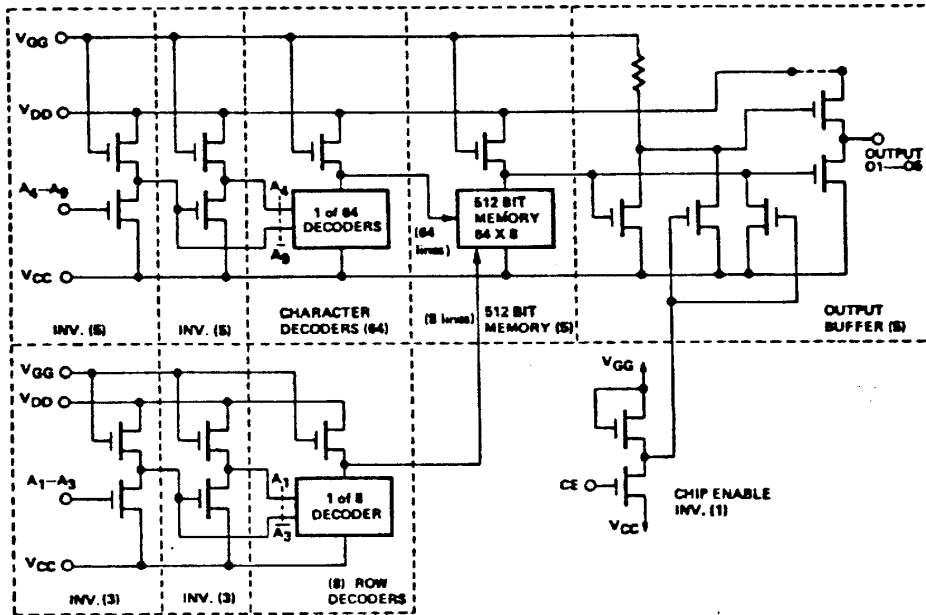
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### DTL/TTL INTERFACING



SIGNETICS 64 X 8 X 5 CHARACTER GENERATOR ■ 2513

DSS-SECTION



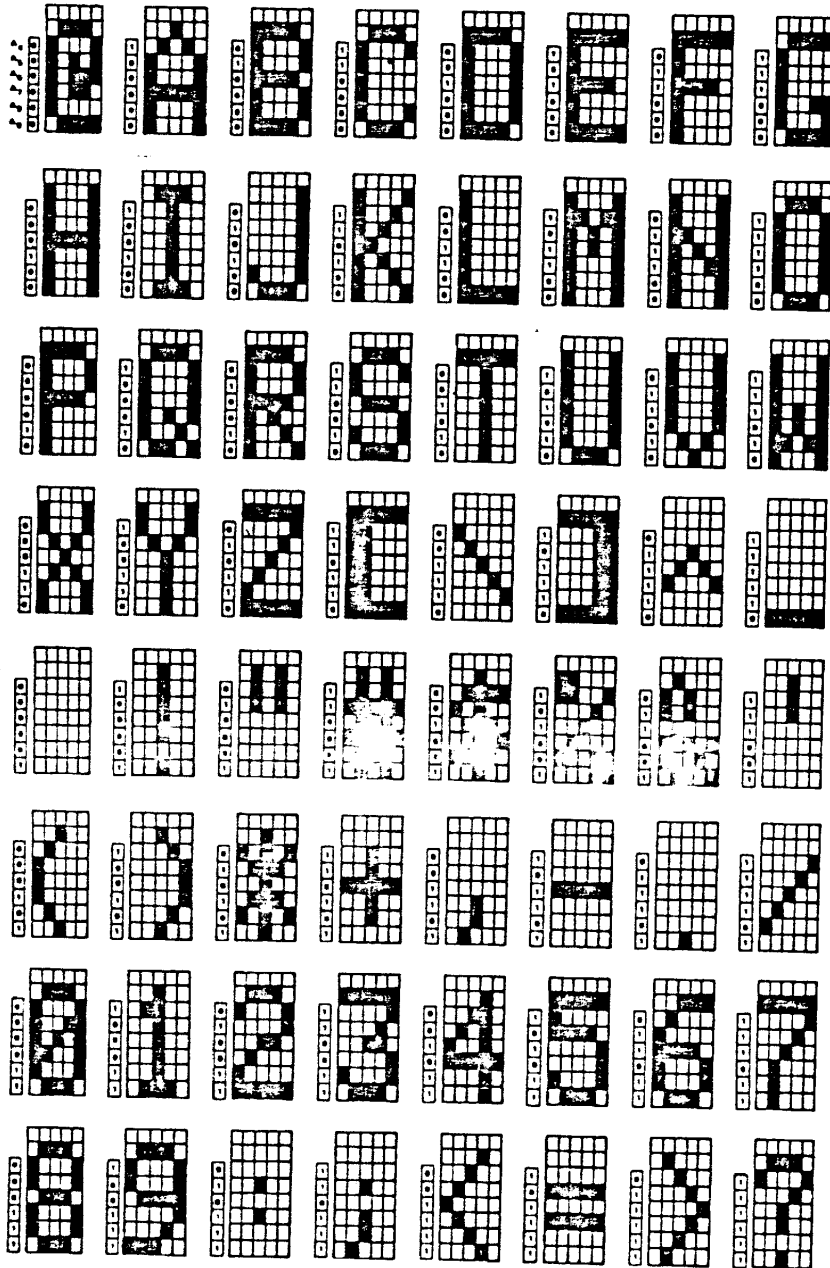
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VERSION

SIGNETICS 64 X 8 X 5 CHARACTER GENERATOR ■ 2513

ASCII CHARACTER FONT

2513N/CM2140

PRE-RELEASE  
VERSION





## 2316A/4316A/8316A\* 16K (2K x 8) ROM

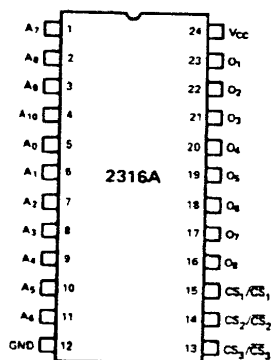
- Single +5 Volts Power Supply Voltage
  - Guaranteed 850ns Access Time
  - Directly TTL Compatible—All Inputs and Outputs
  - Three Programmable Chip Select Inputs for Easy Memory Expansion
- Three-State Output—OR-Tie Capability
  - Fully Decoded—On Chip Address Decode
  - Inputs Protected—All Inputs Have Protection Against Static Charge

The Intel 2316A is a 16,384 bit static MOS read only memory organized as 2048 words by 8 bits. This ROM is designed for memory applications where high performance, large bit storage, and simple interfacing are important design objectives. The inputs and outputs are fully TTL compatible. This device operates with a single +5V power supply. The three chip select inputs are programmable. Any combination of active high or low level chip select inputs can be defined by the designer and the desired chip select logic level is fixed during the masking process. These three programmable chip select inputs, as well as OR-tie compatibility on the outputs, facilitates easy memory expansion.

The 2316A read only memory is fabricated with N-channel silicon gate technology. This technology provides the designer with high performance, easy-to-use MOS circuits. Only a single +5V power supply is needed and all devices are directly TTL compatible.

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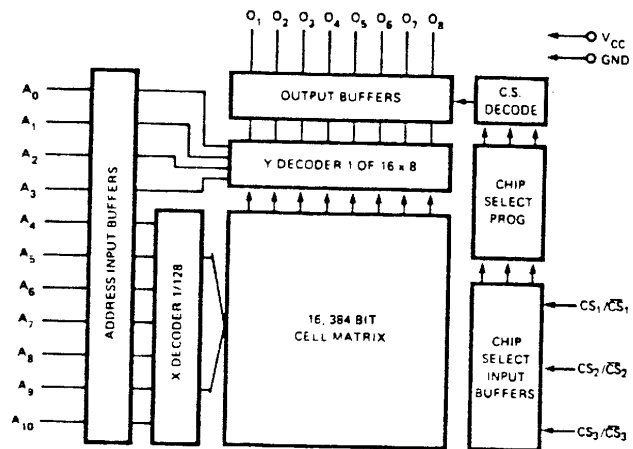
PIN CONFIGURATION



PIN NAMES

$A_0$ - $A_{10}$	ADDRESS INPUTS
$O_1$ - $O_8$	DATA OUTPUTS
$CS_1$ - $CS_3$	PROGRAMMABLE CHIP SELECT INPUTS

BLOCK DIAGRAM



\*All 4316A and 8316A specifications are identical to the 2316A specifications.

## 2316A

### A.C. Characteristics $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$ . $V_{CC} = +5\text{V} \pm 5\%$ unless otherwise specified

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN.	TYP. <sup>(1)</sup>	MAX.	
$t_A$	Address to Output Delay Time		400	850	nS
$t_{CO}$	Chip Select to Output Enable Delay Time			300	nS
$t_{DF}$	Chip Deselect to Output Data Float Delay Time	0		300	nS

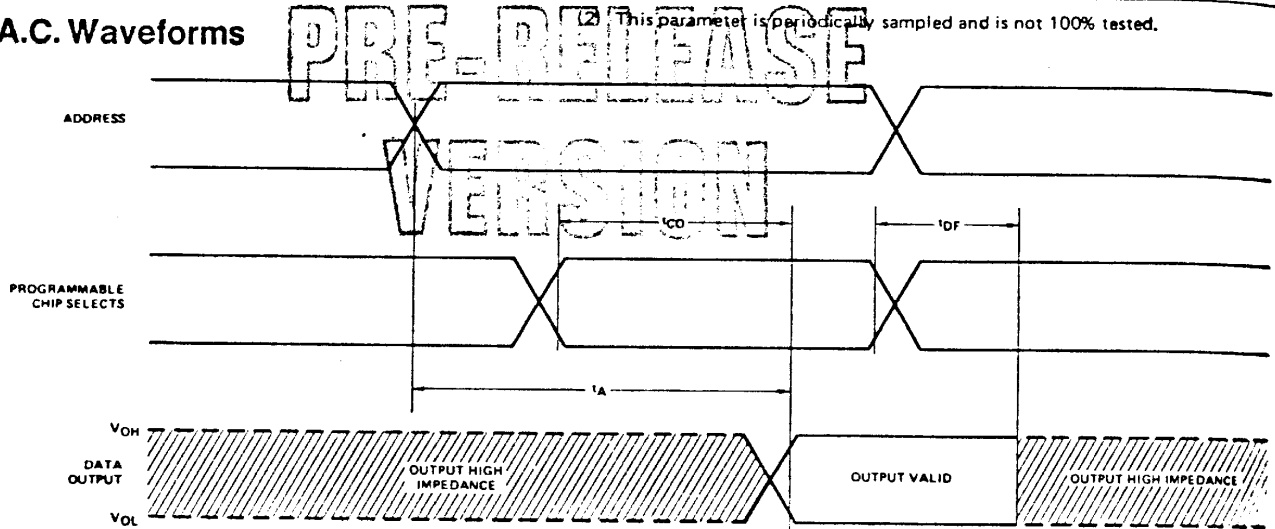
#### CONDITIONS OF TEST FOR A.C. CHARACTERISTICS

Output Load . . . 1 TTL Gate, and  $C_{LOAD} = 100\text{ pF}$   
 Input Pulse Levels . . . . . 0.8 to 2.0V  
 Input Pulse Rise and Fall Times . (10% to 90%) 20 nS  
 Timing Measurement Reference Level  
 Input . . . . . 1.5V  
 Output . . . . . 0.45V to 2.2V

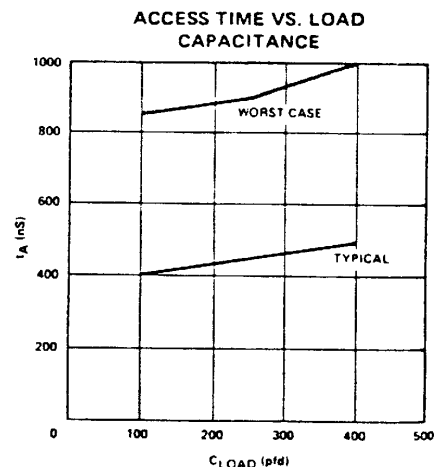
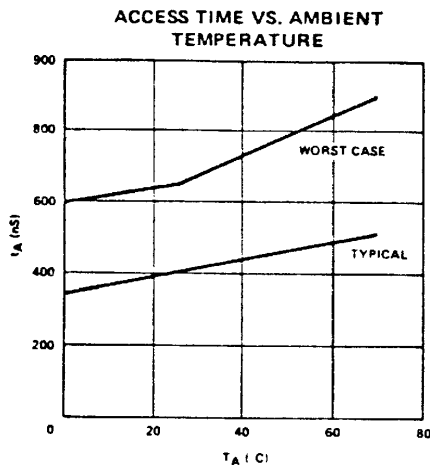
#### CAPACITANCE<sup>(2)</sup> $T_A = 25^\circ\text{C}$ , $f = 1\text{ MHz}$

SYMBOL	TEST	LIMITS	
		TYP.	MAX.
$C_{IN}$	All Pins Except Pin Under Test Tied to AC Ground	4 pF	10 pF
$C_{OUT}$	All Pins Except Pin Under Test Tied to AC Ground	8 pF	15 pF

### A.C. Waveforms



### Typical A.C. Characteristics



2316A

**ABSOLUTE MAXIMUM RATINGS\***

Ambient Temperature Under Bias	-10°C to 80°C
Storage Temperature	-65°C to +150°C
Voltage On Any Pin With Respect To Ground	-0.5V to +7V
Power Dissipation	1.0 Watt

\*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

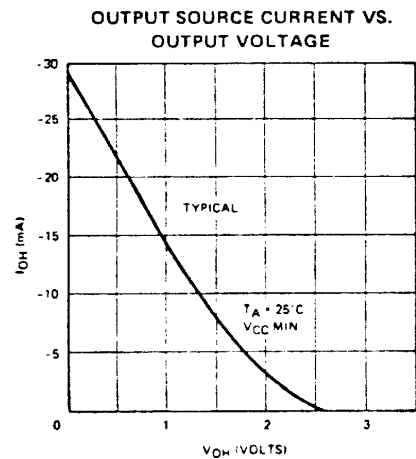
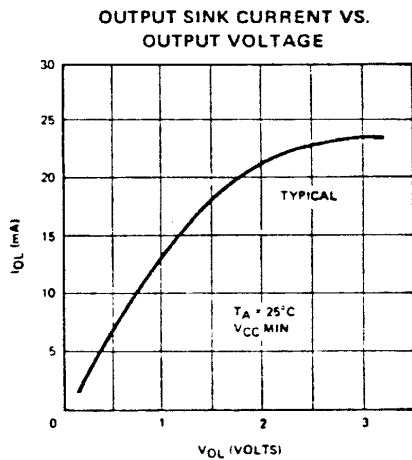
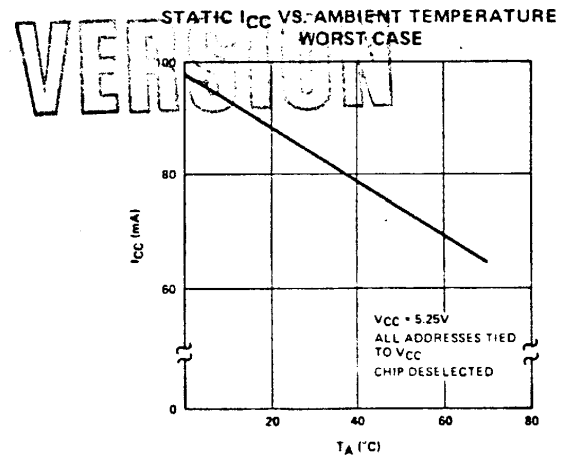
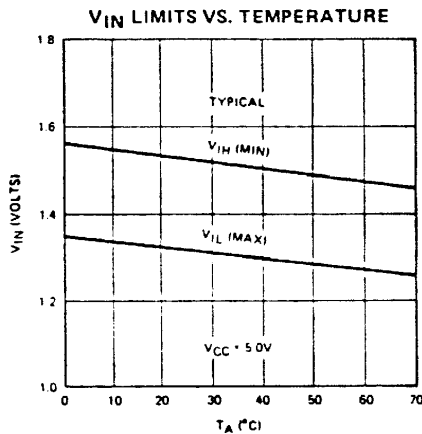
**D.C. AND OPERATING CHARACTERISTICS**  $T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ ,  $V_{CC} = 5\text{V} \pm 5\%$  unless otherwise specified

SYMBOL	PARAMETER	LIMITS			UNIT	TEST CONDITIONS
		MIN.	TYP. (1)	MAX.		
$I_{LI}$	Input Load Current (All Input Pins)		1	10	$\mu\text{A}$	$V_{IN} = 0$ to $5.25\text{V}$
$I_{LOH}$	Output Leakage Current			10	$\mu\text{A}$	$V_{OUT} = 4.0\text{V}$
$I_{LOL}$	Output Leakage Current			-20	$\mu\text{A}$	$V_{OUT} = 0.45\text{V}$
$I_{CC}$	Power Supply Current		40	98	$\text{mA}$	All inputs $5.25\text{V}$ Data Out Open
$V_{IL}$	Input "Low" Voltage	-0.5		0.8	$\text{V}$	
$V_{IH}$	Input "High" Voltage	2.0		$V_{CC} + 1.0\text{V}$	$\text{V}$	
$V_{OL}$	Output "Low" Voltage			0.45	$\text{V}$	$I_{OL} = 2.0\text{mA}$
$V_{OH}$	Output "High" Voltage	2.2			$\text{V}$	$I_{OH} = 100\mu\text{A}$

(1) Typical values for  $T_A = 25^\circ\text{C}$  and nominal supply voltage.

PRE-RELEASE  
VERSION

**TYPICAL D.C. CHARACTERISTICS**



REV.	ZONE	ECO #	REVISION	APPD
A		655	INITIAL RELEASE	<i>[Signature]</i>

**PRE-RELEASE  
VERSION**

**ENGINEERING RELEASE**  
 This revision supersedes all previous versions.  
 Please destroy all old copies.  
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**ENGINEERING SPECIFICATION**


P/N 333-0001

DESCRIPTION: IC, Ram 16,384 X 1, 4116 type.

Part is to have a 200nS, or less access time (trac).

Specification Sheet of a typical RAM is to be filed under  
 Apple P/N 333-0001.

DRAWING NUMBER  
333-0001-A  
SH 1 OF 13

<b>TOLERANCES</b> UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES.  DECIMALS .X ± _____ .XX ± _____ .XXX ± _____ ANGLES XX.X ± _____ FRACTIONS ± _____ DIMENSIONS IN PARENTHESIS ARE IN MILLIMETERS.	DRAWN BY C. Brown	DATE 3-25-81	 <b>apple computer inc.</b>	
	CHECKED BY <i>P. Brown</i>	DATE 3/3/81		TITLE IC, Ram, 16K, 200NS, W0/Logo, W0/burn-in
	APPROVED BY <i>P. Brown</i>	DATE 4/1/81		
	MATERIAL:	RELEASED BY <i>[Signature]</i>		DATE 4/15/81
NEXT ASSY.	FINISH:	SCALE:	SHEET 1 OF 13	

**PRE-RELEASE**  
**VERSION**  
**MOSTEK**  
 16,384 X 1-BIT DYNAMIC RAM  
**MK4116(P/N)-2/3**

**FEATURES**

- Recognized industry standard 16-pin configuration from MOSTEK
- 150ns access time, 375ns cycle (MK 4116-2)  
200ns access time, 375ns cycle (MK 4116-3)
- ± 10% tolerance on all power supplies (+12V, ±5V)
- Low power: 462mW active, 20mW standby (max)
- Output data controlled by  $\overline{\text{CAS}}$  and unlatched at end of cycle to allow two dimensional chip selection and extended page boundary
- Common I/O capability using "early write" operation
- Read-Modify-Write,  $\overline{\text{RAS}}$ -only refresh, and Page-mode capability
- All inputs TTL compatible, low capacitance, and protected against static charge
- 128 refresh cycles
- ECL compatible on VBB power supply (-5.7V)

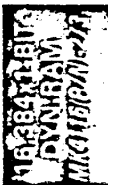
**DESCRIPTION**

The MK 4116 is a new generation MOS dynamic random access memory circuit organized as 16,384 words by 1 bit. As a state-of-the-art MOS memory device, the MK 4116 (16K RAM) incorporates advanced circuit techniques designed to provide wide operating margins, both internally and to the system user, while achieving performance levels in speed and power previously seen only in MOSTEK's high performance MK 4027 (4K RAM).

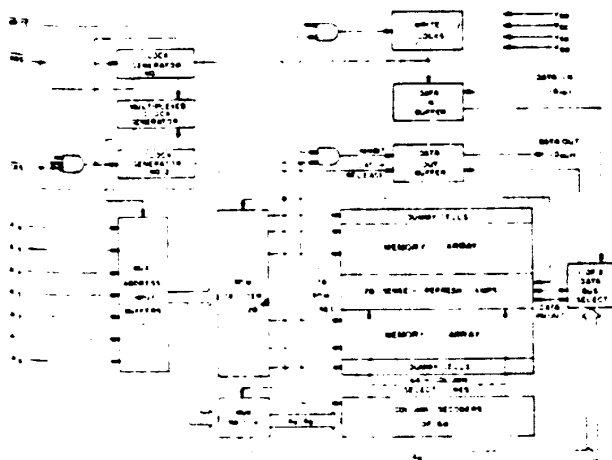
The technology used to fabricate the MK 4116 is MOSTEK's double-poly, N-channel silicon gate, POLY II  $\oplus$  process. This process, coupled with the use of a single transistor dynamic storage cell, provides the maximum possible circuit density and reliability, while maintaining high performance

capability. The use of dynamic circuitry throughout, including sense amplifiers, assures that power dissipation is minimized without any sacrifice in speed or operating margin. These factors combine to make the MK 4116 a truly superior RAM product.

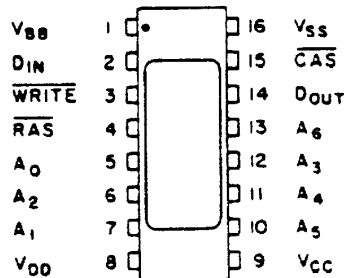
Multiplexed address inputs (a feature pioneered by MOSTEK for its 4K RAMS) permits the MK 4116 to be packaged in a standard 16-pin DIP. This recognized industry standard package configuration, while compatible with widely available automated testing and insertion equipment, provides highest possible system bit densities and simplifies system upgrade from 4K to 16K RAMs for new generation applications. Non-critical clock timing requirements allow use of the multiplexing technique while maintaining high performance.



**FUNCTIONAL DIAGRAM**



**PIN CONNECTIONS**



**PIN NAMES**

- A<sub>0</sub> A<sub>6</sub> ADDRESS INPUTS
- CAS COLUMN ADDRESS STROBE
- D<sub>IN</sub> DATA IN
- D<sub>OUT</sub> DATA OUT
- RAS ROW ADDRESS STROBE
- WRITE READ/WRITE INPUT
- V<sub>BB</sub> POWER (-5V)
- V<sub>CC</sub> POWER (+5V)
- V<sub>DD</sub> POWER (+12V)
- V<sub>SS</sub> GROUND

P/N 333-

**ABSOLUTE MAXIMUM RATINGS\***

Voltage on any pin relative to VBB ..... -0.5V to +20V  
 Voltage on VDD, VCC supplies relative to VSS ..... -1.0V to +15.0V  
 VBB-VSS (VDD-VSS > 0V) ..... 0V  
 Operating temperature, T<sub>A</sub> (Ambient) ..... 0°C to +70°C  
 Storage temperature (Ambient) Ceramic ..... -55°C to +150°C  
 Storage temperature, (Ambient) Plastic ..... -55°C to +125°C  
 Short circuit output current ..... 50mA  
 Power dissipation ..... 500mWatt

\*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

PRE-RELEASE VERSION

**RECOMMENDED DC OPERATING CONDITIONS**  
 (0°C ≤ T<sub>A</sub> ≤ 70°C)

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES	
Supply Voltage	VDD	10.5	12.0	Volts	2	
	VCC	4.5	5.0	Volts	2,3	
	VSS	0	0	Volts	2	
	VBB	-4.5	-5.0	Volts	2	
Input High (Logic 1) Voltage, RAS, CAS, WRITE	V <sub>IHC</sub>	2.4	-	7.0	Volts	2
Input High (Logic 1) Voltage, all inputs except RAS, CAS, WRITE	V <sub>IH</sub>	2.2	-	7.0	Volts	2
Input Low (Logic 0) Voltage, all inputs	V <sub>IL</sub>	-1.0	-	.8	Volts	2

**DC ELECTRICAL CHARACTERISTICS**  
 (0°C ≤ T<sub>A</sub> ≤ 70°C) (VDD = 12.0V ± 10%; VCC = 5.0V ± 10%; -5.7V ≤ VBB ≤ -4.5V; VSS = 0V)

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
OPERATING CURRENT Average power supply operating current (RAS, CAS cycling; t <sub>RC</sub> = t <sub>RC</sub> Min)	I <sub>DD1</sub>		35	mA	4
	I <sub>CC1</sub>		200	μA	5
	I <sub>BB1</sub>				
STANDBY CURRENT Power supply standby current (RAS = V <sub>IHC</sub> , DOUT = High Impedance)	I <sub>DD2</sub>	-10	1.5	mA	
	I <sub>CC2</sub>		10	μA	
	I <sub>BB2</sub>		100	μA	
REFRESH CURRENT Average power supply current, refresh mode (RAS cycling, CAS = V <sub>IHC</sub> ; t <sub>RC</sub> = t <sub>RC</sub> Min)	I <sub>DD3</sub>	-10	25	mA	4
	I <sub>CC3</sub>		10	μA	
	I <sub>BB3</sub>		200	μA	
PAGE MODE CURRENT Average power supply current, page-mode operation (RAS = V <sub>IL</sub> , CAS cycling; t <sub>PC</sub> = t <sub>PC</sub> Min)	I <sub>DD4</sub>		27	mA	4
	I <sub>CC4</sub>		200	μA	5
	I <sub>BB4</sub>				
INPUT LEAKAGE Input leakage current, any input (VBB = -5V, 0V ≤ V <sub>IN</sub> ≤ +7.0V, all other pins not under test = 0 volts)	I <sub>I(L)</sub>	-10	10	μA	
OUTPUT LEAKAGE Output leakage current (DOUT is disabled, 0V ≤ V <sub>OUT</sub> ≤ +5.5V)	I <sub>O(L)</sub>	-10	10	μA	
OUTPUT LEVELS Output high (Logic 1) voltage (I <sub>OUT</sub> = -5mA)	V <sub>OH</sub>	2.4		Volts	3
	V <sub>OL</sub>		0.4	Volts	

**NOTES:**

- T<sub>A</sub> is specified here for operation at frequencies to t<sub>RC</sub> > t<sub>RC</sub> (min). Operation at higher cycle rates with reduced ambient temperatures and higher power dissipation is permissible, however, provided AC operating parameters are met. See figure 1 for derating curve.
- All voltages referenced to VSS.
- Output voltage will swing from VSS to VCC when activated with no current loading. For purposes of maintaining data in standby mode, VCC may be reduced to VSS without affecting refresh operations or data retention. However, the V<sub>OH</sub> (min) specification is not guaranteed in this mode.
- I<sub>DD1</sub>, I<sub>DD3</sub>, and I<sub>DD4</sub> depend on cycle rate. See figures 2, 3, or 4 for I<sub>DD</sub> limits at other cycle rates.
- I<sub>CC1</sub> and I<sub>CC4</sub> depend upon output loading. During readout of high level data VCC is connected through a low impedance (135Ω typ) to data out. At all other times I<sub>CC</sub> consists of leakage currents only.

**ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (6,7,8)**  
 (0°C < TA < 70°C)<sup>1</sup> (VDD = 12.0V ± 10%; VCC = 5.0V ± 10%, VSS = 0V, VBB = -5.7V ≤ VBB ≤ -4.5V)

PARAMETER	SYMBOL	MK 4116-2		MK 4116-3		UNITS	NOTES
		MIN	MAX	MIN	MAX		
Random read or write cycle time	tRC	375		375		ns	9
Read-write cycle time	tRWC	375		375		ns	9
Read modify write cycle time	tRMW	320		405		ns	9
Page mode cycle time	tPC	170		225		ns	9, 10, 12
Access time from RAS	tRAC		150		200	ns	10, 12
Access time from CAS	tCAC		100		135	ns	11, 12
Output buffer turn-off delay	tOFF	0	40	0	50	ns	13
Transition time (rise and fall)	tT	3	35	3	50	ns	8
RAS precharge time	tRP	100		120		ns	
RAS pulse width	tRAS	150	10,000	200	10,000	ns	
RAS hold time	tRSH	100		135		ns	
CAS hold time	tCSH	150		200		ns	
CAS pulse width	tCAS	100	10,000	135	10,000	ns	
RAS to CAS delay time	tRCD	20	50	25	65	ns	14
RAS to RAS precharge time	tCRP	-20		-20		ns	
Row Address set-up time	tASR	0		0		ns	
Row Address hold time	tRAH	20		25		ns	
Column Address set-up time	tASC	-10		-10		ns	
Column Address hold time	tCAH	45		55		ns	
Column Address hold time referenced to RAS	tAR	95		120		ns	
Read command set-up time	tRCS	0		0		ns	
Read command hold time	tRCH	0		0		ns	
Write command hold time	tWCH	45		55		ns	
Write command hold time referenced to RAS	tWCR	95		120		ns	
Write command pulse width	tWP	45		55		ns	
Write command to RAS lead time	tRWL	50		70		ns	
Write command to CAS lead time	tCWL	50		70		ns	
Data-in set-up time	tDS	0		0		ns	15
Data-in hold time	tDH	45		55		ns	15
Data-in hold time referenced to RAS	tDHR	95		120		ns	
CAS precharge time (for page-mode cycle only)	tCP	60		80		ns	
Refresh period	tREF		2		2	ms	
WRITE command set-up time	tWCS	-20		-20		ns	16
CAS to WRITE delay	tCWD	60		80		ns	16
RAS to WRITE delay	tRWD	110		145		ns	16

**NOTES (Continued)**

- 6. Several cycles are required after power-up before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.
- 7. AC measurements assume t<sub>f</sub> = 5ns.
- 8. VIH (min) or VIL (min) and VIL (max) are reference levels for measuring timing of input signals. Also transition times are measured between VIH or VIL and VIL.
- 9. The specifications for tRC (min), tRMW (min) and tRWC (min) are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ TA ≤ 70°C) is assured.
- 10. Assumes that tRCD ≥ tRCD (Max). If tRCD is greater than the maximum recommended value shown in this table, tRAC will increase by the amount that tRCD exceeds the value shown.
- 11. Assumes that tRCD (max).
- 12. Measured with a load equivalent to 2 TTL loads and 10pF.
- 13. tOFF (max) defines the time at which the output reaches the open-circuit condition and is not referenced to output voltage levels.

- 14. Operation within the tRCD (max) limit insures that tRAC (max) can be met. tRCD (max) is specified as a reference point only if tRCD is greater than the specified tRCD (max) limit, then access time is controlled exclusively by tCAC.
- 15. These parameters are referenced to CAS leading edge in early write cycles and to WRITE leading edge in delayed write or read-modify-write cycles.
- 16. tWCS, tCWD and tRWD are restrictive operating parameters in read write and read modify write cycles only. If tWCS ≥ tWCS (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle. If tCWD ≥ tCWD (min) and tRWD ≥ tRWD (min), the cycle is a read-write cycle and the data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied the condition of the data out at access time is indeterminate.
- 17. Effective capacitance calculated from the equation C<sub>eff</sub> = I<sub>DD</sub> / V with V = 3 volts and power supplies at nominal levels.
- 18. CAS = VIH to disable DOUT.

MICROFILM  
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 UNIVERSITY MICROFILMS  
 SERIALS ACQUISITION  
 DEPARTMENT

RELEASE  
 VERSION

**AC ELECTRICAL CHARACTERISTICS**

(0°C ≤ T<sub>A</sub> ≤ 70°C) (V<sub>DD</sub> = 12.0V ± 10%; V<sub>SS</sub> = 0V; V<sub>BB</sub> = -5.7V ≤ V<sub>BB</sub> ≤ -4.5V)

PARAMETER	SYMBOL	TYP	MAX	UNITS	NOTES
Input Capacitance (A <sub>0</sub> -A <sub>6</sub> ), D <sub>IN</sub>	C <sub>11</sub>	4	5	pF	17
Input Capacitance $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ , $\overline{\text{WRITE}}$	C <sub>12</sub>	8	10	pF	17
Output Capacitance (D <sub>OUT</sub> )	C <sub>0</sub>	5	7	pF	17,18

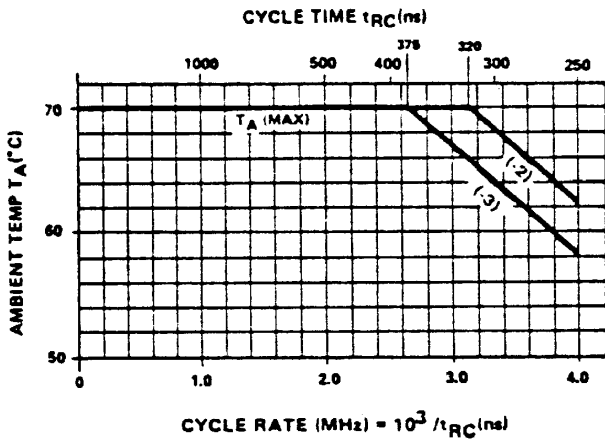


Fig. 1 Maximum ambient temperature versus cycle rate for extended frequency operation. T<sub>A</sub> (max) for operation at cycling rates greater than 2.66 MHz (t<sub>CYC</sub> < 375ns) is determined by T<sub>A</sub> (max) °C = 70 - 9.0 × (cycle rate MHz - 2.66) for -3. T<sub>A</sub> (max) °C = 70 - 9.0 × cycle rate MHz - 3.125MHz for -2 only.

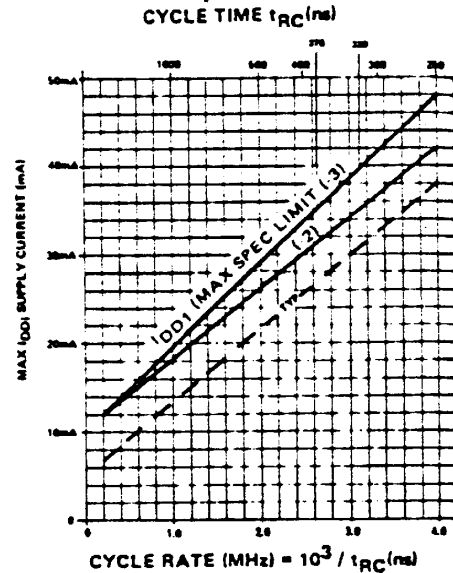


Fig. 2 Maximum I<sub>DD1</sub> versus cycle rate for device operation at extended frequencies. I<sub>DD1</sub> (max) curve is defined by the equation:

$$I_{DD1} \text{ (max) mA} = 10 + 9.4 \times \text{cycle rate [MHz]} \text{ for } -3$$

$$I_{DD1} \text{ (max) mA} = 10 + 8.0 \times \text{cycle rate [MHz]} \text{ for } -2$$

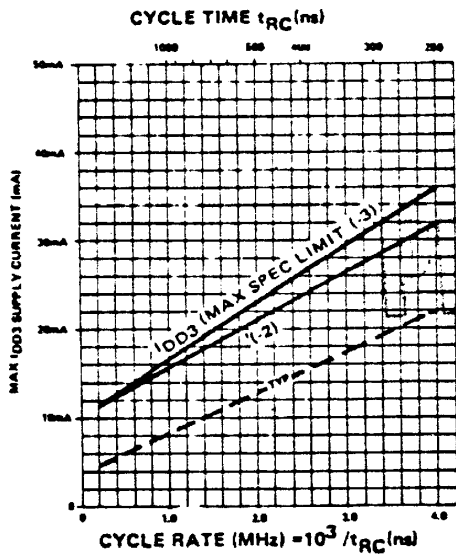


Fig. 3 Maximum I<sub>DD3</sub> versus cycle rate for device operation at extended frequencies. I<sub>DD3</sub> (max) curve is defined by the equation:

$$I_{DD3} \text{ (max) mA} = 10 + 6.5 \times \text{cycle rate [MHz]} \text{ for } -3$$

$$I_{DD3} \text{ (max) mA} = 10 + 5.5 \times \text{cycle rate [MHz]} \text{ for } -2$$

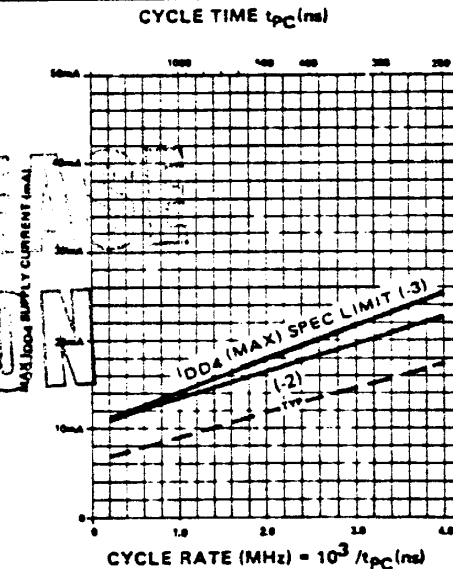


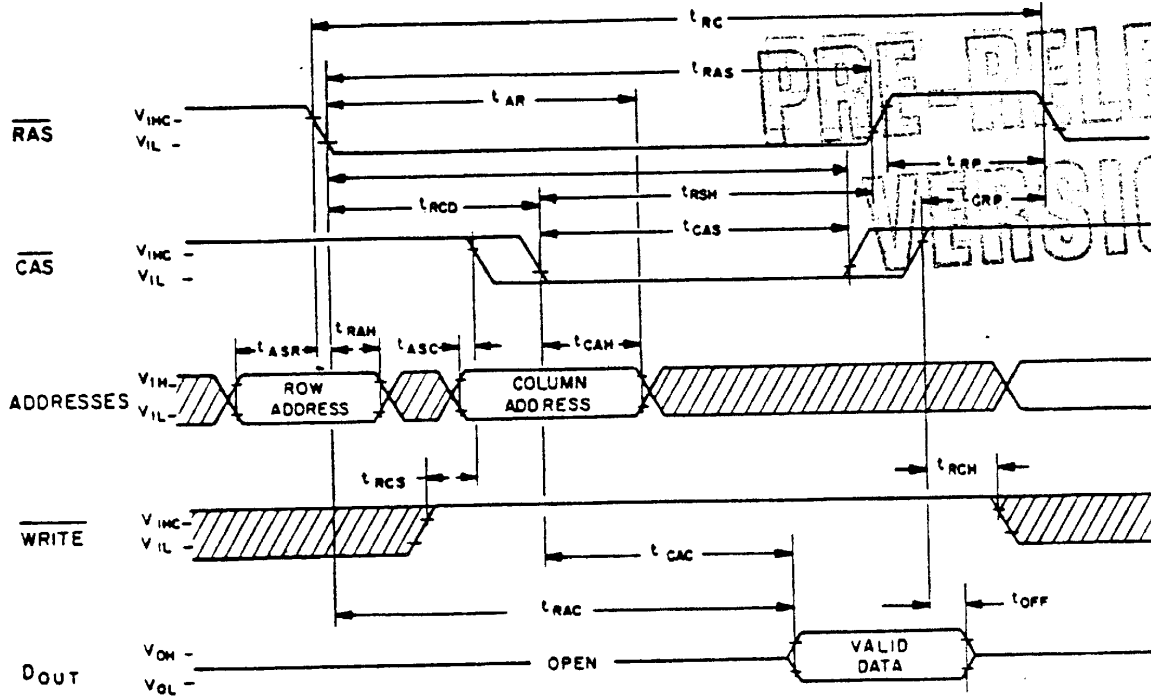
Fig. 4 Maximum I<sub>DD4</sub> versus cycle rate for device operation in page mode. I<sub>DD4</sub> (max) curve is defined by the equation:

$$I_{DD4} \text{ (max) mA} = 10 + 3.75 \times \text{cycle rate [MHz]} \text{ for } -3$$

$$I_{DD4} \text{ (max) mA} = 10 + 3.2 \times \text{cycle rate [MHz]} \text{ for } -2$$

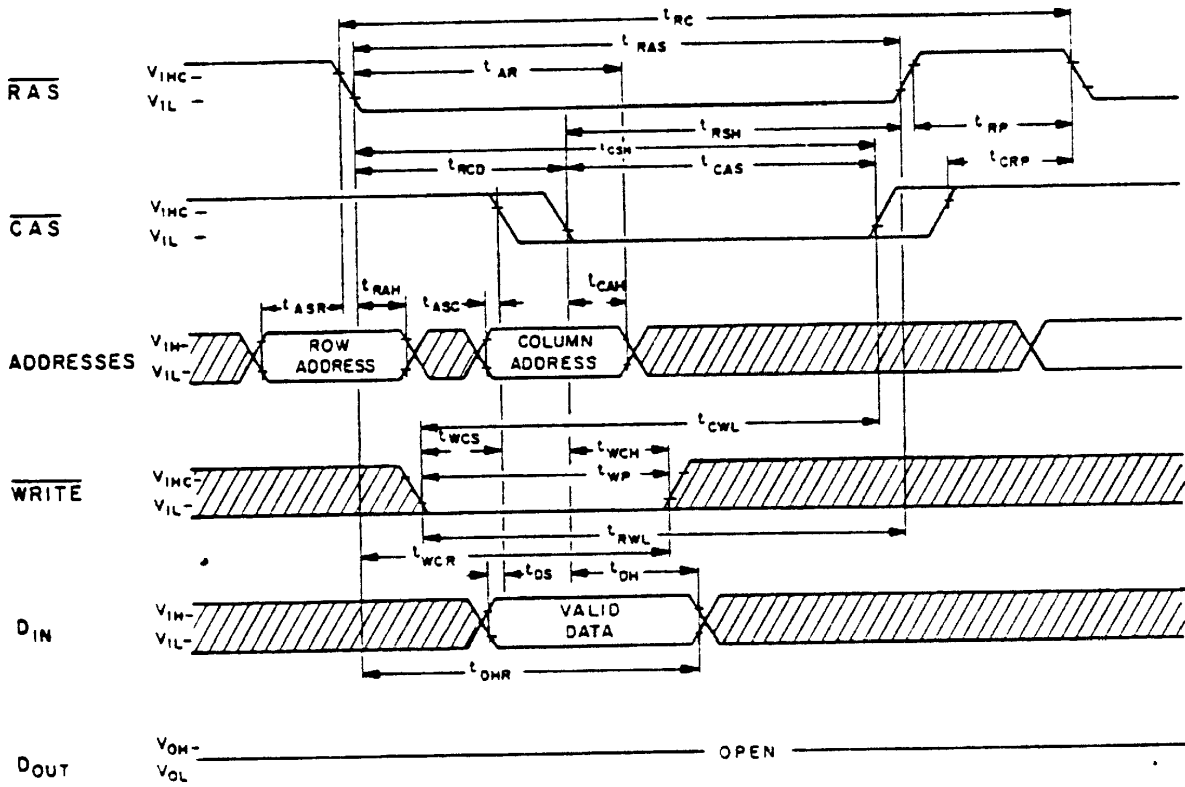
RE-RELEASED  
VERSION

READ CYCLE

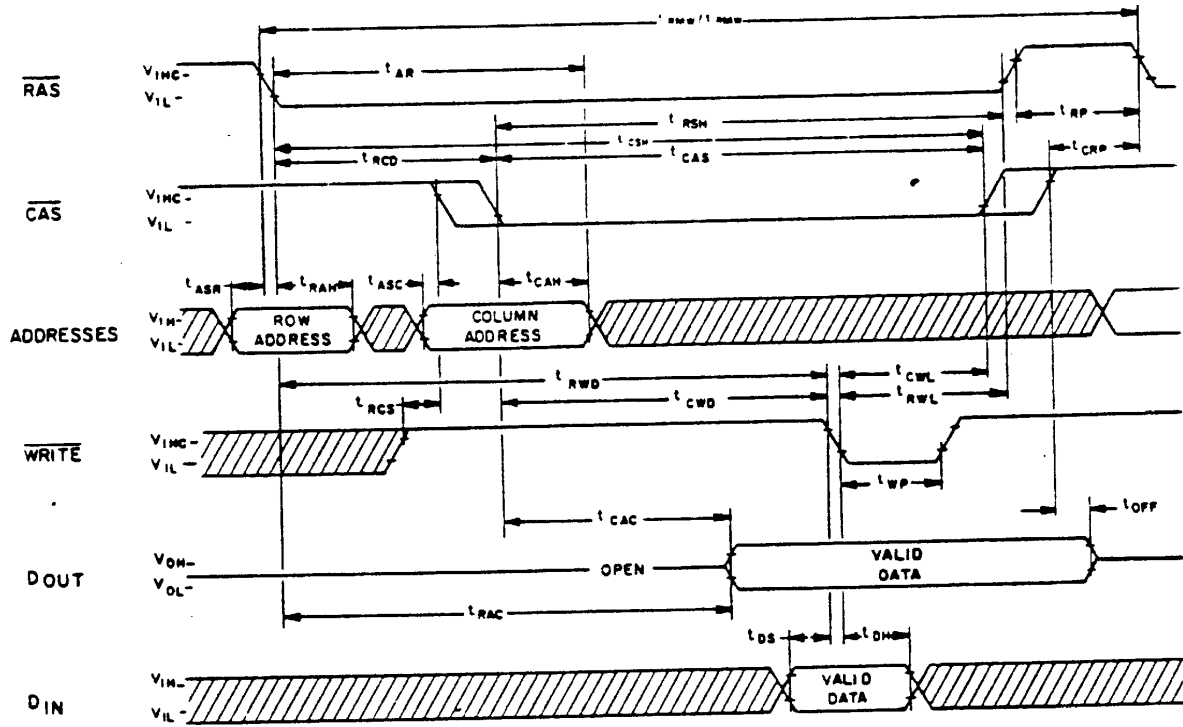


16 BIT DYNAMIC MEMORY

WRITE CYCLE (EARLY WRITE)

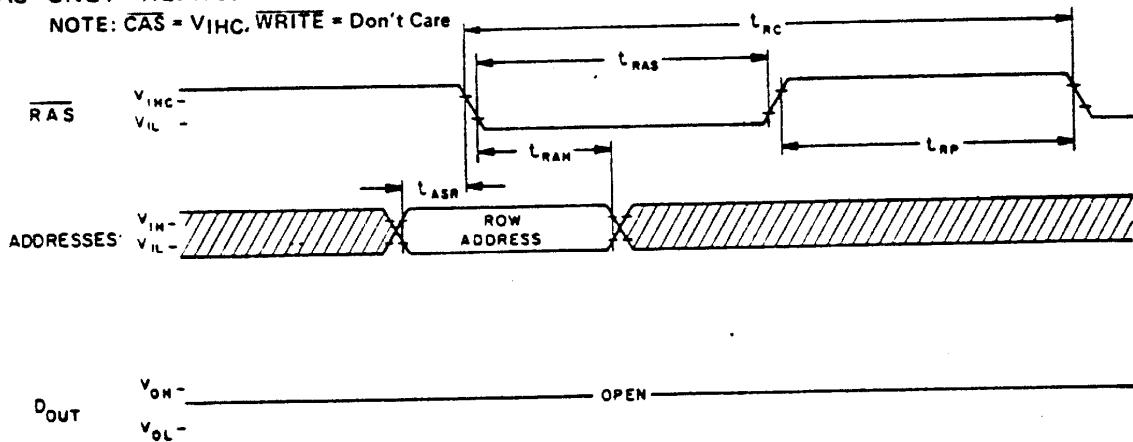


READ-WRITE/READ-MODIFY-WRITE CYCLE



"RAS-ONLY" REFRESH CYCLE

NOTE: CAS = VIH, WRITE = Don't Care



PRE-RELEASE  
VERSION



**DESCRIPTION (continued)**

System oriented features include  $\pm 10\%$  tolerance on all power supplies, direct interfacing capability with high performance logic families such as Schottky TTL, maximum input noise immunity to minimize "false triggering" of the inputs (a common cause of soft errors), on-chip address and data registers which eliminate the need for interface registers, and two chip select methods to allow the user to determine the appropriate speed/power characteristics of his memory system. The MK 4116 also incorporates several flexible timing/operating modes. In addition to the usual read, write, and read-modify-write cycles, the MK 4116 is capable of delayed write cycles, page-mode operation and RAS-only refresh. Proper control of the clock inputs (RAS, CAS and WRITE) allows common I/O capability, two dimensional chip selection, and extended page boundaries (when operating in page mode).

**ADDRESSING**

The 14 address bits required to decode 1 of the 16,384 cell locations within the MK 4116 are multiplexed onto the 7 address inputs and latched into the on-chip address latches by externally applying two negative going TTL-level clocks. The first clock, the Row Address Strobe (RAS), latches the 7 row address bits into the chip. The second clock, the Column Address Strobe (CAS), subsequently latches the 7 column address bits into the chip. Each of these signals, RAS and CAS, triggers a sequence of events which are controlled by different delayed internal clocks. The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical path timing sequence for read data access. The later events in the CAS clock sequence are inhibited until the occurrence of a delayed signal derived from the RAS clock chain. This "gated CAS" feature allows the CAS clock to be externally activated as soon as the Row Address Hold Time specification (TRAH) has been satisfied and the address inputs have been changed from Row address to Column address information.

Note that CAS can be activated at any time after TRAH and it will have no effect on the worst case data access time (tRAC) up to the point in time when the delayed row clock no longer inhibits the remaining sequence of column clocks. Two timing endpoints result from the internal gating of CAS which are called tRCD (min) and tRCD (max). No data storage or reading errors will result if CAS is applied to the MK 4116 at a point in time beyond the tRCD (max) limit. However, access time will then be determined exclusively by the access time from CAS (tCAC) rather than from RAS (tRAC), and access time from RAS will be lengthened by the amount that tRCD exceeds the tRCD (max) limit.

**DATA INPUT/OUTPUT**

Data to be written into a selected cell is latched into an on-chip register by a combination of WRITE and CAS while RAS is active. The later of the signals (WRITE or CAS) to make its negative transition is the strobe for the Data In (DIN) register. This permits several options in the write cycle timing. In a write cycle, if the WRITE input is brought low (active)

prior to CAS, the DIN is strobed by CAS, and the set-up and hold times are referenced to CAS. If the input data is not available at CAS time or if it is desired that the cycle be a read-write cycle, the WRITE signal will be delayed until after CAS has made its negative transition. In this "delayed write cycle" the data input set-up and hold times are referenced to the negative edge of WRITE rather than CAS. (To illustrate this feature, DIN is referenced to WRITE in the timing diagrams depicting the read-write and page-mode write cycles while the "early write" cycle diagram shows DIN referenced to CAS).

Data is retrieved from the memory in a read cycle by maintaining WRITE in the inactive or high state throughout the portion of the memory cycle in which CAS is active (low). Data read from the selected cell will be available at the output within the specified access time.

**DATA OUTPUT CONTROL**

The normal condition of the Data Output (DOUT) of the MK 4116 is the high impedance (open-circuit) state. That is to say, anytime CAS is at a high level, the DOUT pin will be floating. The only time the output will turn on and contain either a logic 0 or logic 1 is at access time during a read cycle. DOUT will remain valid from access time until CAS is taken back to the inactive (high level) condition.

If the memory cycle in progress is a read, read-modify write, or a delayed write cycle, then the data output will go from the high impedance state to the active condition, and at access time will contain the data read from the selected cell. This output data is the same polarity (not inverted) as the input data. Once having gone active, the output will remain valid until CAS is taken to the precharge (logic 1) state, whether or not RAS goes into precharge.

If the cycle in progress is an "early-write" cycle (WRITE active before CAS goes active), then the output pin will maintain the high impedance state throughout the entire cycle. Note that with this type of output configuration, the user is given full control of the DOUT pin simply by controlling the placement of WRITE command during a write cycle, and the pulse width of the Column Address Strobe during read operations. Note also that even though data is not latched at the output, data can remain valid from access time until the beginning of a subsequent cycle without paying any penalty in overall memory cycle time (stretching the cycle).

This type of output operation results in some very significant system implications.

**Common I/O Operation** — If all write operations are handled in the "early write" mode, then DIN can be connected directly to DOUT for a common I/O data bus.

**Data Output Control** — DOUT will remain valid during a read cycle from tCAC until CAS goes back to a high level (precharge), allowing data to be valid from one cycle up until a new memory cycle begins with no penalty in cycle time. This also makes the RAS/CAS clock timing relationship very flexible.

**Two Methods of Chip Selection** — Since DOUT

is not latched,  $\overline{CAS}$  is not required to turn off the outputs of unselected memory devices in a matrix. This means that both  $\overline{CAS}$  and/or  $\overline{RAS}$  can be decoded for chip selection. If both  $\overline{RAS}$  and  $\overline{CAS}$  are decoded, then a two dimensional (X,Y) chip select array can be realized.

**Extended Page Boundary** — Page-mode operation allows for successive memory cycles at multiple column locations of the same row address. By decoding  $\overline{CAS}$  as a page cycle select signal, the page boundary can be extended beyond the 128 column locations in a single chip. (See page-mode operation).

### OUTPUT INTERFACE CHARACTERISTICS

The three state data output buffer presents the data output pin with a low impedance to VCC for a logic 1 and a low impedance to VSS for a logic 0. The effective resistance to VCC (logic 1 state) is 420  $\Omega$  maximum and 135 $\Omega$  typically. The resistance to VSS (logic 0 state) is 95  $\Omega$  maximum and 35  $\Omega$  typically. The separate VCC pin allows the output buffer to be powered from the supply voltage of the logic to which the chip is interfaced. During battery standby operation, the VCC pin may have power removed without affecting the MK 4116 refresh operation. This allows all system logic except the  $\overline{RAS}$  timing circuitry and the refresh address logic to be turned off during battery standby to conserve power.

### PAGE MODE OPERATION

The "Page Mode" feature of the MK 4116 allows for successive memory operations at multiple column locations of the same row address with increased speed without an increase in power. This is done by strobing the row address into the chip and maintaining the  $\overline{RAS}$  signal at a logic 0 throughout all successive memory cycles in which the row address is common. This "page-mode" of operation will not dissipate the power associated with the negative going edge of  $\overline{RAS}$ . Also, the time required for strobing in a new row address is eliminated, thereby decreasing the access and cycle times.

The page boundary of a single MK 4116 is limited to the 128 column locations determined by all combinations of the 7 column address bits. However, in system applications which utilize more than 16,384 data words, (more than one 16K memory block), the page boundary can be extended by using  $\overline{CAS}$  rather than  $\overline{RAS}$  as the chip select signal.  $\overline{RAS}$  is applied to all devices to latch the row address into each device and then  $\overline{CAS}$  is decoded and serves as a page cycle select signal. Only those devices which receive both  $\overline{RAS}$  and  $\overline{CAS}$  signals will execute a read or write cycle.

### REFRESH

Refresh of the dynamic cell matrix is accomplished performing a memory cycle at each of the 128 addresses within each 2 millisecond time interval. Although any normal memory cycle will perform the refresh operation, this function is most easily accomplished with "RAS-only" cycles. RAS-only refresh results in a substantial reduction in operating power. This reduction in power is reflected in the IDD3 specification.

### POWER CONSIDERATIONS

Most of the circuitry used in the MK 4116 is dynamic and most of the power drawn is the result of an address strobe edge. Consequently, the dynamic power is primarily a function of operating frequency rather than active duty cycle (refer to the MK 4116 current waveforms in figure 5). This current characteristic of the MK 4116 precludes inadvertent burn out of the device in the event that the clock inputs become shorted to ground due to system malfunction.

Although no particular power supply noise restriction exists other than the supply voltages remain within the specified tolerance limits, adequate decoupling should be provided to suppress high frequency noise resulting from the transient current of the device. This insures optimum system performance and reliability. Bulk capacitance requirements are minimal since the MK 4116 draws very little steady state (DC) current.

In system applications requiring lower power dissipation, the operating frequency (cycle rate) of the MK 4116 can be reduced and the (guaranteed maximum) average power dissipation of the device will be lowered in accordance with the IDD1 (max) spec limit curve illustrated in figure 2. NOTE: The MK 4116 family is guaranteed to have a maximum IDD1 requirement of 35mA @ 375ns cycle (320ns cycle for the -2) with an ambient temperature range from 0° to 70°C. A lower operating frequency, for example 1 microsecond cycle, results in a reduced maximum IDD1 requirement of under 20mA with an ambient temperature range from 0° to 70°C.

It is possible the MK4116 family (-2 and 3 speed selections for example) at frequencies higher than specified, provided all AC operating parameters are met. Operation at shorter cycle times (<TRC min) results in higher power dissipation and, therefore, a reduction in ambient temperature is required. Refer to Figure 1 for derating curve.

NOTE: Additional power supply tolerance has been included on the VBB supply to allow direct interface capability with both -5V systems -5.2V ECL systems.

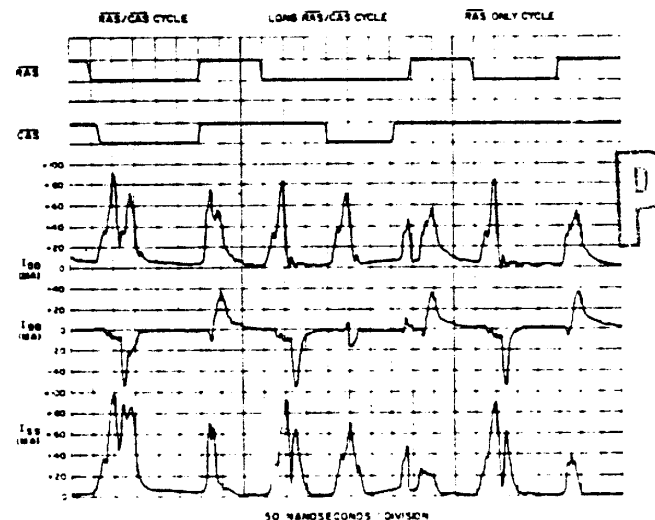


Fig. 5 Typical Current Waveforms

Although  $\overline{RAS}$  and/or  $\overline{CAS}$  can be decoded and used as a chip select signal for the MK 4116, overall system power is minimized if the Row Address Strobe ( $\overline{RAS}$ ) is used for this purpose. All unselected devices (those which do not receive a  $\overline{RAS}$ ) will remain in a low power (standby) mode regardless of the state of  $\overline{CAS}$ .

#### POWER UP

The MK 4116 requires no particular power supply sequencing so long as the Absolute Maximum Rating Conditions are observed. However, in order to insure compliance with the Absolute Maximum Ratings, MOSTEK recommends sequencing of power supplies

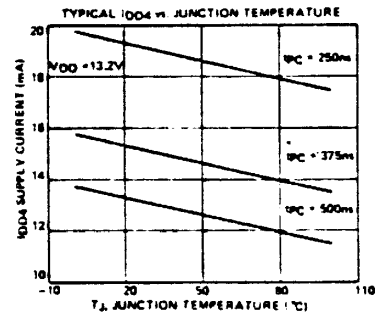
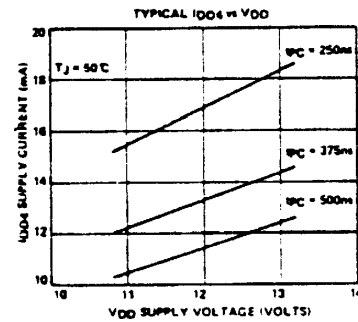
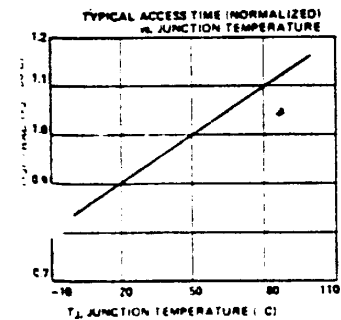
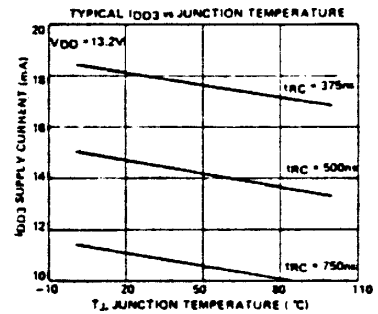
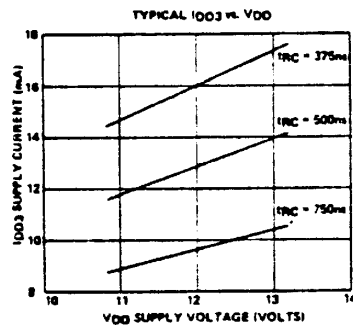
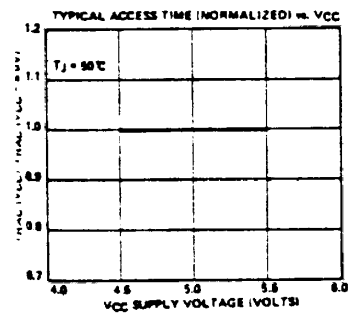
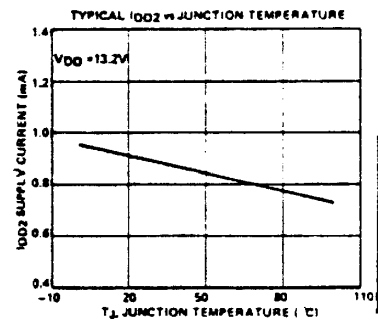
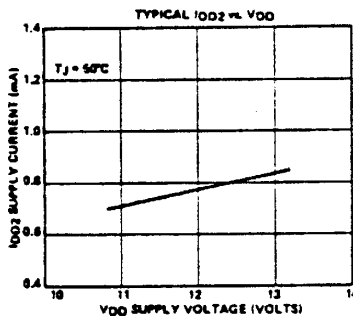
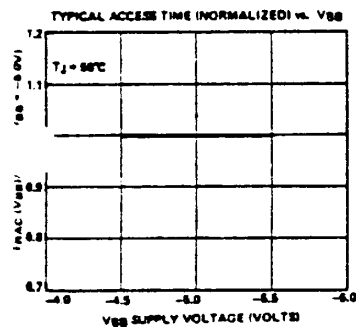
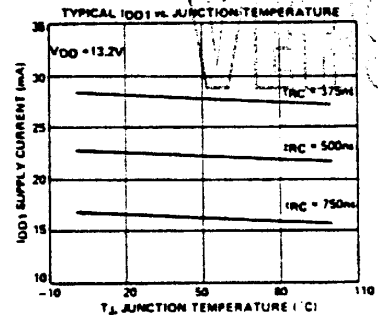
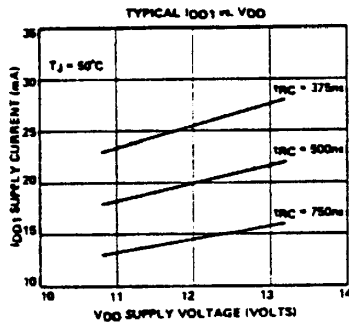
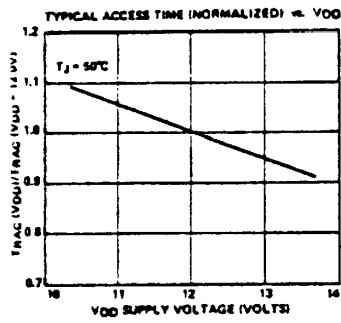
such that  $V_{BB}$  is applied first and removed last.  $V_{BB}$  should never be more positive than  $V_{SS}$  when power is applied to  $V_{DD}$ .

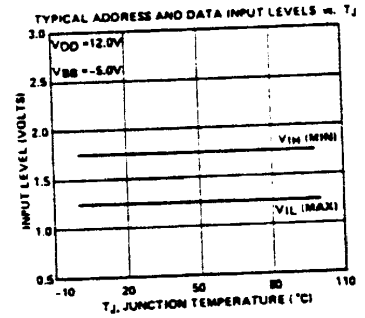
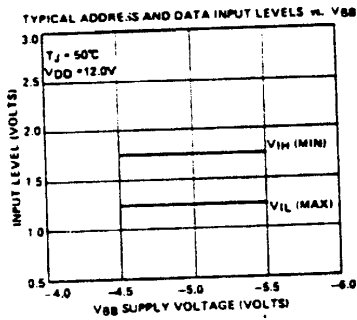
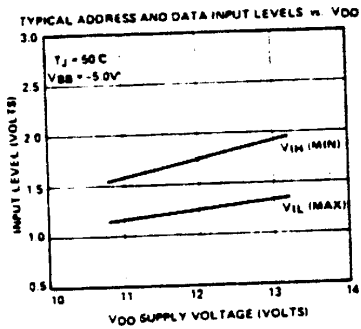
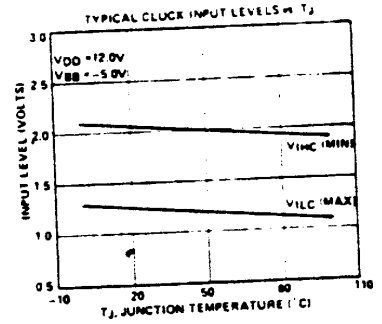
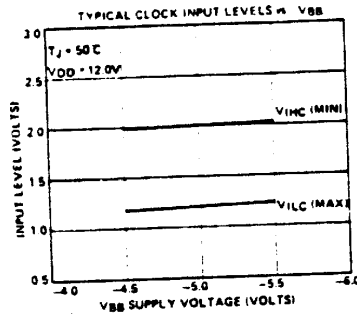
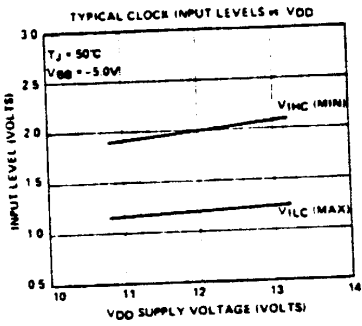
Under system failure conditions in which one or more supplies exceed the specified limits significant additional margin against catastrophic device failure may be achieved by forcing  $\overline{RAS}$  and  $\overline{CAS}$  to the inactive state (high level).

After power is applied to the device, the MK 4116 requires several cycles before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.

PRE-RELEASE  
VERSION

TYPICAL CHARACTERISTICS





PRE-RELEASE  
VERSION

REV.	ZONE	ECO #	REVISION	APPD
A		655	INITIAL RELEASE	<i>[Signature]</i>

**PRE-RELEASE  
VERSION**

OLD VERSIONS: ... CASE  
 This revision supersedes all previous versions.  
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 NOTICE OF PROPRIETARY PROPERTY: Inc.  
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**ENGINEERING SPECIFICATION**


P/N 333-0002

DESCRIPTION: IC, Ram 32,768 X 1, MK4332.

Part is to have a 200nS. or less access time (trac).

Specification Sheet of a MK4332 RAM is to be filed under Apple P/N 333-0002.

DRAWING NUMBER  
333-0002-A  
SH 1 OF 13

<b>TOLERANCES</b> UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES.  DECIMALS .X ± _____ .XX ± _____ .XXX ± _____ ANGLES XX.X ± _____ FRACTIONS ± _____ DIMENSIONS IN PARENTHESIS ARE IN MILLIMETERS.	DRAWN BY C. Brown	DATE 3-15-81	 <b>apple computer inc.</b>	
	CHECKED BY <i>P. Brown</i>	DATE 3/20/81		TITLE IC, Ram, 32K, 200NS, W0/Logo, W0/burn-in
	APPROVED BY <i>P. Quinn</i>	DATE 4/1/81		
	MATERIAL:	REDESIGNED BY <i>[Signature]</i>		DATE 4/1/81
NEXT ASSY.	FINISH:	SCALE:	SHEET 1 OF 13	

# PRELIMINARY ~~FINAL RELEASE~~ MOSTEK

PRELIMINARY

## 32,768 x 1-BIT DYNAMIC RAM MK4332(P)-3

### FEATURES

- Utilizes two industry standard MK 4116 devices in an 18-pin package configuration
- 200ns access time, 375ns cycle (MK 4116-3)
- Separate  $\overline{RAS}$ ,  $\overline{CAS}$  Clocks
- $\pm 10\%$  tolerance on all power supplies (+12V,  $\pm 5V$ )
- Low power: 482mW active, 40mW standby (max)
- Output data controlled by  $\overline{CAS}$  and unlatched at end of cycle to allow two dimensional chip selection and extended page boundary
- Common I/O capability using "early write" operation
- Read-Modify-Write,  $\overline{RAS}$ -only refresh, and Page-mode capability
- All inputs TTL compatible, low capacitance, and protected against static charge
- 128 refresh cycles for each MK 4116 device in the dual density configuration
- Pin compatible to MK 4116 and MK 4164

### DESCRIPTION

The MK 4332 is a new generation MOS dynamic random access memory circuit organized as 32,768 words by 1 bit. As a state-of-the-art MOS memory device, the MK4332 (32K RAM) incorporates advanced circuit techniques designed to provide wide operating margins, both internally and to the system user.

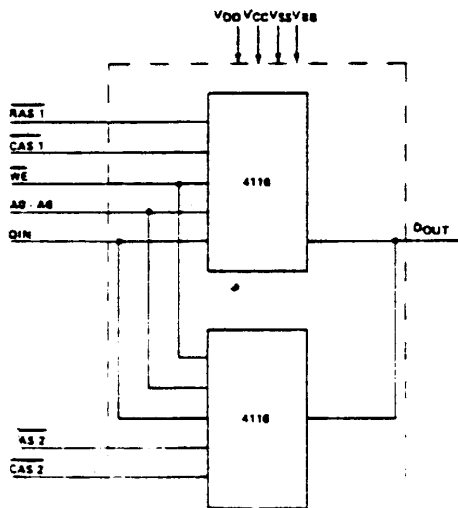
The technology used to fabricate the MK 4332 is MOSTEK's double-poly, N-channel silicon gate, POLY II  $\oplus$  process. This process, coupled with the use of a single transistor dynamic storage cell, provides the maximum possible circuit density and reliability, while maintaining high performance capability. The use of dynamic circuitry throughout, including sense amplifiers, assures that power

dissipation is minimized without any sacrifice in speed or operating margin. These factors combine to make the MK 4332 a truly superior RAM product.

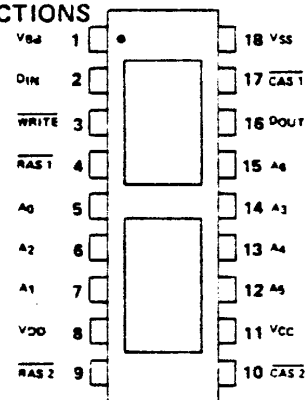
Multiplexed address inputs (a feature pioneered by MOSTEK for its 4K RAMs) permits the MK 4332 to be packaged in a standard 18-pin DIP. This standard package configuration, is compatible with widely available automated testing and insertion equipment, and it provides the highest possible system bit densities and simplifies system upgrade from 16K to 64K RAMs for new generation applications. Non-critical clock timing requirements allow use of the multiplexing technique while maintaining high performance.

32,768 x 1-BIT

### FUNCTIONAL DIAGRAM



### PIN CONNECTIONS



PIN NAMES

A0-A6	ADDRESS INPUTS
CAS	COLUMN ADDRESS STROBE
DIN	DATA IN
DOUT	DATA OUT
RAS	ROW ADDRESS STROBE
WRITE	EARLY WRITE INPUT
VSB	STANDBY POWER SUPPLY
VCC	POWER SUPPLY
VDD	POWER SUPPLY
VSS	GROUND

P/N

**ABSOLUTE MAXIMUM RATINGS\***

Voltage on any pin relative to V<sub>BB</sub> ..... -0.5V to +20V  
 Voltage on V<sub>DD</sub>, V<sub>CC</sub> supplies relative to V<sub>SS</sub> ..... -1.0V to +15.0V  
 V<sub>BB</sub>-V<sub>SS</sub> (V<sub>DD</sub>-V<sub>SS</sub>>0V) ..... 0V  
 Operating temperature, T<sub>A</sub> (Ambient) ..... 0°C to + 70°C  
 Storage temperature (Ambient) ..... -65°C to + 150°C  
 Short circuit output current ..... 50mA  
 Power dissipation ..... 1 Watt

\*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**RECOMMENDED DC OPERATING CONDITIONS<sup>6</sup>**  
 (0°C ≤ T<sub>A</sub> ≤ 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V <sub>DD</sub>	10.8	12.0	13.2	Volts	2
	V <sub>CC</sub>	4.5	5.0	5.5	Volts	2,3
	V <sub>SS</sub>	0	0	0	Volts	2
	V <sub>BB</sub>	-4.5	-5.0	-5.7	Volts	2
	Input High (Logic 1) Voltage, RAS, CAS, WRITE	V <sub>IHC</sub>	2.4	-	7.0	Volts
Input High (Logic 1) Voltage, all inputs except RAS, CAS, WRITE	V <sub>IH</sub>	2.2	-	7.0	Volts	2
Input Low (Logic 0) Voltage, all inputs	V <sub>IL</sub>	-1.0	-	.8	Volts	2

**DC ELECTRICAL CHARACTERISTICS**

(0°C ≤ T<sub>A</sub> ≤ 70°C) (V<sub>DD</sub> = 12.0V ± 10%; V<sub>CC</sub> = 5.0V ± 10%; -5.7V ≤ V<sub>BB</sub> ≤ -4.5V; V<sub>SS</sub> = 0V)

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
OPERATING CURRENT Average power supply operating current (RAS, CAS cycling; t <sub>RC</sub> = t <sub>RC</sub> Min)	I <sub>DD1</sub>		36.5	mA	4, 19
	I <sub>CC1</sub>		5	μA	5
	I <sub>BB1</sub>		300	μA	19
STANDBY CURRENT Power supply standby current (RAS = V <sub>IHC</sub> , DOUT = High Impedance)	I <sub>DD2</sub>	-20	3.0	mA	
	I <sub>CC2</sub>		20	μA	
	I <sub>BB2</sub>		200	μA	
REFRESH CURRENT Average power supply current, refresh mode (RAS cycling, CAS = V <sub>IHC</sub> ; t <sub>RC</sub> = t <sub>RC</sub> Min)	I <sub>DD3</sub>	-20	26.5	mA	4, 19
	I <sub>CC3</sub>		20	μA	
	I <sub>BB3</sub>		300	μA	19
PAGE MODE CURRENT Average power supply current, page-mode operation (RAS = V <sub>IL</sub> , CAS cycling; t <sub>PC</sub> = t <sub>PC</sub> Min)	I <sub>DD4</sub>		28.5	mA	4, 19
	I <sub>CC4</sub>		5	μA	5
	I <sub>BB4</sub>		300	μA	19
INPUT LEAKAGE Input leakage current, any input (V <sub>BB</sub> = -5V, 0V ≤ V <sub>IN</sub> ≤ +7.0V, all other pins not under test = 0 volts)	I <sub>I(L)</sub>	-20	20	μA	
	I <sub>O(L)</sub>	-20	20	μA	
OUTPUT LEAKAGE Output leakage current (DOUT is disabled, 0V ≤ V <sub>OUT</sub> ≤ +5.5V)	I <sub>O(L)</sub>	-20	20	μA	
OUTPUT LEVELS Output high (Logic 1) voltage (I <sub>OUT</sub> = -5mA)	V <sub>OH</sub>	2.4		Volts	3
	V <sub>OL</sub>		0.4	Volts	

**NOTES:**

- T<sub>A</sub> is specified here for operation at frequencies to t<sub>RC</sub> ≥ t<sub>RC</sub> (min). Operation at higher cycle rates with reduced ambient temperatures and higher power dissipation is permissible, however, provided AC operating parameters are met. See figure 1 for derating curve.
- All voltages referenced to V<sub>SS</sub>.
- Output voltage will swing from V<sub>SS</sub> to V<sub>CC</sub> when activated with no current loading. For purposes of maintaining data in standby mode, V<sub>CC</sub> may be reduced to V<sub>SS</sub> without affecting refresh operations or data retention. However, the V<sub>OH</sub> (min) specification is not guaranteed in this mode.
- I<sub>DD1</sub>, I<sub>DD3</sub>, and I<sub>DD4</sub> depend on cycle rate. See figures 2, 3, and 4 for I<sub>DD</sub> limits at other cycle rates.
- I<sub>CC1</sub> and I<sub>CC4</sub> depend upon output loading. During readout of high level data V<sub>CC</sub> is connected through a low impedance (135 Ω typ) to data out. At all other times I<sub>CC</sub> consists of leakage currents only.

PRE-REVIEW

**ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (6,7,8)**  
 (0°C < T<sub>A</sub> < 70°C)<sup>1</sup> (V<sub>DD</sub> = 12.0V ± 10%; V<sub>CC</sub> = 5.0V ± 10%, V<sub>SS</sub> = 0V, -5.7V < V<sub>BB</sub> < -4.5V)

PARAMETER	SYMBOL	MK 4332		UNITS	NOTES
		MIN	MAX		
Random read or write cycle time	t <sub>RC</sub>	375		ns	9
Read-write cycle time	t <sub>RWC</sub>	375		ns	9
Read modify write cycle time	t <sub>RMW</sub>	405		ns	9
Page mode cycle time	t <sub>PC</sub>	225		ns	9
Access time from RAS	t <sub>RAC</sub>		200	ns	10,12
Access time from CAS	t <sub>CAC</sub>		135	ns	11,12
Output buffer turn-off delay	t <sub>OFF</sub>	0	50	ns	13
Transition time (rise and fall)	t <sub>T</sub>	3	50	ns	8
RAS precharge time	t <sub>RP</sub>	120		ns	
RAS pulse width	t <sub>RAS</sub>	200	10,000	ns	
RAS hold time	t <sub>RSH</sub>	135		ns	
CAS hold time	t <sub>CSH</sub>	200		ns	
CAS pulse width	t <sub>CAS</sub>	135	10,000	ns	
RAS to CAS delay time	t <sub>RCD</sub>	25	65	ns	14
to RAS precharge time	t <sub>CRP</sub>	-20		ns	
Address set-up time	t <sub>ASR</sub>	0		ns	
Row Address hold time	t <sub>RAH</sub>	25		ns	
Column Address set-up time	t <sub>ASC</sub>	-10		ns	
Column Address hold time	t <sub>CAH</sub>	55		ns	
Column Address hold time referenced to RAS	t <sub>AR</sub>	120		ns	
Read command set-up time	t <sub>RCS</sub>	0		ns	
Read command hold time	t <sub>RCH</sub>	0		ns	
Write command hold time	t <sub>WCH</sub>	55		ns	
Write command hold time referenced to RAS	t <sub>WCR</sub>	120		ns	
Write command pulse width	t <sub>WP</sub>	55		ns	
Write command to RAS lead time	t <sub>RWL</sub>	70		ns	
Write command to CAS lead time	t <sub>CWL</sub>	70		ns	
Data-in set-up time	t <sub>DS</sub>	0		ns	15
Data-in hold time	t <sub>DH</sub>	55		ns	15
Data-in hold time referenced to RAS	t <sub>DHR</sub>	120		ns	
CAS precharge time (for page-mode cycle only)	t <sub>CP</sub>	80		ns	
Refresh period	t <sub>REF</sub>		2	ms	
WRITE command set-up time	t <sub>WCS</sub>	-20		ns	16
CAS to WRITE delay	t <sub>CWD</sub>	80		ns	16
RAS to WRITE delay	t <sub>RWD</sub>	145		ns	16

NOTES: Continued

- 6. Several cycles are required after power up before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.
- 7. AC measurements assume t<sub>p</sub> = 5ns.
- 8. V<sub>IHC</sub> (min) or V<sub>IH</sub> (min) and V<sub>IL</sub> (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V<sub>IHC</sub> or V<sub>IH</sub> and V<sub>IL</sub>.
- 9. The specifications for t<sub>RC</sub> (min), t<sub>RMW</sub> (min) and t<sub>RWC</sub> (min) are used only to indicate cycle time at which proper operation over the full temperature range (0°C < T<sub>A</sub> < 70°C) is assured.
- 10. Assumes that t<sub>RCD</sub> > t<sub>RCD</sub> (max). If t<sub>RCD</sub> is greater than the maximum recommended value shown in this table, t<sub>RAC</sub> will increase by the amount that t<sub>RCD</sub> exceeds the value shown.
- 11. Assumes that t<sub>RCD</sub> > t<sub>RCD</sub> (max).
- 12. Measured with a load equivalent to 2 TTL loads and 100pF.
- 13. t<sub>OFF</sub> (max) is the time it takes for the output to reach the output circuit condition and does not refer to the output buffer levels.
- 14. Operation within the t<sub>RCD</sub> (max) limit insures that t<sub>RAC</sub> (max) can be met. t<sub>RCD</sub> (max) is specified as a reference point only. If t<sub>RCD</sub> is greater than the specified t<sub>RCD</sub> (max) limit, then access time is controlled exclusively by t<sub>CAC</sub>.
- 15. These parameters are referenced to CAS leading edge in early write cycles and to WRITE leading edge in delayed write or read modify write cycles.
- 16. t<sub>WCS</sub>, t<sub>CWD</sub> and t<sub>RWD</sub> are restrictive operating parameters in read, write and read modify write cycles only. If t<sub>WCS</sub> > t<sub>WCS</sub> (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle. If t<sub>CWD</sub> > t<sub>CWD</sub> (min) and t<sub>RWD</sub> > t<sub>RWD</sub> (min), the cycle is a read-write cycle and the data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
- 17. Effective capacitance calculated from the equation C = I<sub>DD</sub> / V, with I<sub>DD</sub> = 3 volts and power supplies at nominal levels.
- 18. CAS = V<sub>IHC</sub> to tri-state Output.
- 19. One 16K RAM is active while the other is in standby mode.

**PRE-RELEASE**  
 32768A1-BU  
 DYNARAM

**AC ELECTRICAL CHARACTERISTICS**

(0°C ≤ T<sub>A</sub> ≤ 70°C) (V<sub>DD</sub> = 12.0V ± 10%; V<sub>SS</sub> = 0V; -5.7V ≤ V<sub>BB</sub> ≤ -4.5V)

PARAMETER	SYMBOL	TYP	MAX	UNITS	NOTES
Input Capacitance (A <sub>0</sub> -A <sub>6</sub> ), DIN	C <sub>I1</sub>	8	10	pF	17
Input Capacitance RAS, CAS	C <sub>I2</sub>	8	10	pF	17
Output Capacitance (DOUT)	C <sub>O</sub>	10	14	pF	17, 18
Input Capacitance WRITE	C <sub>I3</sub>	16	20	pF	17

**AC Characteristics and Timing Diagrams of MK4116-3.**

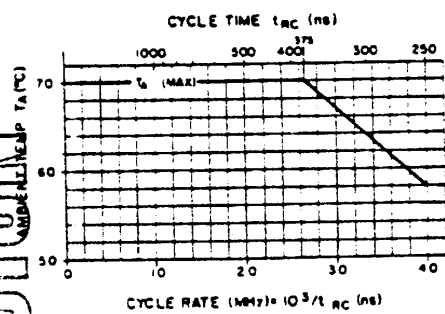


Fig. 1 Maximum ambient temperature versus cycle rate for extended frequency operation. T<sub>A</sub> (max) for operation at cycling rates greater than 2.66 MHz (t<sub>CYC</sub> < 375ns) is determined by T<sub>A</sub> (max) °C = 70 - 9.0 × (cycle rate MHz - 2.66) for -3.

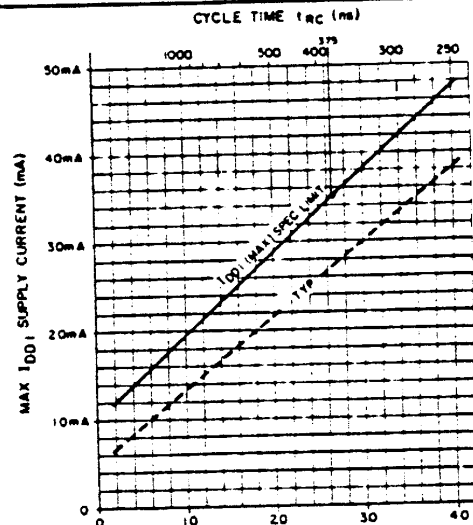


Fig. 2 Maximum I<sub>DD1</sub> versus cycle rate for device operation at extended frequencies. I<sub>DD1</sub> (max) curve is defined by the equation:

$$I_{DD1}(\text{max}) \text{ mA} = 10 + 9.4 \times \text{cycle rate (MHz)} \text{ for } -3$$

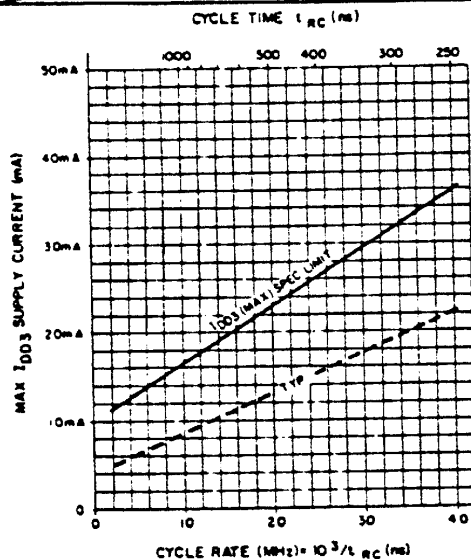


Fig. 3 Maximum I<sub>DD3</sub> versus cycle rate for device operation at extended frequencies. I<sub>DD3</sub> (max) curve is defined by the equation:

$$I_{DD3}(\text{max}) \text{ mA} = 10 + 6.5 \times \text{cycle rate (MHz)} \text{ for } -3$$

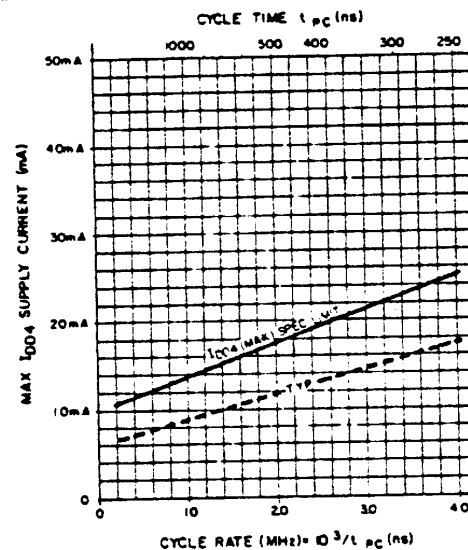


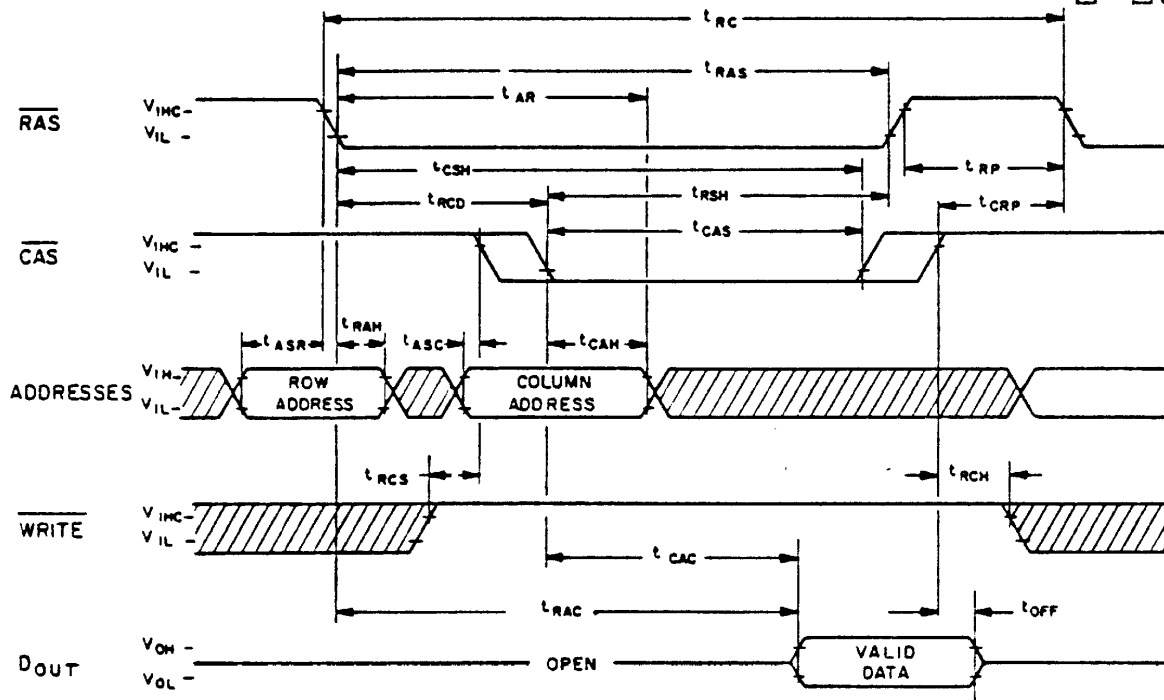
Fig. 4 Maximum I<sub>DD4</sub> versus cycle rate for device operation in page mode. I<sub>DD4</sub> (max) curve is defined by the equation:

$$I_{DD4}(\text{max}) \text{ mA} = 10 + 3.75 \times \text{cycle rate (MHz)} \text{ for } -3$$

PRE-RELEASE  
 REVISION

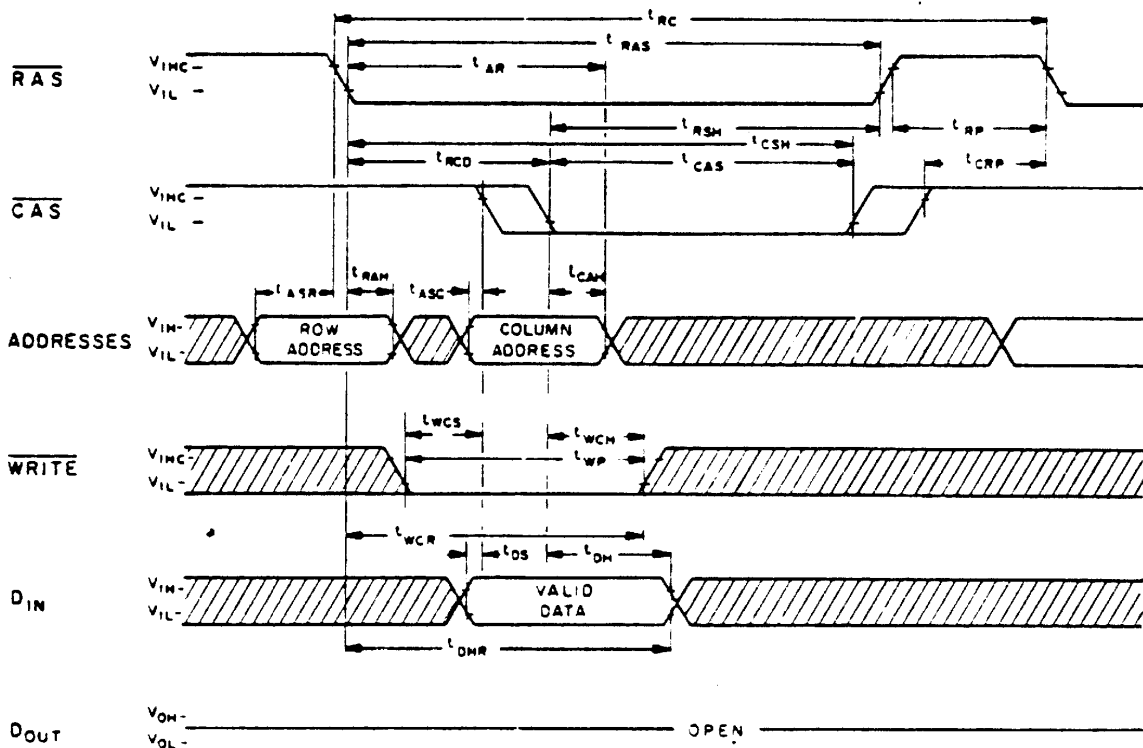
PRE-  
VI

READ CYCLE

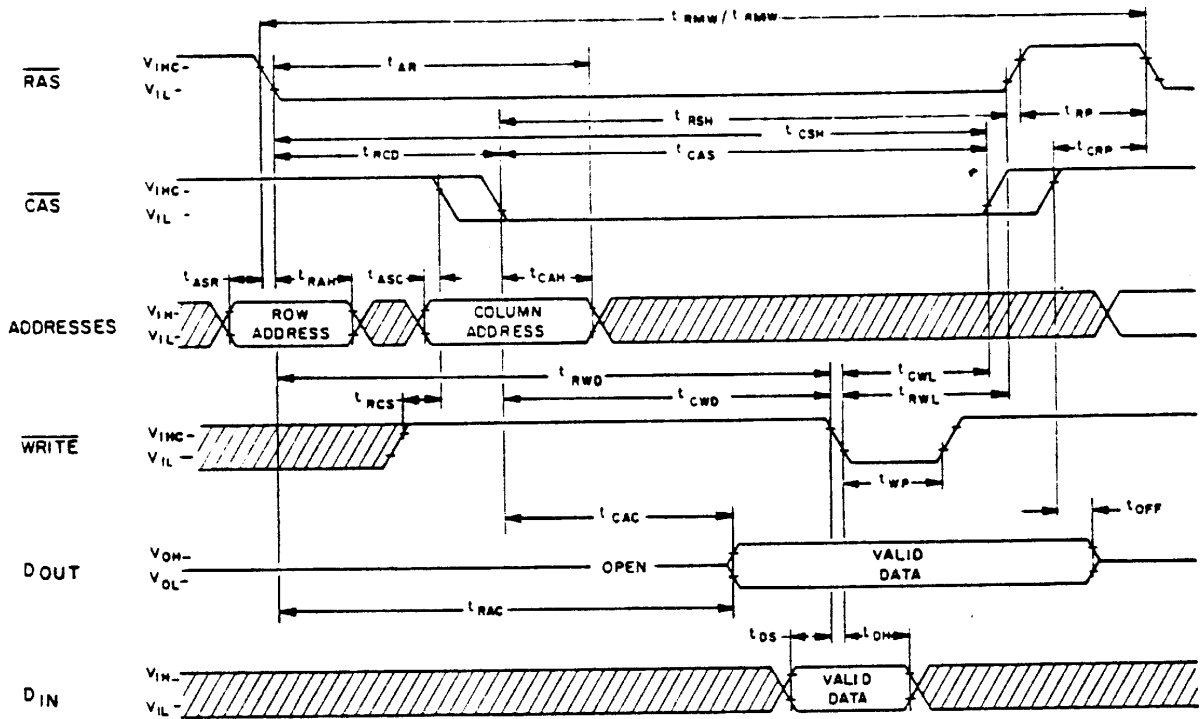


27B011A  
DYNABYTE

WRITE CYCLE (EARLY WRITE)

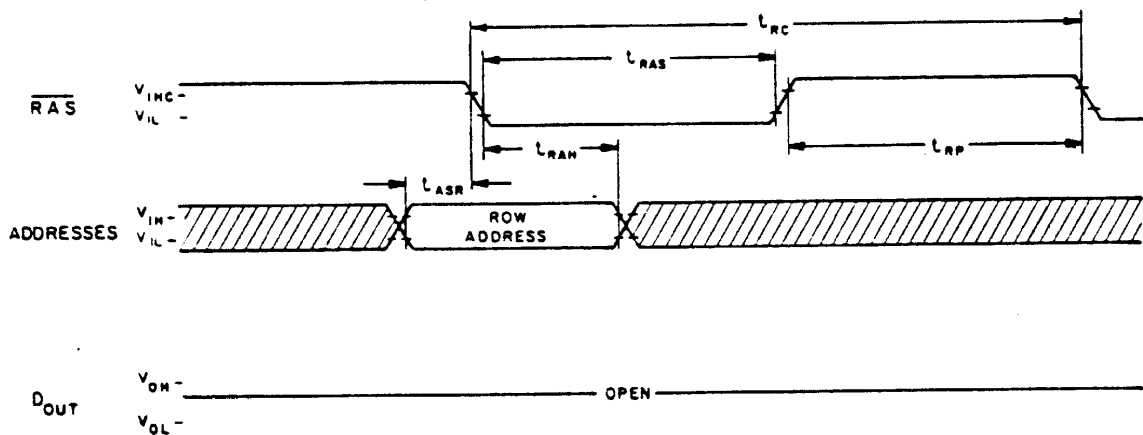


READ-WRITE/READ-MODIFY-WRITE CYCLE



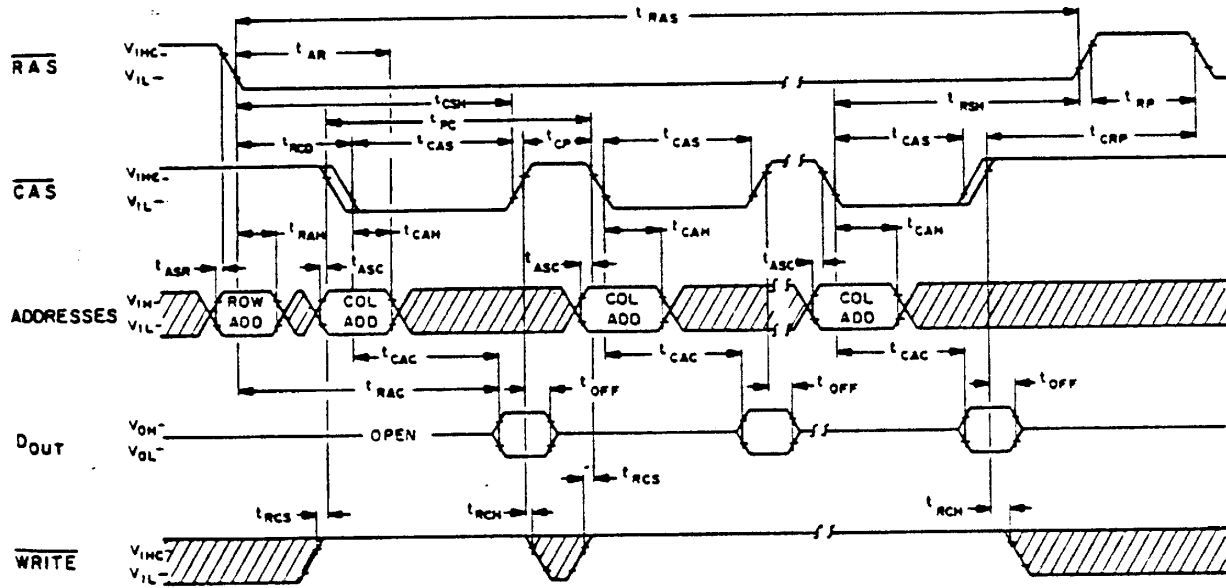
"RAS-ONLY" REFRESH CYCLE

NOTE:  $\overline{CAS} = V_{IH}$ ,  $\overline{WRITE} = \text{Don't Care}$

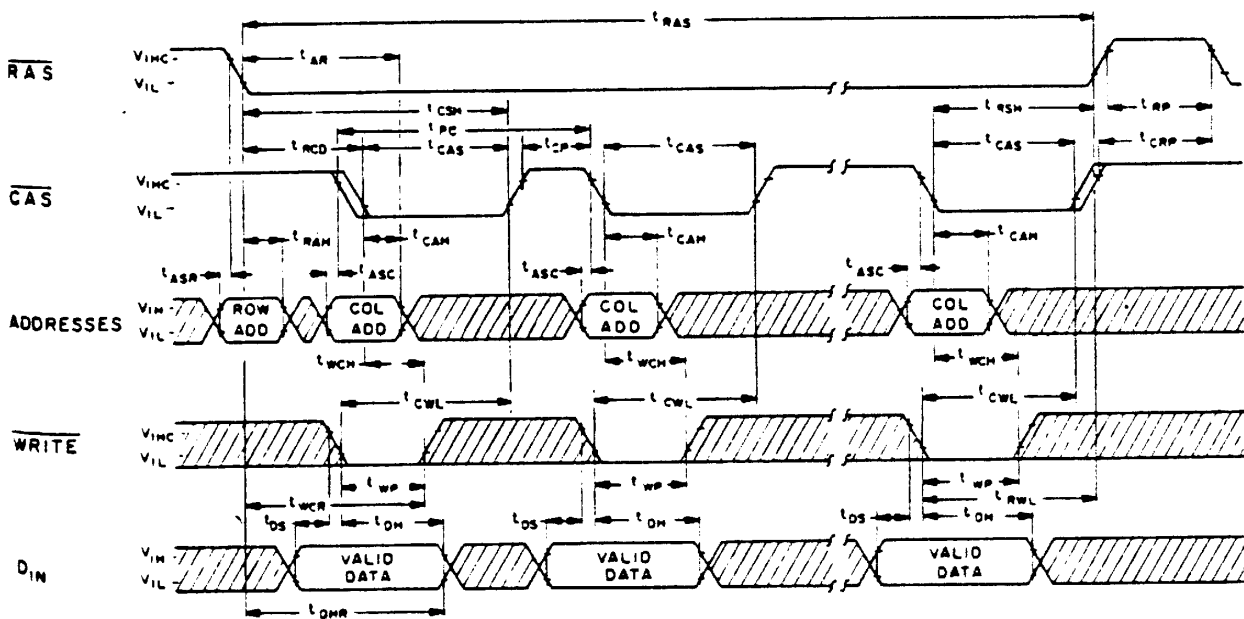


PRE-RELEASE  
VERSION

PAGE MODE READ CYCLE



PAGE MODE WRITE CYCLE



32768x16BIT  
DYN RAM  
17M55100A

PRE-RELEASE  
VERSION

DESCRIPTION (continued)

System features include  $\pm 10\%$  tolerance on all power supplies, direct interfacing capability with high performance logic families such as Schottky TTL, maximum input noise immunity to minimize "false triggering" of the inputs (a common cause of soft errors), on-chip address and data registers which eliminate the need for interface registers, and two chip select methods. The MK 4332 also incorporates several flexible timing/operating modes. In addition to the usual read, write, and read-modify-write cycles, the MK 4332 is capable of delayed write cycles, page-mode operation and RAS-only refresh. Proper control of the clock inputs (RAS, CAS and WRITE) allows common I/O capability, two dimensional chip selection, and extended page boundaries (when operating in page mode).

### ADDRESSING

User access of a unique memory location is accomplished by multiplexing 14 address bits onto 7 address inputs and by proper control of the RAS and CAS clocks in a manner identical to operation of the MK 4116 in a memory array board. The 14 address bits required to decode 1 of the 16,384 cell locations within each MK 4116 are multiplexed onto the 7 address inputs and latched into the on-chip address latches by externally applying two negative going TTL-level clocks. The first clock, the Row Address Strobe (RAS), latches the 7 row address bits into the chip. The second clock, the Column Address Strobe (CAS), subsequently latches the 7 column address bits into the chip. Each of these signals, RAS and CAS, triggers a sequence of events which are controlled by different delayed internal clocks. The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical path timing sequence for read data access. The later events in the CAS clock sequence are inhibited until the occurrence of a delayed signal derived from the RAS clock chain. This "gated CAS" feature allows the CAS clock to be externally activated as soon as the Row Address Hold Time specification ( $t_{RAH}$ ) has been satisfied and the address inputs have been changed from Row address to Column address information.

Note that CAS can be activated at any time after  $t_{RAH}$  and it will have no effect on the worst case data access time ( $t_{RAC}$ ) up to the point in time when the delayed row clock no longer inhibits the remaining sequence of column clocks. Two timing end-points result from the internal gating of CAS which are called  $t_{RCD}(\text{min})$  and  $t_{RCD}(\text{max})$ . No data storage or reading errors will result if CAS is applied to the MK 4332 at a point in time beyond the  $t_{RCD}(\text{max})$  limit. However, access time will then be determined exclusively by the access time from CAS ( $t_{CAC}$ ) rather than from RAS ( $t_{RAC}$ ), and access time from RAS will be lengthened by the amount that  $t_{RCD}$  exceeds the  $t_{RCD}(\text{max})$  limit.

### DATA INPUT/OUTPUT

Data to be written into a selected cell is latched into an on-chip register by a combination of WRITE and CAS while RAS is active. The later of the signals (WRITE or CAS) to make its negative transition is the strobe for the Data In (DIN) register. This permits

several options in the write cycle timing. In a write cycle, if the WRITE input is brought low (active) prior to CAS, the DIN is strobed by CAS, and the set-up and hold times are referenced to CAS. If the input data is not available at CAS time or if it is desired that the cycle be a read-write cycle, the WRITE signal will be delayed until after CAS has made its negative transition. In this "delayed write cycle" the data input set-up and hold times are referenced to the negative edge of WRITE rather than CAS. (To illustrate this feature, DIN is referenced to WRITE in the timing diagrams depicting the read-write and page-mode write cycles while the "early write" cycle diagram shows DIN referenced to CAS). Data is retrieved from the memory in a read cycle by maintaining WRITE in the inactive or high state throughout the portion of the memory cycle in which CAS is active (low). Data read from the selected cell will be available at the output within the specified access time.

### DATA OUTPUT CONTROL

The normal condition of the Data Output (DOUT) of the MK 4332 is the high impedance (open-circuit) state. That is to say, anytime CAS is at a high level, the DOUT pin will be floating. The only time the output will turn on and contain either a logic 0 or logic 1 is at access time during a read cycle. DOUT will remain valid from access time until CAS is taken back to the inactive (high level) condition.

Since the outputs to both 16K devices are tied together, care must be taken with the timing relationships of the two devices. Both devices cannot be activated at the same time as a data output conflict can occur.

If the memory cycle in progress is a read, read-modify write, or a delayed write cycle, then the data output will go from the high impedance state to the active condition, and at access time will contain the data read from the selected cell. This output data is the same polarity (not inverted) as the input data. Once having gone active, the output will remain valid until CAS is taken to the precharge (logic 1) state, whether or not RAS goes into precharge.

If the cycle in progress is an "early-write" cycle (WRITE active before CAS goes active), then the output pin will maintain the high impedance state throughout the entire cycle. Note that with this type of output configuration, the user is given full control of the DOUT pin simply by controlling the placement of WRITE command during a write cycle, and the pulse width of the Column Address Strobe during read operations. Note also that even though data is not latched at the output, data can remain valid from access time until the beginning of a subsequent cycle without paying any penalty in overall memory cycle time (stretching the cycle).

This type of output operation results in some very significant system implications.

**Common I/O Operation** - If all write operations are handled in the "early write" mode, then DIN can be connected directly to DOUT for a common I/O data bus.

**Data Output Control** - DOUT will remain valid during a read cycle from  $t_{CAC}$  until CAS goes back to a high level (precharge), allowing data to be valid from one cycle up until a new memory cycle begins

with no penalty in cycle time. This also makes the RAS/CAS clock timing relationship very flexible.

**Two Methods of Chip Selection** — Since DOUT is not latched, CAS is not required to turn off the outputs of unselected memory devices in a matrix. This means that both CAS and/or RAS can be decoded for chip selection. If both RAS and CAS are decoded, then a two dimensional (X,Y) chip select array can be realized.

**Extended Page Boundary** — Page-mode operation allows for successive memory cycles at multiple column locations of the same row address. By decoding CAS as a page cycle select signal, the page boundary can be extended beyond the 128 column locations in a single chip. (See page-mode operation).

### OUTPUT INTERFACE CHARACTERISTICS

The three state data output buffer presents the data output pin with a low impedance to VCC for a logic 1 and a low impedance to VSS for a logic 0. The effective resistance to VCC (logic 1 state) is 420 Ω maximum and 135Ω typically. The resistance to VSS (logic 0 state) is 95 Ω maximum and 35 Ω typically. The separate VCC pin allows the output buffer to be powered from the supply voltage of the logic to which the chip is interfaced. During battery standby operation, the VCC pin may have power removed without affecting the MK 4332 refresh operation. This allows all system logic except the RAS timing circuitry and the refresh address logic to be turned off during battery standby to conserve power.

### PAGE MODE OPERATION

The "Page Mode" feature of the MK 4332 allows for successive memory operations at multiple column locations of the same row address with increased speed without an increase in power. This is done by strobing the row address into the chip and maintaining the RAS signal at a logic 0 throughout all successive memory cycles in which the row address is common. This "page-mode" of operation will not dissipate the power associated with the negative going edge of RAS. Also, the time required for strobing in a new row address is eliminated, thereby decreasing the access and cycle times.

The page boundary of a single MK 4116 is limited to the 128 column locations determined by all combinations of the 7 column address bits. However, the page boundary of the MK4332 can be extended by using CAS rather than RAS as the chip select signal. RAS is applied to all devices to latch the row address into each device and then CAS is decoded and serves as a page cycle select signal. Only those devices which receive both RAS and CAS signals will execute a read or write cycle.

### REFRESH

Refresh of the MK4116 is accomplished by performing a memory cycle at each of the 128 row addresses within each 2 millisecond time interval. Each MK4116 in the MK4332 Assembly must receive all 128 refresh cycles within the 2ms time interval in order to completely refresh all 32,768 memory cells.

Although any normal memory cycle will perform the refresh operation, this function is most easily accomplished with "RAS-only" cycles. RAS-only refresh results in a substantial reduction in operating power. This reduction in power is reflected in the IDD3 specification.

### POWER CONSIDERATIONS

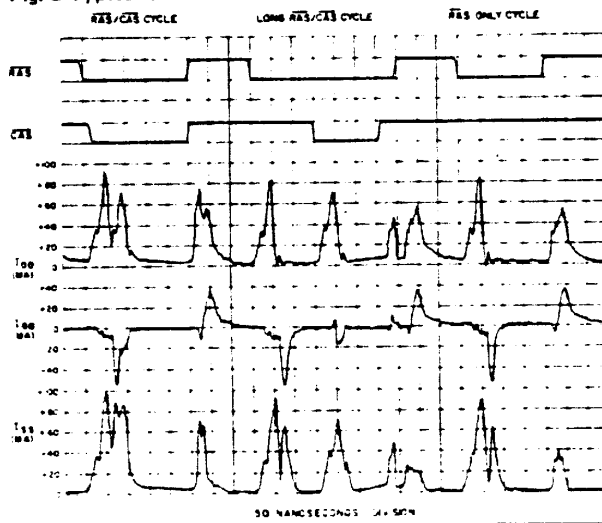
Most of the circuitry used in the MK 4332 is dynamic and most of the power drawn is the result of an address strobe edge. Consequently, the dynamic power is primarily a function of operating frequency rather than active duty cycle (refer to the MK 4116 current waveforms in figure 5). This current characteristic of the MK 4332 precludes inadvertent burn out of the device in the event that the clock inputs become shorted to ground due to system malfunction.

Although no particular power supply noise restriction exists other than the supply voltages remain within the specified tolerance limits, adequate decoupling should be provided to suppress high frequency noise resulting from the transient current of the device. This insures optimum system performance and reliability. Bulk capacitance requirements are minimal since the MK 4332 draws very little steady state (DC) current.

In system applications requiring lower power dissipation, the operating frequency (cycle rate) of the MK 4332 can be reduced and the (guaranteed maximum) average power dissipation of the device will be lowered in accordance with the IDD1 (max) spec limit curve illustrated in figure 2. NOTE: The MK 4332 family is guaranteed to have a maximum IDD1 requirement of 36.5mA @ 375ns cycle with an ambient temperature range from 0° to 70° C. A lower operating frequency, for example 1 microsecond cycle, results in a reduced maximum IDD1 requirement of under 20mA with an ambient temperature range from 0° to 70° C.

NOTE: Additional power supply tolerance has been included on the Vgg supply to allow direct interface capability with both -5V systems -5.2V ECL systems.

Fig. 5 Typical Current Waveforms for the MK 4116



32-768-1161  
 DYNAMIC  
 MEMORY  
 REFRESH

Although  $\overline{RAS}$  and/or  $\overline{CAS}$  can be decoded and used as a chip select signal for the MK 4116, overall system power is minimized if the Row Address Strobe ( $\overline{RAS}$ ) is used for this purpose. All unselected devices (those which do not receive a  $\overline{RAS}$ ) will remain in a low power (standby) mode regardless of the state of  $\overline{CAS}$ .

#### POWER UP

The MK 4332 requires no particular power supply sequencing so long as the Absolute Maximum Rating Conditions are observed. However, in order to insure compliance with the Absolute Maximum Ratings, MOSTEK recommends sequencing of power supplies

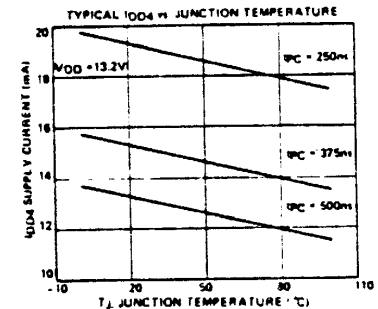
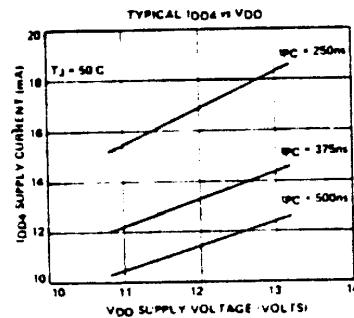
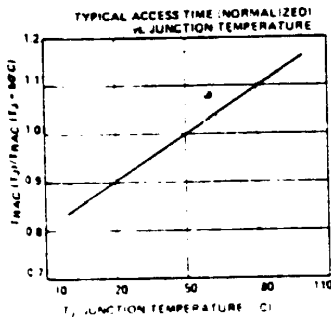
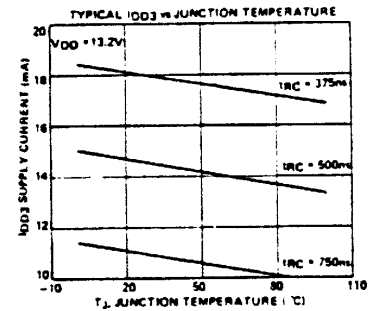
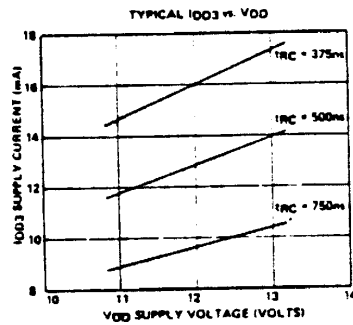
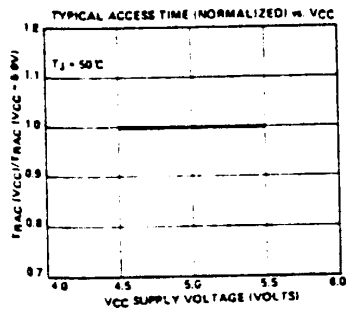
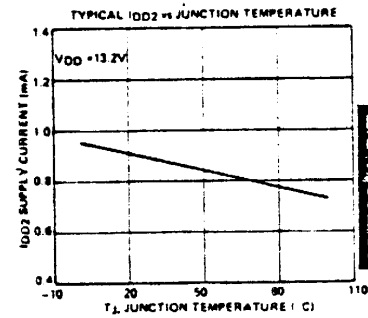
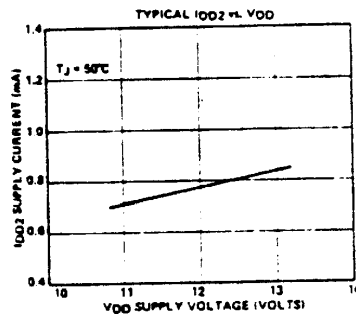
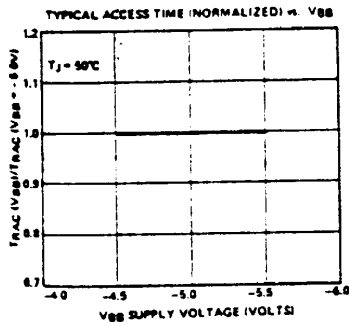
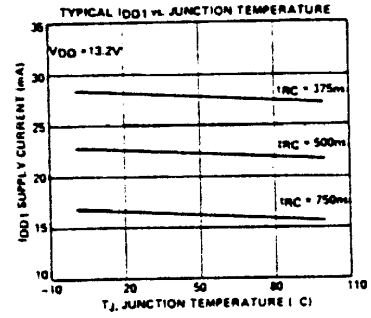
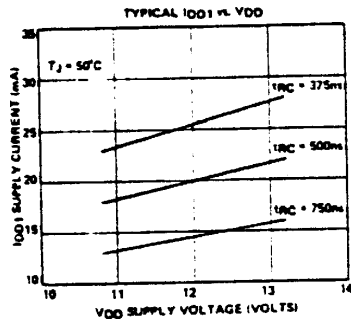
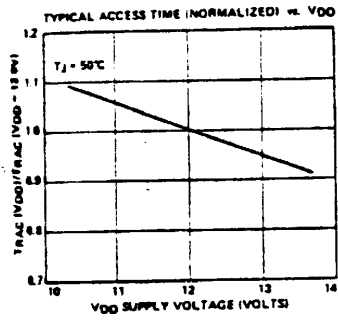
such that  $V_{BB}$  is applied first and removed last.  $V_{BB}$  should never be more positive than  $V_{SS}$  when power is applied to  $V_{DD}$ .

Under system failure conditions in which one or more supplies exceed the specified limits significant additional margin against catastrophic device failure may be achieved by forcing  $\overline{RAS}$  and  $\overline{CAS}$  to the inactive state (high level).

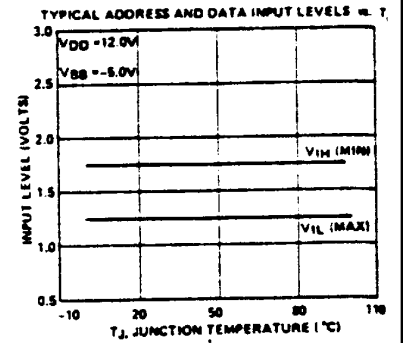
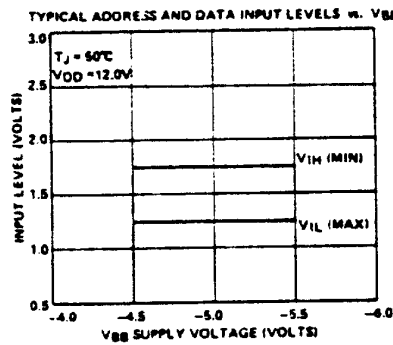
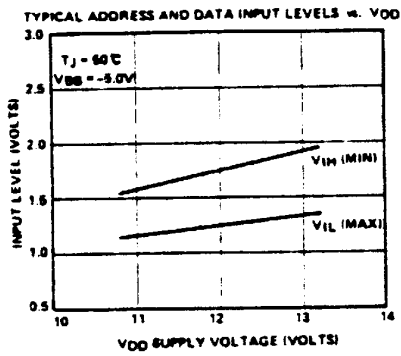
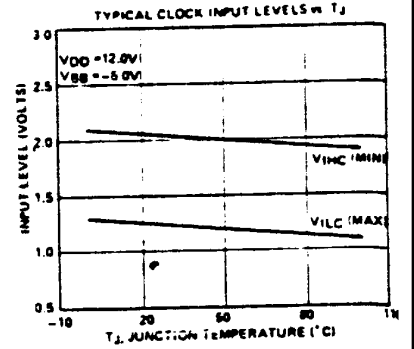
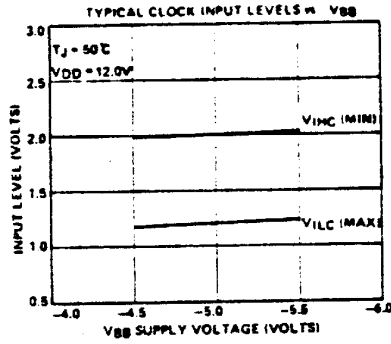
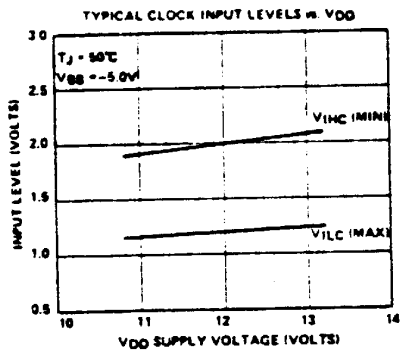
After power is applied to the device, the MK 4332 requires several cycles before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose. Each MK 4116 device must receive the 8 initialization cycles.

PRE-RELEASE  
VERSION

TYPICAL CHARACTERISTICS OF THE MK 4116



DigiBarn Computer Museum



PRE-RELEASE  
VERSION

REV.	ZONE	ECO #	REVISION	APPD
A		655	INITIAL RELEASE	

**PRE-RELEASE  
VERSION**

**ENGINEERING RELEASE**  
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**ENGINEERING SPECIFICATION**


P/N 333-0007

DESCRIPTION: IC, Ram, 65,536 X 1, 4164 type, 128 cycle, refresh.

Part is to have a 200nS, or less access time (trac).

Specification Sheet of a typical 4164 RAM is to be filed under  
 Apple P/N 333-0007.

DRAWING NUMBER  
 333-0007-A  
 SH 1 OF 7

<b>TOLERANCES</b> UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES.  DECIMALS    .X ± _____ .XX ± _____ .XXX ± _____ ANGLES       XX.X ± _____ FRACTIONS     ± _____ DIMENSIONS IN PARENTHESIS ARE IN MILLIMETERS.	DRAWN BY                      DATE C Brown                      3-25-81	 TITLE IC, Ram, 64K, 200NS, 128 cycle, refresh, W0/Logo, W0/burn-in
	CHECKED BY                      DATE P. Boorn                      3/30/81	
	APPROVED BY                      DATE P. Conn                      4/1/81	
	RELEASED BY                      DATE [Signature]                      4/15/81	
MATERIAL:	SIZE A	DRAWING NUMBER 333-0007-A
NEXT ASSY.    FINISH:	SCALE:	SHEET 1 OF 7



# μPD4164

Operating Temperature	0°C to +70°C
Storage Temperature (Ceramic Package)	-55°C to +150°C
(Plastic Package)	-55°C to +125°C
Supply Voltages On Any Pin Except VCC	-1 to +7 Volts ①
Supply Voltage VCC	-0.5 to +7 Volts ①
Short Circuit Output Current	50 mA
Power Dissipation	1 Watt

## ABSOLUTE MAXIMUM RATINGS\*

Note: ① Relative to VSS

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

\*T<sub>a</sub> = 25°C

T<sub>a</sub> = 0° to 70°C ① : VCC = +5V ± 10%; VSS = 0V

## DC CHARACTERISTICS

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Supply Voltage	VCC	4.5	5.0	5.5	V	All Voltages Referenced to VSS
	VSS	0	0	0	V	
High Level Input Voltage (RAS, CAS, WE)	V <sub>IHC</sub>	2.4		5.5	V	
High Level Input Voltage, All Inputs Except RAS, CAS, WE	V <sub>IH</sub>	2.4		5.5	V	
Low Level Input Voltage, All Inputs	V <sub>IL</sub>	-2.0		0.8	V	
Operating Current Average Power Supply Operating Current RAS, CAS Cycling; t <sub>RC</sub> = t <sub>RC</sub> (Min.)	I <sub>CC1</sub>			45	mA	
				50		
				60		
Standby Current Power Supply Standby Current (RAS = V <sub>IHC</sub> , DOUT = Hi-Impedance)	I <sub>CC2</sub>			5.0	mA	
Refresh Current Average Power Supply Current, Refresh Mode; RAS Cycling, CAS = V <sub>IHC</sub> , t <sub>RC</sub> = t <sub>RC</sub> (Min.)	I <sub>CC3</sub>			35	mA	②
				40		
				45		
Page Mode Current Average Power Supply Current, Page Mode Operation RAS = V <sub>IL</sub> , CAS Cycling t <sub>PC</sub> = t <sub>PC</sub> (Min.)	I <sub>CC4</sub>			35	mA	②
				40		
				45		
Input Leakage Current Any Input V <sub>IN</sub> = 0 to +5.5 Volts, All Other Pins Not Under Test = 0V	I <sub>I(L)</sub>	-10		10	μA	
Output Leakage Current DOUT is Disabled, V <sub>OUT</sub> = 0 to +5.5 Volts	I <sub>O(L)</sub>	-10		10	μA	
Output Levels High Level Output Voltage (I <sub>O</sub> = 5 mA)	V <sub>OH</sub>	2.4		VCC	V	
	V <sub>OL</sub>	0		0.4	V	

Notes: ① T<sub>a</sub> is specified here for operation at frequencies to t<sub>RC</sub> ≥ t<sub>RC</sub> (min). Operation at higher cycle rates with reduced ambient temperatures and high power dissipation is permissible, however, provided AC operating parameters are met.

② I<sub>CC1</sub>, I<sub>CC3</sub> and I<sub>CC4</sub> depend on output loading and cycle rates. Specified rates are obtained with the output open.

PRE-RELEASED VERSION

μPD4164

AC CHARACTERISTICS

T<sub>a</sub> = 0° to +70°C ①; V<sub>CC</sub> = +5V ± 10%; V<sub>SB</sub> = 0V ② ③

PARAMETER	SYMBOL	LIMITS						UNITS	TEST CONDITIONS
		μPD4164-1		μPD4164-2		μPD4164-3			
		MIN	MAX	MIN	MAX	MIN	MAX		
Random Read or Write Cycle Time	t <sub>RC</sub>	410		338		270		ns	①
Read Write Cycle Time	t <sub>RWC</sub>	488		338		270		ns	①
Page Mode Cycle Time	t <sub>PC</sub>	275		225		170		ns	
Access Time from RAS	t <sub>RAC</sub>		250		200		150	ns	① ④
Access Time from CAS	t <sub>CAC</sub>		186		135		100	ns	⑦ ⑧
Output Buffer Turn-Off Delay	t <sub>OFF</sub>	0	60	0	60	0	40	ns	③
Transition Time (Rise and Fall)	t <sub>T</sub>	3	30	3	30	3	30	ns	④
RAS Precharge Time	t <sub>RP</sub>	150		120		100		ns	
RAS Pulse Width	t <sub>RA5</sub>	250	10,000	200	10,000	150	10,000	ns	
RAS Hold Time	t <sub>RSH</sub>	186		135		100		ns	
CAS Pulse Width	t <sub>CAS</sub>	186	10,000	135	10,000	100	10,000	ns	
CAS Hold Time	t <sub>CSH</sub>	250		200		150		ns	
RAS to CAS Delay Time	t <sub>RCD</sub>	35	85	30	65	25	50	ns	⑤
CAS to RAS Precharge Time	t <sub>CRP</sub>	0		0		0		ns	
CAS Precharge Time	t <sub>CPH</sub>	35		30		25		ns	
CAS Precharge Time (Per Page Mode Cycle Only)	t <sub>CP</sub>	100		80		60		ns	
RAS Precharge CAS Hold Time	t <sub>RPC</sub>	0		0		0		ns	
Row Address Set-Up Time	t <sub>ASR</sub>	0		0		0		ns	
Row Address Hold Time	t <sub>RAH</sub>	25		20		15		ns	
Column Address Set-Up Time	t <sub>ASC</sub>	0		0		0		ns	
Column Address Hold Time	t <sub>CAH</sub>	75		55		45		ns	
Column Address Hold Time Referenced to RAS	t <sub>AR</sub>	160		120		95		ns	
Read Command Set-Up Time	t <sub>RCS</sub>	0		0		0		ns	
Read Command Hold Time Referenced to RAS	t <sub>RRH</sub>	30		25		20		ns	⑥
Read Command Hold Time	t <sub>RCH</sub>	0		0		0		ns	⑥
Write Command Hold Time Referenced to RAS	t <sub>WRH</sub>	75		55		45		ns	
Write Command Hold Time	t <sub>WCH</sub>	160		120		95		ns	
Write Command Pulse Width	t <sub>WP</sub>	75		55		45		ns	
Write Command to RAS Lead Time	t <sub>RWL</sub>	100		55		45		ns	
Write Command to CAS Lead Time	t <sub>WWL</sub>	100		55		45		ns	
Data-In Set-Up Time	t <sub>DS</sub>	0		0		0		ns	①
Data-In Hold Time	t <sub>DH</sub>	75		55		45		ns	①
Data-In Hold Time Referenced to RAS	t <sub>DHR</sub>	160		120		95		ns	
Refresh Period	t <sub>REF</sub>		2		2		2	ns	
WRITE Command Set-Up Time	t <sub>WCS</sub>	-20		-20		-20		ns	⑥
CAS to WRITE Delay	t <sub>CWD</sub>	115		80		60		ns	⑥
RAS to WRITE Delay	t <sub>RWD</sub>	200		140		110		ns	⑥

- Notes:
- ① T<sub>a</sub> is specified here for operation at frequencies to t<sub>RC</sub> > t<sub>RC</sub> (min). Operation at higher cycle rates with reduced ambient temperatures and higher power dissipation is permissible, however, provided AC operating parameters are met.
  - ② An initial pulse of 100 ns is required after power-up followed by any 2 RAS cycles before greater device operation is allowed.
  - ③ AC measurements assume t<sub>T</sub> = 5 ns.
  - ④ V<sub>TRC</sub> (max) or V<sub>IH</sub> (min) and V<sub>IL</sub> (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V<sub>IHC</sub> or V<sub>IH</sub> and V<sub>IL</sub>.
  - ⑤ The specifications for t<sub>RC</sub> (min) and t<sub>RP</sub> (min) are used only to indicate cycle times at which greater operation over the full temperature range (0°C < T<sub>a</sub> < 70°C) is assured.
  - ⑥ Assumes that t<sub>RCS</sub> < t<sub>RCD</sub> (max). If t<sub>RCS</sub> is greater than the maximum recommended value shown in this table, t<sub>RAC</sub> will increase by the amount that t<sub>RCD</sub> exceeds the values shown.
  - ⑦ Assumes that t<sub>RCD</sub> > t<sub>RCD</sub> (max).
  - ⑧ Measured with a load equivalent to 2 TTL loads and 100 pF.
  - ⑨ t<sub>OFF</sub> (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
  - ⑩ Operation within the t<sub>RCD</sub> (max) limit ensures that t<sub>RAC</sub> (max) can be met. t<sub>RCD</sub> (max) is specified as a reference point only; if t<sub>RCD</sub> is greater than the specified t<sub>RCD</sub> (max) limit, then access time is controlled exclusively by t<sub>CAC</sub>.
  - ⑪ These parameters are referenced to CAS leading edge in early write cycles and to WRITE leading edge in delayed write or read-modify-write cycles.
  - ⑫ t<sub>RCS</sub>, t<sub>CWD</sub> and t<sub>RWD</sub> are restrictive operating parameters in read-write and read-modify-write cycles only. If t<sub>RCS</sub> > t<sub>RCD</sub> (min), the cycle is an early write cycle and the data output will remain open circuit throughout the entire cycle. If t<sub>CWD</sub> > t<sub>CWD</sub> (min) and t<sub>RWD</sub> > t<sub>RWD</sub> (min), the cycle is a read-write and the data output will contain data read from the selected cell. If neither of the above conditions are met the condition of the data out let access time and until CAS goes back to V<sub>IH</sub> is indeterminate.
  - ⑬ Either t<sub>RAH</sub> or t<sub>RCH</sub> must be satisfied for a read cycle.



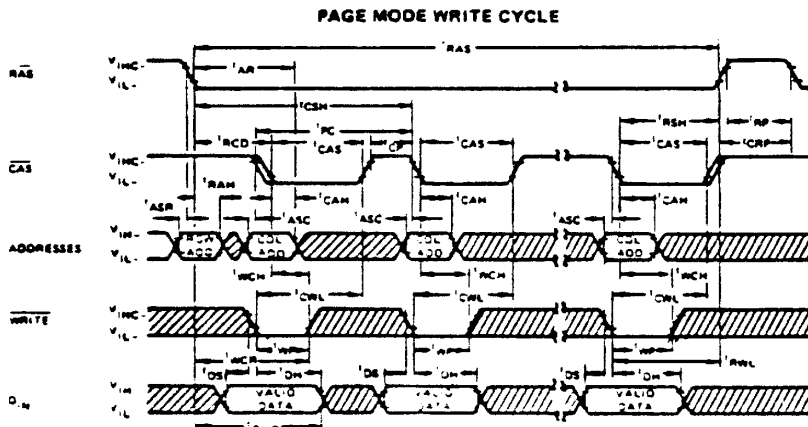
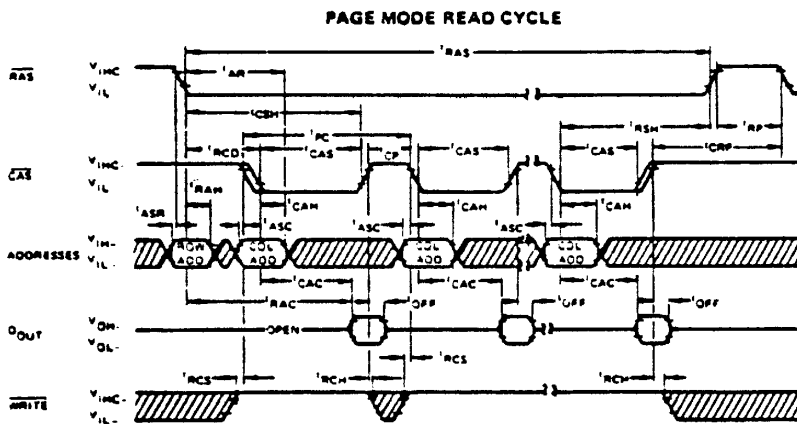
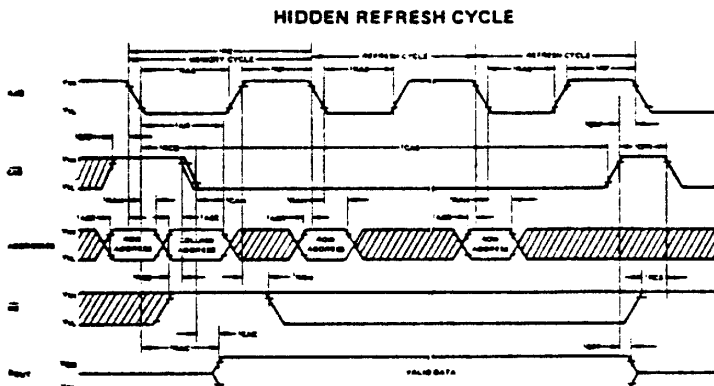
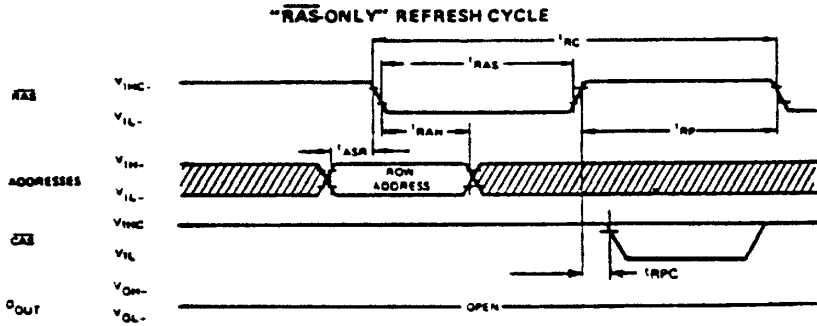
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μPD4164

TIMING WAVEFORMS  
(CONT.)



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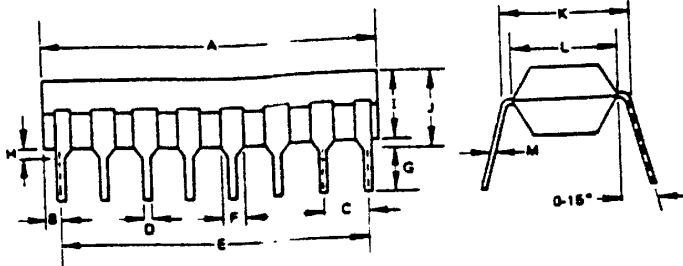
**μPD4164**

**CAPACITANCE**

$T_a = 0^\circ \text{ to } +70^\circ \text{C}; V_{CC} = +5V \pm 10\%; V_{SS} = 0V$

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input Capacitance (A <sub>0</sub> -A <sub>7</sub> ), DIN	C <sub>I1</sub>		5	6	pF	
Input Capacitance RAS, CAS, WRITE	C <sub>I2</sub>			10	pF	
Output Capacitance (DOUT)	C <sub>O</sub>			7	pF	

**PACKAGE OUTLINES  
μPD4164C**

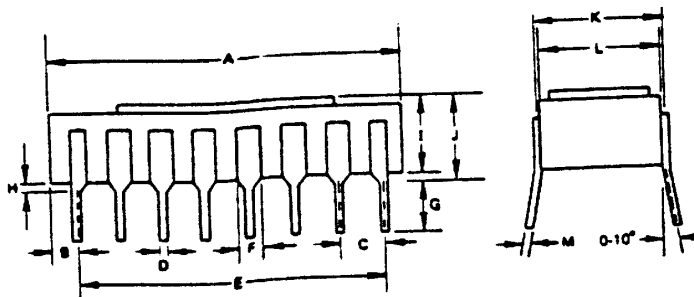


Plastic

ITEM	MILLIMETERS	INCHES
A	19.4 MAX	0.76 MAX
B	0.82	0.03
C	2.54	0.10
D	0.5	0.02
E	17.78	0.70
F	1.3	0.051
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.02 MIN
I	4.05 MAX	0.16 MAX
J	4.55 MAX	0.18 MAX
K	7.62	0.30
L	6.4	0.25
M	0.25 <sup>+0.10</sup> / <sub>0.05</sub>	0.01

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**μPD4164D**



Ceramic

ITEM	MILLIMETERS	INCHES
A	20.8 MAX	0.81 MAX
B	1.28	0.05
C	2.54	0.10
D	0.5	0.02
E	17.78	0.70
F	1.3	0.051
G	2.5 MIN	0.10 MIN
H	0.5 MIN	0.02 MIN
I	4.6 MAX	0.18 MAX
J	5.1 MAX	0.20 MAX
K	7.6	0.30
L	7.3	0.29
M	0.27	0.01

4164DS-9-80-CAT

## Bidirectional Transceiver

### General Description

The DP7304B/DP8304B are 8-bit TRI-STATE® Schottky transceivers. They provide bidirectional drive for bus-oriented microprocessor and digital communications systems. Straight through bidirectional transceivers are featured, with 16 mA drive capability on the A ports and 48 mA bus drive capability on the B ports. PNP inputs are incorporated to reduce input loading.

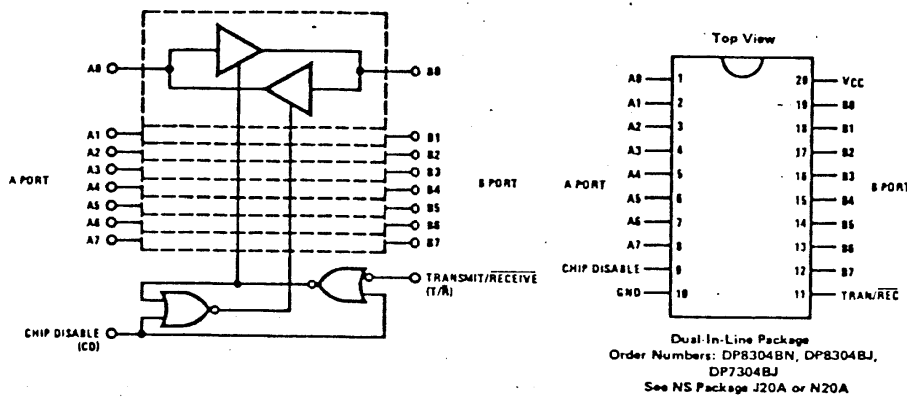
Transmit/Receive inputs determine the direction of logic signals through the bidirectional transceiver. The Chip Disable input disables both A and B ports by placing them in a TRI-STATE condition.

The output high voltage ( $V_{OH}$ ) is specified at  $V_{CC} - 1.15V$  minimum to allow interfacing with MOS, CMOS, TTL, ROM, RAM, or microprocessors.

### Features

- 8 Bit Bidirectional Data Flow Reduced System Package Count
- Bidirectional TRI-STATE Inputs/Outputs Interface with Bus-Oriented Systems
- PNP Inputs Reduce Input-Loading
- Output High Voltage Interfaces with TTL, MOS, and CMOS
- 48 mA/300 pF Bus Drive Capability
- Pinouts Simplify System Interconnections
- Transmit/Receive and Chip Disable Simplify Control Logic
- Compact 20-Pin Dual-In-Line Package
- Low  $I_{CC}$  Power (8 mA per bidirectional bit)

### Logic and Connection Diagrams



### Logic Table

Inputs		Resulting Conditions	
Chip Disable	Transmit/Receive	A Port	B Port
0	0	OUT	IN
0	1	IN	OUT
1	X	TRI-STATE	TRI-STATE

X = Don't Care

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Absolute Maximum Ratings (Note 1)		Recommended Operating Conditions		
Supply Voltage	7V	Min	Max	Units
Input Voltage	5.5V			
Output Voltage	5.5V			
Storage Temperature	-65°C to +150°C	Supply Voltage (V <sub>CC</sub> )		
Lead Temperature (soldering, 10 seconds)	300°C	DP7304B	4.6	5.5 V
Power Dissipation		DP8304B	4.75	5.25 V
Cavity Package (J)	730 mW at 125°C	Temperature (T <sub>A</sub> )		
Molded Package (N)	600 mW at 70°C	DP7304B	-55	125 °C
		DP8304B	0	70 °C

**Electrical Characteristics** (Notes 2 and 3)

Parameter	Conditions	Min	Typ	Max	Units
<b>A Port (A0-A7)</b>					
V <sub>IH</sub> Logical "1" Input Voltage	CD = 0.8V, T/R = 2.0V	2.0			V
V <sub>IL</sub> Logical "0" Input Voltage	CD = 0.8V, T/R = 2.0V	DP8304B		0.8	V
		DP7304B		0.7	V
V <sub>OH</sub> Logical "1" Output Voltage	CD = 0.8V, T/R = 0.8V, I <sub>OH</sub> = -0.4 mA	V <sub>CC</sub> - 1.15	V <sub>CC</sub> - 0.7		V
		I <sub>OH</sub> = -3 mA	2.7	3.95	V
V <sub>OL</sub> Logical "0" Output Voltage	CD = T/R = 0.8V	I <sub>OL</sub> = 16 mA (8304B)	0.35	0.5	V
		I <sub>OL</sub> = 8 mA (both)	0.3	0.4	V
I <sub>OS</sub> Output Short Circuit Current	CD = 0.8V, T/R = 0.8V, V <sub>O</sub> = 0V, V <sub>CC</sub> = max, Note 4	-10	-38	-75	mA
I <sub>IH</sub> Logical "1" Input Current	CD = 0.8V, T/R = 2.0V, V <sub>IH</sub> = 2.7V		0.1	80	μA
I <sub>I</sub> Input Current at Maximum Input Voltage	CD = 2.0V, V <sub>CC</sub> = max, V <sub>IH</sub> = 5.25V			1	mA
I <sub>IL</sub> Logical "0" Input Current	CD = 0.8V, T/R = 2.0V, V <sub>IL</sub> = 0.4V		-70	-200	μA
V <sub>CLAMP</sub> Input Clamp Voltage	CD = 2.0V, I <sub>IN</sub> = -12 mA		-0.7	-1.5	V
I <sub>OD</sub> Output/Input TRI-STATE Current	CD = 2.0V	V <sub>IN</sub> = 0.4V		-200	μA
		V <sub>IN</sub> = 4.0V		80	μA
<b>B Port (B0-B7)</b>					
V <sub>IH</sub> Logical "1" Input Voltage	CD = 0.8V, T/R = 0.8V	2.0			V
V <sub>IL</sub> Logical "0" Input Voltage	CD = 0.8V, T/R = 0.8V	DP8304B		0.8	V
		DP7304B		0.7	V
V <sub>OH</sub> Logical "1" Output Voltage	CD = 0.8V, T/R = 2.0V	I <sub>OH</sub> = -0.4 mA	V <sub>CC</sub> - 1.15	V <sub>CC</sub> - 0.8	V
		I <sub>OH</sub> = -5 mA	2.7	3.9	V
		I <sub>OH</sub> = -10 mA	2.4	3.6	V
V <sub>OL</sub> Logical "0" Output Voltage	CD = 0.8V, T/R = 2.0V	I <sub>OL</sub> = 20 mA	0.3	0.4	V
		I <sub>OL</sub> = 48 mA	0.4	0.5	V
I <sub>OS</sub> Output Short Circuit Current	CD = 0.8V, T/R = 2.0V, V <sub>O</sub> = 0V, V <sub>CC</sub> = max, Note 4	-25	-50	-150	mA
I <sub>IH</sub> Logical "1" Input Current	CD = 0.8V, T/R = 0.8V, V <sub>IH</sub> = 2.7V		0.1	80	μA
I <sub>I</sub> Input Current at Maximum Input Voltage	CD = 2.0V, V <sub>CC</sub> = max, V <sub>IH</sub> = 5.25V			1	mA
I <sub>IL</sub> Logical "0" Input Current	CD = 0.8V, T/R = 0.8V, V <sub>IL</sub> = 0.4V		-70	-200	μA
V <sub>CLAMP</sub> Input Clamp Voltage	CD = 2.0V, I <sub>IN</sub> = -12 mA		-0.7	-1.5	V
I <sub>OD</sub> Output/Input TRI-STATE Current	CD = 2.0V	V <sub>IN</sub> = 0.4V		-200	μA
		V <sub>IN</sub> = 4.0V		+200	μA

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Electrical Characteristics (cont'd.) (Notes 2 and 3)

Parameter	Conditions	Min	Typ	Max	Units	
Control Inputs CD, T/R						
V <sub>IH</sub> Logical "1" Input Voltage		2.0			V	
V <sub>IL</sub> Logical "0" Input Voltage				0.8	V	
I <sub>IH</sub> Logical "1" Input Current	V <sub>IH</sub> = 2.7V		0.5	20	μA	
I <sub>I</sub> Input Current at Maximum Input Voltage	V <sub>CC</sub> = max, V <sub>IH</sub> = 5.25V			1.0	mA	
I <sub>IL</sub> Logical "0" Input Current	V <sub>IL</sub> = 0.4V	T/R		-0.1	-0.25	mA
		CD		-0.25	-0.5	mA
V <sub>CLAMP</sub> Input Clamp Voltage	I <sub>IN</sub> = -12 mA		-0.8	-1.5	V	
Power Supply Current						
I <sub>CC</sub> Power Supply Current	CD = 2.0V, V <sub>IN</sub> = 0.4V, V <sub>CC</sub> = max		60	100	mA	
	CD = V <sub>INA</sub> = 0.4V, T/R = 2V, V <sub>CC</sub> = max		80	130	mA	

Switching Characteristics V<sub>CC</sub> = 5V, T<sub>A</sub> = 25°C

Parameter	Conditions	Min	Typ	Max	Units
A Port Data/Mode Specifications					
t <sub>PDHLA</sub> Propagation Delay to a Logical "0" from B Port to A Port	CD = 0.4V, T/R = 0.4V (figure A), R1 = 1k, R2 = 5k, C1 = 30 pF		14	18	ns
t <sub>PDLHA</sub> Propagation Delay to a Logical "1" from B Port to A Port	CD = 0.4V, T/R = 0.4V (figure A), R1 = 1k, R2 = 5k, C1 = 30 pF		13	18	ns
t <sub>PLZA</sub> Propagation Delay from a Logical "0" to TRI-STATE from CD to A Port	B0 to B7 = 0.4V, T/R = 0.4V (figure C), S3 = 1, R5 = 1k, C4 = 15 pF		11	15	ns
t <sub>PHZA</sub> Propagation Delay from a Logical "1" to TRI-STATE from CD to A Port	B0 to B7 = 2.4V, T/R = 0.4V (figure C), S3 = 0, R5 = 1k, C4 = 15 pF		8	15	ns
t <sub>PZLA</sub> Propagation Delay from TRI-STATE to a Logical "0" from CD to A Port	B0 to B7 = 0.4V, T/R = 0.4V (figure C), S3 = 1, R5 = 1k, C4 = 30 pF		27	35	ns
t <sub>PZHA</sub> Propagation Delay from TRI-STATE to a Logical "1" from CD to A Port	B0 to B7 = 2.4V, T/R = 0.4V (figure C), S3 = 0, R5 = 5k, C4 = 30 pF		19	25	ns
B Port Data/Mode Specifications					
t <sub>PDHLB</sub> Propagation Delay to a Logical "0" from A Port to B Port	CD = 0.4V, T/R = 2.4V (figure A), R1 = 100Ω, R2 = 1k, C1 = 300 pF, R1 = 667Ω, R2 = 5k, C1 = 45 pF		18	23	ns
			11	18	ns
t <sub>PDLHB</sub> Propagation Delay to a Logical "1" from A Port to B Port	CD = 0.4V, T/R = 2.4V (figure A), R1 = 100Ω, R2 = 1k, C1 = 300 pF, R1 = 667Ω, R2 = 5k, C1 = 45 pF		16	23	ns
			11	18	ns
t <sub>PLZB</sub> Propagation Delay from a Logical "0" to TRI-STATE from CD to B Port	A0 to A7 = 0.4V, T/R = 2.4V (figure C), S3 = 1, R5 = 1k, C4 = 15 pF		13	18	ns
t <sub>PHZB</sub> Propagation Delay from a Logical "1" to TRI-STATE from CD to B Port	A0 to A7 = 2.4V, T/R = 2.4V (figure C), S3 = 0, R5 = 1k, C4 = 15 pF		8	15	ns
t <sub>PZLB</sub> Propagation Delay from TRI-STATE to a Logical "0" from CD to B Port	A0 to A7 = 0.4V, T/R = 2.4V (figure C), S3 = 1, R5 = 100Ω, C4 = 300 pF, S3 = 1, R5 = 667Ω, C4 = 45 pF		32	40	ns
			16	22	ns
t <sub>PZHB</sub> Propagation Delay from TRI-STATE to a Logical "1" from CD to B Port	A0 to A7 = 2.4V, T/R = 2.4V (figure C), S3 = 0, R5 = 1k, C4 = 300 pF, S3 = 0, R5 = 5k, C4 = 45 pF		26	35	ns
			14	22	ns

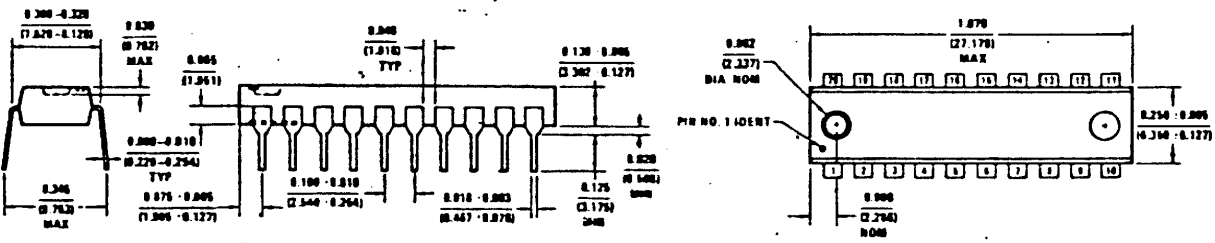
Switching Characteristics (cont'd.) $V_{CC} = 5V, T_A = 25^\circ C$						
Parameter		Conditions	Min	Typ	Max	Units
Transmit/Receive Mode Specifications						
$t_{PHZR}$	Propagation Delay from a Logical "1" to TRI-STATE from T/R to A Port	$CD = 0.4V$ (figure B) $S1 = 1, R4 = 100\Omega, C3 = 300pF$ $S2 = 0, R3 = 1k, C2 = 15pF$		7	12	ns
$t_{PLZR}$	Propagation Delay from a Logical "0" to TRI-STATE from T/R to A Port	$CD = 0.4V$ (figure B) $S1 = 0, R4 = 1k, C3 = 300pF$ $S2 = 1, R3 = 1k, C2 = 15pF$		10	14	ns
$t_{PHZT}$	Propagation Delay from a Logical "1" to TRI-STATE from T/R to B Port	$CD = 0.4V$ (figure B) $S1 = 0, R4 = 1k, C3 = 15pF$ $S2 = 1, R3 = 5k, C2 = 30pF$		16	22	ns
$t_{PLZT}$	Propagation Delay from a Logical "0" to TRI-STATE from T/R to B Port	$CD = 0.4V$ (figure B) $S1 = 1, R4 = 1k, C3 = 15pF$ $S2 = 0, R3 = 1k, C2 = 30pF$		17	22	ns
$t_{PRL}$	Propagation Delay from Transmit Mode to a Logical "0," T/R to A Port	$t_{PRL} = t_{PHZT} + t_{PDHLA}$		25	40	ns
$t_{PRH}$	Propagation Delay from Transmit Mode to a Logical "1," T/R to A Port	$t_{PRH} = t_{PLZT} + t_{PDLHA}$		30	40	ns
$t_{PTL}$	Propagation Delay from Receive Mode to a Logical "0," T/R to B Port	$t_{PTL} = t_{PHZR} + t_{PDHLB}$		25	35	ns
$t_{PTH}$	Propagation Delay from Receive Mode to a Logical "1," T/R to B Port	$t_{PTH} = t_{PLZR} + t_{PDLHB}$		26	35	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Unless otherwise specified, min/max limits apply across the supply and temperature range listed in the table of Recommended Operating Conditions. All typical values given are for  $V_{CC} = 5V$  and  $T_A = 25^\circ C$ .

Note 3: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 4: Only one output at a time should be shorted.



20-Lead Molded DIP (N)


PRE-RELEASE  
VERSION

REV.	ZONE	ECO #	REVISION	APPD
00		352	INITIAL RELEASE	<i>[Signature]</i>
B			PRE-PRODUCTION RELEASE - Sh. 9 all unspecified XY locations were "0"	<i>[Signature]</i>
B		500	ECO RELEASE; Sh. 3 - added part identification.	<i>[Signature]</i>

ENGINEERING RELEASE.  
 This revision supersedes all previous versions.  
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PRE-RELEASE  
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DRAWING NUMBER  
 331-0931 - B  
 SH 1 OF 9

<b>TOLERANCES</b> UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES.  DECIMALS    .X ± — .XX ± — .XXX ± — ANGLES        XX.X ± — FRACTIONS    ± — DIMENSIONS IN PARENTHESIS ARE IN MILLIMETERS	DRAWN BY <i>Dawson</i>	DATE 3-17 80	 <b>apple computer inc.</b>		
	CHECKED BY <i>[Signature]</i>	DATE 1/18/80		TITLE KEYBOARD, ENCODER	
	APPROVED BY <i>[Signature]</i>	DATE 1-19-80		SIZE A	DRAWING NUMBER 331-0931 - B
	RELEASED BY <i>[Signature]</i>	DATE 5-19-80		SCALE: N.A.	SHEET 1 OF 9
MATERIAL: N.A.	NEXT ASSY.				

**ELECTRICAL SPECS**

**Minimum Ratings**

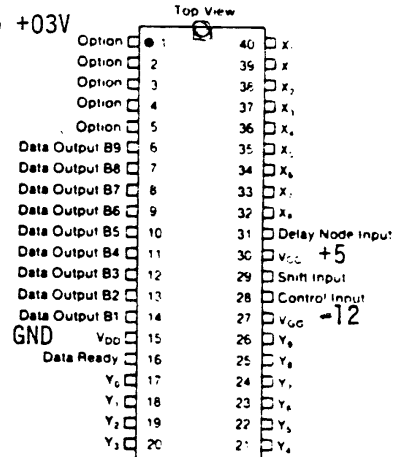
- 1) VDD & VGG (w/respect to Vcc): -20V to + 0.3V
- 2) Logic input voltages (w/respect to Vcc): -20 to +0.3V
- 3) Storage temp: -65°C to 150°C
- 4) Operating temp range: 0°C to +70°C

NOTE: Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied - operating ranges are specified under "standard conditions" listed next.

**STANDARD CONDITIONS**

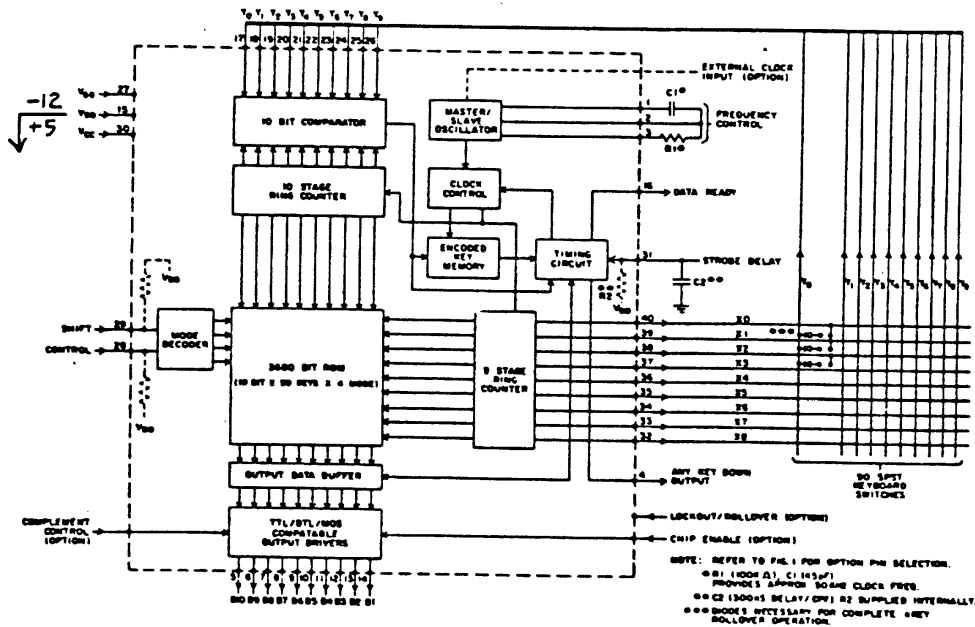
Vcc = +5 volts ± 0.5 volts  
 VGG = 12 volts ± 1.0 volts VDD = GND  
 (Vcc = substrate voltage)  
 Operating temperature (Ta) = 0°C to +70°C

**PIN CONFIGURATION**  
 40 LEAD DUAL IN LINE



**PRE-RELEASE  
 VERSION**

**BLOCK DIAGRAM**



	SIZE <b>A</b>	DRAWING NUMBER <b>331-0931- B</b>
	SCALE:	SHEET <b>2</b> OF <b>9</b>

CUSTOM CODING INFORMATION

The custom coding information for the Keyboard Encoder ROM should be transmitted in the form of 80 column punched cards. Each ROM pattern requires 92 cards (1 title card, 1 circuit option card and 90 ROM pattern cards). (See Note 1)


If it is not possible to supply punched cards, then the Truth Table should be completed (See Note 1). However, there would be a substantial savings in both the coding charge and turn-around time if punched cards were used. Upon receipt of the punched cards or the Truth Table, vendor will prepare a computer-generated Truth Table which will be returned to the used for verification.

OPTIONS USED: Pins 1, 2, & 3 External Clock  
Pin 4 AKO

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PART IDENTIFICATION

Part shall be marked with part number and revision.

 <b>apple computer inc.</b>	SIZE A	DRAWING NUMBER 331-0931-B
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ELECTRICAL CHARACTERISTICS

Characteristics	Sym	Min	Typ**	Max	Units	Conditions
Clock Frequency	f	10	50	100	kHz	See Block diagram footnote <sup>1</sup> for typical R-C values
External Clock Width		7	—	—	μs	
Data & Clock Input (Shift, Control, Complement Control, Lockout/Rollover, Chip Enable & External Clock)						
Logic "0" Level	V <sub>IL</sub>	V <sub>IL</sub>	—	+0.8	V	
Logic "1" Level	V <sub>IH</sub>	V <sub>IH</sub> -1.5	—	V <sub>IH</sub> +0.3	V	
Shift & Control Input Current	I <sub>CC</sub>	75	95	120	μA	V <sub>CC</sub> = +5V
X Output (X <sub>0</sub> -X <sub>4</sub> )						
Logic "1" Output Current	I <sub>OL</sub>	40	170	400	μA	V <sub>CC</sub> = V <sub>IL</sub> (See Note 2)
		600	1300	2500	μA	V <sub>CC</sub> = V <sub>IL</sub> -1.3V
		900	1600	3500	μA	V <sub>CC</sub> = V <sub>IL</sub> -2.0V
		1500	3800	6000	μA	V <sub>CC</sub> = V <sub>IL</sub> -5V
		3000	6000	10000	μA	V <sub>CC</sub> = V <sub>IL</sub> -10V
Logic "0" Output Current	I <sub>OH</sub>	8	15	50	μA	V <sub>CC</sub> = V <sub>IH</sub>
		6	11	35	μA	V <sub>CC</sub> = V <sub>IH</sub> -1.3V
		5	10	30	μA	V <sub>CC</sub> = V <sub>IH</sub> -2.0V
		2	5	15	μA	V <sub>CC</sub> = V <sub>IH</sub> -5V
		—	0.5	5	μA	V <sub>CC</sub> = V <sub>IH</sub> -10V
Y Input (Y <sub>0</sub> -Y <sub>4</sub> )						
Trip Level	V <sub>T</sub>	V <sub>IH</sub> -5	V <sub>IH</sub> -3	V <sub>IH</sub> -2	V	Y Input Going Positive (See Note 2)
Hysteresis	ΔV <sub>T</sub>	0.5	0.9	1.4	V	(See Note 1)
Selected Y Input Current	I <sub>Y</sub>	18	36	100	μA	V <sub>CC</sub> = V <sub>IH</sub>
		14	28	90	μA	V <sub>CC</sub> = V <sub>IH</sub> -1.3V
		13	25	80	μA	V <sub>CC</sub> = V <sub>IH</sub> -2.0V
		6	12	60	μA	V <sub>CC</sub> = V <sub>IH</sub> -5V
		—	1	30	μA	V <sub>CC</sub> = V <sub>IH</sub> -10V
Unselected Y Input Current	I <sub>Y</sub>	9	18	50	μA	V <sub>CC</sub> = V <sub>IH</sub>
		7	14	45	μA	V <sub>CC</sub> = V <sub>IH</sub> -1.3V
		6	13	40	μA	V <sub>CC</sub> = V <sub>IH</sub> -2.0V
		3	6	30	μA	V <sub>CC</sub> = V <sub>IH</sub> -5V
		—	0.5	15	μA	V <sub>CC</sub> = V <sub>IH</sub> -10V
Input Capacitance	C <sub>IN</sub>	—	3	10	pF	at 0V (All Inputs)
X-Y Precharge Characteristics	αP	1500	3500	5000	μA	V = V <sub>IH</sub>
		200	600	1500	μA	V = V <sub>IH</sub> -5 (See Note 2)
Switch Characteristics						
Minimum Switch Closure		—	—	—	—	See Timing Diagram
Contact Closure Resistance	Z <sub>CL</sub>	—	—	300	Ω	
	Z <sub>CS</sub>	1 × 10 <sup>4</sup>	—	—	Ω	
Strobe Delay						
Trip Level (Pin 31)	V <sub>ST</sub>	V <sub>IH</sub> -4	V <sub>IH</sub> -3	V <sub>IH</sub> -2	V	
Hysteresis	ΔV <sub>ST</sub>	0.5	0.9	1.4	V	(See Note 1)
Quiescent Voltage (Pin 31)	V <sub>Q</sub>	-3	-5	-8	V	With Internal Switched Resistor
Data Output (B1-B10), Any Key Down Output, Data Ready						
Logic "0"		—	—	0.4	V	I <sub>OL</sub> = 1.6mA
Logic "1"		V <sub>IH</sub> -1	—	—	V	I <sub>OH</sub> = 1.0mA
		V <sub>IH</sub> -2	—	—	V	I <sub>OL</sub> = 2.2mA
Power						
I <sub>CC</sub>		—	8	12	mA	V <sub>CC</sub> = +5V
I <sub>CS</sub>		—	8	12	mA	V <sub>CC</sub> = -12V

\*\*Typical values are at +25°C and nominal voltages

NOTE

- 1 Hysteresis is defined as the amount of return required to unlatch an input
- 2 Precharge of X outputs and Y inputs occurs during each scanned clock cycle



SIZE  
A

DRAWING NUMBER  
331-0931-B

SCALE:

SHEET 4 OF 9

**OPERATION**

The Encoder contains (see Block Diagram), a 3600 bit ROM, 9-stage and 10-stage ring counters, a 10 bit comparator, timing circuitry, a 90 bit memory to store the location of encoded keys for n key rollover operation, an externally controllable delay network for eliminating the effect of contact bounce, an output data buffer, and TTL/DTL/MOS compatible output drivers.

The ROM portion of the chip is a 360 by 10 bit memory arranged into four 90-word by 10-bit groups. The appropriate levels on the Shift and Control Inputs selects one of the four 90-word groups, the 90-individual word locations are addressed by the two ring counters. Thus, the ROM address is formed by combining the Shift and Control Inputs with the two ring counters.

The external outputs of the 9-stage ring counter and the external inputs to the 10-bit comparator are wired to the keyboard to form an X-Y matrix with the 90-keyboard switches as the crosspoints. In the standby condition, when no key is depressed, the two ring counters are clocked and sequentially address the ROM, thereby scanning the key switches for key closures.

When a key is depressed, a single path is completed between one output of the 9-stage ring counter (X0 thru X8) and one input of the 10-bit comparator (Y0-Y9). After a number of clock cycles, a condition will occur where a level on the selected path to the comparator matches a level on the corresponding comparator input from the 10-stage ring counter.

**N KEY ROLLOVER**

— When a match occurs, and the key has not been encoded, the switch bounce delay network is enabled. If the key is still de-

pressed at the end of the selected delay time, the code for the depressed key is transferred to the output data buffer, the data ready signal appears, a one is stored in the encoded key memory and the scan sequence is resumed. If a match occurs at another key location, the sequence is repeated thus encoding the next key. If the match occurs for an already encoded key, the match is not recognized. The code of the last key encoded remains in the output data buffer.

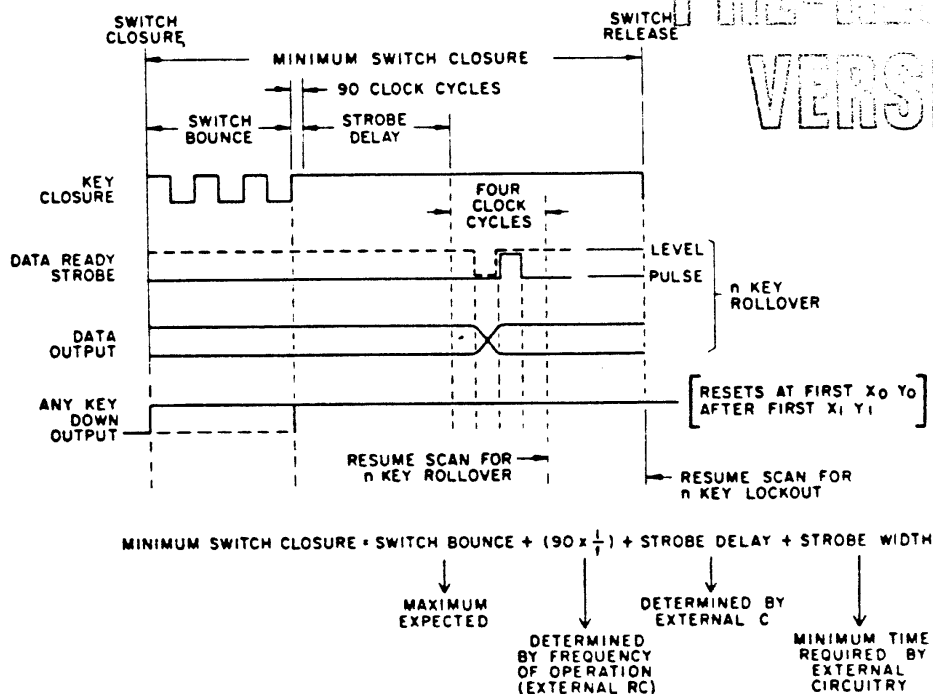
**N KEY LOCKOUT**

— When a match occurs, the delay network is enabled. If the key is still depressed at the end of the selected delay time, the code for the depressed key is transferred to the output data buffer, the data ready signal appears and the remaining keys are locked out by halting the scan sequence. The scan sequence is resumed upon key release. The output data buffer stores the code of the last key encoded.

**SPECIAL PATTERNS**

— Since the selected coding of each key and all the options are defined during the manufacture of the chip, the coding and options can be changed to fit any particular application of the keyboard. Up to 360 codes of up to 10 bits can be programmed into the Encoder ROM covering most popular codes such as ASCII, EBCDIC, Selectric, etc., as well as many specialized codes. The ASCII code in conjunction with internal oscillator, 10 data outputs and any key down output, is available as a standard pattern (See Figure 2).

**TIMING DIAGRAM**



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A

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SCALE:

SHEET 5 OF 9

SYMBOL	MODE				SYMBOL	MODE			
	N	S	C	SC		N	S	C	SC
A		81 Y8 80 Y8		81 Y7	SDH			80 Y8	85 Y0 80 Y9
B		80 Y7		87 Y7	STX			81 Y8	84 Y0 81 Y8
C		85 Y3		83 Y7	STZ	84 Y8	84 Y4	84 Y4	84 Y6 85 Y0
D		87 Y3		84 Y7	STP				84 Y7
E		87 Y7		85 Y7	END				83 Y7
F		87 Y7		85 Y7	ACT			87 Y8	87 Y7 87 Y8
G		87 Y7		87 Y7	BE			83 Y8	86 Y7 83 Y8
H	80 Y5	80 Y5 85 Y7	80 Y5	80 Y5	BI				83 Y4
I		87 Y1		80 Y4	BI	80 Y4	80 Y4	80 Y4 80 Y8	88 Y8
J		86 Y7		87 Y6	LI	87 Y6	87 Y6	87 Y6	
K		87 Y7		86 Y6	LI	83 Y7	83 Y7	83 Y7	83 Y7
L	82 Y6	82 Y6 88 Y7	82 Y6	83 Y6	LI	87 Y8		87 Y8	87 Y8
M		87 Y3		82 Y6	CR		83 Y5	83 Y5 81 Y6	
N		86 Y3		83 Y5	SO	80 Y7		80 Y7 81 Y8	80 Y7 81 Y8
O		88 Y1		84 Y5	S-	81 Y7	81 Y7	81 Y7	81 Y7
P		86 Y6		80 Y7 80 Y7	LIH				80 Y7
Q		80 Y1		81 Y3	OP-				85 Y1
R		83 Y1		87 Y3	OP+				86 Y7
S		81 Y7		84 Y3	OK-				87 Y7
T		84 Y1		85 Y3	OK+				87 Y0
U		80 Y1		86 Y3	SNP				85 Y6
V		84 Y3		87 Y3	SNB				81 Y0
W		81 Y1		86 Y5	CAN	83 Y4		83 Y4	
X		81 Y3		88 Y7	EM				88 Y0
Y		85 Y1		85 Y6	SUR				80 Y0
Z		85 Y3		85 Y5	ESC				87 Y7
[			80 Y7		CS				87 Y4
\			85 Y3		CS				
]			82 Y3		US	81 Y4	81 Y4	81 Y4	
^			87 Y7		SP	82 Y7	82 Y7	82 Y7	82 Y7
_			87 Y1			83 Y3 84 Y8	84 Y8 83 Y3	84 Y8 83 Y3	84 Y8 83 Y3
0			83 Y7			85 Y8	85 Y8 80 Y8	85 Y8	85 Y8
1			84 Y7			86 Y8	83 Y8 87 Y5 81 Y8	83 Y8	83 Y8 87 Y5
2			85 Y7				86 Y8 82 Y0	86 Y8	86 Y8
3			87 Y1				87 Y5 83 Y0	87 Y5	87 Y5
4			87 Y1				87 Y5 84 Y0	87 Y5	87 Y5
5			86 Y7				86 Y8 86 Y8 87 Y8	86 Y8	86 Y8
6			87 Y7				83 Y8	87 Y5	87 Y4
7			88 Y7				87 Y4 83 Y4 88 Y0	87 Y8	87 Y8
8			86 Y3				84 Y8 84 Y7 88 Y8	84 Y8	84 Y8
9			88 Y1				85 Y8 85 Y8 87 Y0 85 Y4	85 Y8	85 Y8
:			86 Y6				80 Y6 85 Y8 87 Y7	80 Y6	80 Y6 87 Y7
;			80 Y1				88 Y3	88 Y3	88 Y3
<			83 Y1				87 Y4	87 Y4	88 Y7
=			81 Y2				88 Y4	88 Y4	88 Y4
>			84 Y1				87 Y4	87 Y4	88 Y4
?			86 Y1				86 Y7 88 Y8	86 Y7 88 Y8	88 Y8
@			84 Y3				80 Y0 80 Y8	80 Y0	80 Y0
A			81 Y1				81 Y0 81 Y8	81 Y0	81 Y0
B			81 Y3				82 Y0	82 Y0	82 Y0
C			85 Y1				83 Y0	83 Y0	83 Y0
D			80 Y3				84 Y0	84 Y0	84 Y0
E			88 Y6 87 Y8				85 Y0 87 Y8	85 Y0	85 Y0
F			81 Y1				86 Y0 83 Y8	86 Y0	86 Y0
G			88 Y6				87 Y0	87 Y0	87 Y0
H			84 Y7 88 Y7				88 Y8 88 Y8	88 Y0	88 Y0
I			83 Y6				85 Y4	88 Y0	88 Y0
J			84 Y5				88 Y5 85 Y6	88 Y5 85 Y6	88 Y5
K							86 Y5	86 Y5	86 Y5
L							86 Y6 87 Y7	86 Y6	86 Y6
M							85 Y5	85 Y5	85 Y5
N							84 Y6	84 Y6	84 Y6
DEL			82 Y8						
NULL	85 Y7	85 Y7	85 Y7 88 Y8	85 Y7 88 Y8					

Note 1: Bits 1 to 6 and bit 8 of the Encoder correspond to bits 1 to 7 of ASCII.

Note 2: Codes 0000011 and 0011111 are not present in the standard Encoder pattern.

Fig.2 STANDARD Encoder CODE ASSIGNMENTS ASCII CODE

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OPTIONS PROVIDED WITH STANDARD ENCODER

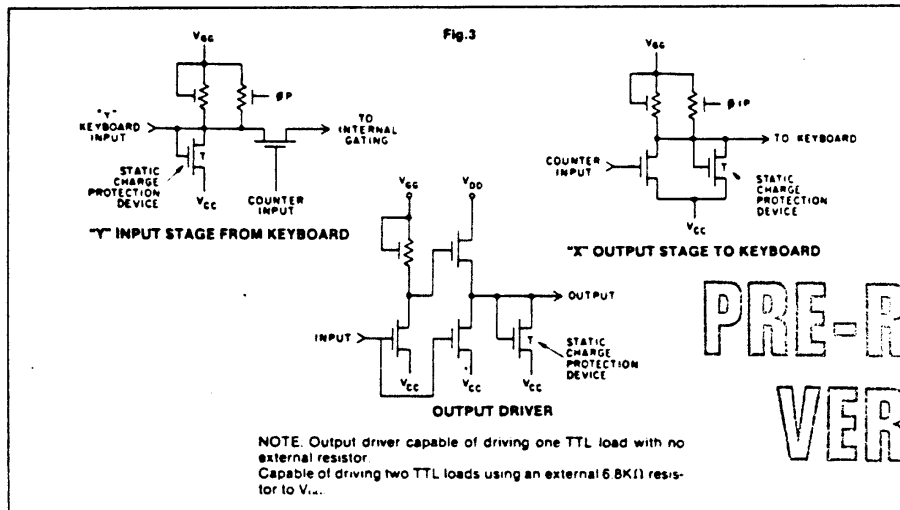
- Device Marking: Encoder
- Internal Oscillator on Pin Nos. 1, 2, 3.
- Any Key Output on Pin No. 4.
- Any Key Output True (Logic 1) During Key Depression.
- Output Data Bit B10 on Pin No. 5.
- N-Key Rollover Only.
- True Outputs Only.
- Pulse Data Ready Signal
- Internal Resistor to V<sub>DD</sub> on Shift/Control Pin
- Plastic Package

apple computer inc.

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TYPICAL CHARACTERISTIC CURVES

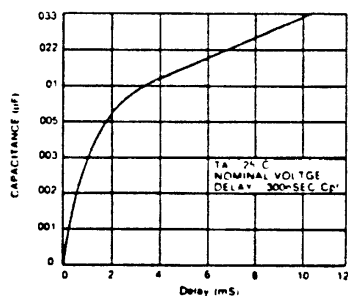


Fig.4 STROBE DELAY vs. C<sub>1</sub>

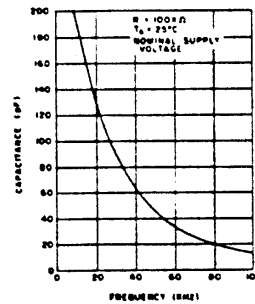


Fig.5 OSCILLATOR FREQUENCY vs. C<sub>2</sub>

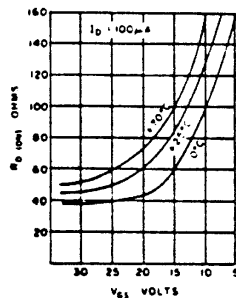


Fig.6 TYPICAL OUTPUT ON RESISTANCE (R<sub>DON</sub>) vs. GATE BIAS VOLTAGE (V<sub>GS</sub>)

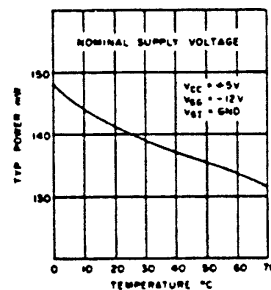


Fig.7 TYPICAL POWER CONSUMPTION (mW)



SIZE  
A

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331-0931-8

SCALE:

SHEET 7 OF 9

LOC XY	NORMAL		SHIFT		CONTROL		SHT/CTR	
	ASCII	HEX	ASCII	HEX	ASCII	HEX	ASCII	HEX
00	3	110011011 1B3	#	110001010 0A3	3	110011011 1B3	#	110001010 0A3
01	4	001011011 1B4	\$	001001010 0A4	4	001011011 1B4	\$	001001010 0A4
02	5	101011011 1B5	%	101001010 0A5	5	101011011 1B5	%	101001010 0A5
03	6	011011011 1B6	&	011001010 0A6	6	011011011 1B6	&	011001010 0A6
04	7	111011011 1B7	'	111001010 0A7	7	111011011 1B7	'	111001010 0A7
05	8	000111011 1B8	(	000101010 0A8	8	000111011 1B8	(	000101010 0A8
06	9	100111011 1B9	)	100101010 0A9	9	100111011 1B9	)	100101010 0A9
07	ϕ	000011011 1B0	ϕ	000011011 1B0	ϕ	000011011 1B0	ϕ	000011011 1B0
08	:	010111011 1BA	*	010101010 0AA	:	010111011 1BA	*	010101010 0AA
09	-	101101010 0AD	=	101111011 1BD	-	101101010 0AD	=	101111011 1BD
10	Q	100010111 1D1	Q	100010101 151	DC1	100010001 111	DC1	100010001 111
11	W	111010111 1D7	W	111010101 157	ETB	111010001 117	ETB	111010001 117
12	E	101000110 0C5	E	101000100 045	ENQ	101000000 105	ENQ	101000000 005
13	R	010010111 1D4	R	010010101 152	DC2	010010001 112	DC2	010010001 112
14	T	001010111 1D4	T	001010101 154	DC4	001010001 114	DC4	001010001 114
15	Y	100110111 1D9	Y	100110101 159	EM	100110001 119	EM	100110001 119
16	U	101010111 1D5	U	101010101 155	NAK	101010001 115	NAK	101010001 115
17	I	100100110 0C9	I	100100100 049	HT	100100000 009	HT	100100000 009
18	O	111100110 0CF	O	111100100 04F	SI	111100000 00F	SI	111100000 00F
19	P	000010111 1D0	@	000000101 140	DLE	000010001 110	NUL	000000000 000
20	D	001000110 0C4	D	001000100 044	EOT	001000000 004	EOT	001000000 004
21	F	011000110 0C6	F	011000100 046	ACK	011000000 006	ACK	011000000 006
22	G	111000110 0C7	G	111000100 047	BEL	111000000 007	BEL	111000000 007
23	H	000100110 0C8	H	000100100 048	BS	000100000 008	BS	000100000 008
24	J	010100110 0CA	J	010100100 04A	LF	010100000 00A	LF	010100000 00A
25	K	110100110 0CB	K	110100100 04B	VT	110100000 00B	VT	110100000 00B
26	L	001100110 0CC	L	001100100 04C	FF	001100000 00C	FF	001100000 00C
27	:	110111011 1BB	+	110101010 0AB	:	110111011 1BB	+	110101010 0AB
28	BS	000100000 008	BS	000100000 008	BS	000100000 008	BS	000100000 008
29	NAK	101010001 115	NAK	101010001 115	NAK	101010001 115	NAK	101010001 115
30	Z	010110111 1DA	Z	010110101 15A	SUB	010110001 11A	SUB	010110001 11A
31	X	000110111 1D8	X	000110101 158	CAN	000110001 118	CAN	000110001 118
32	C	110000110 0C3	C	110000100 043	ETX	110000000 003	ETX	110000000 003
33	V	011010111 1D6	V	011010101 156	SYN	011010001 116	SYN	011010001 116
34	B	010000110 0C2	B	010000100 042	STX	010000000 002	STX	010000000 002

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SCALE:

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LOC XY	ASCII	BBBBBBBB 123456789	HEX	ASCII	BBBBBBBB 123456789	HEX	ASCII	BBBBBBBB 123456789	HEX	ASCII	BBBBBBBB 123456789	HEX
	NORMAL			SHIFT			CONTROL			SHT/CTR		
35	N	011100110	0CE	^	011110100	05E	SO	011100000	00E	RS	011110001	11E
36	M	101100110	0CD	]	101110100	05D	CR	101100000	00D	GS	101110001	11D
37	,	001101010	0AC	<	001110111	1BC	,	001101010	0AC	<	001110111	1BC
38	.	011101010	0AE	>	011111011	1BE	.	011101010	0AE	>	011111011	1BE
39	/	111101010	0AF	?	111111011	1BF	/	111101010	0AF	?	111111011	1BF
40	S	110010111	1D3	S	110010101	153	DC3	110010001	113	DC3	110010001	113
41	2	010011011	1B2	"	010001010	0A2	2	010011011	1B2	"	010001010	0A2
42	1	100011011	1B1	!	100001010	0A1	1	100011011	1B1	!	100001010	0A1
43	ESC	110110001	11B	ESC	110110001	11B	ESC	110110001	11B	ESC	110110001	11B
44	A	100000110	0C1	A	100000100	041	SOH	100000000	001	SOH	100000000	001
45	SP	000001010	0A0	SP	000001010	0A0	SP	000001010	0A0	SP	000001010	0A0
49	CR	101100000	00D	CR	101100000	00D	CR	101100000	00D	CR	101100000	00D
56	Ø	000011011	1B0	Ø	000011011	1B0	Ø	000011011	1B0	Ø	000011011	1B0
57	4	001011011	1B4	4	001011011	1B4	4	001011011	1B4	4	001011011	1B4
58	8	000111011	1B8	8	000111011	1B8	8	000111011	1B8	8	000111011	1B8
59	+	110101010	0AB	+	110101010	0AB	+	110101010	0AB	+	110101010	0AB
66	1	100011011	1B1	1	100011011	1B1	1	100011011	1B1	1	100011011	1B1
67	5	101011011	1B5	5	101011011	1B5	5	101011011	1B5	5	101011011	1B5
68	9	100111011	1B9	9	100111011	1B9	9	100111011	1B9	9	100111011	1B9
69	-	101101010	0AD	-	101101010	0AD	-	101101010	0AD	-	101101010	0AD
76	2	010011011	1B2	2	010011011	1B2	2	010011011	1B2	2	010011011	1B2
77	6	011011011	1B6	6	011011011	1B6	6	011011011	1B6	6	011011011	1B6
78	.	011101010	0AE	.	011101010	0AE	.	011101010	0AE	.	011101010	0AE
79	CR	101100000	00D	CR	101100000	00D	CR	101100000	00D	CR	101100000	00D
86	3	110011011	1B3	3	110011011	1B3	3	110011011	1B3	3	110011011	1B3
87	7	111011011	1B7	7	111011011	1B7	7	111011011	1B7	7	111011011	1B7
88	,	001101010	0AC	,	001101010	0AC	,	001101010	0AC	,	001101010	0AC

NOTES:

- Pin option assignments Pin 1, Pin 2, Pin 3 = Internal Oscillator Pin 4 = AKO.
- Non-specified X-Y locations to be filled as follows: B1 B2 B3 B4 B5 B6 B7 B8 B9 B10  
 HEX 2AØ (negative logic) 0 0 0 0 0 1 0 1 0 1
- Output to be negative logic, ie "1" = low output (0.4V), "0" = high output (2.4V)
- ASCII bit weight: B1 = Pin 14 (LSB), B2 = Pin 13, B3 = Pin 12, B4 = Pin 11, B5 = Pin 10, B6 = Pin 9, B7 = Pin 8, B8 = Pin 8, B8 = Pin 7, B9 = Pin 6 (MSB)
- Reference document 050-0021 (Logic, Number Pad Style Keyboard).
- B10 = "Ø" in all locations.

PIONEER RELEASE  
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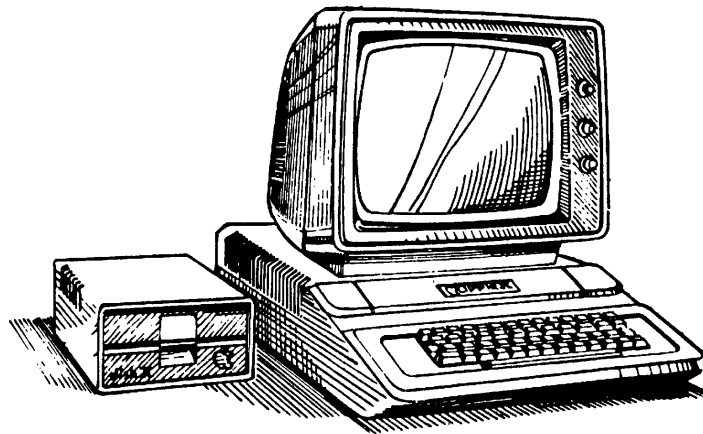


## Apple II Computer Technical Information

# APPLE II / APPLE II-PLUS LEVEL II SERVICE REFERENCE MANUAL

Pre-Release Version

## APPENDIX A 6502 INSTRUCTIONS



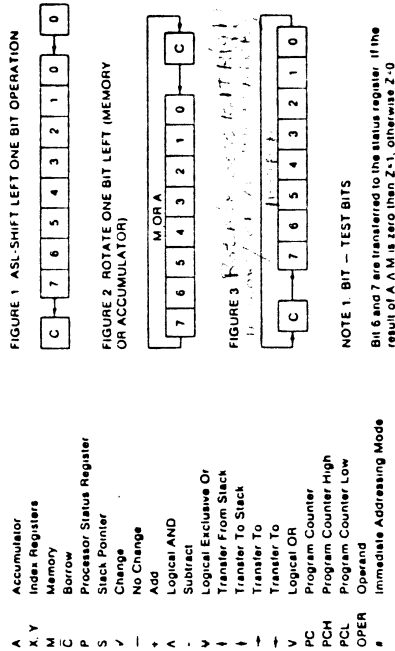
Written by  
**Apple Computer, Inc. • Level II Service Center**  
1981

( This page is not part of the original service manual )

6502 MICROPROCESSOR INSTRUCTIONS

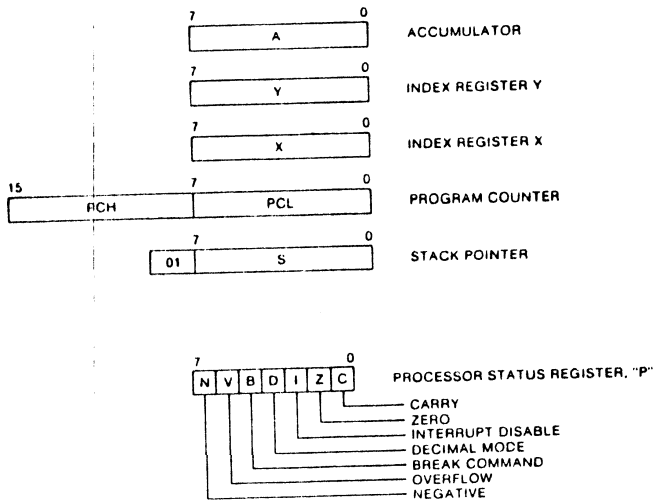
<b>ADC</b>	Add Memory to Accumulator with Carry	<b>LDA</b>	Load Accumulator with Memory
<b>AND</b>	"AND" Memory with Accumulator	<b>LDX</b>	Load Index X with Memory
<b>ASL</b>	Shift Left One Bit (Memory or Accumulator)	<b>LDY</b>	Load Index Y with Memory
<b>BCC</b>	Branch on Carry Clear	<b>LSR</b>	Shift Right One Bit (Memory or Accumulator)
<b>BCS</b>	Branch on Carry Set	<b>NOP</b>	No Operation
<b>BEO</b>	Branch on Result Zero	<b>ORA</b>	"OR" Memory with Accumulator
<b>BIT</b>	Test Bits in Memory with Accumulator	<b>PHA</b>	Push Accumulator on Stack
<b>BMI</b>	Branch on Result Minus	<b>PHP</b>	Push Processor Status on Stack
<b>BNE</b>	Branch on Result not Zero	<b>PLA</b>	Pop Accumulator from Stack
<b>BPL</b>	Branch on Result Plus	<b>PLP</b>	Pop Processor Status from Stack
<b>BRK</b>	Force Break	<b>ROL</b>	Rotate One Bit Left (Memory or Accumulator)
<b>BVC</b>	Branch on Overflow Clear	<b>ROR</b>	Rotate One Bit Right (Memory or Accumulator)
<b>BVS</b>	Branch on Overflow Set	<b>RTI</b>	Return from Interrupt
<b>CLC</b>	Clear Carry Flag	<b>RTS</b>	Return from Subroutine
<b>CLD</b>	Clear Decimal Mode	<b>SBC</b>	Subtract Memory from Accumulator with Borrow
<b>CLI</b>	Clear Interrupt Disable Bit	<b>SEC</b>	Set Carry Flag
<b>CLV</b>	Clear Overflow Flag	<b>SED</b>	Set Decimal Mode
<b>CMF</b>	Compare Memory and Accumulator	<b>SEI</b>	Set Interrupt Disable Status
<b>CPX</b>	Compare Memory and Index X	<b>STX</b>	Store Index X in Memory
<b>CPY</b>	Compare Memory and Index Y	<b>STY</b>	Store Index Y in Memory
<b>DEC</b>	Decrement Memory by One	<b>TAX</b>	Transfer Accumulator to Index X
<b>DEX</b>	Decrement Index X by One	<b>TAY</b>	Transfer Accumulator to Index Y
<b>DEY</b>	Decrement Index Y by One	<b>TSX</b>	Transfer Stack Pointer to Index X
<b>EOB</b>	"Exclusive-Or" Memory with Accumulator	<b>TXA</b>	Transfer Index X to Accumulator
<b>INC</b>	Increment Memory by One	<b>TXS</b>	Transfer Index X to Stack Pointer
<b>INX</b>	Increment Index X by One	<b>TYA</b>	Transfer Index Y to Accumulator
<b>INY</b>	Increment Index Y by One		
<b>JMP</b>	Jump to New Location		
<b>JSR</b>	Jump to New Location Saving Return Address		

THE FOLLOWING NOTATION APPLIES TO THIS SUMMARY:



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### PROGRAMMING MODEL



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### INSTRUCTION CODES

Name Description	Operation	Addressing Mode	Assembly Language Form	HEX OP Code	No Bytes	"P" Status Reg N Z C I D V
<b>ADC</b> Add memory to accumulator with carry	A-M-C → A+C	Immediate Zero Page Zero Page X Absolute Absolute X Absolute Y (indirect X) (indirect Y)	ADC #Oper ADC Oper ADC Oper.X ADC Oper.X ADC Oper.X ADC Oper.Y ADC (Oper.X) ADC (Oper.Y)	69 65 75 60 70 79 61 71	2 2 2 3 3 3 2 2	✓✓✓✓✓
<b>AND</b> "AND" memory with accumulator	A&M → A	Immediate Zero Page Zero Page X Absolute Absolute X Absolute Y (indirect X) (indirect Y)	AND #Oper AND Oper AND Oper.X AND Oper.X AND Oper.X AND Oper.Y AND (Oper.X) AND (Oper.Y)	29 25 35 2D 30 39 21 31	2 2 2 3 3 3 2 2	✓✓-----
<b>ASL</b> Shift left one bit (Memory or Accumulator)	(See Figure 1)	Accumulator Zero Page Zero Page X Absolute Absolute X	ASL A ASL Oper ASL Oper.X ASL Oper ASL Oper.X	0A 06 16 0E 1E	1 2 2 3 3	✓✓✓✓---
<b>BCC</b> Branch on carry clear	Branch on C=0	Relative	BCC Oper	90	2	-----
<b>BCS</b> Branch on carry set	Branch on C=1	Relative	BCS Oper	80	2	-----
<b>BEQ</b> Branch on result zero	Branch on Z=1	Relative	BEQ Oper	F0	2	-----
<b>BIT</b> Test bits in memory with accumulator	A&A.M <sub>7</sub> → N, M <sub>6</sub> → V	Zero Page Absolute	BIT# Oper BIT# Oper	24 2C	2 3	M <sub>7</sub> ✓---M <sub>6</sub>
<b>BMI</b> Branch on result minus	Branch on N=1	Relative	BMI Oper	30	2	-----
<b>BNE</b> Branch on result not zero	Branch on Z=0	Relative	BNE Oper	D0	2	-----
<b>BPL</b> Branch on result plus	Branch on N=0	Relative	BPL Oper	10	2	-----
<b>BRK</b> Force Break	Forced Interrupt PC=PC+1	Implied	BRK#	00	1	---1---
<b>BVC</b> Branch on overflow clear	Branch on V=0	Relative	BVC Oper	50	2	-----

Note 1: M<sub>6</sub>, M<sub>7</sub>, and 7 are transferred to the status register. If the result of A&M<sub>6</sub> is 1, then the 1 otherwise Z=0. Note 2: A BCC, BCS, BEQ, or BNE may be masked by setting I=1.

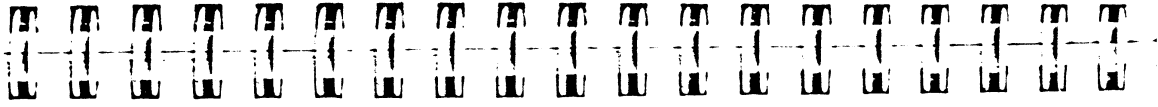
*Handwritten notes:*  
BCC, BCS, BEQ, BNE  
M<sub>6</sub>, M<sub>7</sub>, and 7 are transferred to the status register.  
If the result of A&M<sub>6</sub> is 1, then the 1 otherwise Z=0.

Name Description	Operation	Addressing Mode	Assembly Language Form	HEX OP Code	No Bytes	"P" Status Flag M Z C I O V
<b>EOR</b> Exclusive-Or memory with accumulator	A V M ← A	Immediate Zero Page X Zero Page X Absolute Absolute X Absolute Y Absolute Y (Indirect X) (Indirect Y)	EOR #Oper EOR Oper EOR Oper,X EOR Oper EOR Oper,X EOR Oper,Y EOR Oper,X EOR (Oper,X) EOR (Oper,Y)	49 45 55 4D 50 59 41 51	2 2 3 3 3 3 2 2	✓ ✓ ✓ ✓ ✓ ✓ ✓ ✓
<b>INC</b> Increment memory by one	M + 1 → M	Zero Page X Zero Page X Absolute Absolute X	INC Oper INC Oper,X INC Oper INC Oper,X	E6 E6 EE EE FE FE	2 2 3 3	✓✓ ✓✓ ✓✓ ✓✓
<b>INX</b> Increment index X by one	X + 1 → X	Implied	INX	E8	1	✓✓ ✓✓
<b>INY</b> Increment index Y by one	Y + 1 → Y	Implied	INY	CB	1	✓✓ ✓✓
<b>JMP</b> Jump to new location	(PC-1) → PC (PC-2) → PC	Absolute Indirect	JMP Oper JMP (Oper)	4C 6C	3 3	✓ ✓
<b>JSR</b> Jump to new location saving return address	PC-2 ↓ (PC-1) → PC (PC-2) → PC	Absolute	JSR Oper	20	3	✓ ✓
<b>LDA</b> Load accumulator with memory	M → A	Immediate Zero Page X Zero Page X Absolute Absolute X Absolute Y Absolute Y (Indirect X) (Indirect Y)	LDA #Oper LDA Oper LDA Oper,X LDA Oper LDA Oper,X LDA Oper,Y LDA Oper,X LDA (Oper,Y)	A9 A5 B5 AD BD B9 A1 B1	2 2 2 3 3 3 2 2	✓✓ ✓✓ ✓✓ ✓✓ ✓✓ ✓✓ ✓✓ ✓✓
<b>LDX</b> Load index X with memory	M → X	Immediate Zero Page Y Zero Page Y Absolute Absolute Y	LDX #Oper LDX Oper LDX Oper,Y LDX Oper LDX Oper,Y	A2 A6 B6 AE BE	2 2 2 3 3	✓✓ ✓✓ ✓✓ ✓✓ ✓✓
<b>LDY</b> Load index Y with memory	M → Y	Immediate Zero Page X Zero Page X Absolute Absolute X	LDY #Oper LDY Oper LDY Oper,X LDY Oper LDY Oper,X	A0 A4 B4 AC BC	2 2 2 3 3	✓✓ ✓✓ ✓✓ ✓✓ ✓✓



Name Description	Operation	Addressing Mode	Assembly Language Form	HEX OP Code	No Bytes	"P" Status Flag M Z C I O V
<b>BVS</b> Branch on overflow set	Branch on V=1	Relative	BVS Oper	70	2	✓ ✓ ✓ ✓ ✓ ✓
<b>CLC</b> Clear carry flag	0 → C	Implied	CLC	18	1	✓ ✓ ✓ ✓ ✓ ✓
<b>CLD</b> Clear decimal mode	0 → D	Implied	CLD	D8	1	✓ ✓ ✓ ✓ ✓ ✓
<b>CLI</b> Clear interrupt disable	0 → I	Implied	CLI	58	1	✓ ✓ ✓ ✓ ✓ ✓
<b>CLV</b> Clear overflow flag	0 → V	Implied	CLV	BB	1	✓ ✓ ✓ ✓ ✓ ✓
<b>CMP</b> Compare memory and accumulator	A - M	Immediate Zero Page X Zero Page X Absolute Absolute X Absolute Y Absolute Y (Indirect X) (Indirect Y)	CMP #Oper CMP Oper CMP Oper,X CMP Oper CMP Oper,X CMP Oper,Y CMP Oper,X CMP (Oper,X) CMP (Oper,Y)	C9 C5 D5 D0 D0 D9 C1 D1	2 2 2 3 3 3 2 2	✓✓ ✓✓ ✓✓ ✓✓ ✓✓ ✓✓ ✓✓ ✓✓
<b>CPX</b> Compare memory and index X	X - M	Immediate Zero Page Absolute	CPX #Oper CPX Oper CPX Oper	E0 E4 EC	2 2 3	✓✓ ✓✓ ✓✓
<b>CPY</b> Compare memory and index Y	Y - M	Immediate Zero Page Absolute	CPY #Oper CPY Oper CPY Oper	C0 C4 CC	2 2 3	✓✓ ✓✓ ✓✓
<b>DEC</b> Decrement memory by one	M - 1 → M	Zero Page X Zero Page X Absolute Absolute X	DEC Oper DEC Oper,X DEC Oper DEC Oper,X	C6 D6 CE DE	2 2 3 3	✓✓ ✓✓ ✓✓ ✓✓
<b>DEX</b> Decrement index X by one	X - 1 → X	Implied	DEX	CA	1	✓✓ ✓✓
<b>DEY</b> Decrement index Y by one	Y - 1 → Y	Implied	DEY	BA	1	✓✓ ✓✓

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Name Description	Operation	Addressing Mode	Assembly Language Form	HEX OP Code	No. Bytes	"P" Status Flag
<b>RTI</b> Return from interrupt	P ← PC	Implied		40	1	From Stack
<b>RTS</b> Return from subroutine	PC ← PC + 1 → PC	Implied		60	1	
<b>SBC</b> Subtract memory from accumulator with borrow	A ← M - C → A	Immediate Zero Page Zero Page, X Absolute Absolute X Absolute Y (Indirect X) (Indirect Y)	SBC #Oper SBC Oper SBC Oper, X SBC Oper, X SBC Oper, X SBC Oper, X SBC (Oper, X) SBC (Oper, Y)	E9 E5 F5 E0 F0 E9 E1 F1	2 2 2 3 3 3 2 2	✓✓✓✓
<b>SEC</b> Set carry flag	1 → C	Implied		38	1	
<b>SED</b> Set decimal mode	1 → D	Implied		F8	1	
<b>SEI</b> Set interrupt disable status	1 → I	Implied		78	1	
<b>STA</b> Store accumulator in memory	A → M	Zero Page Zero Page, X Absolute Absolute X Absolute Y (Indirect X) (Indirect Y)	STA Oper STA Oper, X STA Oper, X STA Oper, X STA Oper, X STA (Oper, X) STA (Oper, Y)	85 95 80 90 80 90 81 91	2 2 3 3 3 2 2	
<b>STX</b> Store index X in memory	X → M	Zero Page Zero Page, X Absolute	STX Oper STX Oper, Y STX Oper	86 96 8E	2 2 3	
<b>STY</b> Store index Y in memory	Y → M	Zero Page Zero Page, X Absolute	STY Oper STY Oper, X STY Oper	84 94 8C	2 2 3	
<b>TAX</b> Transfer accumulator to index X	A → X	Implied		AA	1	✓✓
<b>TAY</b> Transfer accumulator to index Y	A → Y	Implied		A8	1	✓✓
<b>TSX</b> Transfer stack pointer to index X	S → X	Implied		BA	1	✓✓

Name Description	Operation	Addressing Mode	Assembly Language Form	HEX OP Code	No. Bytes	"P" Status Flag
<b>LSR</b> Shift right one bit (memory or accumulator)	(See Figure 1)	Accumulator Zero Page Zero Page, X Absolute Absolute X	LSR A LSR Oper LSR Oper, X LSR Oper, X LSR Oper, X	4A 46 56 4E 5E	1 2 2 3 3	0✓✓
<b>NOP</b> No operation	No Operation	Implied		EA	1	
<b>ORA</b> "OR" memory with accumulator	A ← V M → A	Immediate Zero Page Zero Page, X Absolute Absolute X Absolute Y (Indirect X) (Indirect Y)	ORA #Oper ORA Oper ORA Oper, X ORA Oper, X ORA Oper, X ORA Oper, X ORA (Oper, X) ORA (Oper, Y)	09 05 15 00 10 00 19 01 11	2 2 2 3 3 3 2 2	✓✓
<b>PHA</b> Push accumulator on stack	A ↓	Implied		48	1	
<b>PHP</b> Push processor status on stack	P ↓	Implied		08	1	
<b>PLA</b> Pull accumulator from stack	A ↑	Implied		68	1	✓✓
<b>PLP</b> Pull processor status from stack	P ↑	Implied		28	1	From Stack
<b>ROL</b> Rotate one bit left (memory or accumulator)	(See Figure 2)	Accumulator Zero Page Zero Page, X Absolute Absolute X	ROL A ROL Oper ROL Oper, X ROL Oper, X ROL Oper, X	2A 26 36 2E 3E	1 2 2 3 3	✓✓✓
<b>ROR</b> Rotate one bit right (memory or accumulator)	(See Figure 3)	Accumulator Zero Page Zero Page, X Absolute Absolute X	ROR A ROR Oper ROR Oper, X ROR Oper, X ROR Oper, X	6A 66 76 6E 7E	1 2 2 3 3	✓✓✓

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HEX OPERATION CODES

00 - BRK	01 - ORA - Indirect, X	2F - NOP	5E - LSR - Absolute, X
01 - ORA - Indirect, X	02 - NOP	30 - BMI	5F - NOP
02 - NOP	03 - AND - Indirect, Y	31 - AND - Indirect, Y	60 - RTS
03 - AND - Indirect, Y	04 - NOP	32 - NOP	61 - ADC - Indirect, X
04 - NOP	05 - ORA - Zero Page	33 - NOP	62 - NOP
05 - ORA - Zero Page	06 - ASL - Zero Page	34 - NOP	63 - NOP
06 - ASL - Zero Page	07 - NOP	35 - AND - Zero Page, X	64 - NOP
07 - NOP	08 - PHP	36 - ROL - Zero Page, X	65 - ADC - Zero Page
08 - PHP	09 - ORA - Immediate	37 - NOP	66 - ROR - Zero Page
09 - ORA - Immediate	0A - ASL - Accumulator	38 - SEC	67 - NOP
0A - ASL - Accumulator	0B - NOP	39 - AND - Absolute, Y	68 - PLA
0B - NOP	0C - NOP	3A - AND - Absolute, Y	69 - ADC - Immediate
0C - NOP	0D - ORA - Absolute	3B - NOP	6A - ROR - Accumulator
0D - ORA - Absolute	0E - ASL - Absolute	3C - NOP	6B - NOP
0E - ASL - Absolute	0F - NOP	3D - AND - Absolute, X	6C - JMP - Indirect
0F - NOP	10 - BPL	3E - ROL - Absolute, X	6D - ADC - Absolute
10 - BPL	11 - ORA - Indirect, Y	3F - NOP	6E - ROR - Absolute
11 - ORA - Indirect, Y	12 - NOP	40 - RTI	6F - NOP
12 - NOP	13 - NOP	41 - EOR - Indirect, X	70 - BVS
13 - NOP	14 - NOP	42 - NOP	71 - ADC - Indirect, Y
14 - NOP	15 - ORA - Zero Page, X	43 - NOP	72 - NOP
15 - ORA - Zero Page, X	16 - ASL - Zero Page, X	44 - NOP	73 - NOP
16 - ASL - Zero Page, X	17 - NOP	45 - EOR - Zero Page	74 - NOP
17 - NOP	18 - CLC	46 - LSR - Zero Page	75 - ADC - Zero Page, X
18 - CLC	19 - ORA - Absolute, Y	47 - NOP	76 - ROR - Zero Page, X
19 - ORA - Absolute, Y	1A - NOP	48 - PHA	77 - NOP
1A - NOP	1B - NOP	49 - EOR - Immediate	78 - SEI
1B - NOP	1C - NOP	4A - LSR - Accumulator	79 - ADC - Absolute, Y
1C - NOP	1D - ORA - Absolute, X	4B - NOP	7A - NOP
1D - ORA - Absolute, X	1E - ASL - Absolute, X	4C - JMP - Absolute	7B - NOP
1E - ASL - Absolute, X	1F - NOP	4D - EOR - Absolute	7C - NOP
1F - NOP	20 - JSR	4E - LSR - Absolute	7D - ADC - Absolute, X, NOP
20 - JSR	21 - AND - Indirect, X	4F - NOP	7E - ROR - Absolute, X, NOP
21 - AND - Indirect, X	22 - NOP	50 - BVC	7F - NOP
22 - NOP	23 - NOP	51 - EOR Indirect, Y	80 - NOP
23 - NOP	24 - BIT - Zero Page	52 - NOP	81 - STA - Indirect, X
24 - BIT - Zero Page	25 - AND - Zero Page	53 - NOP	82 - NOP
25 - AND - Zero Page	26 - ROL - Zero Page	54 - NOP	83 - NOP
26 - ROL - Zero Page	27 - NOP	55 - EOR - Zero Page, X	84 - STY - Zero Page
27 - NOP	28 - PLP	56 - LSR - Zero Page, X	85 - STA - Zero Page
28 - PLP	29 - AND - Immediate	57 - NOP	86 - STX - Zero Page
29 - AND - Immediate	2A - ROL - Accumulator	58 - CLI	87 - NOP
2A - ROL - Accumulator	2B - NOP	59 - EOR - Absolute, Y	88 - DEY
2B - NOP	2C - BIT - Absolute	5A - NOP	89 - NOP
2C - BIT - Absolute	2D - AND - Absolute	5B - NOP	8A - TXA
2D - AND - Absolute	2E - ROL - Absolute	5C - NOP	8B - NOP
2E - ROL - Absolute		5D - EOR - Absolute, X	8C - STY - Absolute



Name Description	Operation	Addressing Mode	Assembly Language Form	HEX OP Code	Mem. Bytes	P. Status Reg. M Z C I V
TXA Transfer index X to accumulator	X → A	Implied	TXA	8A	1	✓✓-----
TXS Transfer index X to stack pointer	X → S	Implied	TXS	9A	1	-----
TYA Transfer index Y to accumulator	Y → A	Implied	TYA	80	1	✓✓-----

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8D - STA - Absolute	B4 - LDY - Zero Page. X	DB - NOP
8E - STX - Absolute	B5 - LDA - Zero Page. X	DC - NOP
8F - NOP	B6 - LDX - Zero Page. Y	DD - CMP - Absolute. X
90 - BCC	B7 - NOP	DE - DEC - Absolute. X
91 - STA - (Indirect). Y	B8 - CLV	DF - NOP
92 - NOP	B9 - LDA - Absolute. Y	E0 - CPX - Immediate
93 - NOP	BA - TSX	E1 - SBC - (Indirect. X)
94 - STY - Zero Page. X	BB - NOP	E2 - NOP
95 - STA - Zero Page. X	BC - LDY - Absolute. X	E3 - NOP
96 - STX - Zero Page. Y	BD - LDA - Absolute. X	E4 - CPX - Zero Page
97 - NOP	BE - LDX - Absolute. Y	E5 - SBC - Zero Page
98 - TYA	BF - NOP	E6 - INC - Zero Page
99 - STA - Absolute. Y	C0 - CPY - Immediate	E7 - NOP
9A - TXS	C1 - CMP - (Indirect. X)	E8 - INX
9B - NOP	C2 - NOP	E9 - SBC - Immediate
9C - NOP	C3 - NOP	EA - NOP
9D - STA - Absolute. X	C4 - CPY - Zero Page	EB - NOP
9E - NOP	C5 - CMP - Zero Page	EC - CPX - Absolute
9F - NOP	C6 - DEC - Zero Page	ED - SBC - Absolute
A0 - LDY - Immediate	C7 - NOP	EE - INC - Absolute
A1 - LDA - (Indirect. X)	C8 - INY	EF - NOP
A2 - LDX - Immediate	C9 - CMP - Immediate	F0 - BEQ
A3 - NOP	CA - DEX	F1 - SBC - (Indirect). Y
A4 - LDY - Zero Page	CB - NOP	F2 - NOP
A5 - LDA - Zero Page	CC - CPY - Absolute	F3 - NOP
A6 - LDX - Zero Page	CD - CMP - Absolute	F4 - NOP
A7 - NOP	CE - DEC - Absolute	F5 - SBC - Zero Page. X
A8 - TAY	CF - NOP	F6 - INC - Zero Page. X
A9 - LDA - Immediate	D0 - BNE	F7 - NOP
AA - TAX	D1 - CMP - (Indirect). Y	F8 - SED
AB - NOP	D2 - NOP	F9 - SBC - Absolute. Y
AC - LDY - Absolute	D3 - NOP	FA - NOP
AD - Absolute	D4 - NOP	FB - NOP
AE - LDX - Absolute	D5 - CMP - Zero Page. X	FC - NOP
AF - NOP	D6 - DEC - Zero Page. X	FD - SBC - Absolute. X
B0 - BCS	D7 - NOP	FE - INC - Absolute. X
B1 - LDA - (Indirect). Y	D8 - CLD	FF - NOP
B2 - NOP	D9 - CMP - Absolute. Y	
B3 - NOP	DA - NOP	

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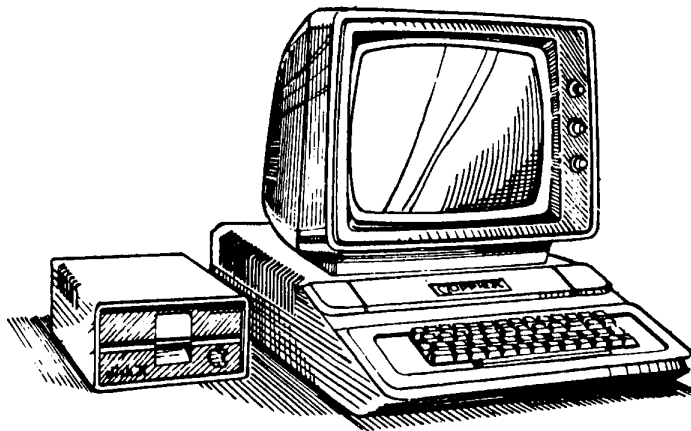


**Apple II Computer Technical Information**

**APPLE II / APPLE II-PLUS  
LEVEL II SERVICE REFERENCE MANUAL**

**Pre-Release Version**

**APPENDIX A  
ROM LISTING -- AUTOSTART MONITOR (1978)**



**Written by  
Apple Computer, Inc. • Level II Service Center  
1981**

( This page is not part of the original service manual )

# AUTOSTART ROM LISTING

```

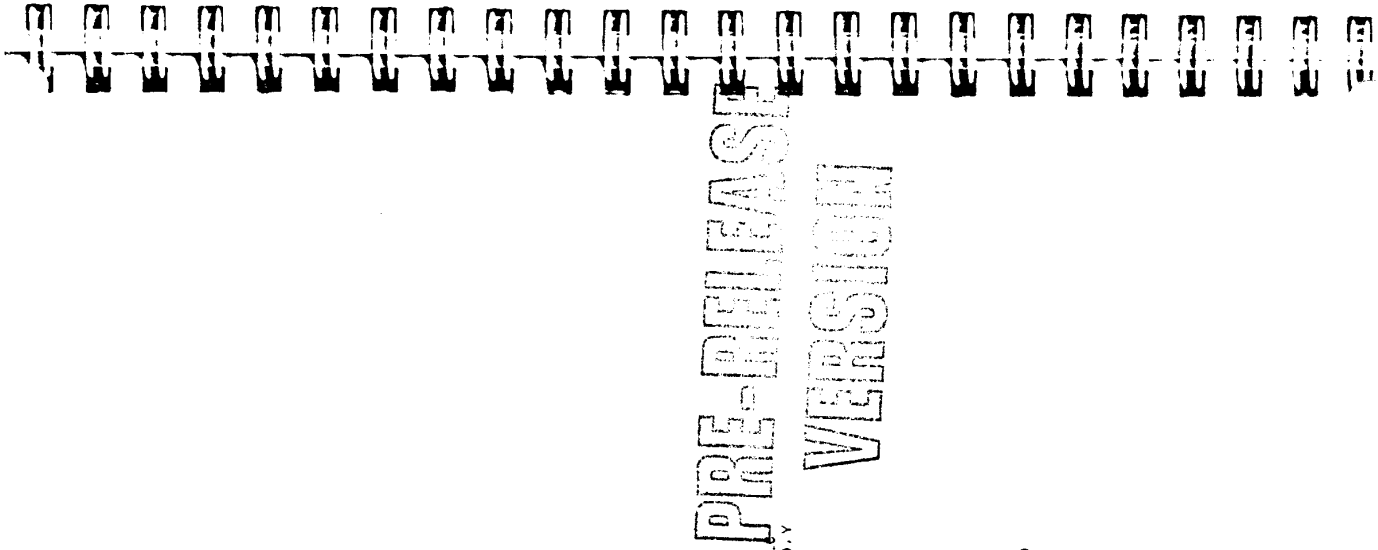
0000 2 *****
0000 3 *
0000 4 * APPLE II
0000 5 * MONITOR II
0000 6 *
0000 7 * COPYRIGHT 1978 BY
0000 8 * APPLE COMPUTER, INC.
0000 9 *
0000 10 * ALL RIGHTS RESERVED
0000 11 *
0000 12 * STEVE WOZNIAK
0000 13 *
0000 14 *****
0000 15 *
0000 16 * MODIFIED NOV 1978
0000 17 * BY JOHN A
0000 18 *
0000 19 *****
FB00 20 ORG $F800
FB00 21 OBJ $2000
FB00 22 *****
FB00 23 LOCO EQU $00
FB00 24 LOC1 EQU $01
FB00 25 WNDLFT EQU $20
FB00 26 WNDWDTH EQU $21
FB00 27 WNDTOP EQU $22
FB00 28 WNDBTM EQU $23
FB00 29 CH EQU $24
FB00 30 CV EQU $25
FB00 31 GBASL EQU $26
FB00 32 GBASH EQU $27
FB00 33 BASL EQU $28
FB00 34 BASH EQU $29
FB00 35 BAS2L EQU $2A
FB00 36 BAS2H EQU $2B
FB00 37 H2 EQU $2C
FB00 38 LMNEM EQU $2C
FB00 39 V2 EQU $2D
FB00 40 RMNEM EQU $2D
FB00 41 MASK EQU $2E
FB00 42 CHKSUM EQU $2E
FB00 43 FORMAT EQU $2E
FB00 44 LASTIN EQU $2F
FB00 45 LENGTH EQU $2F
FB00 46 SIGN EQU $2F
FB00 47 COLOR EQU $30
FB00 48 MODE EQU $31
FB00 49 INVFLG EQU $32
FB00 50 PROMPT EQU $33
FB00 51 YSAV EQU $34
FB00 52 YSAV1 EQU $35
FB00 53 CSWL EQU $36
FB00 54 CSWH EQU $37
FB00 55 KSWL EQU $38
FB00 56 KSWH EQU $39
FB00 57 PCL EQU $3A
FB00 58 PCH EQU $3B
FB00 59 A1L EQU $3C
FB00 60 A1H EQU $3D
FB00 61 A2L EQU $3E
FB00 62 A2H EQU $3F
FB00 63 A3L EQU $40
FB00 64 A3H EQU $41
FB00 65 A4L EQU $42
FB00 66 A4H EQU $43
FB00 67 A5L EQU $44
FB00 68 ASH EQU $45
    
```

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```

FB00 69 ACC EQU $45 ; NOTE OVERLAP WITH A5H!
FB00 70 XREG EQU $46
FB00 71 YREG EQU $47
FB00 72 STATUS EQU $48
FB00 73 SPNT EQU $49
FB00 74 RNDL EQU $4E
FB00 75 RNDH EQU $4F
FB00 76 PICK EQU $95
FB00 77 IN EQU $0200
FB00 78 BRKV EQU $3F0 ; NEW VECTOR FOR BRK
FB00 79 SOFTEV EQU $3F2 ; VECTOR FOR WARM START
FB00 80 PWREDUP EQU $3F4 ; THIS MUST = EOR $6A5 OF SOFTEV+1
FB00 81 AMPERV EQU $3F5 ; APPLESOFT & EXIT VECTOR
FB00 82 USGRADR EQU $03FB
FB00 83 NMI EQU $03FB
FB00 84 IRQLOC EQU $3FE
FB00 85 LINE1 EQU $400
FB00 86 MSLOT EQU $07FB
FB00 87 IOADR EQU $C000
FB00 88 KBD EQU $C000
FB00 89 KBDSTRB EQU $C010
FB00 90 TAPEOUT EQU $C020
FB00 91 SPKR EQU $C030
FB00 92 TXTCLR EQU $C050
FB00 93 TXTSET EQU $C051
FB00 94 MIXCLR EQU $C052
FB00 95 MIXSET EQU $C053
FB00 96 LOWSCR EQU $C054
FB00 97 HISCR EQU $C055
FB00 98 LORES EQU $C056
FB00 99 HIRES EQU $C057
FB00 100 SETAN0 EQU $C058
FB00 101 CLRAN0 EQU $C059
FB00 102 SETAN1 EQU $C05A
FB00 103 CLRAN1 EQU $C05B
FB00 104 SETAN2 EQU $C05C
FB00 105 CLRAN2 EQU $C05D
FB00 106 SETAN3 EQU $C05E
FB00 107 CLRAN3 EQU $C05F
FB00 108 TAPEIN EQU $C060
FB00 109 PADDLO EQU $C064
FB00 110 PTRIG EQU $C070
FB00 111 CLRROM EQU $CFFF
FB00 112 BASIC EQU $E000
FB00 113 BASIC2 EQU $E003
FB00 114 PAGE
FB00 4A 115 PLOT LSR A
FB01 0B 116 PHP
FB02 20 47 FB 117 JSR GBASCALC
FB05 28 118 PLP
FB06 A9 0F 119 LDA ##OF
FB0B 90 02 120 BCC RTMASK
FB0A 69 E0 121 ADC ##E0
FB0C B5 2E 122 RTMASK STA MASK
FB0E B1 26 123 PLOT1 LDA (GBASL),Y
FB10 45 30 124 EOR COLOR
FB12 25 2E 125 AND MASK
FB14 51 26 126 EOR (GBASL),Y
FB16 91 26 127 STA (GBASL),Y
FB1B 60 128 RTS
FB19 20 00 FB 129 HLINE JSR PLOT
FB1C C4 2C 130 HLINE1 CPY H2
FB1E B0 11 131 BCS RTS1
FB20 C8 132 INY
FB21 20 0E FB 133 JSR PLOT1
FB24 90 F6 134 BCC HLINE1
FB26 E9 01 135 VLINEZ ADC ##01
FB2B 48 136 VLINE PHA
FB29 20 00 FB 137 JSR PLOT
FB2C 68 138 PLA
FB2D C5 2D 139 CMP V2
FB2F 90 F5 140 BCC VLINEZ
FB31 60 141 RTS1 RTS
    
```



F832	A0 2F	142 CLRSCR	LDY #52F
F834	D0 0C	143 BNE CLRSC2	
F836	A0 27	144 CLRTPU	LDY #527
F838	B4 2U	145 CLRSC2	STY V2
F83A	A0 27	146 LDY #527	
F83C	A9 00	147 CLRSC3	LDA #500
F83E	B5 30	148 STA COLOR	
F840	20 28 FB	149 JSR VLINE	
F843	BB	150 DEY	
F844	10 F6	151 BPL CLRSC3	
F846	60	152 RTS	
F847	48	153 PAGE	
F848	4A	154 GBASCALC PHA	
F849	29 03	155 LSR A	
F84B	C9 04	156 AND #503	
F84D	65 27	157 ORA #504	
F84F	56	158 STA GBASH	
F850	29 18	159 PLR	
F852	9C 02	160 AND #518	
F854	65 7F	161 BCC GBALC	
F856	B5 25	162 ADC #57F	
F858	0A	163 GBALC	STA GBASL
F859	0A	164 ASL A	
F85A	05 26	165 ORA GBASL	
F85C	85 26	166 STA GBASL	
F85E	60	167 RTS	
F85F	A5 30	168 LDA COLOR	
F861	18	169 CLC	
F862	49 03	170 ADC #503	
F864	29 0F	171 AND #50F	
F866	65 30	172 SETCOL	STA COLOR
F868	0A	173 ASL A	
F869	0A	174 ASL A	
F86A	0A	175 ASL A	
F86B	0A	176 ASL A	
F86C	05 30	177 ORA COLOR	
F86E	B5 30	178 STA COLOR	
F870	60	179 RTS	
F871	4A	180 LSR A	
F872	06	181 PHP	
F873	20 47 FB	182 JSR GBASCALC	LDY #500
F874	01 26	183 LDA (GBASL),Y	
F878	2B	184 PLP	
F879	50 04	185 BCC RTHSKZ	
F87B	4A	186 LSR A	
F87C	4A	187 LSR A	
F87D	4A	188 LSR A	
F87E	4A	189 LSR A	
F87F	29 0F	190 RTHSKZ	AND #50F
F881	60	191 RTS	
F882	As 3A	192 PAGE	
F884	A4 3B	193 INSDS1	LDX PCL
F886	20 96 FD	194 LDY PCH	
F889	20 48 F9	195 JSR PRYX2	
F88C	A1 3A	196 JSR PRBLNK	
F88E	AB	197 LDA (PCL,X)	
F890	4A	198 INSDS2	TAY
F892	90 09	199 LSR A	
F893	6A	200 BCC IEVEN	
F895	80 10	201 ROR A	
F897	F0 0C	202 RCS ERR	
F899	29 B7	203 CMP #A2	
F89B	4A	204 BEQ ERR	
F89C	AA	205 AND #B7	
F89D	DD 62 F9	206 LSR A	
F89E	20 79 FB	207 TAX	
F8A3	00 04	208 LDA FMT1,X	
F8A5	A0 60	209 JSR SCRNI	
F8A7	A9 00	210 BNE GETFTT	
F8A9	AA	211 LDY #580	
F8AB	AA	212 ERK	
F8AC	AA	213 LDA #500	
F8AD	AA	214 GETFTT	TAX

F8AA	BD A6 F9	215	LDY #503
F8AB	65 2E	216	STA FMT2,X
F8AF	59 03	217	AND #503
F8B1	85 2F	218	STA LENGTH
F8B3	98	219	TVA
F8B4	25 BF	220	AND #5BF
F8B6	AA	221	TAX
F8B7	9B	222	TVA
F8B8	A0 03	223	LDY #503
F8BA	E0 8A	224	CPX #5BA
F8BC	F0 0B	225	BEG MNNDX3
F8BE	94	226	LSR A
F8BF	90 0B	227	BCC MNNDX3
F8C1	4A	228	LSR A
F8C2	4A	229 MNNDX2	LSR A
F8C3	09 20	230	DRA #520
F8C5	86	231	DEV
F8C6	00 FA	232	BNE MNNDX2
F8C8	CB	233	INY
F8C9	BB	234 MNNDX3	DEV
F8CA	D0 F2	235	BNE MNNDX1
F8CC	60	236	RTS
F8CD	FF FF FF	237	DFB \$FF,\$FF,\$FF
F8DD	20 82 FB	238	PAGE
F8DE	48	239 INSDS1	JSR INSDS1
F8E3	48	240 PHA	
F8E4	51 3A	241 PRNTP	LDA (PCL),Y
F8E6	20 DA FD	242 JSR PRBYTE	
F8E9	A2 01	243	LDX #501
F8EB	20 4A F9	244 PRNTBL	JSR PRBL2
F8EE	C4 2F	245	CPY LENGTH
F8F0	CB	246	INY
F8F1	90 F1	247	BCC PRNTP
F8F3	A2 03	248	LDX #503
F8F5	C0 04	249	CPY #504
F8F7	90 F2	250	BCC PRNTBL
F8F9	68	251	PLA
F8FA	39 C0 F9	252	TAY
F8FB	85 2C	253	LDA MNEML,Y
F8FC	D9 00 FA	254	STA LNEM
F8FD	85 20	255	LDA MNEML,Y
F8FE	A9 00	256	STA RNEM
F8FF	A0 05	257	LDY #505
F8F9	06 2D	258	LDY #505
F8FB	26 2C	259	ASL RNEM
F8FD	2A	260	ROL LNEM
F8FE	86	261	ROL A
F8FF	00 FB	262	DEY
F901	69 BF	263	BNE PRM2
F903	20 ED FD	264	ADC #5BF
F906	CA	265	JSR COUT
F907	D0 EC	266	DEX
F909	20 4B F9	267	BNE NXTCOL
F90C	A4 2F	268	JSR PRBLNK
F90E	A2 06	269	LDY LENGTH
F910	E0 03	270	LDX #506
F912	F0 1C	271	CPX #503
F914	06 2E	272	BEG PRADR5
F916	8D B3 F9	273	ASL FMTAT
F918	20 ED FD	274	BCC PRADR3
F91E	DD 09 F9	275	LDA CHAR1-1,X
F921	F0 03	276	JSR COUT
F923	20 ED FD	277	LDA CHAR2-1,X
F925	CA	278	BEG PRADR3
F927	D0 E7	279	JSR COUT
F929	60	280	DEX
F92A	8B	281	BNE PRADR1
F92B	30 E7	282	RTS
F92D	20 DA FD	283	PRADR4
F92E	A5 2E	284	DM1 PRADR2
F932	C9 EB	285	JSR PRBYTE
F933	C9 EB	286	LDA FMTAT
F934	C9 EB	287	CMP #5EB

F98F CB	341	DFB \$CB
F990 44	342	DFB \$A9
F991 A9	343	DFB \$01
F992 01	344	DFB \$22
F993 22	345	DFB \$44
F994 44	346	DFB \$33
F995 33	347	DFB \$0D
F996 0D	348	DFB \$04
F997 04	370	DFB \$90
F998 04	371	DFB \$01
F999 90	372	DFB \$22
F99A 01	373	DFB \$44
F99B 22	374	DFB \$33
F99C 44	375	DFB \$0D
F99D 33	376	DFB \$04
F99E 0D	377	DFB \$90
F99F 04	378	DFB \$01
F9A0 04	379	DFB \$22
F9A1 90	380	DFB \$44
F9A2 22	381	DFB \$33
F9A3 44	382	DFB \$0D
F9A4 0D	383	DFB \$04
F9A5 9A	384	DFB \$9A
F9A6 00	385	DFB \$21
F9A7 21	386	DFB \$81
F9A8 81	387	DFB \$82
F9A9 82	388	DFB \$00
F9AA 00	389	DFB \$00
F9AB 00	390	DFB \$39
F9AC 59	391	DFB \$4D
F9AD 4D	392	DFB \$91
F9AE 91	393	DFB \$92
F9AF 92	394	DFB \$86
F9B0 6A	395	DFB \$A4
F9B1 4A	396	DFB \$85
F9B2 85	397	DFB \$9D
F9B3 9D	398	DFB \$AC
F9B4 AC	399	DFB \$AC
F9B5 49	400	DFB \$AC
F9B6 AC	401	DFB \$A3
F9B7 A3	402	DFB \$AB
F9B8 AB	403	DFB \$A4
F9B9 A4	404	DFB \$D9
F9BA D9	405	DFB \$00
F9BB 00	406	DFB \$DB
F9BC DB	407	DFB \$A4
F9BD A4	408	DFB \$A4
F9BE A4	409	DFB \$00
F9BF 00	410	DFB \$1C
F9C0 1C	411	DFB \$8A
F9C1 8A	412	DFB \$1C
F9C2 1C	413	DFB \$23
F9C3 23	414	DFB \$5D
F9C4 5D	415	DFB \$8D
F9C5 8D	416	DFB \$1B
F9C6 1B	417	DFB \$A1
F9C7 A1	418	DFB \$9D
F9C8 9D	419	DFB \$8A
F9C9 8A	420	DFB \$1D
F9CA 1D	421	DFB \$23
F9CB 23	422	DFB \$9D
F9CC 9D	423	DFB \$8B
F9CD 8B	424	DFB \$1D
F9CE 1D	425	DFB \$A1
F9CF A1	426	DFB \$00
F9D0 00	427	DFB \$29
F9D1 29	428	DFB \$19
F9D2 19	429	DFB \$AE
F9D3 AE	430	DFB \$69
F9D4 69	431	DFB \$A8
F9D5 A8	432	DFB \$19
F9D6 19	433	DFB \$23
F9D7 23		

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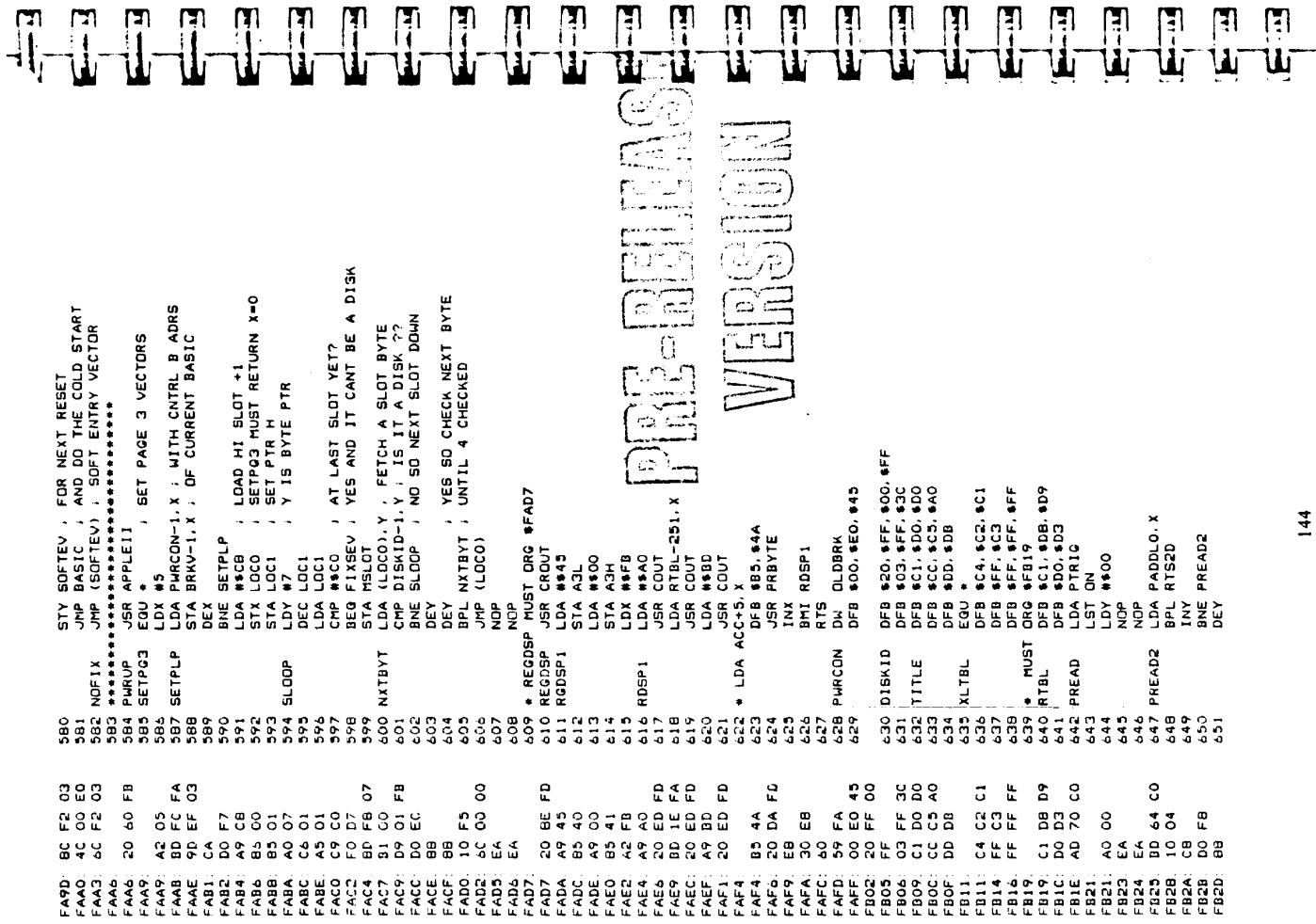
F93A B1 3A	288	LDA (PCL)Y
F93B 90 F2	289	BCC PADR4
F93C 20 56 F9	290	PAGE PCADJ3
F93D 6A	291	JSR PCADJ3
F93E EB	292	TAX
F93F 00 01	293	INX
F940 9E	294	DNE PRNTX
F941 20 DA FD	295	INX
F942 BA	296	PRNTX
F943 4C DA FD	297	JSR PRBYTE
F944 A2 03	298	TXA
F945 A9 A0	299	TXA
F946 20 ED FD	300	JMP PRBYTE
F947 CA	301	LDX #03
F948 60	302	LDA #A0
F949 20	303	JSR COUT
F94A 00	304	DEX
F94B 00	305	BNE PRBL2
F94C 00	306	RTS
F94D 00	307	SEC
F94E 00	308	PCADJ
F94F 00	309	LDA LENGTH
F950 00	310	LDY PCH
F951 00	311	TAX
F952 00	312	BPL PCADJ4
F953 00	313	DEY
F954 00	314	ADC PCL
F955 00	315	BCC RT52
F956 00	316	INX
F957 00	317	RTS
F958 00	318	FMT1
F959 00	319	DFB \$04
F95A 00	320	DFB \$20
F95B 00	321	DFB \$54
F95C 00	322	DFB \$80
F95D 00	323	DFB \$04
F95E 00	324	DFB \$90
F95F 00	325	DFB \$22
F960 00	326	DFB \$54
F961 00	327	DFB \$80
F962 00	328	DFB \$04
F963 00	329	DFB \$90
F964 00	330	DFB \$20
F965 00	331	DFB \$54
F966 00	332	DFB \$80
F967 00	333	DFB \$04
F968 00	334	DFB \$90
F969 00	335	DFB \$20
F96A 00	336	DFB \$54
F96B 00	337	DFB \$80
F96C 00	338	DFB \$04
F96D 00	339	DFB \$90
F96E 00	340	DFB \$20
F96F 00	341	DFB \$54
F970 00	342	DFB \$80
F971 00	343	DFB \$04
F972 00	344	DFB \$90
F973 00	345	DFB \$20
F974 00	346	DFB \$54
F975 00	347	DFB \$80
F976 00	348	DFB \$04
F977 00	349	DFB \$90
F978 00	350	DFB \$20
F979 00	351	DFB \$54
F97A 00	352	DFB \$80
F97B 00	353	DFB \$04
F97C 00	354	DFB \$90
F97D 00	355	DFB \$20
F97E 00	356	DFB \$54
F97F 00	357	DFB \$80
F980 00	358	DFB \$04
F981 00	359	DFB \$90
F982 00	360	DFB \$20
F983 00	361	DFB \$54
F984 00	362	DFB \$80
F985 00	363	DFB \$04
F986 00	364	DFB \$90
F987 00	365	DFB \$20
F988 00	366	DFB \$54
F989 00	367	DFB \$80
F98A 00	368	DFB \$04
F98B 00	369	DFB \$90
F98C 00	370	DFB \$20
F98D 00	371	DFB \$54
F98E 00	372	DFB \$80
F98F 00	373	DFB \$04
F990 00	374	DFB \$90
F991 00	375	DFB \$20
F992 00	376	DFB \$54
F993 00	377	DFB \$80
F994 00	378	DFB \$04
F995 00	379	DFB \$90
F996 00	380	DFB \$20
F997 00	381	DFB \$54
F998 00	382	DFB \$80
F999 00	383	DFB \$04
F99A 00	384	DFB \$90
F99B 00	385	DFB \$20
F99C 00	386	DFB \$54
F99D 00	387	DFB \$80
F99E 00	388	DFB \$04
F99F 00	389	DFB \$90
F9A0 00	390	DFB \$20
F9A1 00	391	DFB \$54
F9A2 00	392	DFB \$80
F9A3 00	393	DFB \$04
F9A4 00	394	DFB \$90
F9A5 00	395	DFB \$20
F9A6 00	396	DFB \$54
F9A7 00	397	DFB \$80
F9A8 00	398	DFB \$04
F9A9 00	399	DFB \$90
F9AA 00	400	DFB \$20
F9AB 00	401	DFB \$54
F9AC 00	402	DFB \$80
F9AD 00	403	DFB \$04
F9AE 00	404	DFB \$90
F9AF 00	405	DFB \$20
F9B0 00	406	DFB \$54
F9B1 00	407	DFB \$80
F9B2 00	408	DFB \$04
F9B3 00	409	DFB \$90
F9B4 00	410	DFB \$20
F9B5 00	411	DFB \$54
F9B6 00	412	DFB \$80
F9B7 00	413	DFB \$04
F9B8 00	414	DFB \$90
F9B9 00	415	DFB \$20
F9BA 00	416	DFB \$54
F9BB 00	417	DFB \$80
F9BC 00	418	DFB \$04
F9BD 00	419	DFB \$90
F9BE 00	420	DFB \$20
F9BF 00	421	DFB \$54
F9C0 00	422	DFB \$80
F9C1 00	423	DFB \$04
F9C2 00	424	DFB \$90
F9C3 00	425	DFB \$20
F9C4 00	426	DFB \$54
F9C5 00	427	DFB \$80
F9C6 00	428	DFB \$04
F9C7 00	429	DFB \$90
F9C8 00	430	DFB \$20
F9C9 00	431	DFB \$54
F9CA 00	432	DFB \$80
F9CB 00	433	DFB \$04
F9CC 00	434	DFB \$90
F9CD 00	435	DFB \$20
F9CE 00	436	DFB \$54
F9CF 00	437	DFB \$80
F9D0 00	438	DFB \$04
F9D1 00	439	DFB \$90
F9D2 00	440	DFB \$20
F9D3 00	441	DFB \$54
F9D4 00	442	DFB \$80
F9D5 00	443	DFB \$04
F9D6 00	444	DFB \$90
F9D7 00	445	DFB \$20
F9D8 00	446	DFB \$54
F9D9 00	447	DFB \$80
F9DA 00	448	DFB \$04
F9DB 00	449	DFB \$90
F9DC 00	450	DFB \$20
F9DD 00	451	DFB \$54
F9DE 00	452	DFB \$80
F9DF 00	453	DFB \$04
F9E0 00	454	DFB \$90
F9E1 00	455	DFB \$20
F9E2 00	456	DFB \$54
F9E3 00	457	DFB \$80
F9E4 00	458	DFB \$04
F9E5 00	459	DFB \$90
F9E6 00	460	DFB \$20
F9E7 00	461	DFB \$54
F9E8 00	462	DFB \$80
F9E9 00	463	DFB \$04
F9EA 00	464	DFB \$90
F9EB 00	465	DFB \$20
F9EC 00	466	DFB \$54
F9ED 00	467	DFB \$80
F9EE 00	468	DFB \$04
F9EF 00	469	DFB \$90
F9F0 00	470	DFB \$20
F9F1 00	471	DFB \$54
F9F2 00	472	DFB \$80
F9F3 00	473	DFB \$04
F9F4 00	474	DFB \$90
F9F5 00	475	DFB \$20
F9F6 00	476	DFB \$54
F9F7 00	477	DFB \$80
F9F8 00	478	DFB \$04
F9F9 00	479	DFB \$90
F9FA 00	480	DFB \$20
F9FB 00	481	DFB \$54
F9FC 00	482	DFB \$80
F9FD 00	483	DFB \$04
F9FE 00	484	DFB \$90
F9FF 00	485	DFB \$20

FA21	AA	507	DFB #AA
FA22	A2	508	DFB #A2
FA23	A2	509	DFB #A2
FA24	74	510	DFB #74
FA25	74	511	DFB #74
FA26	74	512	DFB #74
FA27	72	513	DFB #72
FA28	44	514	DFB #44
FA29	6B	515	DFB #6B
FA2A	B2	516	DFB #B2
FA2B	B2	517	DFB #B2
FA2C	B2	518	DFB #B2
FA2D	00	519	DFB #00
FA2E	00	520	DFB #00
FA2F	00	521	DFB #00
FA30	1A	522	DFB #1A
FA31	1A	523	DFB #1A
FA32	26	524	DFB #26
FA33	26	525	DFB #26
FA34	72	526	DFB #72
FA35	72	527	DFB #72
FA36	BB	528	DFB #BB
FA37	CB	529	DFB #CB
FA38	C4	530	DFB #C4
FA39	CA	531	DFB #CA
FA3A	26	532	DFB #26
FA3B	4B	533	DFB #4B
FA3C	44	534	DFB #44
FA3D	44	535	DFB #44
FA3E	A2	536	DFB #A2
FA3F	CB	537	DFB #CB
FA40	B5 45	538	PAGE
FA41	B5 45	539	STA ACC
FA42	6B	540	PLA
FA43	4B	541	PHA
FA44	0A	542	ASL A
FA45	0A	543	ASL A
FA46	0A	544	ASL A
FA47	30 03	545	BMI BREAK
FA48	6C FE 03	546	JMP (IRGLOC)
FA49	28	547	PLP
FA4A	28	548	JSR SAVI
FA4B	6B	549	PLA
FA4C	6B	550	STA PCL
FA4D	B5 3A	551	PLA
FA4E	B5 3B	552	STA PCH
FA4F	6C F0 03	553	JMP (BRKV) ; BRKV WRITTEN OVER BY DISK BOOT
FA50	20 82 FB	554	JSR INSDSI
FA51	20 DA FA	555	JSR RQDSP1
FA52	4C 65 FF	556	JMP MON ; DO THIS FIRST THIS TIME
FA53	DB	557	CLD
FA54	20 84 FE	558	JSR SETNORM
FA55	20 2F FD	559	JSR INIT
FA56	20 93 FE	560	JSR SETVID
FA57	20 89 FE	561	JSR SETKBD
FA58	AD 58 CO	562	LDA SETANO ; ANO = TTL HI
FA59	AD 5A CO	563	LDA SETANI ; ANI = TTL HI
FA5A	AD 5D CO	564	LDA CLRAN2 ; AN2 = TTL LO
FA5B	AD 5F CO	565	LDA CLRAN3 ; AN3 = TTL LO
FA5C	AD FF CF	566	LDA CLRARM ; TURN OFF EXTNSN ROM
FA5D	2C 10 CO	567	BIT KBDSTRB ; CLEAR KEYBOARD
FA5E	DB	568	CLD
FA5F	20 3A FF	569	JSR BELL ; CAUSES DELAY IF KEY BOUNCES
FA60	AD F3 03	570	LDA SDFTEV+1 ; ITS RESET HI
FA61	49 A3	571	FOR #A3 ; A FUNNY COMPLEMENT OF THE
FA62	49 A3	572	CMR PHREDUP ; PWR UP BYTE ???
FA63	DD F4 03	573	BNE PHRUP ; NO SD PHRUP
FA64	DD F4 03	574	LDA SDFTEV ; YES SEE IF COLD START
FA65	DD 0F	575	BNE NDEIX ; HAS BEEN DONE YET?
FA66	DD 0F	576	LDA #00 ; ??
FA67	A9 E0	577	CMR SDFTEV+1 ; ??
FA68	CD F3 03	578	BNE NDFIX ; YES SO REENTER SYSTEM
FA69	DD 0B	579	LDA #3 ; NO SO POINT AT WARM START
FA6A	AD 03		DFB #A0

F9D8	24	434	DFB #24
F9D9	53	435	DFB #53
F9DA	1B	436	DFB #1B
F9DB	23	437	DFB #23
F9DC	24	438	DFB #24
F9DD	53	439	DFB #53
F9DE	19	440	DFB #19
F9DF	A1	441	DFB #A1
F9E0	00	442	DFB #00
F9E1	1A	443	DFB #1A
F9E2	5B	444	DFB #5B
F9E3	5B	445	DFB #5B
F9E4	A5	446	DFB #A5
F9E5	69	447	DFB #69
F9E6	24	448	DFB #24
F9E7	24	449	DFB #24
F9E8	AE	450	DFB #AE
F9E9	AE	451	DFB #AE
F9EA	AB	452	DFB #AB
F9EB	AD	453	DFB #AD
F9EC	29	454	DFB #29
F9ED	00	455	DFB #00
F9EE	7C	456	DFB #7C
F9EF	00	457	DFB #00
F9F0	15	458	DFB #15
F9F1	9C	459	DFB #9C
F9F2	6D	460	DFB #6D
F9F3	9C	461	DFB #9C
F9F4	A5	462	DFB #A5
F9F5	A5	463	DFB #A5
F9F6	29	464	DFB #29
F9F7	53	465	DFB #53
F9F8	B4	466	DFB #B4
F9F9	13	467	DFB #13
F9FA	34	468	DFB #34
F9FB	11	469	DFB #11
F9FC	A5	470	DFB #A5
F9FD	69	471	DFB #69
F9FE	23	472	DFB #23
F9FF	AO	473	DFB #AO
FA00	DB	474	DFB #DB
FA01	62	475	DFB #62
FA02	5A	476	DFB #5A
FA03	4B	477	DFB #4B
FA04	26	478	DFB #26
FA05	62	479	DFB #62
FA06	9A	480	DFB #9A
FA07	6C	481	DFB #6C
FA08	54	482	DFB #54
FA09	44	483	DFB #44
FA0A	CB	484	DFB #CB
FA0B	54	485	DFB #54
FA0C	6B	486	DFB #6B
FA0D	44	487	DFB #44
FA0E	EB	488	DFB #EB
FA0F	94	489	DFB #94
FA10	00	490	DFB #00
FA11	04	491	DFB #04
FA12	0B	492	DFB #0B
FA13	84	493	DFB #84
FA14	74	494	DFB #74
FA15	84	495	DFB #84
FA16	2B	496	DFB #2B
FA17	5E	497	DFB #5E
FA18	74	498	DFB #74
FA19	F4	499	DFB #F4
FA1A	CC	500	DFB #CC
FA1B	4A	501	DFB #4A
FA1C	72	502	DFB #72
FA1D	F2	503	DFB #F2
FA1E	A4	504	DFB #A4
FA1F	BA	505	DFB #BA
FA20	00	506	DFB #00

PRE-RELEASE  
VERSION

652	RTSQD	RTS	#S00	LDA	RTS
2	INIT	RTS	#S00	STA	STATUS
3		LDA	LDRES	LDA	LDRES
4		LDA	LDMSCR	LDA	LDMSCR
5	SETTXT	LDA	#S00	LDA	LDMSCR
6		REG	SETLND	REG	SETLND
7		LDA	TXTLR	LDA	TXTLR
8		LDA	MISET	LDA	MISET
9	SETOR	JSR	CLRTOP	JSR	CLRTOP
10		LDA	#S14	LDA	#S14
11		STA	WINDTP	STA	WINDTP
12	SETMND	LDA	#S00	LDA	#S00
13		STA	WINDLF	STA	WINDLF
14		LDA	#S2B	LDA	#S2B
15		STA	WINDWTH	STA	WINDWTH
16		LDA	#S18	LDA	#S18
17		STA	WINDBTH	STA	WINDBTH
18		LDA	#S17	LDA	#S17
19		STA	CV	STA	CV
20	TABV	JMP	VTAB	JMP	VTAB
21		JSR	HOME	JSR	HOME
22	APPLEII	LDA	#B	LDA	#B
23		LDA	#B	LDA	#B
24	STITLE	LDA	TITLE-1,Y	LDA	TITLE-1,Y
25		STA	LINE1-14,Y	STA	LINE1-14,Y
26		DEY	STITLE	DEY	STITLE
27		BNE	STITLE	BNE	STITLE
28		RTS		RTS	
29	SETPHRC	LDA	SOFTV+1	LDA	SOFTV+1
30		EDR	#A5	EDR	#A5
31		STA	PHREDUP	STA	PHREDUP
32		RTS		RTS	
33	VIDWAIT	EGU	*	EGU	*
34		CPY	#BD	CPY	#BD
35		BNE	NOWAIT	BNE	NOWAIT
36		LDA	KBD	LDA	KBD
37		BPL	NOWAIT	BPL	NOWAIT
38		CPY	#93	CPY	#93
39		BNE	NOWAIT	BNE	NOWAIT
40		BIT	KDSTRB	BIT	KDSTRB
41		LDA	KBD	LDA	KBD
42	KBDWAIT	BPL	KBDWAIT	BPL	KBDWAIT
43		CPY	#B3	CPY	#B3
44		BEG	NOWAIT	BEG	NOWAIT
45		BIT	KDSTRB	BIT	KDSTRB
46		JMP	VIDOUT	JMP	VIDOUT
47	NOWAIT	PAGE		PAGE	
48		JMP	ESC1	JMP	ESC1
49	ESCOLD	TAY		TAY	
50		LDA	XLTLB-SC9,Y	LDA	XLTLB-SC9,Y
51	ESCNDH	JSR	ESCOLD	JSR	ESCOLD
52		JSR	RKEY	JSR	RKEY
53		CPY	#CE	CPY	#CE
54	ESCNEW	BCS	ESCOLD	BCS	ESCOLD
55		CPY	#C9	CPY	#C9
56		BCC	ESCOLD	BCC	ESCOLD
57		CPY	#CC	CPY	#CC
58		BEG	ESCOLD	BEG	ESCOLD
59		BNE	ESCNDH	BNE	ESCNDH
60		NOP		NOP	
61		NOP		NOP	
62		NOP		NOP	
63		NOP		NOP	
64		NOP		NOP	
65		NOP		NOP	
66		NOP		NOP	
67		NOP		NOP	
68		NOP		NOP	
69		NOP		NOP	



580	FAD7	20	BE	FD	* REGDSP MUST ORG #FAD7
581	FAD8	20	BE	FD	* REGDSP MUST ORG #FAD7
582	FAD9	20	BE	FD	* REGDSP MUST ORG #FAD7
583	FADA	20	BE	FD	* REGDSP MUST ORG #FAD7
584	FADB	20	BE	FD	* REGDSP MUST ORG #FAD7
585	FADC	20	BE	FD	* REGDSP MUST ORG #FAD7
586	FADD	20	BE	FD	* REGDSP MUST ORG #FAD7
587	FAD E	20	BE	FD	* REGDSP MUST ORG #FAD7
588	FAD F	20	BE	FD	* REGDSP MUST ORG #FAD7
589	FAD G	20	BE	FD	* REGDSP MUST ORG #FAD7
590	FAD H	20	BE	FD	* REGDSP MUST ORG #FAD7
591	FAD I	20	BE	FD	* REGDSP MUST ORG #FAD7
592	FAD J	20	BE	FD	* REGDSP MUST ORG #FAD7
593	FAD K	20	BE	FD	* REGDSP MUST ORG #FAD7
594	FAD L	20	BE	FD	* REGDSP MUST ORG #FAD7
595	FAD M	20	BE	FD	* REGDSP MUST ORG #FAD7
596	FAD N	20	BE	FD	* REGDSP MUST ORG #FAD7
597	FAD O	20	BE	FD	* REGDSP MUST ORG #FAD7
598	FAD P	20	BE	FD	* REGDSP MUST ORG #FAD7
599	FAD Q	20	BE	FD	* REGDSP MUST ORG #FAD7
600	FAD R	20	BE	FD	* REGDSP MUST ORG #FAD7
601	FAD S	20	BE	FD	* REGDSP MUST ORG #FAD7
602	FAD T	20	BE	FD	* REGDSP MUST ORG #FAD7
603	FAD U	20	BE	FD	* REGDSP MUST ORG #FAD7
604	FAD V	20	BE	FD	* REGDSP MUST ORG #FAD7
605	FAD W	20	BE	FD	* REGDSP MUST ORG #FAD7
606	FAD X	20	BE	FD	* REGDSP MUST ORG #FAD7
607	FAD Y	20	BE	FD	* REGDSP MUST ORG #FAD7
608	FAD Z	20	BE	FD	* REGDSP MUST ORG #FAD7
609	FAD 0	20	BE	FD	* REGDSP MUST ORG #FAD7
610	FAD 1	20	BE	FD	* REGDSP MUST ORG #FAD7
611	FAD 2	20	BE	FD	* REGDSP MUST ORG #FAD7
612	FAD 3	20	BE	FD	* REGDSP MUST ORG #FAD7
613	FAD 4	20	BE	FD	* REGDSP MUST ORG #FAD7
614	FAD 5	20	BE	FD	* REGDSP MUST ORG #FAD7
615	FAD 6	20	BE	FD	* REGDSP MUST ORG #FAD7
616	FAD 7	20	BE	FD	* REGDSP MUST ORG #FAD7
617	FAD 8	20	BE	FD	* REGDSP MUST ORG #FAD7
618	FAD 9	20	BE	FD	* REGDSP MUST ORG #FAD7
619	FAD A	20	BE	FD	* REGDSP MUST ORG #FAD7
620	FAD B	20	BE	FD	* REGDSP MUST ORG #FAD7
621	FAD C	20	BE	FD	* REGDSP MUST ORG #FAD7
622	FAD D	20	BE	FD	* REGDSP MUST ORG #FAD7
623	FAD E	20	BE	FD	* REGDSP MUST ORG #FAD7
624	FAD F	20	BE	FD	* REGDSP MUST ORG #FAD7
625	FAD G	20	BE	FD	* REGDSP MUST ORG #FAD7
626	FAD H	20	BE	FD	* REGDSP MUST ORG #FAD7
627	FAD I	20	BE	FD	* REGDSP MUST ORG #FAD7
628	FAD J	20	BE	FD	* REGDSP MUST ORG #FAD7
629	FAD K	20	BE	FD	* REGDSP MUST ORG #FAD7
630	FAD L	20	BE	FD	* REGDSP MUST ORG #FAD7
631	FAD M	20	BE	FD	* REGDSP MUST ORG #FAD7
632	FAD N	20	BE	FD	* REGDSP MUST ORG #FAD7
633	FAD O	20	BE	FD	* REGDSP MUST ORG #FAD7
634	FAD P	20	BE	FD	* REGDSP MUST ORG #FAD7
635	FAD Q	20	BE	FD	* REGDSP MUST ORG #FAD7
636	FAD R	20	BE	FD	* REGDSP MUST ORG #FAD7
637	FAD S	20	BE	FD	* REGDSP MUST ORG #FAD7
638	FAD T	20	BE	FD	* REGDSP MUST ORG #FAD7
639	FAD U	20	BE	FD	* REGDSP MUST ORG #FAD7
640	FAD V	20	BE	FD	* REGDSP MUST ORG #FAD7
641	FAD W	20	BE	FD	* REGDSP MUST ORG #FAD7
642	FAD X	20	BE	FD	* REGDSP MUST ORG #FAD7
643	FAD Y	20	BE	FD	* REGDSP MUST ORG #FAD7
644	FAD Z	20	BE	FD	* REGDSP MUST ORG #FAD7
645	FAD 0	20	BE	FD	* REGDSP MUST ORG #FAD7
646	FAD 1	20	BE	FD	* REGDSP MUST ORG #FAD7
647	FAD 2	20	BE	FD	* REGDSP MUST ORG #FAD7
648	FAD 3	20	BE	FD	* REGDSP MUST ORG #FAD7
649	FAD 4	20	BE	FD	* REGDSP MUST ORG #FAD7
650	FAD 5	20	BE	FD	* REGDSP MUST ORG #FAD7
651	FAD 6	20	BE	FD	* REGDSP MUST ORG #FAD7

FBBC EA	70	NOP	FC2C	69	FD	143	ADC #BFD	ESC-E OR F CHECK
FBBD EA	71	NOP	FC2E	70	FC	144	BCC CLEOL	ELSE CLEAR TO END OF LINE
FBBE EA	72	NOP	FC40	70	E9	145	BNE RTS4	ELSE NOT F RETURN
FBCA EA	73	NOP	FC42	A4	24	146	LDY CH	ESC F 15 CLR TO END OF PAGE
FBCB EA	74	NOP	FC44	A5	23	147	LDA CV	
FBCD EA	75	NOP	FC46	48	24	148	PHA VTABZ	
FBC1 4B	76	* MUST ORG #BFC1	FC47	20	24	149	JSR CLEOLZ	
FBC2 4A	77	BASCALC PHA	FC4A	20	9E	150	LDY #B00	
FBC3 29 03	78	LSR A	FC4F	68		151	PLA	
FBC5 09 04	79	AND #B03	FC50	69	00	152	ADC #B00	
FBC7 85 29	80	ORA #B04	FC52	90	23	153	CMR HNDPTH	
FBC9 68	81	STA BASH	FC54	90	F0	154	BCC CLEOP1	
FBCA 29 1B	82	PLA	FC56	B0	CA	155	BCC VTAB	
FBCB 29 1B	83	AND #B1B	FC58	A5	22	156	LDA HNDTOP	
FBCD 90 02	84	BCC BASCLC2	FC5A	B5	25	157	STA CV	
FBCD 69 7F	85	ADC #B7F	FC5C	A0	00	158	LDY #B00	
FBD0 85 2B	86	BASCLC2 STA BASL	FC5E	B4	24	159	STY CH	
FBD2 0A	87	ASL A	FC60	F0	E4	160	BEG CLEOP1	
FBD3 0A 2B	88	ASL A	FC62	A9	00	161	PAGE	
FBD4 05 2B	89	ORA BASL	FC64	B5	24	162	LDA #B00	
FBD6 85 2B	90	STA BASL	FC66	E6	25	163	STA CH	
FBD8 60	91	RIS	FC68	A5	25	164	INC CV	
FBD9 C9 B7	92	CMR #B7	FC6A	C5	23	165	LDA CV	
FBD8 D0 12	93	BNE RTS2B	FC6C	C5	23	166	CMR HNDPTH	
FBD9 49 40	94	LDA #B40	FC6E	90	B6	167	BCC VTABZ	
FBD7 20 AB FC	95	JSR WAIT	FC70	A5	22	168	DEC CV	
FBE2 A9 0C	96	LDY #B0C	FC72	48		169	LDA HNDTOP	
FBE4 A9 0C	97	BELL2 LDA #B0C	FC73	20	24	170	PHA	
FBE6 20 AB FC	98	JSR WAIT	FC75	A5	28	171	JSR VTABZ	
FBE9 A9 0C	99	LDA SPAR	FC77	20	24	172	LDA BASL	
FBEA 20 AB FC	100	DEY	FC78	B5	2A	173	STA BASH	
FBE8 8B	101	BNE BELL2	FC7A	A5	29	174	LDA BASH	
FBE9 D0 F3	102	RIS	FC7C	B5	28	175	STA BASH	
FBEF 60	103	PAGE	FC7E	A4	21	176	LDY HNDPTH	
FBF0 A4 24	104	STORADV LDY CH	FC80	88		177	DEY	
FBF2 91 2B	105	ADVANCE INC CH	FC82	69	01	178	PLA	
FBF4 E6 24	106	LDA CH	FC84	C5	23	179	ADC #B01	
FBF5 A5 24	107	CMR HNDPTH	FC86	D0	0D	180	CMR HNDPTH	
FBF6 C5 21	108	BCC CR	FC88	48		181	BCC SCRL3	
FBF8 80 66	109	RIS	FC89	20	24	182	PHA	
FBF9 C9 A0	110	RIS3	FC8B	B1	2B	183	JSR VTABZ	
FBF0 60 EF	111	VIDDUT	FC8E	91	2A	184	LDA (BASL),Y	
FBF1 60 EF	112	CMR #B0	FC90	88		185	STA (BASL),Y	
FC01 AB	113	TAY	FC91	10	F9	186	DEY	
FC02 10 EC	114	BPL STORADV	FC93	30	E1	187	BPL SCRL2	
FC04 C9 BD	115	CMR #BD	FC95	A0	00	188	BMI SCRL1	
FC06 F0 5A	116	BEG CR	FC97	20	9E	189	LDY #B00	
FC08 C9 BA	117	CMR #BA	FC99	B0	B4	190	SCRL3	
FC0A F0 5A	118	BEG LF	FC9A	B0	B4	191	JSR CLEOLZ	
FC0C C9 BB	119	CMR #BB	FC9C	A4	24	192	LDY CH	
FC0E D0 C9	120	BNE BELL1	FC9E	A9	A0	193	CLEOLZ	
FC10 C6 24	121	DEC CH	FC9F	91	2B	194	LDA #B40	
FC12 10 EB	122	BPL RTS3	FC9D	C4	21	195	STA (BASL),Y	
FC14 A5 21	123	LDA HNDPTH	FC9E	C4	21	196	INY HNDPTH	
FC16 B5 24	124	STA CH	FC9F	90	F9	197	BCC CLEOLZ	
FC18 C6 24	125	DEC CH	FC97	60		198	RTS	
FC1A A5 22	126	LDA HNDTOP	FC98	2B		199	SEC	
FC1C C5 25	127	CMR CV	FC9A	E9	01	200	HAIT	
FC1E B0 08	128	BCC RTS4	FC9C	E9	01	201	HAIT	
FC20 C6 25	129	DEC CV	FC9E	D0	FC	202	HAIT3	
FC22 A5 25	130	STORADV	FC9F	E8	01	203	PLA	
FC24 65 20	131	CMR #B0	FC9D	50	F6	204	SBC #B01	
FC27 65 20	132	ADW HNDLFT	FC9E	50	F6	205	SBC #B01	
FC29 85 2B	133	STA BASL	FC9F	50	F6	206	BNE HAIT2	
FC2B 60	134	RIS	FC9D	50	F6	207	RTS	
FC2C 49 C0	135	ESC #7	FC9E	50	F6	208	NXTA4	
FC2E F0 2B	136	BEG HOME	FC9F	50	F6	209	INC NXTA1	
FC30 69 FD	137	ADC #BFD	FC9D	50	F6	210	INC A4H	
FC32 90 C0	138	BCC ADVANCE	FC9E	50	F6	211	LDL A4L	
FC34 69 DA	139	BEG B5	FC9F	50	F6	212	CMR A2L	
FC36 69 FD	140	ADVANCE	FC9D	50	F6	213	LDA A4H	
FC38 69 FD	141	ESC-C OR D CHECK	FC9E	50	F6	214	SBC A4H	
FC3A F0 DE	142	BEG UP	FC9F	50	F6	215	INC A4L	

PRE-RELEASE  
VERSION

ESC # 7  
IF B0 DO HOME AND CLEAR  
ESC-A OR B CHECK  
A ADVANCE  
B BACKSPACE  
ESC-C OR D CHECK  
C DOWN  
D GO UP



PRE-RELEASE  
 VERSION

FC4:	DO 02	BNE RTS4B	LDA IN, X
FC6:	E6 3D	INC A1H	CHP #6B
FC8:	60	RTS	BEG BCKSPC
FC9:		PAGE	CHP #9B
FC9:	A0 4B	LDY #4B	BEG CANCEL
FCB:	20 0B FC	JSR ZERDLY	CPX #8FB
CC2:		BNE HEADR	BCC NOTCR1
CC2:		ADC #8FE	JSR BELL
CC2:	B0 F5	BDS HEADR	BNE NATCHAR
CC2:	A0 21	LDY #21	LDA #8DC
CC4:	20 0B FC	JSR ZERDLY	JSR COUT
CC9:	08	INV	301 GETLNZ
CCB:	08	INV	302 GETLN
CCB:	08	DEV	JSR COUT
CCB:	08	BNE ZERDLY	304 LDX #601
CCB:	08	BCC WRTAPE	TXA
CCB:	08	LDY #32	BEG GETLNZ
CCB:	08	DEV	DEX
CCB:	08	BNE ONEDLY	JSR RDCHAR
CCB:	08	LDY TAPEUT	CHP #95
CCB:	08	LDY #2C	LDA (BASL),Y
CCB:	08	RTS	BCC ADDINP
CCB:	08	PHX	AND #8DF
CCB:	08	PLA	STA IN, X
CCB:	08	ROL	CHP #8B
CCB:	08	LDY #3A	BNE NOTCR
CCB:	08	DEX	JSR CLREDL
CCB:	08	BNE RDBYT2	LDA #8B
CCB:	08	RTS	BNE COUT
CCB:	08	JSR RDBIT	LDY A1H
CCB:	08	DEV	LDX A1L
CCB:	08	LDY TAPEIN	JSR CRQUT
CCB:	08	BPL RDBIT	JSR PRINTX
CCB:	08	EOR LASTIN	LDY #00
CCB:	08	EOR LASTIN	LDA #8A
CCB:	08	STA LASTIN	LDA #8A
CCB:	08	CPY #80	JMP COUT
CCB:	08	RTS	PAGE
CCB:	08	LDY CH	LDA A1L
CCB:	08	LDA (BASL),Y	ORA #07
CCB:	08	PHA	STA A2L
CCB:	08	AND #3F	LDA A1H
CCB:	08	ORA #40	LDA A1H
CCB:	08	STA (BASL),Y	STA A2H
CCB:	08	PLA	LDA A1L
CCB:	08	JMP (KSHL)	AND #07
CCB:	08	INC RNDL	BNE DATAUT
CCB:	08	BNE KEYIN2	JSR PRAI
CCB:	08	INC RNDH	LDA #8A
CCB:	08	BIT KBD	LDA (A1L),Y
CCB:	08	BPL KEYIN	JSR PRBYTE
CCB:	08	STA (BASL),Y	JSR NXTAI
CCB:	08	LDA KBD	BCC HODBCHK
CCB:	08	BIT KBDSTRB	RTS
CCB:	08	RTS	LSR A
CCB:	08	JSR RDKEY	BCC XAM
CCB:	08	JSR ESCNW	LSR A
CCB:	08	JSR RDKEY	LSR A
CCB:	08	CHP #9B	LDA A2L
CCB:	08	BEG ESC	BCC ADD
CCB:	08	PAGE	EOR #8FF
CCB:	08	LDA INVFLG	ADC A1L
CCB:	08	PHA	PHA
CCB:	08	LDA #8FF	LDA #8B
CCB:	08	STA INVFLG	JSR COUT
CCB:	08	LDA IN, X	PLA
CCB:	08	JSR COUT	LSR A
CCB:	08	PLA	LSR A
CCB:	08	STA INVFLG	LSR A

FC4:	DO 02	BNE RTS4B	LDA IN, X
FC6:	E6 3D	INC A1H	CHP #6B
FC8:	60	RTS	BEG BCKSPC
FC9:		PAGE	CHP #9B
FC9:	A0 4B	LDY #4B	BEG CANCEL
FCB:	20 0B FC	JSR ZERDLY	CPX #8FB
CC2:		BNE HEADR	BCC NOTCR1
CC2:		ADC #8FE	JSR BELL
CC2:	B0 F5	BDS HEADR	BNE NATCHAR
CC2:	A0 21	LDY #21	LDA #8DC
CC4:	20 0B FC	JSR ZERDLY	JSR COUT
CC9:	08	INV	301 GETLNZ
CCB:	08	INV	302 GETLN
CCB:	08	DEV	JSR COUT
CCB:	08	BNE ZERDLY	304 LDX #601
CCB:	08	BCC WRTAPE	TXA
CCB:	08	LDY #32	BEG GETLNZ
CCB:	08	DEV	DEX
CCB:	08	BNE ONEDLY	JSR RDCHAR
CCB:	08	LDY TAPEUT	CHP #95
CCB:	08	LDY #2C	LDA (BASL),Y
CCB:	08	RTS	BCC ADDINP
CCB:	08	PHX	AND #8DF
CCB:	08	PLA	STA IN, X
CCB:	08	ROL	CHP #8B
CCB:	08	LDY #3A	BNE NOTCR
CCB:	08	DEX	JSR CLREDL
CCB:	08	BNE RDBYT2	LDA #8B
CCB:	08	RTS	BNE COUT
CCB:	08	JSR RDBIT	LDY A1H
CCB:	08	DEV	LDX A1L
CCB:	08	LDY TAPEIN	JSR CRQUT
CCB:	08	BPL RDBIT	JSR PRINTX
CCB:	08	EOR LASTIN	LDY #00
CCB:	08	EOR LASTIN	LDA #8A
CCB:	08	STA LASTIN	LDA #8A
CCB:	08	CPY #80	JMP COUT
CCB:	08	RTS	PAGE
CCB:	08	LDY CH	LDA A1L
CCB:	08	LDA (BASL),Y	ORA #07
CCB:	08	PHA	STA A2L
CCB:	08	AND #3F	LDA A1H
CCB:	08	ORA #40	LDA A1H
CCB:	08	STA (BASL),Y	STA A2H
CCB:	08	PLA	LDA A1L
CCB:	08	JMP (KSHL)	AND #07
CCB:	08	INC RNDL	BNE DATAUT
CCB:	08	BNE KEYIN2	JSR PRAI
CCB:	08	INC RNDH	LDA #8A
CCB:	08	BIT KBD	LDA (A1L),Y
CCB:	08	BPL KEYIN	JSR PRBYTE
CCB:	08	STA (BASL),Y	JSR NXTAI
CCB:	08	LDA KBD	BCC HODBCHK
CCB:	08	BIT KBDSTRB	RTS
CCB:	08	RTS	LSR A
CCB:	08	JSR RDKEY	BCC XAM
CCB:	08	JSR ESCNW	LSR A
CCB:	08	JSR RDKEY	LSR A
CCB:	08	CHP #9B	LDA A2L
CCB:	08	BEG ESC	BCC ADD
CCB:	08	PAGE	EOR #8FF
CCB:	08	LDA INVFLG	ADC A1L
CCB:	08	PHA	PHA
CCB:	08	LDA #8FF	LDA #8B
CCB:	08	STA INVFLG	JSR COUT
CCB:	08	LDA IN, X	PLA
CCB:	08	JSR COUT	LSR A
CCB:	08	PLA	LSR A
CCB:	08	STA INVFLG	LSR A

SHIFT TO UPPER CASE



FD	FE	FF	PRHEXZ
362	20	E5	JSR PRHEXZ
363	68	0F	PLA
364	29	0F	AND #0F
365	09	B0	ORA #B0
366	09	B0	ORA #B0
367	09	B0	ORA #B0
368	09	B0	ORA #B0
369	09	B0	ORA #B0
370	09	B0	ORA #B0
371	09	B0	ORA #B0
372	09	B0	ORA #B0
373	09	B0	ORA #B0
374	09	B0	ORA #B0
375	09	B0	ORA #B0
376	09	B0	ORA #B0
377	09	B0	ORA #B0
378	09	B0	ORA #B0
379	09	B0	ORA #B0
380	09	B0	ORA #B0
381	09	B0	ORA #B0
382	09	B0	ORA #B0
383	09	B0	ORA #B0
384	09	B0	ORA #B0
385	09	B0	ORA #B0
386	09	B0	ORA #B0
387	09	B0	ORA #B0
388	09	B0	ORA #B0
389	09	B0	ORA #B0
390	09	B0	ORA #B0
391	09	B0	ORA #B0
392	09	B0	ORA #B0
393	09	B0	ORA #B0
394	09	B0	ORA #B0
395	09	B0	ORA #B0
396	09	B0	ORA #B0
397	09	B0	ORA #B0
398	09	B0	ORA #B0
399	09	B0	ORA #B0
400	09	B0	ORA #B0
401	09	B0	ORA #B0
402	09	B0	ORA #B0
403	09	B0	ORA #B0
404	09	B0	ORA #B0
405	09	B0	ORA #B0
406	09	B0	ORA #B0
407	09	B0	ORA #B0
408	09	B0	ORA #B0
409	09	B0	ORA #B0
410	09	B0	ORA #B0
411	09	B0	ORA #B0
412	09	B0	ORA #B0
413	09	B0	ORA #B0
414	09	B0	ORA #B0
415	09	B0	ORA #B0
416	09	B0	ORA #B0
417	09	B0	ORA #B0
418	09	B0	ORA #B0
419	09	B0	ORA #B0
420	09	B0	ORA #B0
421	09	B0	ORA #B0
422	09	B0	ORA #B0
423	09	B0	ORA #B0
424	09	B0	ORA #B0
425	09	B0	ORA #B0
426	09	B0	ORA #B0
427	09	B0	ORA #B0
428	09	B0	ORA #B0
429	09	B0	ORA #B0
430	09	B0	ORA #B0
431	09	B0	ORA #B0
432	09	B0	ORA #B0
433	09	B0	ORA #B0
434	09	B0	ORA #B0

GO CHECK FOR PAUSE

PRE-RELEASE  
VERSION

FE	FF	PRHEXZ	
435	E9	01	SBC #01
436	D0	EF	BNE LIST2
437	60		RTS
438			PAGE
439	BA		TXA
440	F0	07	BEG AIPCRTS
441	B5	3C	LDA AIL,X
442	95	3A	STA PCL,X
443	CA		DEX
444	10	F9	SPL A1PCLP
445	60		RTS
446	A0	3F	BEG AIPCRTS
447	D0	02	LDY #0F
448	00	02	BNE SETIFLG
449	00	02	LDY #0F
450	84	32	SETIFLG STV INVFLG
451	00		RTS
452	A0	00	SETKBD LDA #00
453	3E		STA A2L
454	3B		LDY #KSWL
455	0B		LDY #KEYIN
456	08		BNE IDPRT
457	00		LDA #00
458	3E		OUTPRT STA A2L
459	3E		OUTPRT LDA #CSWL
460	F6		LDY #COUT1
461	3E		IDPRT LDA A2L
462	0F		AND #0F
463	00		BEG IDPRT1
464	00		ORA #IDADR/256
465	00		LDY #00
466	02		BEG IDPRT2
467	02		LDY #COUT1/256
468	00		RTS
469	94	00	FEAR: 94 00
470	01		FEAB: 95 01
471	EA		FEAE: EA
472	EA		FEAF: EA
473	00	00	FEBO: 4C 00 00
474	03	00	FEBC: 4C 03 00
475	FE	FE	FEBD: 20 75 FE
476	FF	FF	FEBE: 20 3F FF
477	00	00	FEBC: 6C 3A 00
478	D7	FA	FEBF: 4C D7 FA
479	60		FECD: 60
480	EA		FECE: EA
481	EA		FECA: 60
482	EA		FECC: EA
483	EA		FECD: EA
484	EA		FECE: EA
485	EA		FECA: EA
486	EA		FECC: EA
487	EA		FECD: EA
488	EA		FECE: EA
489	EA		FECA: EA
490	EA		FECC: EA
491	EA		FECD: EA
492	EA		FECE: EA
493	EA		FECA: EA
494	EA		FECC: EA
495	EA		FECD: EA
496	EA		FECE: EA
497	EA		FECA: EA
498	EA		FECC: EA
499	EA		FECD: EA
500	EA		FECE: EA
501	EA		FECA: EA
502	EA		FECC: EA
503	EA		FECD: EA
504	EA		FECE: EA
505	EA		FECA: EA
506	EA		FECC: EA
507	EA		FECD: EA

STEP IS DONE

```

FFEC: 17
FFED: 17
FFEE: 28
FFEF: 1F
FFFO: B3
FFF1: 7F
FFF2: 5D
FFF3: CC
FFF4: B5
FFF5: FC
FFF6: 17
FFF7: 17
FFF8: F5
FFF9: 03 03
FFFA: FB 03
FFFB: 62 FA
FFFC: 62 FA
FFFE: 40 FA
ENDASH
    
```

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434
435
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470
    
```

```

DFB $17
DFB $20
DFB $1F
DFB $B3
DFB $7F
DFB $5D
DFB $CC
DFB $B5
DFB $FC
DFB $17
DFB $17
DFB $F5
DFB $03
DW NMI
DW RESET
DW IRQ
    
```

# PRE-RELEASE VERSION

## MONITOR ROM LISTING

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1 .....
2 .....
3 .....
4 .....
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```

```

*****
APPLE II
SYSTEM MONITOR
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S. MOZNIK
A. BAUM
*****
"APPLE II SYSTEM MONITOR"
    
```

```

LOC0 EP2 $00
LOC1 EP2 $01
WMDLFT EP2 $20
WMDMDIH EP2 $21
WMDTOP EP2 $22
WMDBTM EP2 $23
CH EP2 $24
CV EP2 $25
GBASL EP2 $26
BASL EP2 $27
BASL EP2 $28
BASL EP2 $29
BAS2L EP2 $2A
BAS2H EP2 $2B
H2 EP2 $2C
LNEM EP2 $2C
RTNL EP2 $2C
V2 EP2 $2D
RMEM EP2 $2D
RTNH EP2 $2D
MASK EP2 $2E
CHRSDM EP2 $2E
FORMAT EP2 $2E
LASTIN EP2 $2E
LENGTH EP2 $2E
SIGN EP2 $2F
COLOR EP2 $30
NODE EP2 $31
INVPFG EP2 $32
PRGMPR EP2 $33
YSAV EP2 $34
YSAVL EP2 $35
CSHL EP2 $36
CSHL EP2 $37
KSMH EP2 $38
KSMH EP2 $39
PCL EP2 $3A
PCL EP2 $3A
KOT EP2 $3C
KOT EP2 $3C
A1H EP2 $3D
A1H EP2 $3D
A2L EP2 $3E
A2L EP2 $3E
A3H EP2 $40
A3H EP2 $40
A4L EP2 $42
A4L EP2 $42
A4H EP2 $43
A4H EP2 $43
ASL EP2 $44
ASL EP2 $44
ACI EP2 $45
ACI EP2 $45
YREG EP2 $46
YREG EP2 $46
STATUS EP2 $47
STATUS EP2 $47
    
```

FEF3	DO FA	508	BNE WRTY12
FEF4	DO FE	509	RTS
FEF5	DO 00	510	CRMON
FEF6	DO 00	511	JSR BL1
FEF7	DO 00	512	PLA
FEF8	DO 6C	513	BNE MONZ
FEF9	DO FA FC	514	JSR RDZB1T
FEFA	DO 16	515	LDA #16
FEFB	DO C9 FC	516	JSR HEADR
FEFC	DO 24	517	STA CHKSUM
FEFD	DO FA FC	518	JSR RDZB1T
FEFE	DO 24	519	LDY #24
FEFF	DO FD FC	520	JSR RDZB1T
FF00	DO FD FC	521	BCC RDZ
FF01	DO FD FC	522	JSR RDZB1T
FF02	DO EC FC	523	LDY #3B
FF03	DO 3C	524	JSR RDBYTE
FF04	DO 2E	525	BTA (ALL, X)
FF05	DO 2E	526	EDR CHKSUM
FF06	DO 2E	527	STA CHKSUM
FF07	DO BA FC	528	JSR NXTA1
FF08	DO 35	529	LDY #35
FF09	DO 35	530	BCC RD3
FF0A	DO EC FC	531	JSR RDBYTE
FF0B	DO 2E	532	CMR CHKSUM
FF0C	DO 2E	533	BEG BELL
FF0D	DO 2E	534	PRERR
FF0E	DO ED FD	535	JSR COUT
FF0F	DO ED FD	536	LDA #802
FF10	DO ED FD	537	JSR COUT
FF11	DO ED FD	538	JSR COUT
FF12	DO ED FD	539	BELL
FF13	DO ED FD	540	JMP COUT
FF14	DO ED FD	541	PAGE
FF15	DO ED FD	542	RESTORE
FF16	DO ED FD	543	LDX STATUS
FF17	DO ED FD	544	LDX A5H
FF18	DO ED FD	545	LDX XREG
FF19	DO ED FD	546	LDY XREG
FF1A	DO ED FD	547	PLP
FF1B	DO ED FD	548	RTS
FF1C	DO ED FD	549	SAVE
FF1D	DO ED FD	550	STY XREG
FF1E	DO ED FD	551	STY YREG
FF1F	DO ED FD	552	PLP
FF20	DO ED FD	553	PLA
FF21	DO ED FD	554	STA STATUS
FF22	DO ED FD	555	TSX
FF23	DO ED FD	556	STX SPNT
FF24	DO ED FD	557	CLD
FF25	DO ED FD	558	RTS
FF26	DO ED FD	559	QLDRST
FF27	DO ED FD	560	JSR INIT
FF28	DO ED FD	561	JSR SETVID
FF29	DO ED FD	562	JSR SETVID
FF2A	DO ED FD	563	PAGE
FF2B	DO ED FD	564	MON
FF2C	DO ED FD	565	CLD
FF2D	DO ED FD	566	JSR BELL
FF2E	DO ED FD	567	LDA #8AA
FF2F	DO ED FD	568	STA PROMPT
FF30	DO ED FD	569	JSR GETLNZ
FF31	DO ED FD	570	JSR ZMODE
FF32	DO ED FD	571	JSR GETNUM
FF33	DO ED FD	572	STY #817
FF34	DO ED FD	573	LDY #817
FF35	DO ED FD	574	DEY
FF36	DO ED FD	575	BHI MON
FF37	DO ED FD	576	CMR CHRTRBL,Y
FF38	DO ED FD	577	BNE CHRTRBL,Y
FF39	DO ED FD	578	JSR TOSUB
FF3A	DO ED FD	579	LDY #8A
FF3B	DO ED FD	580	JMP NXT1TH
FF3C	DO ED FD	581	LDX #803

# PRE-RELEASE VERSION

FFBC	0A	581	ASL A
FFBD	0A	582	ASL A
FFBE	0A	583	ASL A
FFBF	0A	584	ASL A
FFC0	0A	585	ASL A
FFC1	0A	586	ASL A
FFC2	0A	587	ASL A
FFC3	0A	588	ASL A
FFC4	0A	589	ASL A
FFC5	0A	590	ASL A
FFC6	0A	591	ASL A
FFC7	0A	592	ASL A
FFC8	0A	593	ASL A
FFC9	0A	594	ASL A
FFCA	0A	595	ASL A
FFCB	0A	596	ASL A
FFCC	0A	597	ASL A
FFCD	0A	598	ASL A
FFCE	0A	599	ASL A
FFCF	0A	600	ASL A
FFD0	0A	601	ASL A
FFD1	0A	602	ASL A
FFD2	0A	603	ASL A
FFD3	0A	604	ASL A
FFD4	0A	605	ASL A
FFD5	0A	606	ASL A
FFD6	0A	607	ASL A
FFD7	0A	608	ASL A
FFD8	0A	609	ASL A
FFD9	0A	610	ASL A
FFDA	0A	611	ASL A
FFDB	0A	612	ASL A
FFDC	0A	613	ASL A
FFDD	0A	614	ASL A
FFDE	0A	615	ASL A
FFDF	0A	616	ASL A
FFE0	0A	617	ASL A
FFE1	0A	618	ASL A
FFE2	0A	619	ASL A
FFE3	0A	620	ASL A
FFE4	0A	621	ASL A
FFE5	0A	622	ASL A
FFE6	0A	623	ASL A
FFE7	0A	624	ASL A
FFE8	0A	625	ASL A
FFE9	0A	626	ASL A
FFEA	0A	627	ASL A
FFEB	0A	628	ASL A
FFEC	0A	629	ASL A
FFED	0A	630	ASL A
FFEE	0A	631	ASL A
FFEF	0A	632	ASL A
FFF0	0A	633	ASL A
FFF1	0A	634	ASL A
FFF2	0A	635	ASL A
FFF3	0A	636	ASL A
FFF4	0A	637	ASL A
FFF5	0A	638	ASL A
FFF6	0A	639	ASL A
FFF7	0A	640	ASL A
FFF8	0A	641	ASL A
FFF9	0A	642	ASL A
FFFA	0A	643	ASL A
FFFB	0A	644	ASL A
FFFC	0A	645	ASL A
FFFD	0A	646	ASL A
FFFE	0A	647	ASL A
FFFF	0A	648	ASL A
	0A	649	ASL A
	0A	650	ASL A
	0A	651	ASL A
	0A	652	ASL A
	0A	653	ASL A

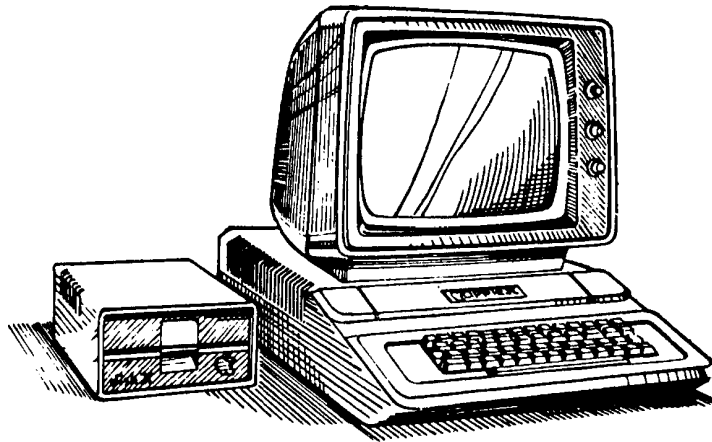


## Apple II Computer Technical Information

# APPLE II / APPLE II-PLUS LEVEL II SERVICE REFERENCE MANUAL

Pre-Release Version

## APPENDIX A ROM LISTING -- MONITOR (1977)



Written by  
Apple Computer, Inc. • Level II Service Center  
1981

( This page is not part of the original service manual )



PRE-RELEASE  
VERSION

F849: 29 U3	AND #S03	GENERATE GBASH=000001FG
F84B: 09 U4	ORA #S04	AND GBASL=HIDEDE000
F84D: 05 27	STA GBASH	
F84F: 08 14	PLA	
F850: 09 14	AND #S18	
F852: 90 U2	BCC GBALC	
F854: 69 7F	ADC #S7F	
F856: 05 26	STA GBASL	
F858: 0A 15	ASL A	
F859: 0A 15	ASL A	
F85A: 05 26	ORA GBASL	
F85C: 05 26	STA GBASL	
F85E: 60 15	RTS	INCREMENT COLOR BY J
F85F: A5 30	LDA COLOR	
F861: 18 10	CLC	
F862: 69 U3	AND #S0F	SETS COLOR=17*A MOD 16
F864: 29 U3	AND #S0F	
F866: 05 30	STA COLOR	BOTH HALF BYTES OF COLOR EQ
F868: 0A 16	ASL A	
F86A: 0A 16	ASL A	
F86B: 0A 16	ASL A	
F86C: 05 30	ORA COLOR	
F86E: 05 30	STA COLOR	
F870: 60 16	RTS	
F871: 4A 16	LSR A	READ SCREEN Y-COORD/2
F872: 09 16	PHP	SAVE LSB (CARRY)
F873: 20 47 P8	JSR GBASCALC	CALC BASE ADDRESS
F876: 01 26	LDA (GBASL),Y	GET BYTE
F878: 26 17	PLP	RESTORE LSB FROM CARRY
F879: 90 U4	BCC RTMSKZ	IF EVEN, USE LO H
F87B: 4A 17	LSR A	
F87C: 4A 17	LSR A	
F87D: 4A 17	LSR A	SHIFT HIGH HALF BYTE DOWN
F87E: 4A 17	LSR A	
F87F: 29 U4	AND #S0F	MASK 4-BITS
F881: 60 17	RTS	
F882: A5 3A	LDA PCL,H	PRINT PCL,H
F884: A5 3A	LDA PCL	
F886: 20 06 FD	LDY #PRX2	
F888: 20 0A P9	JSR PRBLNK	FOLLOWED BY A BLANK
F88C: A1 3A	LDA (PCL),X	GET OF CODE
F88E: 4A 18	LSR A	
F88F: 4A 18	LSR A	EVEN/ODD TEST
F890: 90 U9	BCC IEVEN	
F892: 6A 18	BCS ERR	91T 1 TEST
F893: C5 A2	CRP #SA2	XXXXXXXX INVALID OP
F897: F0 UC	BEQ ERR	
F899: 29 07	AND #S87	OPCODE \$99 INVALID
F89B: 4A 19	LSR A	LSB INTO CARRY FOR L/R TEST
F89C: 4A 19	LSR A	
F89D: 00 62 P9	LDA #PRT1,X	GET FORMAT INDEX BYTE
F8A0: 20 79 P8	JSR SCRN2	R/L II-BYTE ON CARRY
F8A3: 00 U4	BHE GETFMT	
F8A5: 00 60	LDY #S90	SUBSTITUTE \$90 FOR INVALID O
F8A7: A9 U0	LDA #S0	SET PRINT FORMAT INDEX TO 0
F8A9: AA 20	TAX	
F8AA: 00 A6 P9	LDA #INT2,X	INDEX INTO PRINT FORMAT TABL
F8AD: 85 2E	STA FORMAT	SAVE FOR ADR FIELD FORMATTN
F8AF: 29 U3	AND #S03	MASK FOR 2-BIT LENGTH
F8B1: 05 2F	STA LENGTH	(P=1 BYTE, 1=2 BYTE)
F8B3: 98 20	TVA	OPCODE
F8B4: 29 0F	AND #S8F	MASK FOR IXXXXIUU TEST
F8B6: AA 20	TAX	SAVE IT
F8B7: 98 20	TVA	OPCODE TO A AGAIN
F8B8: 0A U3	LDY #S03	
F8BA: 00 A3	CEX #S8A	
F8BC: FV UB	BEQ MNDXJ	
F8BE: 4A 21	LSR A	FORM INDEX INTO MNEHONIC TAB
F8BF: 90 U8	BCC MNDXJ	
F8C1: 4A 21	LSR A	

F800: 4A	F800: 4A	ORG #F800	ROM START ADDRESS
F801: 0D	F801: 0D	LSR A	Y-COORD/2
F802: 20 47 P8	F802: 20 47 P8	JSR GBASCALC	SAVE LSB IN CARRY
F803: 26 17	F803: 26 17	LDA (GBASL),Y	CALC BASE ADR IN GBASL,H
F804: 09 U4	F804: 09 U4	PLP	RESTORE LSB FROM CARRY
F805: 09 U4	F805: 09 U4	PLP	MASK SUP IF EVEN
F806: 90 U2	F806: 90 U2	BCC RTMSK	MASK \$E0 IF ODD
F808: 85 2E	F808: 85 2E	ADC #S0	DATA
F809: 69 EU	F809: 69 EU	STA MASK	XOR COLOR
F80A: 20 06 FD	F80A: 20 06 FD	LDY #PRX2	AND MASK
F80C: 20 0A P9	F80C: 20 0A P9	JSR PRBLNK	XOR DATA
F80E: 51 26	F80E: 51 26	AND #S0	TO DATA
F810: 45 30	F810: 45 30	LDY #S0	PLOT SQUARE
F812: 25 2E	F812: 25 2E	AND #S0	DONE?
F814: 51 26	F814: 51 26	LDY #S0	YES, RETURN
F816: 91 26	F816: 91 26	STA (GBASL),Y	NO, INCR INDEX (X-COORD)
F818: 60 11	F818: 60 11	RTS	ALWAYS TAKEN
F819: 20 00 P8	F819: 20 00 P8	JSR HLINE	NEXT Y-COORD
F81C: C4 2C	F81C: C4 2C	CPY H2	SAVE ON STACK
F81E: 00 11	F81E: 00 11	BCS RTS1	PLOT SQUARE
F820: C8 11	F820: C8 11	INY	DONE?
F821: 20 DE P8	F821: 20 DE P8	JSR PLOT1	NO, LOOP.
F824: 90 P6	F824: 90 P6	BCC HLINE1	MAX Y, FULL SCRIN CLR
F826: 69 01	F826: 69 01	ADC #S01	ALWAYS TAKEN
F828: 4B 12	F828: 4B 12	PHA	MAX Y, TOP SCRIN CLR
F829: 20 00 P8	F829: 20 00 P8	JSR PLOT	STORE AS BOTTOM COORD
F82C: 68 12	F82C: 68 12	PLA	FOR VLINE CALLS
F82D: C5 2D	F82D: C5 2D	CMP V2	RIGHTMOST X-COORD (COLUMN)
F82F: 90 F5	F82F: 90 F5	BCC VLINEZ	TOP COORD FOR VLINE CALLS
F831: 60 12	F831: 60 12	RTS1	CLEAR COLOR (BLACK)
F832: A0 2F	F832: A0 2F	CLASCR	DRAW VLINE
F834: 00 U2	F834: 00 U2	BNE CLRSC2	NEXT LEFTMOST X-COORD
F836: A0 27	F836: A0 27	LDY #S27	LOOP UNTIL DONE.
F838: 84 2D	F838: 84 2D	STY V2	FOR INPUT 000DEFGH
F83A: A0 27	F83A: A0 27	LDY #S27	
F83B: A9 U0	F83B: A9 U0	LDA #S0	
F83C: 95 30	F83C: 95 30	STA COLOR	
F840: 20 28 P8	F840: 20 28 P8	JSR VLINE	
F843: 88 13	F843: 88 13	DEY	
F844: 10 P6	F844: 10 P6	BPL CLRSC3	
F846: 60 14	F846: 60 14	RTS	
F847: 4A 14	F847: 4A 14	LSR A	
F848: 4A 14	F848: 4A 14	LSR A	





FA09:	BA 10 23 144	DBR	\$1B,\$A1,\$9D,\$
FA0C:	9D 03 10	DBR	\$90,\$8B,\$1D,\$
FA0E:	A1 0A 29 145	DBR	\$19,\$AE,\$59,\$
FA0D:	19 3E 69	DBR	\$24,\$53,\$1B,\$
FA05:	AA 19 23 146	DBR	\$19,\$A1
FA08:	24 53 18	DBR	\$0B,\$1A,\$5B,\$
FA04:	23 24 53 147	DBR	\$24,\$24
FA0E:	00 1A 5B 148	DBR	\$AE,\$AE,\$A4,\$
FA03:	5B 45 69 149	DBR	\$7C,\$50
FA06:	24 24 24 150	DBR	\$15,\$9C,\$8D,\$
FA08:	3C 45 69 151	DBR	\$84,\$13,\$34,\$
FA09:	15 0C 6D 152	DBR	\$21,\$A0
FA0E:	3C 45 69 153	DBR	\$0B,\$62,\$5A,\$
FA0F:	29 33 14 154	DBR	\$94,\$58,\$54,\$
FA08:	84 13 14 155	DBR	\$68,\$44,\$5E,\$
FA0E:	11 0A 69 156	DBR	\$0A,\$84,\$74,\$
FA0F:	23 00 34 158	DBR	\$7A,\$F4,\$CC,\$
FA03:	48 26 62 157	DBR	\$4,\$84,\$8A
FA06:	94 8C 34 158	DBR	\$00,\$A4,\$A2,\$
FA0C:	68 44 6D 159	DBR	\$74,\$72,\$72
FA0E:	94 00 84 159	DBR	\$44,\$38,\$82,\$
FA12:	08 84 74	DBR	\$22,\$50
FA15:	84 28 6E 160	DBR	\$1A,\$1A,\$2A,\$
FA18:	74 84 CC	DBR	\$88,\$8C
FA1B:	4A 72 72 161	DBR	\$1A,\$1A,\$2A,\$
FA1E:	A4 84 42	DBR	\$00,\$A4,\$A2,\$
FA20:	00 8A 42	DBR	\$00,\$A4,\$A2,\$
FA23:	A2 74 74 163	DBR	\$74,\$72,\$72
FA26:	74 72 74 164	DBR	\$74,\$72,\$72
FA2B:	44 68 82	DBR	\$44,\$38,\$82,\$
FA2E:	32 82 00 165	DBR	\$22,\$50
FA32:	22 00 166	DBR	\$1A,\$1A,\$2A,\$
FA30:	1A 1A 2A	DBR	\$88,\$8C
FA33:	2A 72 72 167	DBR	\$1A,\$1A,\$2A,\$
FA36:	88 8C	DBR	\$88,\$8C
FA38:	C4 CA 2A	DBR	\$C4,\$CA,\$2A,\$
FA3A:	4D 44 44 169	DBR	\$A2,\$C8
FA3E:	A2 C8	DBR	\$FE,\$FF,\$FF
FA40:	FE FE FE 171	DBR	\$FF,\$FF,\$FF
FA43:	20 DU FB 172	DBR	\$FF,\$FF,\$FF
FA46:	68 173	DBR	\$FF,\$FF,\$FF
FA47:	85 2C 174	DBR	\$FF,\$FF,\$FF
FA49:	85 2C 175	DBR	\$FF,\$FF,\$FF
FA4A:	85 2D 176	DBR	\$FF,\$FF,\$FF
FA4C:	A2 0A 177	DBR	\$FF,\$FF,\$FF
FA4E:	9C 10 FB 178	DBR	\$FF,\$FF,\$FF
FA51:	95 3C 179	DBR	\$FF,\$FF,\$FF
FA53:	CA 3A 180	DBR	\$FF,\$FF,\$FF
FA54:	DU FA 181	DBR	\$FF,\$FF,\$FF
FA56:	A1 JA 182	DBR	\$FF,\$FF,\$FF
FA58:	FU 42 183	DBR	\$FF,\$FF,\$FF
FA5A:	A4 2F 184	DBR	\$FF,\$FF,\$FF
FA5C:	C9 20 185	DBR	\$FF,\$FF,\$FF
FA5E:	F0 59 186	DBR	\$FF,\$FF,\$FF
FA60:	C9 50 187	DBR	\$FF,\$FF,\$FF
FA62:	F0 59 187	DBR	\$FF,\$FF,\$FF
FA64:	C9 45 188	DBR	\$FF,\$FF,\$FF
FA66:	F0 5C 189	DBR	\$FF,\$FF,\$FF
FA68:	C9 59 190	DBR	\$FF,\$FF,\$FF
FA6A:	F0 59 191	DBR	\$FF,\$FF,\$FF
FA6C:	C9 40 192	DBR	\$FF,\$FF,\$FF
FA6E:	F0 55 193	DBR	\$FF,\$FF,\$FF
FA70:	Z9 1F 194	DBR	\$FF,\$FF,\$FF
FA72:	49 14 195	DBR	\$FF,\$FF,\$FF
FA74:	C9 04 197	DBR	\$FF,\$FF,\$FF
FA76:	F0 02 198	DBR	\$FF,\$FF,\$FF
FA78:	B1 3A 199	DBR	\$FF,\$FF,\$FF
FA7A:	99 3C 00 400	DBR	\$FF,\$FF,\$FF

FA7D:	BR	401	DBR	\$1B,\$A1,\$9D,\$
FA7E:	10 FB	402	DBR	\$90,\$8B,\$1D,\$
FA80:	20 3E FE	403	DBR	\$19,\$AE,\$59,\$
FA83:	4C 3C 00 404	DBR	\$24,\$53,\$1B,\$	
FA86:	85 45	405	DBR	\$19,\$A1
FA88:	88	406	DBR	\$0B,\$1A,\$5B,\$
FA89:	48	407	DBR	\$24,\$24
FA8A:	0A	408	DBR	\$AE,\$AE,\$A4,\$
FA8B:	0A	409	DBR	\$7C,\$50
FA8C:	0A	410	DBR	\$15,\$9C,\$8D,\$
FA8D:	0A	411	DBR	\$84,\$13,\$34,\$
FA8E:	30 03	412	DBR	\$21,\$A0
FA8F:	6C FE 03 413	DBR	\$0B,\$62,\$5A,\$	
FA92:	24 4C FE 414	DBR	\$94,\$58,\$54,\$	
FA93:	68	415	DBR	\$68,\$44,\$5E,\$
FA96:	68	416	DBR	\$0A,\$84,\$74,\$
FA97:	65 3A	417	DBR	\$7A,\$F4,\$CC,\$
FA99:	68 3A	418	DBR	\$4,\$84,\$8A
FA9A:	65 38	419	DBR	\$00,\$A4,\$A2,\$
FA9C:	20 A2 FA 420	DBR	\$74,\$72,\$72	
FA9E:	20 DA FA 420	DBR	\$44,\$38,\$82,\$	
FAA2:	4C 05 FE 421	DBR	\$22,\$50	
FAA3:	18	422	DBR	\$1A,\$1A,\$2A,\$
FAA4:	18	423	DBR	\$88,\$8C
FAA5:	68	424	DBR	\$1A,\$1A,\$2A,\$
FAA6:	68	425	DBR	\$00,\$A4,\$A2,\$
FAA7:	68	426	DBR	\$74,\$72,\$72
FAA8:	68	427	DBR	\$44,\$38,\$82,\$
FAA9:	85 3B	428	DBR	\$22,\$50
FAAB:	A5 2F	429	DBR	\$1A,\$1A,\$2A,\$
FAAC:	20 5E	430	DBR	\$88,\$8C
FAAD:	84 3B	431	DBR	\$1A,\$1A,\$2A,\$
FAAE:	18	432	DBR	\$00,\$A4,\$A2,\$
FAAF:	90 14	433	DBR	\$74,\$72,\$72
FAB7:	18	434	DBR	\$44,\$38,\$82,\$
FAB9:	20 54	435	DBR	\$22,\$50
FABD:	AA	436	DBR	\$1A,\$1A,\$2A,\$
FABE:	98	437	DBR	\$88,\$8C
FABF:	98	438	DBR	\$1A,\$1A,\$2A,\$
FAC0:	48	439	DBR	\$00,\$A4,\$A2,\$
FAC1:	DA	440	DBR	\$74,\$72,\$72
FAC2:	48	441	DBR	\$44,\$38,\$82,\$
FAC3:	A0 02	442	DBR	\$22,\$50
FAC4:	1D	443	DBR	\$1A,\$1A,\$2A,\$
FAC5:	B1 3A	444	DBR	\$88,\$8C
FAC7:	AA	445	DBR	\$1A,\$1A,\$2A,\$
FAC8:	88	446	DBR	\$00,\$A4,\$A2,\$
FAC9:	B1 3A	447	DBR	\$74,\$72,\$72
FACB:	66 3B	448	DBR	\$44,\$38,\$82,\$
FACD:	85 3A	449	DBR	\$22,\$50
FACF:	80 F3	450	DBR	\$1A,\$1A,\$2A,\$
FAD0:	A5 2D	451	DBR	\$88,\$8C
FAD1:	48	452	DBR	\$1A,\$1A,\$2A,\$
FAD3:	A5 2C	453	DBR	\$00,\$A4,\$A2,\$
FAD4:	48	454	DBR	\$74,\$72,\$72
FAD6:	20 BE FD	455	DBR	\$44,\$38,\$82,\$
FAD7:	A9 45	456	DBR	\$22,\$50
FADA:	A9 45	457	DBR	\$1A,\$1A,\$2A,\$
FADC:	45 40	458	DBR	\$88,\$8C
FAD8:	A9 00	459	DBR	\$1A,\$1A,\$2A,\$
FAD9:	85 41	460	DBR	\$00,\$A4,\$A2,\$
FAB2:	A2 FB	461	DBR	\$74,\$72,\$72
FAB3:	A9 AU	462	DBR	\$44,\$38,\$82,\$
FAB4:	A9 AU	463	DBR	\$22,\$50
FAB5:	20 ED FD	464	DBR	\$1A,\$1A,\$2A,\$
FAB6:	BD 1E FA 462	465	DBR	\$88,\$8C
FAB7:	20 ED FD 463	466	DBR	\$1A,\$1A,\$2A,\$
FAB8:	A9 BD FD 465	467	DBR	\$00,\$A4,\$A2,\$
FAB9:	BD 1E FA 462	468	DBR	\$74,\$72,\$72
FAB0:	A9 BD FD 465	469	DBR	\$44,\$38,\$82,\$
FAB1:	20 ED FD 463	470	DBR	\$22,\$50
FAB2:	BD 1E FA 462	471	DBR	\$1A,\$1A,\$2A,\$
FAB3:	A9 BD FD 465	472	DBR	\$88,\$8C
FAB4:	BD 1E FA 462	473	DBR	\$1A,\$1A,\$2A,\$

FA7D:	BR	401	DBR	\$1B,\$A1,\$9D,\$
FA7E:	10 FB	402	DBR	\$90,\$8B,\$1D,\$
FA80:	20 3E FE	403	DBR	\$19,\$AE,\$59,\$
FA83:	4C 3C 00 404	DBR	\$24,\$53,\$1B,\$	
FA86:	85 45	405	DBR	\$19,\$A1
FA88:	88	406	DBR	\$0B,\$1A,\$5B,\$
FA89:	48	407	DBR	\$24,\$24
FA8A:	0A	408	DBR	\$AE,\$AE,\$A4,\$
FA8B:	0A	409	DBR	\$7C,\$50
FA8C:	0A	410	DBR	\$15,\$9C,\$8D,\$
FA8D:	30 03	411	DBR	\$84,\$13,\$34,\$
FA8E:	6C FE 03 413	DBR	\$21,\$A0	
FA92:	24 4C FE 414	DBR	\$0B,\$62,\$5A,\$	
FA93:	68	415	DBR	\$94,\$58,\$54,\$
FA96:	68	416	DBR	\$68,\$44,\$5E,\$
FA97:	65 3A	417	DBR	\$0A,\$84,\$74,\$
FA99:	68 3A	418	DBR	\$7A,\$F4,\$CC,\$
FA9A:	65 38	419	DBR	\$4,\$84,\$8A
FA9C:	20 A2 FA 420	DBR	\$00,\$A4,\$A2,\$	
FA9E:	20 DA FA 420	DBR	\$74,\$72,\$72	
FAA2:	4C 05 FE 421	DBR	\$44,\$38,\$82,\$	
FAA3:	18	422	DBR	\$22,\$50
FAA4:	18	423	DBR	\$1A,\$1A,\$2A,\$
FAA5:	68	424	DBR	\$88,\$8C
FAA6:	68	425	DBR	\$1A,\$1A,\$2A,\$
FAA7:	68	426	DBR	\$00,\$A4,\$A2,\$
FAA8:	68	427	DBR	\$74,\$72,\$72
FAA9:	85 3B	428	DBR	\$44,\$38,\$82,\$
FAAB:	A5 2F	429	DBR	\$22,\$50
FAAC:	20 5E	430	DBR	\$1A,\$1A,\$2A,\$
FAAD:	84 3B	431	DBR	\$88,\$8C
FAAE:	18	432	DBR	\$1A,\$1A,\$2A,\$
FAB7:	90 14	433	DBR	\$00,\$A4,\$A2,\$
FAB9:	20 54	434	DBR	\$74,\$72,\$72
FABD:	AA	435	DBR	\$44,\$38,\$82,\$
FABE:	98	436	DBR	\$22,\$50
FABF:	98	437	DBR	\$1A,\$1A,\$2A,\$
FAC0:	48	438	DBR	\$88,\$8C
FAC1:	DA	439	DBR	\$1A,\$1A,\$2A,\$
FAC2:	48	440	DBR	\$00,\$A4,\$A2,\$
FAC3:	A0 02	441	DBR	\$74,\$72,\$72
FAC4:	1D	442	DBR	\$44,\$38,\$82,\$
FAC5:	B1 3A	443	DBR	\$22,\$50
FAC7:	AA	444	DBR	\$1A,\$1A,\$2A,\$
FAC8:	88	445	DBR	\$88,\$8C
FAC9:	B1 3A	446	DBR	\$1A,\$1A,\$2A,\$
FACB:	66 3B	447	DBR	\$00,\$A4,\$A2,\$
FACD:	85 3A	448	DBR	\$74,\$72,\$72
FACF:	80 F3	449	DBR	\$44,\$38,\$82,\$
FAD0:	A5 2D	450	DBR	\$22,\$50
FAD1:	48	451	DBR	\$1A,\$1A,\$2A,\$
FAD3:	A5 2C	452	DBR	\$88,\$8C
FAD4:	48	453	DBR	\$1A,\$1A,\$2A,\$
FAD6:	20 BE FD	454	DBR	\$00,\$A4,\$A2,\$
FAD7:	A9 45	455	DBR	\$74,\$72,\$72
FADA:	A9 45	456	DBR	\$44,\$38,\$82,\$
FADC:	45 40	457	DBR	\$22,\$50
FAD8:	A9 00	458	DBR	\$1A,\$1A,\$2A,\$
FAD9:	85 41	459	DBR	\$88,\$8C
FAB2:	A2 FB	460	DBR	\$1A,\$1A,\$2A,\$
FAB3:	A9 AU	461	DBR	\$00,\$A4,\$A2,\$
FAB4:	A9 AU	462	DBR	\$74,\$72,\$72
FAB5:	20 ED FD	463	DBR	\$44,\$38,\$82,\$
FAB6:	BD 1E FA 462	464	DBR	\$22,\$50
FAB7:	20 ED FD 463	465	DBR	\$1A,\$1A,\$2A,\$
FAB8:	A9 BD FD 465	466	DBR	\$88,\$8C
FAB9:	BD 1E FA 462	467	DBR	\$1A,\$1A,\$2A,\$
FAB0:	A9 BD FD 465	468	DBR	\$00,\$A4,\$A2,\$
FAB1:	20 ED FD 463	469	DBR	\$74,\$72,\$72
FAB2:	BD 1E FA 462	470	DBR	\$44,\$38,\$82,\$
FAB3:	A9 BD FD 465	471	DBR	\$22,\$50
FAB4:	BD 1E FA 462	472	DBR	\$1A,\$1A,\$2A,\$
FAB5:	A9 BD FD 465	473	DBR	\$88,\$8C

FA7D:	BR	401	DBR	\$1B,\$A1,\$9D,\$
FA7E:	10 FB	402	DBR	\$90,\$8B,\$1D,\$
FA80:	20 3E FE	403	DBR	\$19,\$AE,\$59,\$
FA83:	4C 3C 00 404	DBR	\$24,\$53,\$1B,\$	
FA86:	85 45	405	DBR	\$19,\$A1
FA88:	88	406	DBR	\$0B,\$1A,\$5B,\$
FA89:	48	407	DBR	\$24,\$24
FA8A:	0A	408	DBR	\$AE,\$AE,\$A4,\$
FA8B:	0A	409	DBR	\$7C,\$50
FA8C:	0A	410	DBR	\$15,\$9C,\$8D,\$
FA8D:	30 03	411	DBR	\$84,\$13,\$34,\$
FA8E:	6C FE 03 413	DBR	\$21,\$A0	
FA92:	24 4C FE 414	DBR	\$0B,\$62,\$5A,\$	
FA93:	68	415	DBR	\$94,\$58,\$54,\$
FA96:	68	416	DBR	\$68,\$44,\$5E,\$
FA97:	65 3A	417	DBR	\$0A,\$84,\$74,\$
FA99:	68 3A	418	DBR	\$7A,\$F4,\$CC,\$
FA9A:	65 38	419	DBR	\$4,\$84,\$8A
FA9C:	20 A2 FA 420	DBR	\$00,\$A4,\$A2,\$	
FA9E:	20 DA FA 420	DBR	\$74,\$72,\$72	
FAA2:	4C 05 FE 421	DBR	\$44,\$38,\$82,\$	
FAA3:	18	422	DBR	\$22,\$50
FAA4:	18	423	DBR	\$1A,\$1A,\$2A,\$
FAA5:	68	424	DBR	\$88,\$8C
FAA6:	68	425	DBR	\$1A,\$1A,\$2A,\$
FAA7:	68	426	DBR	\$00,\$A4,\$A2,\$
FAA8:	68	427	DBR	\$74,\$72,\$72
FAA9:	85 3B	428	DBR	\$44,\$38,\$82,\$
FAAB:	A5 2F	429	DBR	\$22,\$50
FAAC:	20 5E	430	DBR	\$1A,\$1A,\$2A,\$
FAAD:	84 3B	431	DBR	\$88,\$8C
FAAE:	18	432	DBR	\$1A,\$1A,\$2A,\$
FAB7:	90 14	433	DBR	\$00,\$A4,\$A2,\$
FAB9:	20 54	434	DBR	\$74,\$72,\$72
FABD:	AA	435	DBR	\$44,\$38,\$82,\$
FABE:	98	436	DBR	\$22,\$50
FABF:	98	437	DBR	\$1A,\$1A,\$2A,\$
FAC0:	48	438	DBR	\$88,\$8C
FAC1:	DA	439	DBR	\$1A,\$1A,\$2A,\$



PC10:	C6 24	620	85	DEC	CH	DECREMENT CURSOR H INDEX
PC11:	10 58	621		DEL	R13	IF POS, OK, ELSE MOVE UP
PC12:	09 21	622		DEL	WINDOW	SET CH TO WINDOW-1
PC13:	09 24	623		DEL	CH	(RIGHTMOST SCREEN POS)
PC14:	09 24	624		DEL	CH	CURSOR V INDEX
PC15:	A5 22	625		UP		
PC16:	A5 22	626				
PC17:	B1 26	627				
PC18:	C6 25	628				
PC19:	C6 25	629				
PC20:	A5 21	630				
PC21:	20 C1	631				
PC22:	65 21	632				
PC23:	85 28	633				
PC24:	00 C0	634				
PC25:	49 28	635				
PC26:	09 28	636				
PC27:	09 28	637				
PC28:	09 28	638				
PC29:	09 28	639				
PC30:	09 28	640				
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PC109:	09 28	719				
PC110:	09 28	720				
PC111:	09 28	721				
PC112:	09 28	722				
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PC130:	09 28	740				
PC131:	09 28	741				
PC132:	09 28	742				
PC133:	09 28	743				
PC134:	09 28	744				
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PC136:	09 28	746				
PC137:	09 28	747				
PC138:	09 28	748				
PC139:	09 28	749				
PC140:	09 28	750				
PC141:	09 28	751				
PC142:	09 28	752				
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PC152:	09 28	762				
PC153:	09 28	763				
PC154:	09 28	764				
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PC156:	09 28	766				
PC157:	09 28	767				
PC158:	09 28	768				
PC159:	09 28	769				
PC160:	09 28	770				
PC161:	09 28	771				
PC162:	09 28	772				
PC163:	09 28	773				
PC164:	09 28	774				
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PC171:	09 28	781				
PC172:	09 28	782				
PC173:	09 28	783				
PC174:	09 28	784				
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PC181:	09 28	791				
PC182:	09 28	792				
PC183:	09 28	793				
PC184:	09 28	794				
PC185:	09 28	795				
PC186:	09 28	796				
PC187:	09 28	797				
PC188:	09 28	798				
PC189:	09 28	799				
PC190:	09 28	800				

FE49: A9 AD 511 LDA #5AD  
 FE4B: 20 ED FD 512 JSR COOT  
 FE4C: 81 42 513 LDA (A4L),Y  
 FE4D: 20 CA FD 514 JSR PRBYTE  
 FE4E: A9 A9 515 LDA #5A9  
 FE4F: 20 ED FD 516 JSR COOT  
 FE50: 20 34 FC 517 JSR NXTA1  
 FE51: 90 D5 518 BCC VFY  
 FE52: 00 519 RTS  
 FE53: 20 75 FE 320 JSR AIPC  
 FE54: A5 14 521 LDA #514  
 FE55: 48 522 PHA  
 FE56: 20 D0 F8 523 JSR INSTDSP  
 FE57: 20 53 F9 524 JSR FCACJ  
 FE58: 05 3A 525 STA FCL  
 FE59: 84 JB 526 STY PCH  
 FE5A: 00 527 PLA  
 FE5B: 28 528 SEC  
 FE5C: E9 01 529 CEV  
 FE5D: D0 EF 530 DNE  
 FE5E: 60 931 RTS  
 FE5F: CA 932 TXA  
 FE60: 05 07 933 BEQ AIPCRTS  
 FE61: 05 3C 934 LDA ALL,X  
 FE62: 05 3A 935 STA PCL,X  
 FE63: CA 536 DEX  
 FE64: 10 F9 937 BPL AIPCLP  
 FE65: A0 0F 938 LDY #53F  
 FE66: D0 02 939 BNE SETIFLG  
 FE67: A3 FF 940 LDY #5FF  
 FE68: 84 32 941 STY INVEFLG  
 FE69: A9 00 942 RTS  
 FE6A: A9 00 943 SETKBD  
 FE6B: 85 3E 944 STA A2L  
 FE6C: A2 38 945 LDX #KSWL  
 FE6D: A0 1B 946 LDY #KEYIN  
 FE6E: D0 08 947 BNE IOPRT  
 FE6F: A9 00 948 SETVID  
 FE70: A2 3E 949 OUTPORT  
 FE71: A2 3E 950 OUTPRT  
 FE72: A2 3E 951 LDX #CSWL  
 FE73: A0 F0 952 LDY #COUT1  
 FE74: A5 3E 953 AND #50F  
 FE75: 20 0F 954 BCO IOPRT1  
 FE76: F0 06 955 JSR IOPRT1  
 FE77: 09 C0 956 LDA #500  
 FE78: F0 02 957 JSR IOPRT2  
 FE79: A9 FC 958 LDA #COUT1/256  
 FE7A: 94 00 959 STA LOC0,X  
 FE7B: 65 01 960 STA LOC1,X  
 FE7C: EA 961 NOP  
 FE7D: EA 962 NOP  
 FE7E: 4C 00 E0 565 JMP BASIC  
 FE7F: 4C 03 E0 566 JMP BASCON  
 FE80: 20 75 FE 567 JSR AIPC  
 FE81: 20 3F FF 568 JSR RESTORE  
 FE82: 0C 3A 00 569 JMP (PCL)  
 FE83: 4C D7 FA 570 JMP RECDSP  
 FE84: C0 34 571 DEC YSAV  
 FE85: 20 75 FE 572 JSR AIPC  
 FE86: 4C FA 573 JMP STEP  
 FE87: 4C FB 03 574 JMP USRADR  
 FE88: A9 40 575 LDA #540  
 FE89: 20 C9 FC 576 JSR HEADR  
 FE8A: A2 27 577 LDY #527  
 FE8B: A2 00 578 EOR #K1  
 FE8C: A2 3C 579 LDA (ALL,X)  
 FE8D: 48 900 PHA  
 FE8E: A1 3C 901 LDA (ALL,X)

FE8F: 20 3A FC 963 JSR NXTA1  
 FE90: A0 1D 964 LDY #51D  
 FE91: 90 EE 965 BCC #R1  
 FE92: A0 22 FE 966 JSR #RBYTE  
 FE93: 20 ED FE 967 BEQ BELL  
 FE94: F0 4D 968 JSR BELL  
 FE95: A2 10 969 LDY #510  
 FE96: 0A 991 ASL A  
 FE97: 20 D6 FC 992 JSR #RBYTE  
 FE98: D0 FA 993 BNE WRBYT2  
 FE99: 60 994 RTS  
 FE9A: 20 00 FE 995 CRMON  
 FE9B: 68 996 PLA  
 FE9C: 08 997 PLA  
 FE9D: D0 6C 998 BNE MONZ  
 FE9E: 20 FA FC 999 JSR RD2BIT  
 FE9F: A9 16 1000 LDA #516  
 FF00: 20 C9 FC 1001 JSR HEADR  
 FF01: 85 2E 1002 STA CHKSUM  
 FF02: 20 FA FC 1003 JSR RD2BIT  
 FF03: A0 24 1004 LDA #524  
 FF04: 20 FD FC 1005 LDY #524  
 FF05: B0 F9 1006 BCS RD2  
 FF06: 20 FD FC 1007 JSR RDBIT  
 FF07: A0 38 1008 LDY #53B  
 FF08: 20 EC FC 1009 RD3 JSR RDBYTE  
 FF09: 81 3C 1010 STA (ALL,X)  
 FF0A: 45 2E 1011 EOR CHKSUM  
 FF0B: 85 2E 1012 STA CHKSUM  
 FF0C: A0 3A FC 1013 JSR NXTA1  
 FF0D: 90 0A 1014 LDY #535  
 FF0E: 20 EC FC 1015 JSR RDBYTE  
 FF0F: C5 2E 1016 CMP CHKSUM  
 FF10: F0 0D 1017 BEQ BELL  
 FF11: A9 C5 1018 LDA #5C5  
 FF12: 20 ED FD 1026 JSR COUT  
 FF13: A9 D2 1027 LDA #5D2  
 FF14: 20 ED FD 1028 JSR COUT  
 FF15: 20 ED FD 1029 JSR COUT  
 FF16: 47 1024 BELL  
 FF17: 4C LD FD 1025 J4P COUT  
 FF18: 4C 48 1026 RESTORE  
 FF19: 40 45 1027 LDA ACC  
 FF20: A4 47 1028 LDY XREG  
 FF21: 20 1029 RESTRI  
 FF22: 20 1030 RESTRI  
 FF23: 20 1031 RESTRI  
 FF24: 05 45 1032 SAVE  
 FF25: 86 46 1033 SAVI  
 FF26: 84 47 1034 SAVI  
 FF27: 08 1035 PIP  
 FF28: 00 1036 STA ACC  
 FF29: 05 45 1037 STA XREG  
 FF2A: 86 46 1038 STA YREG  
 FF2B: 84 47 1039 STA YREG  
 FF2C: 08 1040 PIP  
 FF2D: 00 1041 STA STATUS  
 FF2E: 05 46 1042 STA STATUS  
 FF2F: 8A 1043 STA XSAV  
 FF30: 86 49 1044 STA SPNT  
 FF31: C8 1045 CLD  
 FF32: 20 64 FE 1042 RESET  
 FF33: 20 2F FE 1043 JSR INIT  
 FF34: 20 53 FE 1044 JSR SERVID  
 FF35: 20 09 FE 1045 JSR SEIKBD  
 FF36: D0 3A FF 1046 MON  
 FF37: A9 4A 1047 JSR BELL  
 FF38: A9 4A 1048 JSR BELL  
 FF39: 20 33 FF 1049 LDA PROMPT  
 FF3A: 20 C7 FF 1050 JSR GETLNZ  
 FF3B: 20 C7 FF 1051 JSR ZMODE  
 FF3C: 20 A7 FF 1052 JSR GETNUM  
 FF3D: 84 34 1053 CHAR IN A-REG  
 FF3E: 84 34 1054 STY YSAV

IF USER SPEC'D ADR  
 COPY FROM A1 TO PC  
 MOVE A1 (2 BYTES) TO  
 PC IF SPEC'D AND  
 DISSEMBLE 2J INSTRS  
 ADJUST PC EACH INSTR

NEXT OF 2J INSTRS

SET FOR INVERSE VID  
 VIA COUT1  
 SET FOR NORMAL VID

SIMULATE PORT #0 INPUT  
 SPECIFIED (KEYIN ROUTINE)

SIMULATE PORT #0 OUTPUT  
 SPECIFIED (COUT1 ROUTINE)

SET RAM IN VECTORS

TO BASIC WITH SCRATCH  
 CONTINUE BASIC  
 ADR TO PC IF SPEC'D  
 RESTORE META REGS  
 GO TO USER SUBR  
 TO REG DISPLAY

ADR TO PC IF SPEC'D  
 TAKE ONE STEP  
 TO USER SUBR AT USRADR  
 WRITE 10-SEC HEADER

MONZ  
 FIND TAPEIN EDGE  
 DELAY 3.5 SECONDS  
 INIT CHKSUM=5FF  
 FIND TAPEIN EDGE  
 LOOK FOR SYNC BIT  
 (SHORT J)  
 LOOP UNTIL FOUND  
 SKIP SECOND SYNC H-CYCLE  
 INDEX FOR J/1 TEST  
 STORE AT (A1)  
 UPDATE RUNNING CHKSUM  
 INCR A1, COMPARE TO A2  
 COMPENSATE W/1 INDEX  
 LOOP UNTIL DONE  
 READ CHKSUM BYTE  
 GOOD, SOUND BELL AND RETURN  
 PRINT "ERR", THEN BELL  
 OUTPUT BELL AND RETURN  
 RESTORE 6502 REG CONTENTS  
 USED BY DEBUG SOFTWARE  
 SAVE 6502 REG CONTENTS  
 SET SCREEN MODE  
 AND INIT MSD/SCREEN  
 AS I/O DEV'S  
 MUST SET HEX MODE!  
 \*\* PROMPT FOR MON  
 READ A LINE  
 CLEAR MON MODE, SCAN IDX  
 GET ITEN, NON-HEX  
 CHAR IN A-REG



FF4C SAV1  
 FF73 NXTITM  
 FF9B NXTBAS  
 FFBE TOSUB

**SYMBOL TABLE  
 (ALPHABETICAL ORDER)**

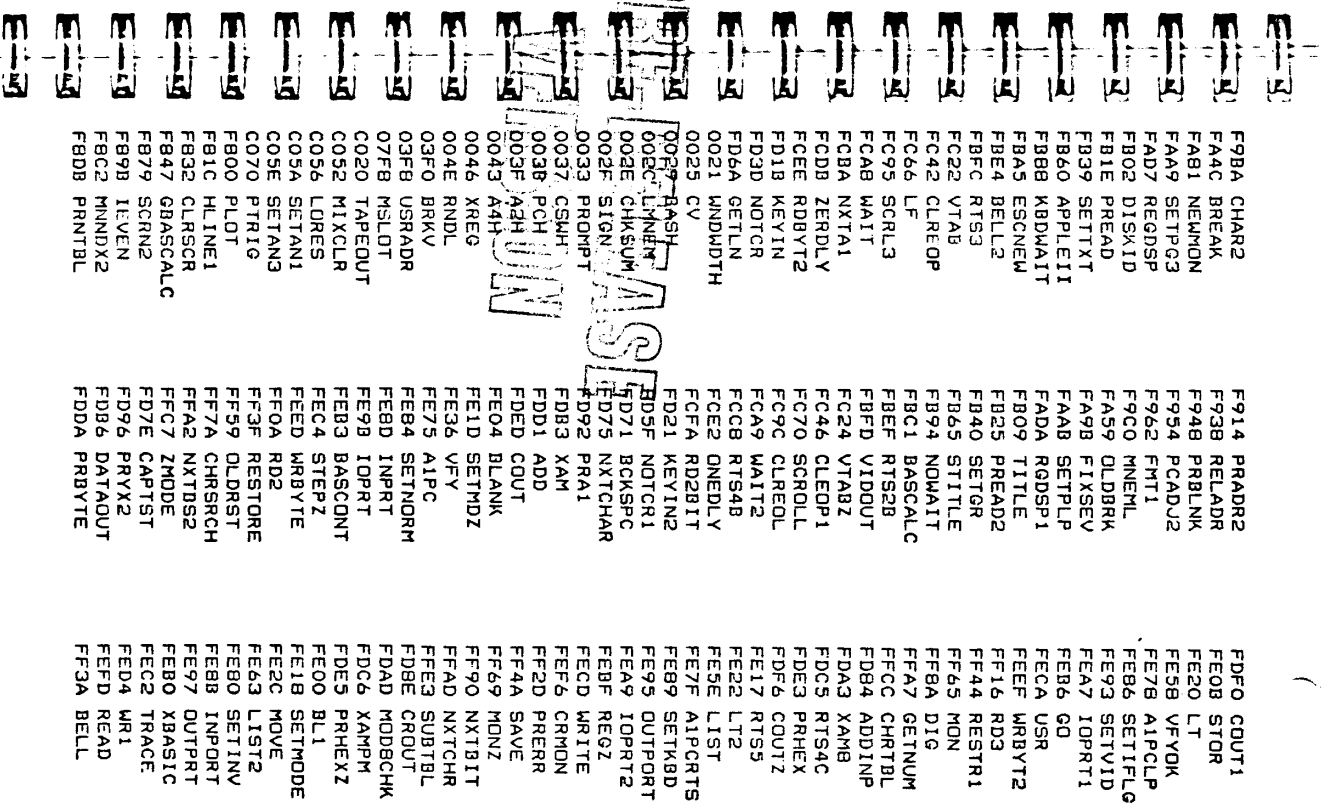
003D A1H	F956 PCADJ3	FEA7 IOPRT1
FE7F A1PCRTS	0095 PICK	FA40 IRG
0040 A3L	F910 PRADR1	FD1B KEYIN
0044 A5L	F930 PRADR5	002F LASTIN
FBF4 ADVANCE	FDDA PRBYTE	FE5E LIST
002A BAS2L	FDE3 PRHEX	0001 LOC1
0029 BASH	FBDB PRNTBL	FE20 LT
FD71 BCKSPC	0033 PROMPT	F9C0 MNEML
FE00 BL1	03F4 PWREDUP	FBC9 MNNDX3
FC10 BS	FF16 RD3	FF65 MON
F9BA CHAR2	FD35 RDCHAR	03FB NMI
0024 CH	FAD7 REGDSP	FB94 NOWAIT
C059 CLRANO	FF3F RESTORE	FF90 NXTBIT
FC9C CLREOL	004F RNDH	FFAD NXTCHR
F83C CLRSC3	F87F RTMSKZ	FF59 OLDRST
FDED COUT	F961 RTS2	C064 PADDLO
FC62 CR	003C A1L	F95C PCADJ4
0025 CV	003F A2H	F80E PLOT1
FBA5 ERR	0043 A4H	F914 PRADR2
FB97 ESCOLD	0045 ACC	F94A PRDL2
F9A6 FMT2	03F5 AMPERV	FB1E PREAD
0026 GBASL	FBC1 BASCALC	FDE5 PRHEXZ
FD6A GETLN	E000 BASIC	FBD4 PRNTOP
FCC9 HEADR	FBD9 BELL1	FD96 PRYX2
FB19 HLINE	FE04 BLANK	FAA6 PWRUP
0200 IN	FD62 CANCEL	FCFD RDBIT
FB82 INSDS1	002E CHKSUM	FD0C RDKY
C000 IOADR	FCA0 CLEOL2	FEBF REGZ
03FE IRGLOC	C05B CLRAN1	FF44 RESTR1
C000 KBD	FC42 CLREOP	004E RNDL
0038 KSWL	F832 CLRSCR	FB31 RTS1
0400 LINE1	FDFO COUT1	FBFC RTS3
0000 LOCO	FEF6 CRMON	FE7B A1PCLP
FE22 LT2	FDB6 DATAUT	003E A2L
C053 MIXSET	FC2C ESC1	0042 A4L
FBC2 MNNDX2	FD2F ESC	FDB4 ADDINP
FF69 MONZ	002E FORMAT	FB60 APPLEII
FAB1 NEWMON	FB56 GBCALC	FBDO BASCLC2
FD5F NOTCR1	FFA7 GETNUM	E003 BASIC2
FF9B NXTBAS	C057 HIRES	FBE4 BELL2
FD75 NXTCHAR	FC5B HOME	FA4C BREAK
FA59 OLDBRK	FB2F INIT	FD7E CAPTST
FE97 OUTPRT	FB8C INSDS2	FF7A CHRSRCH

PRE-RELEASE  
 VERSION

FC9E CLEOLZ	FF3A BELL	C05C SETAN2
C05D CLRAN2	03F0 BRKV	FE86 SETIFLG
CFFD CLRROM	F9B4 CHAR1	FE18 SETMODE
F836 CLRTOP	FFCC CHRTBL	FB6F SETPWRC
FDF6 COUTZ	FC46 CLEOP1	002F SIGN
0037 CSWH	C05F CLRANG3	0049 SPNT
FFBA DIG	F83B CLRSC2	FE0B STOR
FBA5 ESCNEW	0030 COLOR	C060 TAPEIN
FA9B FIXSEV	FD8E CROUT	FEC2 TRACE
F847 GBASCALC	0036 CSWL	FECA USR
FBA9 GETFMT	FB02 DISKID	FE5B VFYOK
FEB6 GO	FB9B ESCNOW	F82B VLINE
C055 HISCR	F962 FMT1	FCAB WAIT
F89B IEVEN	0027 GBASH	0022 WNDTOP
FE8B INPORT	FD67 GETLNZ	FEEF WRBYT2
FBDO INSTDSP	002C H2	FDA3 XAMB
FEA9 IOPRT2	FB1C HLINE1	FB11 XLTBL
C010 KBDSTRB	FA6F INITAN	0034 YSAV
FD21 KEYIN2	FE8D INPRT	FC8C SCRL2
002F LENGTH	0032 INVFLG	FC70 SCROLL
FE63 LIST2	FE9B IOPRT	C05E SETAN3
C056 LORES	FB8B KBDWAIT	FE80 SETINV
002E MASH	0039 KSWH	FE84 SETNORM
FA00 MNEMR	FC66 LF	FB39 SETTXT
FDAD MODBCHK	002C LMNEM	FABA SLOOP
FE26 MOVE	C054 LOWSCR	0048 STATUS
FAA3 NOFIX	C052 MIXCLR	FBFO STORADV
FCBA NXTA1	FB8E MNNDX1	C020 TAPEOUT
FFA2 NXTBS2	0031 MODE	C050 TXTCLR
FBF5 NXTCOL	07FB MSLDT	03FB USRADR
FCE2 ONEDLY	FD3D NOTCR	FBFD VIDOUT
F954 PCADJ2	FCB4 NXTA4	FC24 VTABZ
003B PCH	FAC7 NXTBYT	FCAA WAIT3
FB00 PLOT	FF73 NXTITM	0021 WNDWOTH
F926 PRADR3	FE95 OUTPORT	FEED WRBYTE
F94C PRBL3	F953 PCADJ	FDC6 XAMP
FB25 PREAD2	003A PCL	0046 XREG
FBF9 PRMN2	FD92 PRA1	FCDB ZERDLY
F944 PRNTX	F92A PRADR4	FF4C SAV1
C070 PTRIG	F94B PRBLNK	FC95 SCRL3
FCFA RD2BIT	FF2D PRERR	C058 SETANO
FCEE RDBYT2	F941 PRNTAX	FB64 SETCOL
FAE4 RDSP1	F940 PRNTYX	FE89 SETKBD
F93B RELADR	FAFD PWRCON	FAA9 SETPG3
FADA RCDSP1	FF0A RD2	FE93 SETVID
FB19 RTBL	FCEC RDBYTE	03F2 SOFTEV
FBF7 RTS2B	FEFD READ	FEC4 STEPZ
FCCB RTS4B	FA62 RESET	FFE3 SUBTBL
FE75 A1PC	002D RMNEM	FB09 TITLE
0041 A3H	FB0C RTMASK	C051 TXTSET
0045 A5H	FB2E RTS2D	002D V2
FDD1 ADD	FDC5 RTS4C	FB7B VIDWAIT
002B BAS2H	FE17 RTS5	FC22 VTAB
FE83 BASCON	FC2B RTS4	0023 WNDBTM
002B BASL	FC76 SCRL1	FED4 WR1
	FB79 SCRN2	

**SYMBOL TABLE  
(NUMERICAL ORDER)**

0000	LOC0	FC76	SCRLL1	FB5B	TABV
0022	WNDTOP	FC9E	CLEDLZ	FB7B	VIDMAIT
0026	GBASL	FCAA	MAIT3	FB9B	ESCNOM
002A	BAS2L	FCG9	HEADR	FB09	BELLI
002D	V2	FCES	WRITAPE	FBF4	ADVANCE
002E	FORMAT	FCFD	RDBIT	FC1A	UP
0030	COLOR	FD2F	ESC	FC2C	ESC1
0034	YSAV	FD62	CANCEL	FC62	CR
003B	KSML	0001	LOC1	FC8C	SCRLL2
003C	A1L	0023	WNDBTM	FC9A	CLEDL2
0040	ASL	0027	GBASH	FCB4	NXTA4
0044	ASL	002B	BAS2H	FC06	WRBIT
0047	YREG	002D	RNMEN	FCCE	RDBYTE
004F	RNDH	002F	LASTIN	FD0C	RDKEY
03F2	SOFTEV	0031	MODE	FD35	RDCHAR
03FB	NMI	0035	YSAV1	FD67	GETLNZ
0000	IOADR	0039	KSWM	0020	WMDLFT
0030	SPKR	003D	A1H	0024	CH
0053	MIXSET	0041	A3H	002B	BASL
0057	HIRES	0045	ASH	002C	H2
0058	CLRAN1	0048	STATUS	002E	MASK
005F	CLRAN3	0095	PICK	002F	LENGTH
00FF	CLRDM	03F4	PUREDUP	0032	INVLG
FB0C	RTMASH	03FE	IRQLDC	0036	CSML
FB26	VLINZ	0000	KBD	003A	PCL
FB36	CLRTOP	0054	XTCLR	003E	A2L
FB56	GBCALC	005A	LWSCR	0042	AAL
FB7F	RTMSKZ	0058	SETANO	0045	ACC
FBA5	ERR	005C	SETAN2	0049	SPNT
FBC9	MNNDX3	0060	TAPEIN	0200	IN
FBF5	NXTCOL	E000	BASIC	03F5	AMPERV
F926	PRADR3	FB0E	PLOT1	0400	LINE1
F940	PRNTYX	FB2B	VLIN	0010	KBDSTRB
F94A	PRBL2	FB3B	CLRSC2	0051	TXTSET
F956	PCADUJ3	FB64	SETCOL	0055	HISCR
F9A6	FMT2	FB82	INSDS1	0059	CLRAN2
FA00	MNEKR	FB82	GETFMT	005D	CLRAN2
FA62	RESET	FB82	INSDS1	0064	PADDLO
FAA3	NOP1X	FB82	PRM2	E003	BASIC2
FABA	SLDOP	FB82	PRADR4	FB19	HLIN
FAB1	XLTLB	F92A	PRADR4	FB31	RTS1
FB2E	RTS2D	F94C	PRBL3	FB3C	CLRSC3
FB4B	SETLND	F95C	PCADUJ4	FB71	SCRN
FB4F	SETPMRC	F9B4	CHAR1	FB8C	INSDS2
FB97	SETCOLD	FA40	IRG	FB8E	MNNDX1
FBDD	BASCLOC2	FA46	PRUP	FBDA	PRNTOP
FBFO	STORADV	FAA6	PWRUP	F910	PRADR1
FC10	BS	FAF7	NXTBYT	F930	PRADR5
FC2B	RTS4	FAFD	PURBLN	F944	PRNTX
FC58	HOME	FB19	RTBL	F953	PCADUJ
		FB2F	INIT	F961	RTS2



FECD WRITE  
FDB3 XAM  
0047 YREG  
FFC7 ZMODE  
FF4A SAVE  
FB71 SCRN  
C05A SETAN1  
FB40 SETGR  
FE1D SETMDZ  
FAAB SETPLP  
FB4B SETWND  
C030 SPKR  
FB65 STITLE  
FB5B TABV  
FFBE TOSUB  
FC1A UP  
FE36 VFY  
FB26 VLINEZ  
FCA9 WAIT2  
0020 WNDLFT  
FCD6 WRBIT  
FCE5 WRTAPE  
FEB0 XBASIC  
0035 YSAV1

PRE-RELEASE  
VERSION

SYMBOL TABLE SIZE  
2589 BYTES USED  
2531 BYTES REMAINING

SLIST 4A

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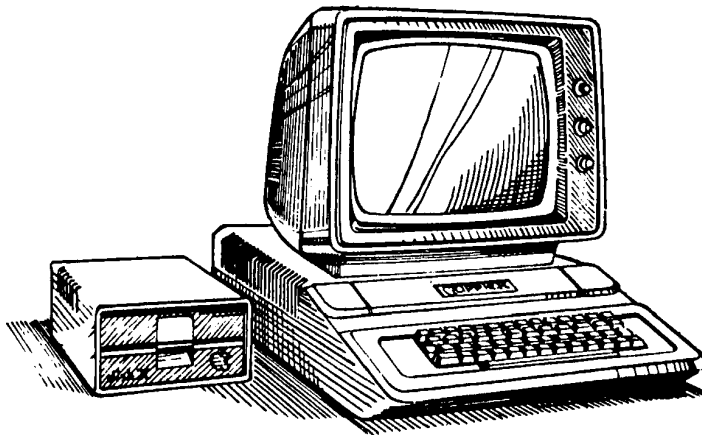


## **Apple II Computer Technical Information**

# **APPLE II / APPLE II-PLUS LEVEL II SERVICE REFERENCE MANUAL**

**Pre-Release Version**

## **APPENDIX B BILL OF MATERIALS**



**Written by  
Apple Computer, Inc. • Level II Service Center  
1981**

( This page is not part of the original service manual )

EFFECTIVITY DATE: 012581

S I N G L E L E V E L B I L L S

PARENT PART: 606-0148 M UNTESTED A2 STD 48K SYSTEM, RFI UM:  
 ERC: B SRCE CODE: A TYPE: 1 ABC:

ITEM NO.	COMPONENT PART NUMBER	E R C	DESCRIPTION REMARKS	PR COMM CD	ST Y C	S P R C N	A P B L U M	EA
000	606-0116D	0	DWG, ASSY A2 STD RFI	EX	* 7	* * EA		
003	333-4116	7 2	IC, 16K RAM MRKD "APPLE" (NO BURN)	RL	P 1	P A P EA		
004	101-4016	0	RES 1/4W 5% 1 MEG OHM K13	RP	P 1	P B P EA		
005	820-0044	A	PCB, A2 MAIN LOGIC BD RFI	RP	P 1	P A P EA		
006	101-4100	0	RES 1/4W 5% 10 OHM J14	RP	P 1	P B P EA		
007	101-4101	0	RES 1/4W 5% 100 OHM 4-J13, K14	RP	P 1	P B P EA		
008	101-4102	0	RES 1/4W 5% 1K OHM F14, A13, B3, 2-D1	RP	P 1	P B P EA		
009	101-4123	0	RES 1/4W 5% 12K OHM 5-K13, B3	RP	P 1	P B P EA		
010	101-4151	0	RES 1/4W 5% 150 OHM A1	RP	P 1	P B P EA		
011	101-4152	0	RES 1/4W 5% 1.5K OHM J14	RP	P 1	P B P EA		
012	101-4202	0	RES 1/4W 5% 2K OHM J14	RP	P 1	P B P EA		
013	101-4225	0	RES 1/4W 5% 2.2 MEG OHM A13	RP	P 1	P B P EA		
014	101-4270	0	RES 1/4W 5% 27 OHM B14, K14	RP	P 1	P B P EA		
015	101-4272	0	RES 1/4W 5% 2.7K OHM J14	RP	P 1	P B P EA		
016	101-4331	0	RES 1/4W 5% 330 OHM A1	RP	P 1	P B P EA		
017	101-4335	0	RES 1/4W 5% 3.3 MEG OHM B3	RP	P 1	P B P EA		
018	101-4470	0	RES 1/4W 5% 47 OHM 2-A1	RP	P 1	P B P EA		
019	101-4472	0	RES 1/4W 5% 4.7K OHM	RP	P 1	P B P EA		

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EFFECTIVITY DATE: 017381

S I N G L E L E V E L B I L L S O F

PARENT PART: 606-0148

M UNTESTED A2 STD 48K SYSTEM, RFI  
ERC: B SRCE CODE: A TYPE: 1

UM: EA  
ABC: A

ITEM NO.	COMPONENT PART NUMBER	E R C	DESCRIPTION REMARKS	PR CD	COMM CODE	S C	T P	S R	A C	P N	EXTEN OT: PEP	
020	101-4473	0	F13 RES 1/4W 5% 47K OHM	RP		P	1	P	B	P	EA	1
021	109-0001	0	J13 POT, TRIM 200 OHMS 20%	RP		P	1	P	B	P	EA	1
022	111-0001	0	J14 RES ARRAY 7 X 1K OHMS	RP		P	1	P	B	P	EA	3
023	131-5701	0	K13,E11,D11 CAP, 47PF 5% N470 50V	RP		P	1	P	B	P	EA	1
024	136-2401	A	H14 CAP, .022UF 10% X7R 50V	RP		P	1	P	B	P	EA	4
025	135-9101	A	4-H13 CAP, .1UF +80-20% Z5U/Y5V 50V	RP		P	1	P	A	P	EA	45
026	138-0001	M 0	F14 CAP, VARIABLE CERAMIC TRIMMER 5-50PF	RP		P	1	P	B	P	EA	1
027	151-5501	B	H14 CHOKE, 27UH 10%	RP		P	1	P	A	P	EA	1
029	301-0166	0	A3 IC, 74166	RI		P	1	P	B	P	EA	1
030	301-9334	0	F14 IC, 9334	RI		P	1	P	A	P	EA	1
031	305-0000	0	A2 IC, 74LS00N	RI		P	1	P	A	P	EA	1
032	305-0002	0	B13,B14,A12,A14 IC, 74LS02N	RI		P	1	P	A	P	EA	4
033	305-0004	0	C11 IC, 74LS04	RI		P	1	P	A	P	EA	1
034	305-0008	0	B11,H1 IC, 74LS08	RI		P	1	P	A	P	EA	2
035	305-0011	0	B12 IC, 74LS11	RI		P	1	P	A	P	EA	1
036	305-0020	0	D2 IC, 74LS20	RI		P	1	P	A	P	EA	1
037	305-0032	0	D2 IC, 74LS32	RI		P	1	P	A	P	EA	1

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EFFECTIVITY DATE: 012381

S I N G L E L E V E L B I L L S O F M

PARENT PART: 606-0148 M UNTESTED A2 STD 48K SYSTEM, RFI UM: EA  
 ERC: B SRCE CODE: A TYPE: 1 ABC: A

I.L.M NO.	COMPONENT PART NUMBER	E R C	DESCRIPTION REMARKS	PR CD	COMM CODE	S T S A P					EXTENDED QTY PER		
						R	Y	P	B	L			
038	305-0051	0	C14 IC, 74LS51	RI		P	1	P	A	P	E	A	1
039	305-0074	0	C13 IC, 74LS74	RI		P	1	P	A	P	E	A	3
040	305-0138	0	B10,J13,A11 IC, 74LS138	RI		P	1	P	A	P	E	A	4
041	305-0139	0	H2,H12,F12,F13 IC, 74LS139	RI		P	1	P	A	P	E	A	1
042	305-0151	0	F2 IC, 74LS151	RI		P	1	P	A	P	E	A	1
043	305-0153	0	A9 IC, 74LS153	RI		P	1	P	A	P	E	A	4
044	305-0161	0	E11,E12,E13,C1 IC, 74LS161	RI		P	1	P	A	P	E	A	4
045	305-0174	0	D11,D12,D13,D14 IC, 74LS174	RI		P	1	P	A	P	E	A	2
046	305-0194	0	B5,B8 IC, 74LS194	RI		P	1	P	A	P	E	A	3
047	305-0251	0	B4,B9,A10 IC, 74LS251	RI		P	1	P	A	P	E	A	1
048	305-0257	0	H14 IC, 74LS257	RI		P	1	P	A	P	E	A	5
049	305-0283	0	B6,B7,J1,C12,A8 IC, 74LS283	RI		P	1	P	A	P	E	A	1
050	307-0086	0	E14 IC, 74S86	RI		P	1	P	A	P	E	A	1
051	307-0175	0	B2 IC, 74S175	RI		P	1	P	A	P	E	A	1
052	307-0195	0	B1 IC, 74S195 OR 93S00	RI		P	1	P	A	P	E	A	1
053	315-8304	0	C2 IC, 8304B 8-BIT TRI-STATE	RI		P	1	P	A	P	E	A	1
054	315-0897	? 0	H10	RI		P	1	P	A	P	E	A	3

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EFFECTIVITY DATE: 012381

S I N G L E L E V E L B I L L S O F

PARENT PART: 606-0148 M UNTESTED A2 STD 48K SYSTEM, RFI UM: EA  
 ERC: B SRCE CODE: A TYPE: 1 ABC: A

ITEM NO.	COMPONENT PART NUMBER	DESCRIPTION REMARKS	PR CD	COMM CODE	R Y C	S T S A P P R C N U M	EXTENS QTY PER
		IC, 8T97 H3,H4,H5				P 1 P B P E A	2
055	329-0555	IC, 555 TIMER B3,A13				P 1 P B P E A	1
056	329-0558	IC, NE558 H13				P 1 P A P E A	1
058	337-6502	IC/MICROPROCESSOR 6502 H7				P 1 P B P E A	1
063	353-0741	IC, 741CN-8 PIN MINIDIP K13				P 1 P B P E A	1
064	371-4148	DIODE, 1N4148 J13				P 1 P B P E A	3
065	372-3904	TRANSISTOR, 2N3904 J14,A13,F13				P 5 P B P E A	2
67	372-4258	TRANSISTOR, XX4258 2-A1				P 1 P B P E A	1
068	376-0003	TRANSISTOR, MPSA13 J14				P 1 P B P E A	3
069	511-0801	SOCKET, IC 8 PIN K13,B3,A13				P 1 P A P E A	16
070	511-1401	SOCKET, IC 14 PIN A2,A11,A12,A14,B2, B10-13,B14,C11,C13, C14,D2,H1,J13				P 1 P A P E A	59
071	511-1601	SOCKET, IC 16 PIN A3,A7-A10,B1, B4-B9,C1-C10,C12, D3-D14,E4-E14,F2, F12-14,H2-5,H12-14, J1,J14				P 1 P B P E A	7
072	511-2401	SOCKET, IC 24 PIN A5,F3,F5,F6,F8, F9,F11				P 1 P B P E A	1
073	511-4001	SOCKET, IC 40 PIN H7				P 1 P A P E A	8
074	513-5001	CONNECTOR 50 PIN					

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APPLE COMPUTER, INC.

EFFECTIVITY DATE: 012381

S I N G L E L E V E L B I L L S O F M

PARENT PART: 606-0148

M UNTESTED A2 STD 48K SYSTEM, RFI  
ERC: B SRCE CODE: A TYPE: 1

UM: EA  
ABC: A

ITEM NO.	COMPONENT PART NUMBER	DESCRIPTION REMARKS	PR COMM CD	ST S A P Y P B L C P R C N U M	EXTENDED QTY PER
075	515-0001	JACK, PHONO RT ANG (MON) K14	RP	P 1 P B P EA	1
076	515-0002	JACK, PHONE 2-K13	RP	P 1 P B P EA	2
077	515-0054	CONN, STRAIGHT HEADER 4 PIN		P * P * P EA	2
078	515-0053	CONN, STRAIGHT HEADER 2 PIN		P * P * P EA	2
080	519-0001	CONNECTOR, 6 PIN AMP 9-350258-1 K1	RC	P 1 P B P EA	1
081	341-0016	ROM, UTILITY DD	RL	P 1 P A P EA	1
082	000-0000	NOT USED THIS ASSEMBLY		D * P B P EA	0
083	341-0001	ROM 16K E0	RL	P 1 P B P EA	1
084	341-0002	ROM 16K E8	RL	P 1 P B P EA	1
085	341-0003	ROM 16K F0	RL	P 1 P B P EA	1
086	341-0004	ROM 16K F8	RL	P 1 P B P EA	1
087	197-0001	CRYSTAL, 14,318630 MHZ	RI	P 1 P B P EA	1
088	908-0003	ADHESIVE, RTV #3145 GRAY	EX	X 1 P B P EA	0,0100
089	341-0036	ROM, SPCL A5	RL 1	P 1 P B P EA	1
090	156-0005	CHOKE, WIDE BAND RFI TYPE 4-J1, K13	RP	P 1 P B P EA	5
091	511-2001	SOCKET, IC 20 PIN H10	RP	P 1 P B P EA	1
092	132-7101	CAP, .001UF 20% Z5R 500VDC K3, K4, K5, K6, K8 K9, 2-K11	RP	P 1 P B P EA	8
093	511-1602	SOCKET, IC 16 PIN DIP (KEYED) E3	RP	P 1 P B P EA	1
094	125-5101	CAP, 10UF 16V K1	RP	P 1 P B P EA	1

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REV. 0

BOARD LOCATION	PART DESCRIPTION	APPLE PART #	OTHER LOCATION	SCHEMATIC DESIGNATION
A1 (2)	.1uf Capacitor	135-9101		C1
A1	330 Ohm Res 1/4W 5%	101-4331		R1
A1 (2)	2N4258 Transistor	372-4258		Q1,Q2
A1	Xtal, 14.318630 MHZ	197-0001		
A1 (2)	47 Ohm Res 1/4W 5%	101-4470		R2,R4
A1	150 Ohm Res 1/4W 5%	101-4151		
A2	Socket 14Pin 143-S3-T	511-1401	A11-12,B2,B10-14,C-11,C13-14 D1-2,E1,F1,H1 J13	
A2	IC 74LS00	305-0000		
A3	Socket 16Pin 163-S3-T	511-1601	A3,A7-10,B1, B4-9,C1-10,C12, D3-14,E2-14,F2, F12-14,H2-5, H10-14,J1,J14	
A3	IC 74166	or 301-0166 305-0166		
A5	Socket 24Pin 246-S4-T	511-2401	A5,F3,F5,F6,F8 F9, F11	
A5	ROM Character Generator	335-2513		
A7	Keyboard Socket	511-1601	B6-7,C12,J1	
A8	IC74LS257	305-0257		
A9	IC 74LS151	305-0151		
A10	IC74LS194	305-0194	B4, B9	
A11	IC74LS74	305-0074	B10,J13	
A12	IC 74LS02	305-0002	B13,B14	
A13	2N3904 Transistor	372-3904	F13,J14	Q5

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TITLE: APPLE II MOTHERBOARD P/N: 600-0001 REV: Page 1 of 6



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BOARD LOCATION	PART DESCRIPTION	APPLE PART #	OTHER LOCATION	SCHEMATIC DESIGNATION
A13	.1uf Capacitor	135-9101		C4
A13	1K Ohm Res 1/4W 5%	101-4102	F14	R14
A13	2.2M Ohm Res 1/4W 5%	101-4225	K13	R26
A13	IC NE555	329-0555	B3	
A13	Socket 8Pin 083-S3-T	511-0801	B3,K13	
A14	.1uf Capacitor	135-9101		C12
B1	IC 74LS175	307-0175		
B2	IC 74S86	307-0086		
B3	IC NE555	329-0555	A13	
B3	12K Ohm 1/4W 5%	101-4123	K14	R12
B3	3.3M Ohm Res 1/4W 5%	101-4335		R13
B3	.1uf Capacitor	135-9101		C15
B4,B9	IC 74LS194	305-0194	A10	
B5,B8	IC 74LS174	305-0174		
B6,B7	IC 74LS257	305-0257		
B10	IC 74LS74	305-0074	A11,J13	
B11	IC 74LS08	305-0008	H1	
B12	IC 74LS11	305-0011		
B13,14	IC 74LS02	305-0002	A12	
B14	27 Ohm Res 1/4W 5%	101-4270	K14	R25
B15	Speaker Jack	515-0004		
B15	.1uf Capacitor	135-9101		
C1	IC 74LS152	305-0153	E11-13	
C2	IC 74LS195	307-0195		

TITLE: APPLE II MOTHERBOARD P/N: 600-0001 REV: Page 2 of 6



BOARD LOCATION	PART DESCRIPTION	APPLE PART #	OTHER LOCATION	SCHEMATIC DESIGNATION
C3,C10	RAM 4K or 16K	(4K) 333-6604 (16K) 333-4116 (16K) 333-0416		
C3-C5	.1uf Capacitor	135-9101		
C7-C9	.1uf Capacitor	135-9101		
C11	IC 74LS04	305-0004		
C12	IC 74LS257	305-0257	A8, B6-7, J1	
C13	IC 74LS32	305-0032		
C15	.1uf Capacitor	135-9101		
D1	Memory Select Plug	*	E1, F1	
D2	IC 74LS20	305-0020		
D3-D10	RAM 16K or 4K	(4K) 333-6604 (16K) 333-4116 (16K) 333-0416		
D3-D5	.1uf Capacitor	135-9101		
D7-D9	.1uf Capacitor	135-9101		
D10 $\frac{1}{2}$	1K Ohm Resistor Array	111-0001	E10 $\frac{1}{2}$ , K12	RA02
D11-D14	IC 74LS161	305-0161		
D11, D15	.1uf Capacitor	135-9101		
E1	Memory Select Block	*	D1, F1	
E2	IC 74LS139	305-0139	F2	
E3-E10	RAM 16K or 4K	(4K) 333-6604 (16K) 333-4116 (16K) 333-0416		
E3-E5	.1uf Capacitor	135-9101		
E7-E9	.1uf Capacitor	135-9101		
E10 $\frac{1}{2}$	1K Ohm Resistor Array	111-0001	D10 $\frac{1}{2}$ , K12	RA03

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BOARD LOCATION	PART DESCRIPTION	APPLE PART #	OTHER LOCATION	SCHEMATIC DESIGNATION
E11	.1uf Capacitor	135-9101		
E11-E13	IC 74LS153	305-0153		
E14	IC 74LS283	305-0283		
E15	.1uf Capacitor	135-9101		
F1	Memory Select Plug	*	D1,E1	
F2	.1uf Capacitor	135-9101		
F2	IC 74LS139	305-0139	E2	
F3	ROM F8	341-0004		
F5	ROM F0	341-0003		
F6	ROM E8	341-0002		
F8	ROM E0	341-0001		
F9				
F11	ROM D0 Programmer's Aid #1	341-0016 (Optional)		
F12-F13	IC 74LS138	305-0138	H2,H12	
F13	2N3904 Transistor	372-3904	A13,J14	Q6
F13½	4.7K Ohm Res 1/4W 5%	101-4472		R27
F14	9334	301-9334		
F15	1K Ohm Res 1/4W 5%	101-4102	A13	R5
F15	.1uf Capacitor	135-9101		
F15	5-50pf Color Trim Cap	138-0001		C3
H1	IC 74LS08	305-0008	B11	
H2	IC 74LS138	305-0138	F12-F13,H12	
H2	.1uf Capacitor	135-9101		

TITLE: APPLE II MOTHERBOARD P/N: 600-0001 REV: \_\_\_\_\_ Page 4 of 6



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BOARD LOCATION	PART DESCRIPTION	APPLE PART #	OTHER LOCATION	SCHEMATIC DESIGNATION
H3-H5	IC 8797	315-0897		
H7	Socket 40Pin 406-S3-7	511-4001		
H7	IC 6502 Microprocessor	337-6502		
H10-H11	IC 8T28	315-0828		
H12	IC 74LS138	305-0138	F12-13,H2	
H13	IC 558	329-0558		
H13 (4)	.22uf Capacitor	133-8401		C5-C7
H13	.1uf Capacitor	135-9101		C9
H14	IC 74LS251	305-0251		
H15	27uh Choke	151-5501		L1
H15	47pf Capacitor	131-5701		C2
H15	.1uf Capacitor	135-9101		
J1	IC 74LS257	305-0257	A8,B6-7,C12	
J13 (4)	100 Ohm Res 1/4W 5%	101-4101	K14	R20-R23
J13	IC 74LS74	305-0074	A11,B10	
J13 (2)	12K Ohm Res 1/4W 5%	101-4123		R19,R29
J14	MPSA13 Transistor	376-0003		Q4
J14	IN914 Diode	371-0914		CR1
J14	47K Ohm 1/4W 5%	101-4473		R23
J14	Game I/O Socket	511-1601		
J14	Single Pin	515-0005		
J14½	200 Ohm Pot	109-0001		R11
J15	2.7K Ohm Res 1/4W 5%	101-4272		R6

TITLE: APPLE II MOTHERBOARD P/N: 600-0001 REV: \_\_\_\_\_ Page 5 of 6



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BOARD LOCATION	PART DESCRIPTION	APPLE PART #	OTHER LOCATION	SCHEMATIC DESIGNATION
J15	2K Ohm Res 1/4W 5%	101-4202		R8
J15	1.5K Ohm Res 1/4W 5%	101-4152		R7
J15	2N3904 Transistor	372-3904	A13,F13	Q3
J15	10 Ohm Res 1/4W 5%	101-4100		R9
K1	Power Supply Socket	519-0001		
K12	1K Resistor Array	111-0001	D10 $\frac{1}{2}$ ,E10 $\frac{1}{2}$	
K13	IC 74IC	353-0741		
K13	2.2M Ohm 1/4W 5%	101-4225	A13	R15
K13 (2)	12K Ohm 1/4W 5%	101-4123	B3	R16,R30
K13	.1uf Capacitor	135-9101		C10
K14	.1uf Capacitor	135-9101		C11
K14	100 Ohm Res 1/4W 5%	101-4101	J13	R18
K14	27 Ohm Res 1/4W 5%	101-4270	B14	R25
K14 (2)	.1uf Capacitor	135-9101		C13,C14
K14	Video O/P Plug	515-0003		
O-7	Connector 50 Pin	513-5001		
Jack (7)	Phono Cassette	515-0002		
Jack	Phone RCA	515-0001		

\* Memory Select Plug

16K	16K	16K	600-0078
16K	4K	4K	600-0077
4K	4K	4K	600-0076

TITLE: APPLE II MOTHERBOARD P/N: 600-0001 REV: \_\_\_\_\_ Page 6 of 6

# PRE-RELEASE

# VERSION

DATE: 29-SEP-81 10:40

APPLE COMPUTER, INC.

INVENTORY DATE: ALL

SINGLE LEVEL BILLS OF MATERIAL

AGENT PART: 805-8116

CHASSIS A2 STD 16K SYSTEM

UN: EA

ERC: 0

SRCE CODE: A

TYPE: 1

ABC: A

QTY	COMPONENT PART NUMBER	DESCRIPTION	REMARKS	STG	PRY	PL	EXTENDED QUANTITY PER	EO	
2	805-8116B	CHASSIS A2 STD 16K SYSTEM		EX	A	7	3 U EA	0	350
1	805-8116	ASSY, PCB, TST, MOTHERBD STD 16K A2		2H	A	1	P A P EA	1	410
2	400-0009	ASSY, SPEAKER		RM	P	1	P C P EA	1	450
3	399-0027	POWER SUPPLY, UL APPD ASTEC (AS RECD)		UX	P	1	P A P EA	1	250
4	805-8105	SUBASSY TST KEYBD A2 W/ENCODER		UX	A	1	P A P EA	1	690
5	805-0001	BASE, CHASSIS APPLE II		RM	P	1	P B P EA	1	350
3	805-0010	STIFFENER, REAR PANEL		EX	P	1	P C P EA	1	050
7	805-0011	BRACKET, MOUNTING APPLE II KEYBOARD		EX	P	1	P C P EA	2	800
	5-0001	HOUSING, PLASTIC APPLE II		RM	P	1	P B P EA	1	720
8	815-0002	LID, PLASTIC APPLE II		RM	P	1	P B P EA	1	350
0	825-0003	LABEL, 'VIDEO/CASSETTE IN-OUT'		EX	X	1	P C P EA	1	800
1	825-0001	LABEL, NAMEPLATE APPLE II		EX	P	1	P C P EA	1	650
2	825-0067	DESOLETE LABEL, SER1APPLE II STD (UL)		EX	X	7	P C P EA	1	850
3	830-0002	FASTENER, HEAD LOCK 3M#9J-3308R		EX	X	1	P C P EA	4	800
4	830-0003	FASTENER, PC BOARD STANDOFF		EX	X	1	P C P EA	6	630
5	400-3606	SCREW, 6-32 X 3/8 FLT HD (CAD)		EX	X	1	P C P EA	6	550
5	400-3610	SCREW, 6-32 X 5/8 FLT HD (CAD)		EX	X	1	P C P EA	1	550
7	844-0001	SCREW, #4-40 X 3/8 SEMS PAN HD (CD)		EX	X	1	P C P EA	4	800
8	844-0004	SCREW, #6-32 X 3/8 SEMS PAN HD (BK)		EX	X	1	P C P EA	8	800
7	850-4605	SCREW, PHILLIPS UNDERCUT #6 X 5/16		EX	X	1	P C P EA	6	
0	860-0008	SPACER, HEX #6-32 X 1/4 (ALUM)		EX	X	1	P C P EA	1	
1	5-0001	FEET, RUBBER		EX	X	1	P C P EA	4	450
2	908-0003	ADHESIVE, RTV #3145 GRAY		EX	X	1	P B P EA	0.0400	300
3	875-0003	(018) REIDENTIFIED SEE 835-0116		EX	X	1	P C P EA	1	100
4	880-0006	WASHER #6 INTERNAL TOOTH		EX	X	1	P C P EA	1	

PRINTED 29-SEP-81 10:41

APPLE COMPUTER, INC.

EFFECTIVITY DATE: ALL

S I N G L E L E V E L B I L L S C

PARENT PART: 605-6116

CHASSIS A2 STD 16K SYSTEM

UM: 2

ERC: C GRDE CODE: A TYPE: 1

ABC: 1

ITEM NO.	COMPONENT PART NUMBER	DESCRIPTION	STSAF	EXTEN
NO.	NO.	REMARKS	FR R Y F B L	QUANTI
			CD C P R C N UM	PER
025	640-0007	WASHER, PLASTIC, .062 THK	EX X 1 P C P EA	1
026	605-5102	TESTED KEYBOARD A2 GREEN	VX A 5 P A P EA	1
027	825-0004	LABEL, SERIAL # A2 STD	EX X 1 P C P EA	1
028	605-5001	TESTED 110/220V A2 POWER S.	2H A 1 P A P EA	1
029	907-0002	ADHESIVE, LOCKTITE #430 SUPERBONDER	EX X 1 P A P EA	0.0
030	825-0043	LABEL, WARNING ASTEC UL P/S	EX X 1 P C P EA	1
031	944-0057	FOAM PAD, SPEAKER	EX X 1 P C P EA	1
033	000-0000	NOT USED THIS ASSEMBLY	D * P D P EA	0
034	030-0096	OPERATING PROCEDURE, ENCODER BD	EX X 1 P C P EA	1
035	825-0104	LABEL, CSA CERTIFICATION	EX X 7 P C P EA	0

NOTES:

- ECO 352 ADDED ITEMS 4,33
- ECO 352 DELETED ITEM 26,7
- ECO 352 CHANGED ITEM 18 QTY FROM 12
- ECO 352 CHANGED ITEM 20 QTY FROM 4
- ECO 384 ADDED ITEM 12
- ECO 384 DELETED ITEM 27
- ECO 377 ADDED ITEM 22,30,31,3
- ECO 377 DELETED ITEM 28,29
- ECO 453 CLOSED ITEM 34
- ECO 472 ADDED ITEM 35

PRE-RELEASE  
VERSION

END OF REPORT

PARENT PART: 606-6548

M CHASSIS A2 PLUS 48K SYSTEM RFI  
 ERC: B SRCE CODE: A TYPE: 1

UM: EA  
 ABC: A

ITEM NO.	COMPONENT PART NUMBER	DESCRIPTION REMARKS	PR CD	COMM CODE	ST C	T R	S P	A P	EXTENDED QTY PER
000	606-6116D	DWG, CHASSIS ASSY A2 STD SYS RFI	EX		*	7	*	* EA	0
001	606-4548	TESTED A2 PLUS 48K MOTHERBOARD, RFI	TS		A	1	P	P EA	1
002	600-0009	ASSY, SPEAKER	RM		P	1	P	B P EA	1
003	699-0048	POWER SUPPLY, ASTEC (85V - 135V)	VX		P	1	P	A P EA	1
004	606-5105	TESTED KEYBOARD, A2 RFI	VX		A	1	P	A P EA	1
005	810-0055	BASE, CHASSIS A2 RFI PAINTED	RM		P	1	P	A P EA	1
008	810-0360	HOUSING, A2 W/EMI PAINTING DETAIL	RM		P	1	P	A P EA	1
009	810-0359	LID, A2 W/EMI PAINTING DETAIL	RM		P	1	P	A P EA	1
010	825-0003	LABEL, "VIDEO/CASSETTE IN-OUT"	EX		X	1	P	B P EA	1
011	825-0036	NAMEPLATE, APPLEII PLUS	EX		X	1	P	B P EA	1
012	825-0068	LABEL, SERIAL # APPLE II PLUS (UL)	EX 1		X	7	P	B P EA	1
013	830-0002	FASTENER, HEAD LOCK 3M#SJ-3308R	EX		X	1	P	B P EA	4
014	830-0003	FASTENER RICHCO TCBS-4N	EX		X	1	P	C P EA	5
015	844-0012	SCREW, #6-32 X 1/2 PAN HD (BLK)	EX		X	7	P	D P EA	4
017	844-0001	SCREW, #4-40 X 3/8 SEMS PAN HD (CD)	EX		X	1	P	C P EA	4
018	844-0004	SCREW, #6-32 X 3/8 SEMS PAN HD (BK)	EX		X	1	P	C P EA	10
021	865-0001	FEET, RUBBER	EX		X	1	P	B P EA	4
022	908-0003	ADHESIVE, RTV #3145 GRAY	EX		X	1	P	B P EA	0,0400
030	825-0043	LABEL, WARNING ASTEC UL P/S	EX		X	1	P	B P EA	1
031	944-0057	FOAM PAD, SPEAKER	EX 1		X	1	P	C P EA	1
033	805-0058	BAR, GROUNDING A2 PCB	RM		P	1	P	C P EA	1
035	825-0205	LABEL, FCC NON-COMPLIANCE	EX		X	1	P	B P EA	1
036	805-0061	CLIP, GROUNDING A2 RFI	RM		P	1	P	C P EA	2
037	844-0013	SCREW, #6-32 X 1/4 SEMS PAN HD (BK)	EX		X	7	P	D P EA	5

PRE-RELEASES  
 VERSION 5

*Patricia dwt*

APPLE COMPUTER, INC.

PRINTED 10-Jul-81 10:43

FML

EFFECTIVITY DATE: ALL  
 S I N G L E L E V E L B I L L S O F M A T E R I A L  
 P A R E N T P A R T : 605-0117  
 U N T E S T E D D C 5 1 D I S C R E T E K E Y B O A R D  
 U M : E A P R O D C O D E : U N E C N :  
 E R C : 0 S R C E C O D E : F T Y P E : I A E C : A P L A N C O D E : F D A T E :

ITEM NO.	COMPONENT NUMBER	DESCRIPTION	REMARKS	PR	CD	CODE	C	P	R	C	N	UM	EXTENDED QUANTITY	PER	CHG	DATE	S/N
000	050-0028	0 SWITCH, APPLE LOGIC KEYBOARD		EX									0		352		
001	519-0019	0 CONN, 25 PIN BOTTOM ENTRY		RC									1		612		13-Feb-80
002	605-0119	0 ASSY, KEYCAP SET A2 LPM		MS	1								1		352		13-Feb-80
003	705-0004	0 SWITCH, DC51-31		RP									50		352		13-Feb-80
004	705-0008	0 RST KY, 9 OZ, #DC51, APPL		EX									1		352		13-Feb-80
005	705-0018	0 SWITCH, 3.5 OZ DC51-35		RP									1		352		13-Feb-80
006	705-0017	0 SWITCH, FWR LGHT DC51-90-ELLFSD		RP									1		352		13-Feb-80
007	815-0061	0 KEY CAP FWR ON INDICATOR		EX									1		352		13-Feb-80
008	830-0022	0 WSHR, NYLN .050THK .150D 5/16D		EX									2		352		13-Feb-80
009	907-0002	0 ADHSV, LOGKIT 1430 SPAREDR		EX									0.0050		352		13-Feb-80
010	710-0001	0 LAMP 02-1376-01		EX									1		352		13-Feb-80

NOTES:

END OF REPORT

**PRE-RELEASE  
 VERSION**

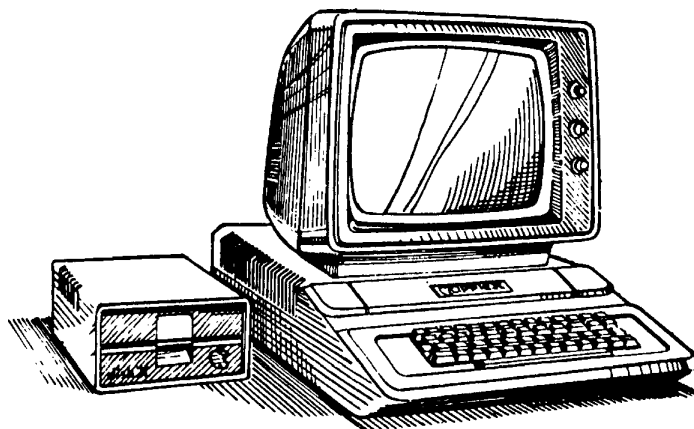


## Apple II Computer Technical Information

# APPLE II / APPLE II-PLUS LEVEL II SERVICE REFERENCE MANUAL

Pre-Release Version

## APPENDIX C REMOVAL AND REPLACEMENT PROCEDURES



Written by  
Apple Computer, Inc. • Level II Service Center  
1981

( This page is not part of the original service manual )

22 September 1981

**To:** Level II Service Managers

**From:** Jess Pack  
Service Engineering

**Subj:** Service Engineering Pre-Release on the Apple II Keyboards.

Enclosed is the pre-release material on the Keyboard Company produced keyboards for the Apple II. Some of the parts have Apple part numbers, these are indicated with an A preceding the part number. Part numbers preceded by a K are keyboard company part numbers.

These part numbers will be on the service cashier up-date for October, use the part number indicated in this material for ordering any piece part for the keyboards.

This package should contain piece part breakdowns on the following:

1. Keyboard Encoder REV C
2. Apple II Alps Switchable (Low Profile Key Caps)
3. Apple II Alps Switchable (Sculptured Key Caps)
4. Apple II Contact Array Keyboard (Low Profile Key Caps)
5. Apple II Contact Array Keyboard (Sculptured Key Caps)

**Note:** Due to manufacturing changes at the keyboard company many parts are not interchangeable. Refer to Service Release SR2-009.

**PRE-RELEASE  
VERSION**

# PRE-RELEASE VERSION

17 September 1981

## Apple II Switchable Keyboard Sculptured Key Caps

Keyboard Company

Part Number: 606-0650

Figure	Description	Part Number
1	Key Cap Set AII B&M	A605-0113
2	Adapter, 0 Degree	K815-0013
3	Switch, KBB Alps Reset	K705-0004
4	Header, Right Angle 26 Pin	K519-0003
5	Lamp	K710-0001
6	Adapter Power	K815-0010
7	Plate Sub assembly	K626-4001
8	Stabilizer 8 Position	K810-0014
9	Standoff, Sawge	K810-0008
10	Guide 0 Degree	K815-0005
11	Pivot Stabilizer	K815-0014
12	Screw 6-32 Pan Head	K842-0002
13	Richco Fastner	A830-0017
14	Switch, KBB ALPS	A705-0015
15	Power Lens Printed	K816-0119

Part Numbers: "K" Indicates Keyboard company  
"A" Indicates Apple MIS

Item 13: Richco fastner is not on illustration, it is used to fasten the external keyboard encoder card to the keyboard.

PRE-RELEASE  
VERSION

# PRE-RELEASE VERSION

17 September 1981

## Apple II Switchable Keyboard B&M Low Profile LKey Caps

Keyboard Company

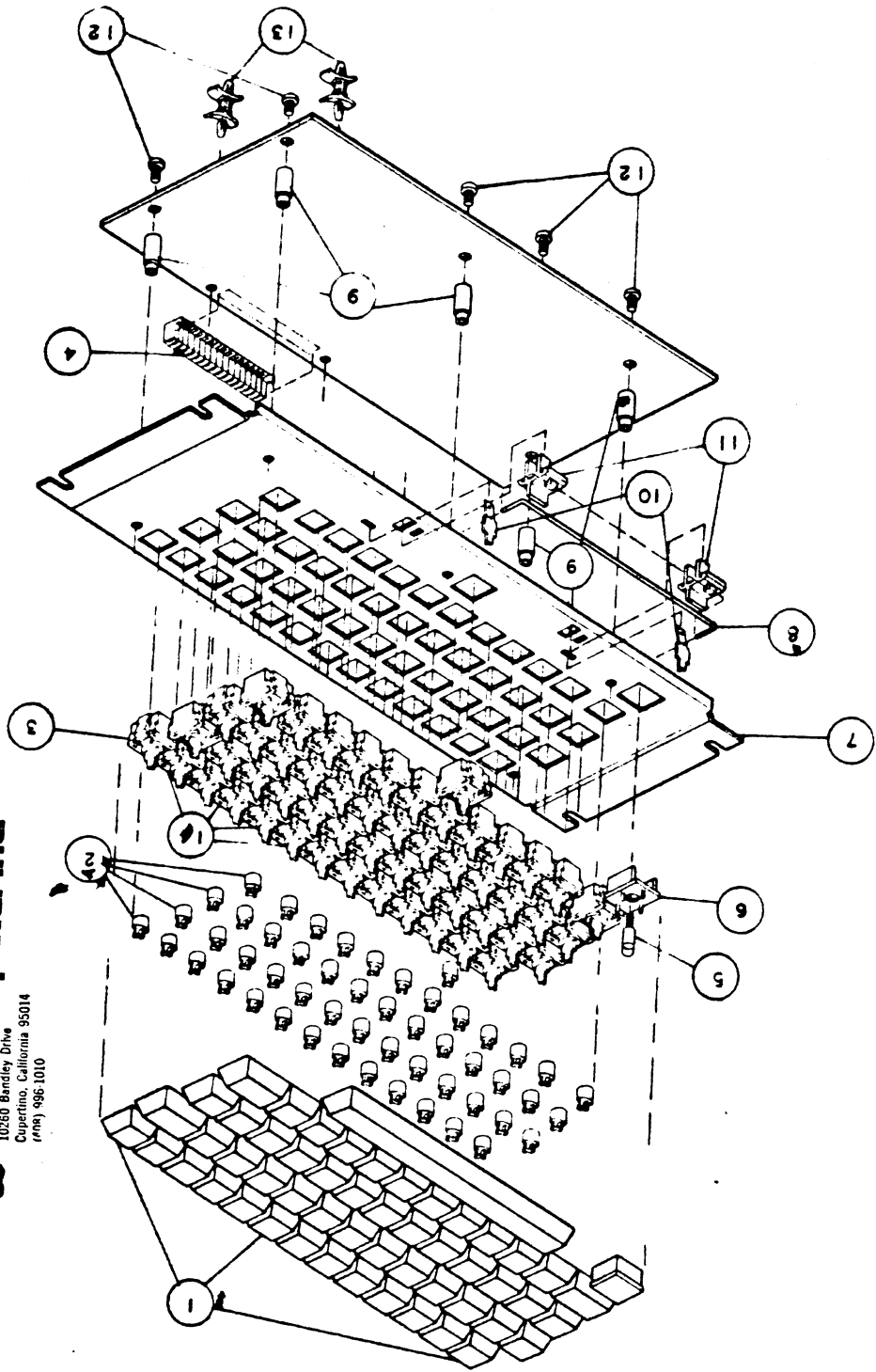
Part Number: 605-0118

Figure	Description	Part Number
1	Key Cap Set All B&M	A605-0119
2	Adapter, 12 Degree	K815-0009
3	Switch, KBB Alps Reset	K705-0004
4	Header, Right Angle 26 Pin	K519-0003
5	Lamp	K710-0001
6	Adapter Power	K815-0010
7	Plate Sub assembly	K626-4001
8	Stabilizer 8 Position	K810-0001
9	Standoff, Sawge	K810-0008
10	Guide 12 Degree	K815-0004
11	Pivot Stablizer	K815-0014
12	Screw 6-32 Pan Head	K842-0002
13	Richco Fastner	A830-0017
14	Switch, KBB ALPS	A705-0015
15	Power Lens Printed	K816-0119

Part Numbers: "K" Indicates Keyboard company  
"A" Indicates Apple MIS

Item 13: Richco fastner is not on illustration, it is used to fasten the external keyboard encoder card to the keyboard.

**Apple Computer Inc.**  
10260 Bandley Drive  
Cupertino, California 95014  
(415) 996-1010



SEP 22 1981

**PRE-RELEASE  
VERSION**

*Apple Switchable  
RTM Low Profile / Sculptured*

# PRE-RELEASE VERSION

16 Septembe 1981

Contact Array Keyboard  
Sculptured Key Caps

Keyboard Company

Part Number: 606-0649

Item	Description	Part Number
1	Sculptured Key Cap Set	A605-0133
2	Lens Power Printed (all keyboards)	K816-0001
3	Sheild 55 Position AII EMI	A810-0089
4	Keystem, Off-Set	K815-0038
5	Spring Reset Key	K870-0006
6	Stabilizer Bar 8 Position	K810-0011
7	Spring Space Bar	K870-0005
8	Guide Off-Set	K815-0037
9	Lamp	K710-0001
10	Connector 25 Pin	K710-0001
11	PC Board 52 Position	K820-0001
12	Richco Fastner (encoder card)	A830-0016

Item 12: Richco Fastner is not on the Illustration, it is used to fasten the external keyboard encoder to the keyboard.

Note: Service on this board is very limited. The following items are not considered field serviceable and are listed for identification purposes only.

Item

- 4 Keystem Off-Set
- 11 PC Board 52 Position

Item number 3 is the EMI Modification for the Contact Array.

# PRE-RELEASE VERSION

16 September 1980

Contact Array Keyboard  
B&M Low Profied key Caps

Keyboard Company

EMI Untested Contact Array Keyboard Part Number 606-0115  
Untested CONTACT Array Keyboard Part Number 605-0115

Figure	Description	Part number
1	Keycap set AII B&M	A605-0119
2	Lens power Printed (all keyboards)	K816-0001
3	Sheild 55 Position AII EMI	A810-0089
4	Keystem 12 Degree	K815-0001
5	Spring Comp, AII Keyboard Reset	A810-0087
6	Space Stabilizer AII Keyboard	A810-0086
7	Spring Comp, AII Keyboard, Space"	A810-0088
8	Guide 12 Deg. AII Array	A815-0381
9	Lamp (AII Array/Switchable)	K710-0001
10	Connector 25 Pin	K519-0002
11	PC Board 52 Pos	K820-0001
12	Richco Fastner (encoder card)	A830-0016

Part Number: "K" Indicates Keyboard Company  
"A" Indicates Apple MIS Number

Item 12: Richco Fastner A830-0016 is not on the Illustrstion, it is used to fasten the external keyboard encoder card to the Keyboard.

Note: Service on this board is very limited. The following items are not considered field servicable and are listed for identification purposes only:

Item:

4 Keystem 12 Deg.  
11 PC Board 52 Pos.

Item number 3 is the part addition to make the array keyboard EMI.

# PRE-RELEASE VERSION

16 September 1981

## EXTERNAL keyboard Encoder Apple II

Part Number: 605-0105 REV C (Current Encoder)

location	Description	Apple PT NO.
R8	Resistor 1/4W 5% 510K OHM	101-4514
R5	Resistor 1/4W 5% 1K OHM	101-4102
R4	Resistor 1/4W 5% 220 OHM	101-4221
R7	Resistor 1/4W 5% 220K OHM	101-4223
R2,3,6	Resistor 1/4W 5% 4.7K OHM	101-4472
R1	Resistor 1/4W 5% 51K OHM	101-4513
R10,5	Resistor 1/4W 5% 3K OHM	101-4302
C1	Capacitor 1UF AL ELEC -10%175% 50V	125-4101
C5	Capacitor 47PF 5% N470 50V	131-5701
C2	Capacitor .022UF 20% Y5P 25V	133-2401
C3,4,6,7,8	Capacitor .1UF +80-20% Z5U/Y5V 50V	135-9101
B3,4	IC 74LS00N	305-0000
B5	IC 74LS04	305-0004
B2	IC 555 Timer	329-0555
B6	MB IC KEYBOARD encoder	331-0931
J1	Socket, IC 16 Pin	511-1601
B	Socket, 40 Pin	511-4001
P1	Connector 25 Pin Molex #4030-25AA	519-0022
S1	Switch SLd #M10-0112-045-01-0	705-0013
PCB	PCB Encoder Discrete Keyboard	820-0026

**Note:**

**#1. REV C**

Capacitor C8 was added to this version of the Encoder for the Contact Array Keyboard.

**#2. REV B / REV A**

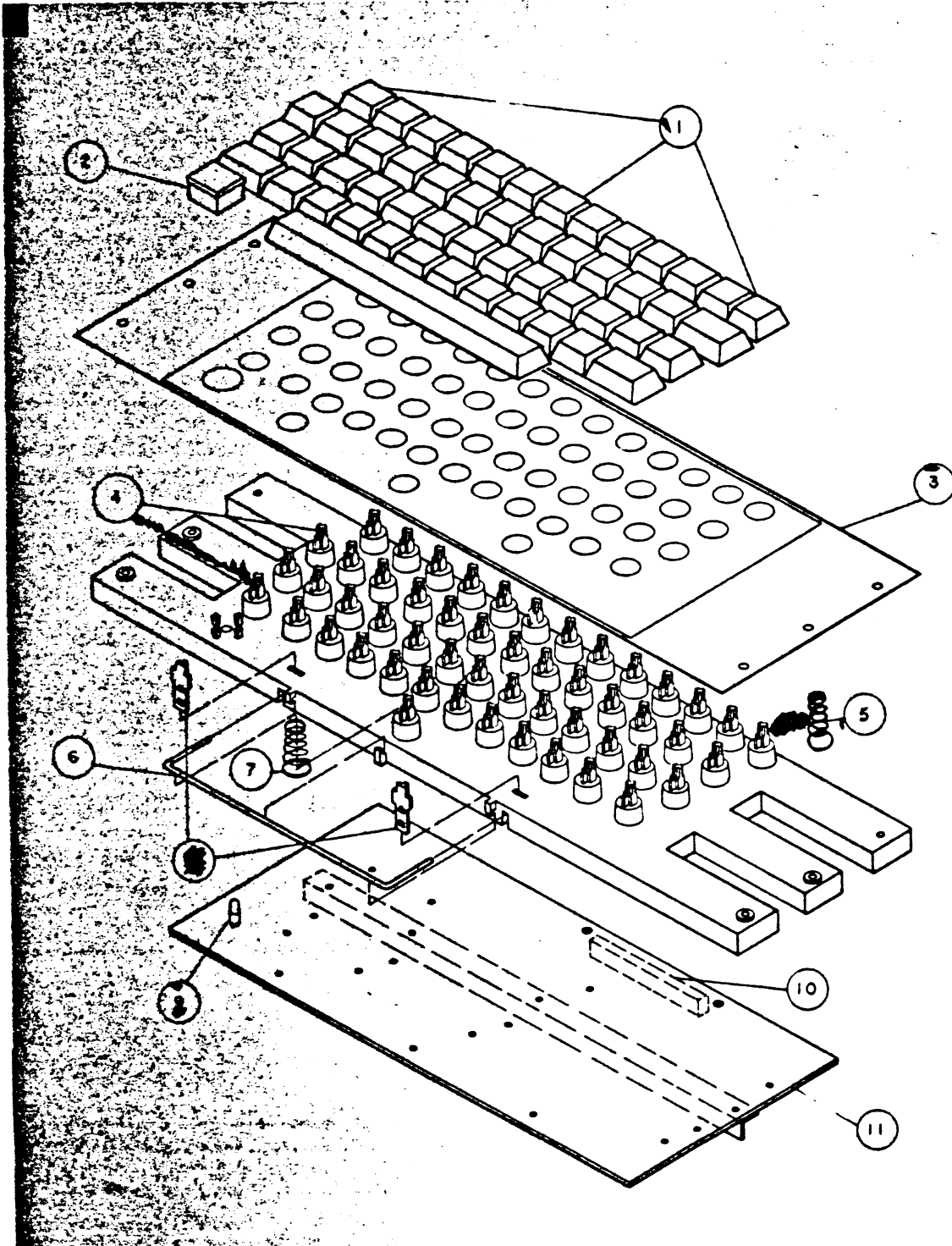
Components are the same as current encoder board, the PCB Traces are different.

*CONTACT ARRAY  
BIM LOW PROFILE / SCULPTURED*

**Apple computer inc.**  
10260 Bandley Drive  
Cupertino, California 95014  
(408) 996-1010

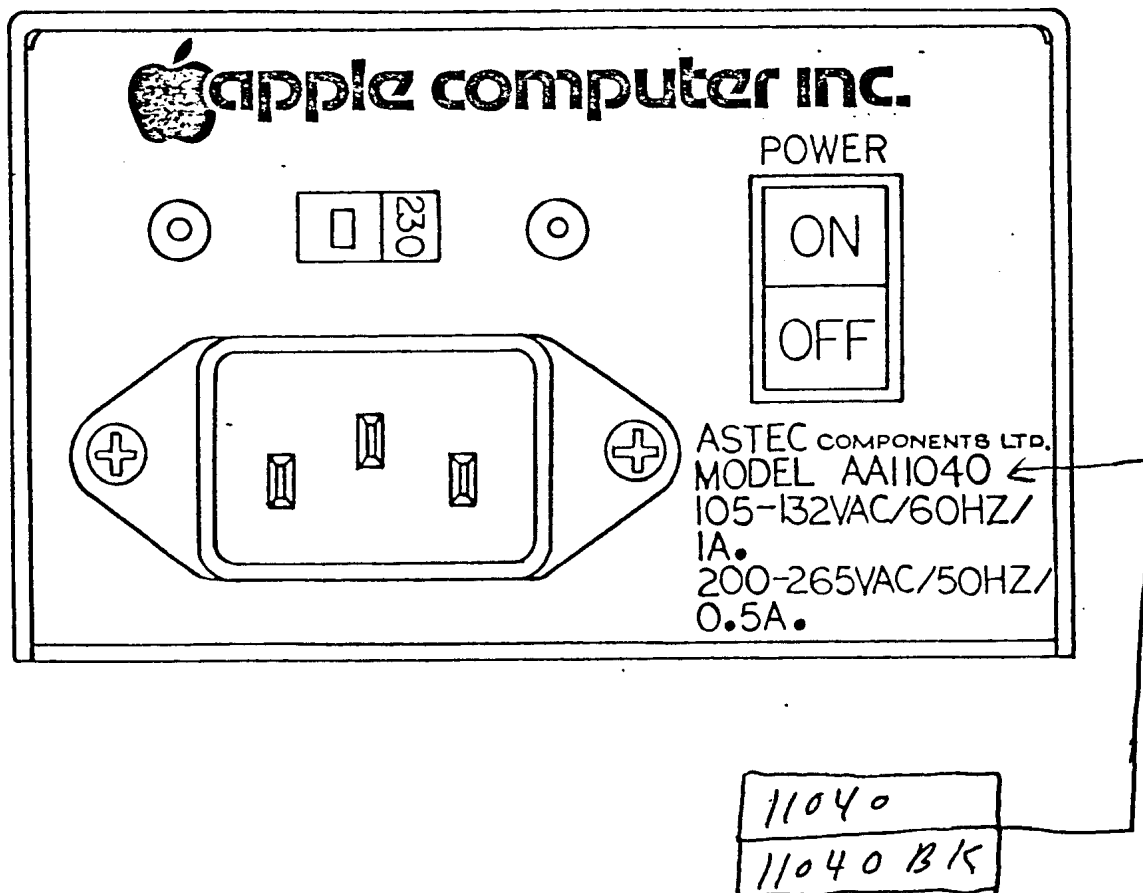
SEP 22 1981

PRE-RELEASE  
VERSION



# PRE-RELEASE VERSION

## ASTECC POWER SUPPLY



# PRE-RELEASE VERSION

## ASTEC 11040 STANDARD POWER SUPPLY

LOCATION	DESCRIPTION	VENDOR NO.	APPLE P/N
C1	POLYESTER CAPACITOR 0.1 UF 400V	058-10400100	u121-010
C2	ELECTROLYTIC CAPACITOR 47 UF 250V	057-47020040	C
C3	ELECTROLYTIC CAPACITOR 47 UF 250V	057-47020040	C u124-000
C4	ELECTROLYTIC CAPACITOR 47 UF 250V	057-47020040	C
C5	ELECTROLYTIC CAPACITOR 47 UF 250V	057-47020040	C
C6	TANTALUM CAPACITOR 22 UF 16V	072-22600040	u127-000
C7	CERAMIC CAPACITOR 1000 PF 3KV	055-10210001	u132-000
C8	CERAMIC CAPACITOR 0.01 UF 1KV	055-10367325	u132-000
C9	ELECTROLYTIC CAPACITOR 1000 UF 10V	057-10220020	C u124-000
C10	ELECTROLYTIC CAPACITOR 1000 UF 10V	057-10220020	C
C11	ELECTROLYTIC CAPACITOR 330 UF 16V	057-33120080	u124-000
C12	ELECTROLYTIC CAPACITOR 220 UF 10V	057-22120060	u124-000
C13	ELECTROLYTIC CAPACITOR 1000 UF 10V	057-10220020	u124-000
C14	POLYESTER CAPACITOR 1000 PF 50V	058-10200020	u121-010
C15	ELECTROLYTIC CAPACITOR 1000 UF 10V	057-10220020	u124-000
C16	ELECTROLYTIC CAPACITOR 220 UF 10V	057-22120060	u124-000
C17	ELECTROLYTIC CAPACITOR 680 UF 16V	057-68120010	u124-000
C18	ELECTROLYTIC CAPACITOR 330 UF 16V	057-33120080	u124-000
D1	RECTIFIER RGP10M	226-10400050	u375-001
D2	SILICON DIODE 1N4150	212-10700050	u371-000
D3	RECTIFIER RGP10M	226-10400100	u375-001
D4	RECTIFIER/HEATSINK ASSEMBLY	853-00200020	} u375-000
D5	RECTIFIER/HEATSINK ASSEMBLY	853-00200020	
D6	RECTIFIER/HEATSINK ASSEMBLY	853-00200020	
D7	RECTIFIER RGP15B	226-10100040	u375-001
D8	RECTIFIER RGP10B	226-10400070	u375-001
D9	SILICON DIODE 1N4150	212-10700050	} u371-415
D10	SILICON DIODE 1N4150	212-10700050	
D11	BLANK		
DB1	BRIDGE RECTIFIER KRP10	226-30500010	u357-000
F1	FUSE 2.75 AMP 250 VOLTS	084-00200040	u740-000
L1	CONTROL CHOKE COIL	328-00150016	u155-000
L2	FILTER CHOKE COIL ASSEMBLY	TF-20100010	u155-000
L3	FILTER CHOKE COIL ASSEMBLY	TF-20100050	u155-000
L4	FILTER CHOKE COIL ASSEMBLY	TF-20100010	u155-000
L5	FILTER CHOKE COIL ASSEMBLY	TF-20100020	u155-000
Q1	TRANSISTOR NPN PE8050	209-11700382	u376-000
Q2	TRANSISTOR NPN 2SC1358	209-10200020	u376-000
Q3	TRANSISTOR NPN PE8050	209-11700382	u376-000
Q4	TRANSISTOR PNP PE8550	210-11700322	u376-000
R1	THERMISTER 4R @25 DEG.CEN +/-10%	258-40970015	u107-010
R2	RESISTOR CARBON FILM 2.2M +/-5%	240-22506033	101-225

"C" Common Component

R3	RESISTOR CARBON FILM 2.2M +-5%	240-22506033	101-2225
R4	RESISTOR CARBON FILM 82R +-5%	240-82006033	101-2220
R5	RESISTOR METAL OXIDE FILM 27R	248-27006052	u107-ccc9
R6	RESISTOR CARBON FILM 4.7R +-5%	240-47906033	101-2547
R7	RESISTOR CARBON FILM 10R +-5%	240-10006022	101-4272
R8	RESISTOR METAL FILM 0.33R +-5%	247-03386054	u107-ccc1c
R9	RESISTOR CARBON FILM 180R +-5%	240-18106022	101-4111
R10	RESISTOR CARBON FILM 12R +-5%	240-12006022	101-412c
R11	RESISTOR CARBON FILM 470R +-5%	240-47106022	101-4471
R12	RESISTOR CARBON FILM 1K +-5%	240-10206022	101-4102
R13	BLANK		
R14	RESISTOR CARBON FILM 1K +-5%	240-10206022	101-410
R15	RESISTOR CARBON FILM 330R +-5%	240-33106022	101-433
R16	RESISTOR CARBON FILM 5.6K +-5%	240-56206022	101-456
R17	RESISTOR CARBON FILM 27R +-5%	240-27006022	101-4271
R18	RESISTOR CARBON FILM 82R +-5%	240-82006033	101-222
R19	RESISTOR CARBON FILM 1K +-5%	240-10206022	101-410
R20	RESISTOR CARBON FILM 2.7K +-5%	240-27206022	101-427
R21	BLANK		
R22	RESISTOR CARBON FILM 100R +-5%	240-10106033	101-2101
R23	RESISTOR CARBON FILM 100R +-5%	240-10106033	101-2101
R24	RESISTOR CARBON FILM 390R +-5%	240-39106022	101-4390
SC1	SILICON CONTROL RECTIFIER 2P 05M	227-12500010	u376-ccc7
T1	POWER TRANSFORMER ASSEMBLY	TF-10200370	u157-ccc4
T2	CONTROL TRANSFORMER ASSEMBLY	TF-10200200	u157-ccc5
T3	COMMON MODE TRANSFORMER ASSEMBLY	TF-20200010	u157-ccc6
Z1	ZENER DIODE 12.2V +-0.2V	222-12295001	u371-ccc2
Z2	ZENER DIODE 6.8V +-0.2V	222-06895003	u371-ccc3
VDRI	VARISTOR 260VAC	256-26100014	u377-ccc7
PCB	PRINTED CIRCUIT BOARD (NO PART'S)	042-02012202	u820-ccc1
CASE	<del>Switch</del> <del>Rock</del> SWITCH (ROCKER TYPE)	278-01200020	705-ccc1
CASE	AC INPUT SOCKET (THREE PRONG GROUND)	149-00200010	199-ccc3
CASE	VOLTAGE SELECTION SWITCH 115/230	283-02200100	<del>105-ccc1</del>
(CASE)	BOTTOM PLATE 1.6 AL SHEET	403-03100700	805-ccc7
(CASE)	COVER (TOP) 1.6 AL SHEET	403-03100810	805-ccc

PRE-RELEASE  
VERSION

# PRE-RELEASE VERSION

ASTEC POWER SUPPLY AA11040B

LOCATION	DESCRIPTION	VENDOR NO.	APPLE P/N
C1	MP CAP 0.1 UF +-20% 250 VAC	068-10400010	U121-0100
C3	CER CAP 2200 PF +-20% 400 VAC	055-22200010	U132-0001
C4	CER CAP 2200 PF +-20% 400 VAC	055-22220001	
C5	ELEC CAP 47 UF +100-10% 250V	057-47020040	U124-0001
C6	ELEC CAP 47 UF +100-10% 250V	057-47020040	
C7	ELEC CAP 220 UF +50 -10% 10V	057-22120080	U126-0001
C8	CER CAP 47 PF +-20% 3KV 250	055-47167728	U131-0001
C9	CER CAP 0.01 UF +-20% 1KV 25U	055-10358925	U131-0002
C10	CER CAP 0.01 UF +-20% 1KV 25V	055-10358925	
C11	POLY CAP 0.22 UF +-10% 100V	058-22400120	U119-0001
C12	ELEC CAP 1000 UF +100 -10% 10V	057-10220020	
C13	ELEC CAP 1000 UF +100 -10% 10V	057-10220020	U124-0003
C14	ELEC CAP 1000 UF +100 -10% 10V	057-10220020	
C15	ELEC CAP 220 UF +100 -10% 10V	057-22120060	U124-0004
C16	ELEC CAP 220 UF +100 -10% 10V	057-22120060	
C17	POLY CAP 0.022 UF +-20% 100V	058-22300080	U119-0002
C18	POLY CAP 0.22 UF +-10% 100V	058-22400120	U119-0001
C19	ELEC CAP 1000 UF +100 -10% 10V	057-10220020	U124-0003
C20	ELEC CAP 580 UF +100 -10% 16V	057-68120010	U124-0005
C21	ELEC CAP 330 UF +100 -10% 16V	057-33120080	U124-0002
C22	ELEC CAP 330 UF +100 -10% 16V	057-33120080	
C23	CER CAP 0.01 UF +-20% 1KV 25U	055-10368925	U132-0002
C24	ELEC CAP 47 UF +100 -10% 250V	057-47020040	U124-0001
C25	ELEC CAP 47 UF +10 -10% 250V	057-47020040	
D1	RECTIFIER RPG10A	226-10400050	U375-0014
D2	RECTIFIER RPG10M	225-10400100	U375-0013
D3	RECTIFIER RPG10M	226-10400100	
D4	SILICON DIODE 1N4606	212-10700210	U371-0001
D5	SILICON DIODE 1N4606	212-10700210	
D6	RECTIFIER ASSY	853-00200210	
D7	RECTIFIER ASSY	853-00200210	U375-0017
D8	RECTIFIER ASSY	853-00200210	
D9	RECTIFIER RGP15B	226-10100040	U375-0015
D10	RECTIFIER RGP15B	226-10400070	U375-0016
D11	SILICON DIODE 1N4606	212-10700210	U371-0001
D12	RECTIFIER RGP15B	226-10100040	U375-0015
DB1	BRIDGE RECTIFIER KBP10	225-30500010	U351-0001
F1	FUSE 2.75A 125V	084-00200040	U-740-0001
ICI	IC TL431CP/TL431CLP	211-10800100	U-327-0001
L1	CHOKE COIL ASSY	852-20100140	U-155-0001
L2	CHOKE COIL ASSY	852-20100140	
L3	BASE CHOKE 2.2 UH	328-00100030	U-155-0002
L4	CHOKE 1.5 MH (PROPRIETARY)	328-00100010	U-155-0003
L5	CHOKE COIL ASSY	852-10100370	U-155-0004

"C" COMMON COMPONENT

L6	CHOKE COIL ASSY	328-20100010	U155-0005
L7	CHOKE COIL	852-10100490 <sup>3</sup>	U155-0006
L8	CHOKE COIL	852-10100490	
Q1	NPN TRANSISTOR 2SD592NC	209-11700400	U376-0001
Q1	NPN TRANSISTOR 2SD467C	209-11700460	(20)
Q2	NPN TRANSISTOR 2SC1875	209-10200030	U376-0002
Q3	PNP TRANSISTOR 2SB621NC	210 11700330	U376-0003
Q3	PNP TRANSISTOR 2SB561C	210-11700350	(20)
Q4	PNP TRANSISTOR 2SB621NC	210-11700330	U376-0003
R1	THERMISTOR 4R +-10% OR 5R	258-40970015	U107-0100
R2	RESISTOR METAL FILM 150K +-5% 1/2 W	240-15406033	U107-0001
R3	RESISTOR METAL FILM 150K +-5% 1/2 W	240-15406033	U107-0002
R4	RESISTOR METAL OXY FILM 27R +-5% 2 W	248-27006063 C	101-4102
R5	RESISTOR CARBON FILM 1K +-5% 1/2 W	240-10206022 C	101-4290
R6	RESISTOR CARBON FILM 27R +-5% 1/2 W	240-27006022 C	101-4680
R7	RESISTOR CARBON FILM +-5% 1/4W 68R	240-68006022	U107-0003
R8	RESISTOR METAL OXY FILM 120R +-5% 1W	248-12106052	101-4082
R9	RESISTOR CARBON FILM 8.2R +-5% 1/4 W	240-82906022	101-4100
R10	RESISTOR CARBON FILM 10R +-5% 1/4 W	240-10006022 C	U107-0004
R11	RESISTOR METAL FILM 0.56 +-5% 1W	247-05686054	101-4680
R12	RESISTOR CARBON FILM 68R+-5% 1/4W	240-68006022	101-2277
R13	RESISTOR CARBON FILM 270R +-5% 1/2W	240-27106033	101-4082
R14	RESISTOR CARBON FIM D270R +-5% 1/2W	240-27106033	101-4390
R15	RESISTOR CARBON FILM 8.2R +-5% 1/2W	240-39106022	101-4220
R16	RESISTOR CARBON FILM 390R +-5% 1/4W	240-39106022 C	101-4101
R17	RESISTOR CARBON FILM 22R +-5% 1/2W	240-22006022	101-4560
R18	RESISTOR CARBON FILM 100R +-5% 1/4W	240-10106022 C	101-4123
R19	RESISTOR CARBON FILM +-5% 1/4W 56R	240-56006022 C	101-4471
R20	RESISTOR CARBON FILM 56R +-5% 1/2W	240-56006022 X	U107-0005
R21	RESISTOR CARBON FILM 12K +-5% 1/4W	240-12306022	101-4104
R22	RESISTOR CARBON FILM 470R +-5% 1/4W	224-27106022	101-4681
R23	RESISTOR METAL FILM 2.7K +-2% 1/4W	247-27015022	101-4182
R24	RESISTOR METAL FILM 2.7K +-2% 1/4W	247-27015022	U107-0006
R25	RESISTOR CARBON FILM 100K +-5% 1/4W	240-10406022	U107-0007
R26	RESISTOR CARBON FILM 680R +-5% 1/4W	240-68106022	U107-0008
R27	RESISTOR CARBON FILM 1.8K +-5% 1/4W	240-18206022	101-4220
R28	RESISTOR METAL FILM +-5% 1W 1R	247-10086-54	
R29	RESISTOR METAL FILM +-5% 1/4W 32R	240-82006033 C	
R30	RESISTOR METAL OXY FILM 220R +-5% 1W	248-22106052	
R31	RESISTOR CARBON FILM 224 +-5% 1/4W	240-22006022	
SCR1	SCR C122U/2N695	227-13000010	U372-0001
T1	COMMON MODE TRANSFORMER ASSY	852-20200950	U157-0001
T2	POWER TRANSFORMER ASSY	852-10200940	U157-0002
T3	POWER TRANSFORMER ASSY (SUB)	852-10200680	U157-0003
Z1	ZENER DIODE 9.8V +-0.2V (2K7)	222-98085002	U371-0002
VDR1	VDR 260 VAC	256-26100014 C	U377-0001
CASE	VOLTAGE SELECTION SWITCH 115/230V	283-02200100 C	705-0003

		<i>Switch Rocker</i>			
CASE	SWITCH ROCKER	278-01200020	C	<i>705-0001</i>	
CASE	AC INPUT SOCKET	149-00200010	C	<i>705-0023</i>	
CASE	BOTTOM PLATE 1.6 AL SHEET	403-03100700	C	<i>805-0077</i>	
CASE	COVER (TOP) 1.6 AL SHEET	403-03100810	C	<i>805-0003</i>	

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# MOTHERBOARD REPLACEMENT PROCEDURE

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## REMOVAL

1. Power off the Apple and remove power cord—first from power source and then from rear of Apple housing
2. Remove Apple lid.
3. Turn Apple upside down so keyboard rests on protective foam pad.
4. Remove six flat-head screws from **three outside edges** of flat portion of Apple base (See A1).
5. Remove four round-head screws and lock washers from front of base (See A2).
6. Grasping both base and housing, turn Apple right side up.
7. Gently lift front of housing slightly off base and unplug keyboard connector from location A7 at front of motherboard (See D1).
8. Lift housing off base and set aside.
9. Pinch sides of plug and release power supply plug from location K1 at top of motherboard (See D2).
10. Unplug speaker connector from location B8 on motherboard (See D3).
11. Remove 5/16 inch nut and lockwasher in middle of motherboard (See D4).
12. Push in on flanges with screwdriver or needle-nose pliers to release four stand-offs at corners of board and two stand-offs between I/O connectors 4 and 5. Lift board up and out (See D5).

## INSTALLATION

1. Place new motherboard into position over four stand-offs at corners of board and two stand-offs between I/O connectors 4 and 5. Press board down into place (See D5).
2. Install washer and nut in middle of board and tighten just until snug (See D4).
3. Reinstall speaker connector at B8 (See D3).
4. Reinstall power supply plug at K1 (See D2).
5. Place housing over base.
6. Gently lift front of housing slightly off base and reinstall keyboard connector at location A7. Be sure pin 1 of connector aligns with pin 1 of socket (See D1 and D10).
7. Grasping both base and housing, turn Apple upside down so keyboard rests on foam pad.
8. Make sure bent tab at back of base fits into slot in housing; then install lock washers and four round-head screws in front of base (See A2).
9. Install six flat-head screws in **three outside edges** of base (See A1).
10. To finish the procedure, complete these steps:
  - a. turn Apple right side up
  - b. replace Apple lid
  - c. reconnect power cord to Apple.



## ROM/RAM/741 REPLACEMENT PROCEDURE

### REMOVAL

1. Power off system and remove power cord—first from power source and then from rear of Apple housing.
2. Remove Apple lid.
3. Locate IC to be removed.
  - Motherboard ROMs (See D6).
  - Motherboard RAMs (See D7).
  - 741 IC (See D12).
  - ROM Card (Applesoft) in I/O connector 0 (See D13).
4. With the special IC extractor, lift out the IC. Use extreme caution when handling the IC to prevent all types of damage—including that caused by static (See D8).

### INSTALLATION

1. Identify correct placement of IC by holding it above socket so that:
  - a. notch in top of IC is toward **front** of Apple and
  - b. dot or dot indentation on top of IC (at pin 1) is next to white dot on board (at pin 1 of socket)—See D9 and D10.
2. Making sure that all pins line up with sockets, press IC firmly into place.
3. To finish the procedure, complete these steps:
  - a. reinstall Apple lid
  - b. reconnect power cord to Apple.

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## POWER SUPPLY REPLACEMENT PROCEDURE

### REMOVAL

1. Power off Apple and remove power cord—first from power source and then from rear of Apple housing.
2. Remove Apple lid.
3. If ROM card is installed in I/O connector 0 next to power supply, remove for easier access.
4. Pinch sides of plug and release power supply plug from location K1 on motherboard (See D2).
5. With the keyboard directly in front of you, turn Apple up onto its left side.
6. Support the power supply unit (See C1) with your left hand and use your right hand to remove the four round-head screws and lock washers on the underside of base (See A3).
7. Turn the Apple back onto its base and lift out power supply unit.

### INSTALLATION:

1. Place new power supply unit into Apple (See C1).
2. Holding the unit in place and facing the front of the keyboard, turn Apple onto its left side.
3. Support the power supply unit with your left hand and install the four lock washers and round-head screws to hold power unit to base (See A3):
4. Reinstall power supply plug at location K1 (See D2).
5. To finish the procedure, complete these steps:
  - a. re-insert ROM card in I/O connector 0 (if removed earlier)
  - b. reinstall Apple lid
  - c. reconnect power cord to Apple.

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# KEYBOARD REPLACEMENT FROM VERSION 1

## REMOVAL

1. Power off the system and remove power cord—first from power source and then from rear of Apple housing.
2. Remove Apple lid.
3. Turn Apple upside down so keyboard rests on protective foam pad.
4. Remove six flat-head screws from **three outside edges** of flat portion of Apple base (See A1).
5. Remove four round-head screws and lock washers from front of base (See A2).
6. Holding both base and housing, turn Apple right side up.
7. Gently lift front of housing slightly up off base and unplug keyboard connector from location A7 at front of motherboard (See D1).
8. Lift housing off base and turn housing upside down onto protective foam pad.
9. Remove four nuts and lock washers (or screws) holding keyboard to housing (See B1).
10. Turn keyboard right side up. Carefully remove cable from top right corner of keyboard (See C6).

## INSTALLATION

1. Install keyboard cable to connector at top right corner of replacement keyboard. Be careful not to bend pins (See C6).
2. To install replacement keyboard, first check to see if there are aluminum mounting brackets mounted on inside of housing at sides of keyboard location (See B2).
  - If brackets are pre-installed, go to step 3.
  - If brackets are **not** pre-installed, complete a through a below:
    - a) remove four threaded rods (bent screws)
    - b) place brackets flat side down on housing
    - c) install screws at top and bottom of brackets (See B2)
3. Place new keyboard over bracket stand-offs and install lock washers and screws to hold keyboard to brackets (See B1).
4. Lift housing and place on base.
5. Lift front of housing slightly off base and reinstall keyboard connector at location A7 (See D1).
6. Holding both base and housing, turn Apple upside down so keyboard rests on foam pad.
7. Install four lock washers and round-head screws at front of base (See A2).
8. Install six flat-head screws at **three outside edges** of Apple base (See A1).
9. To finish the procedure, complete these steps:
  - a) turn Apple right side up
  - b) reinstall Apple lid
  - c) reconnect power cord to Apple.



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## ENCODER IC REPLACEMENT PROCEDURE

### REMOVAL

1. Power off the system and remove power cord—first from power source and then from rear of Apple housing.
2. Remove Apple lid.
3. Turn Apple upside down so keyboard rests on protective foam pad.
4. Remove six flat-head screws from **three outside edges** of flat portion of Apple base (See A1).
5. Remove four round-head screws and lock washers from front of base (See A2).
6. Holding both base and housing, turn Apple right side up.
7. Gently lift front of housing slightly up off base and unplug keyboard connector from location A7 at front of motherboard (See D1).
8. Lift housing off base and turn housing upside down onto protective foam pad.
9. Remove four nuts and lock washers (or screws) holding keyboard to housing (See B1).
10. Turn keyboard right side up on protective foam.
11. Remove encoder IC (See C5) by pulling up on both ends with your thumb and index finger. Use extreme caution to protect the IC from damage, including that caused by static.

### INSTALLATION

1. Install replacement encoder, ensuring that pin 1 of IC lines up with pin 1 of socket (See D9 and D10).
2. With keyboard still resting on foam, attach keyboard cable to location A7 on motherboard (See D1).
3. Power on system and run keyboard test again.
  - If test is good, power system off and go to step 4
  - If test fails, power off system and complete these steps:
    - a. gently remove cable from top right corner of keyboard (See C6)
    - b. obtain replacement keyboard
4. Unplug keyboard connector from location A7 on motherboard (See D1).
5. Reinstall keyboard according to the following instructions:
  - If the test run in step 3 was good and you are reinstalling the same keyboard, place it onto housing and reinstall lock washers and nuts (or screws) (See B1).
  - If the test run in step 3 fails and you are installing a **replacement** keyboard, complete these steps:
    - a. Attach keyboard cable to plug at top right corner of keyboard (See C6). Exercise care not to bend pins and be sure plug aligns properly with socket.



ENCODER IC REPLACEMENT. continued

- b. Check to see if there are two aluminum brackets mounted on inside of Apple housing where keyboard is to be attached (See B2).
  1. If brackets are **pre-installed**, go to step 3 below.
  2. If the brackets are **not pre-installed**, first remove four threaded rods. Then place brackets flat side down on housing and install screws at top and bottom of each bracket in place of rods.
  3. Place new keyboard over bracket stand-offs and install lock washers and screws to hold keyboard to brackets.
6. Lift housing and place on base.
7. Lift front of housing slightly off base and reinstall keyboard connector at location A7 (See D1).
8. Holding both base and housing, turn Apple upside down so keyboard rests on foam pad.
9. Install four lock washers and round-head screws at front of base (See A2).
10. Install six flat-head screws at three outside edges of Apple base (See A1).
11. To finish the procedure, complete these steps:
  - a. turn Apple right side up
  - b. reinstall Apple lid
  - c. reconnect power cord to Apple.

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## POWER LIGHT BULB REPLACEMENT PROCEDURE

### REMOVAL

1. Lift off power light cap at bottom left of keyboard (See C2).
2. Lift off shift key cap directly above power light cap for easier access to bulb (See C3).
3. Gently lift light bulb from sockets (See C4).

### REPLACEMENT

1. Insert replacement bulb, making sure both wires go into the small sockets (See C4).
2. Reinstall shift key (See C3).
3. Reinstall power light cap (See C2).

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## BRIGHTNESS ADJUSTMENT PROCEDURE

If the Apple is connected directly to a monitor and the image on the screen is too dim or too bright, adjust the composite video pot to get optimum clarity.

1. Power off Apple and remove lid.
2. Unplug game paddles if installed at game I/O connector (See D14).
3. Power on Apple.
4. Locate video pot at location J14 directly in back of game I/O plug (See D11). Using your thumb and index finger, turn pot:
  - clockwise to brighten image, or
  - counterclockwise to dim image.

## ELIMINATING SPEAKER RESONANCE

If the speaker is resonating at certain tones, install the supplied foam doughnut in accordance with the following instructions.

1. Power off Apple and remove lid.
2. Cut slit in one side of foam doughnut as shown (See F1).
3. Apply Dow Corning Silicone Rubber Sealant to bottom of doughnut and to inside of circular cut-out.
4. Carefully fit cut-out in foam around base of speaker in position shown (See F2). Press down firmly to ensure good contact between foam and Apple base.
5. Allow glue adequate time to dry before testing speaker.

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## KEY SWITCH REPLACEMENT PROCEDURE

Once you have completed the keyboard diagnostic test and identified the faulty key switch, replace it by following these procedures.

### *BEFORE YOU BEGIN, MAKE SURE YOU HAVE THE FOLLOWING MATERIALS.*

- 60 watt, 700° (F) soldering iron with small, flat tip
- "SOLDAPULLT" solder-sucker, model DS 017
- 60/40 solder for printed circuit boards
- number 1 phillips screw driver

### REMOVE KEYBOARD

1. Power off the system and remove power cord—first from power source and then from rear of Apple housing.
2. Remove Apple lid.
3. Turn Apple upside down so keyboard rests on protective foam pad.
4. Remove six flat-head screws from **three outside edges** of flat portion of Apple Base (See A1).
5. Remove four round-head screws and lock washers from front of base (See A2).
6. Holding both base and housing, turn Apple right side up.
7. Gently lift front of housing slightly up off base and unplug keyboard connector from location A7 at front of motherboard (See D1).
8. Lift housing off base and turn housing upside down onto protective foam pad.
9. Remove four nuts and lock washers (or screws) holding keyboard to housing (See B1).

### REMOVE KEY SWITCH

1. Turn the keyboard upside down onto protective padding. Note that the printed circuit board has numbers for each key. Check Figure A below to identify the number of the key you want to remove. The "H" key, for instance, is number 34.

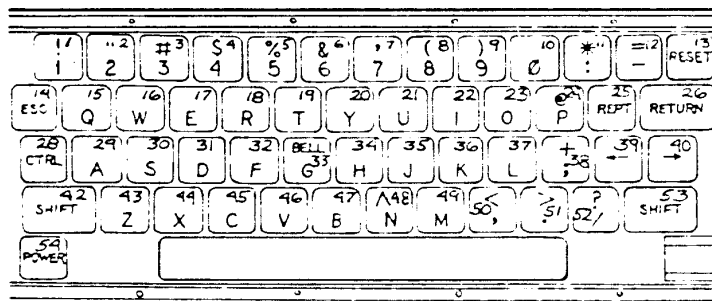


Figure A



2. To prepare the solder-sucker, push the plunger down as far as it will go.
3. Heat the soldering iron and make sure it is clean and well-tinned.
4. When the soldering iron is ready, take it in one hand and the solder-sucker in the other as shown in Figure B. Hold the soldering iron at a 45° angle so that one side of the flat tip is firmly in contact with the pin and the other side of the tip is firmly in contact with the pad at the base of the pin. When the solder melts, quickly push the release button or lever of the solder-sucker to pick it up.

**CAUTION:** DO NOT APPLY THE SOLDERING IRON FOR MORE THAN THREE SECONDS. IT MAY LIFT THE TRACES OFF THE BOARD AND DESTROY IT.

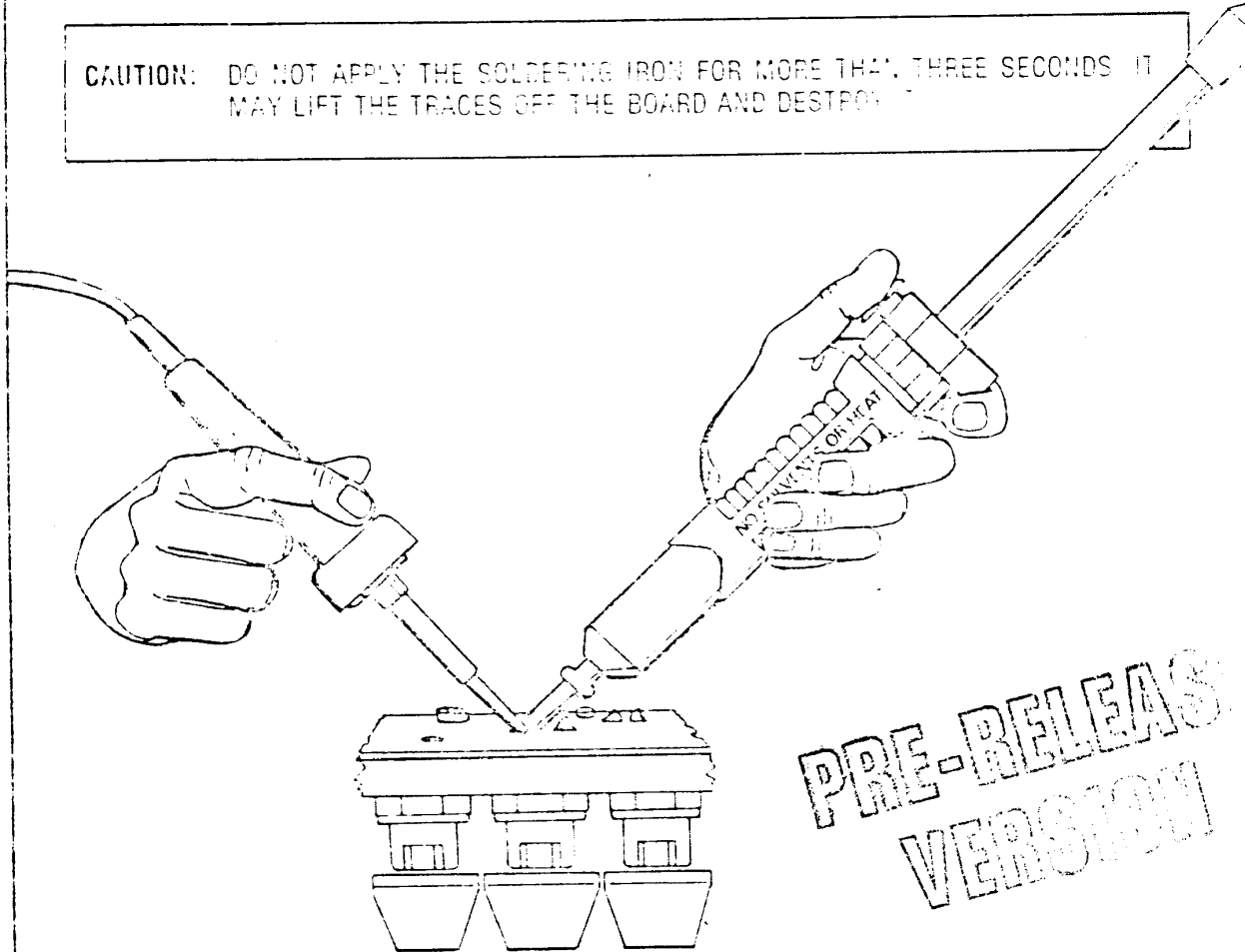


Figure B

5. Repeat this procedure for the second pin, being careful to hold the soldering iron just as before and to observe the 3-second limit.
6. If any solder remains around the base of the pin, or if it was not soldered properly to begin with, apply a little solder to the joint, again placing the flat edges of the iron against both pin and pad. Then repeat step 4 to make sure all solder is removed.

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7. Using a number 1 phillips screwdriver, remove the screw holding the key switch to the board.
8. Turn the keyboard right-side up and pull up on the key cap to remove the key switch assembly (see Figure C).
9. Pull the key cap straight up off the key switch and discard the *switch*.

### INSTALL REPLACEMENT KEY SWITCH:

1. To place cap onto the replacement key switch, hold the switch and cap as shown in Figure C so that:
  - the pins on the bottom of the switch are on the side furthest from you.
  - the white top of the switch bends to your left
  - the letter on the key cap is at the side of the key on your right

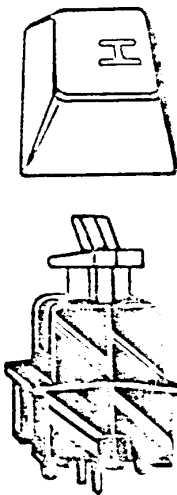


Figure C

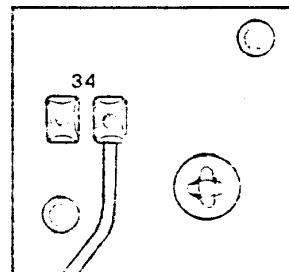
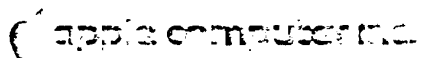


Figure D

2. Insert the key switch into the board so that:
  - the pins go through the feed-through holes
  - the short black plastic placement prongs fit into their holes on the board. (Figure D shows a properly installed switch—from the back side of the board.)
3. Holding the key in place with one hand, turn the keyboard up-side-down onto the pad.
4. Reinstall the screw that holds the key in place.
5. Apply a little solder to the iron. Then, with the flat sides of the iron's tip in contact with both the pin and the pad that surrounds the pin hole, apply the new solder. **Again, be sure that you do not overheat the board!**
6. Check the joint to be sure that the solder has completely filled the hole around the pin and that the solder is built up in a little cone around the pin. If the joint is not filled, apply more solder.

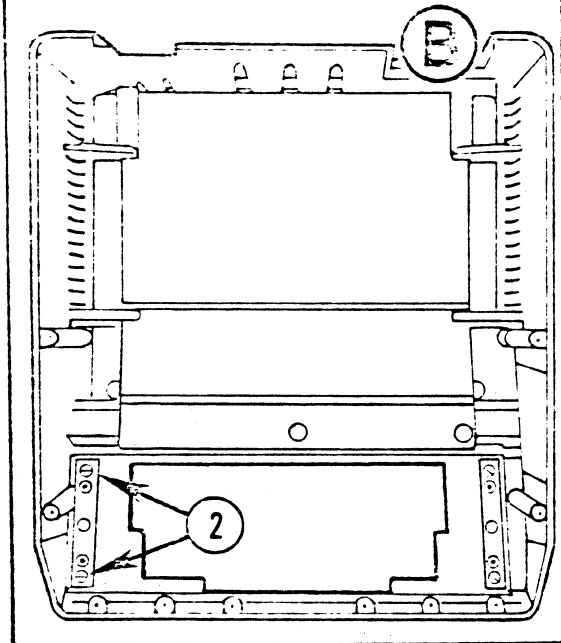
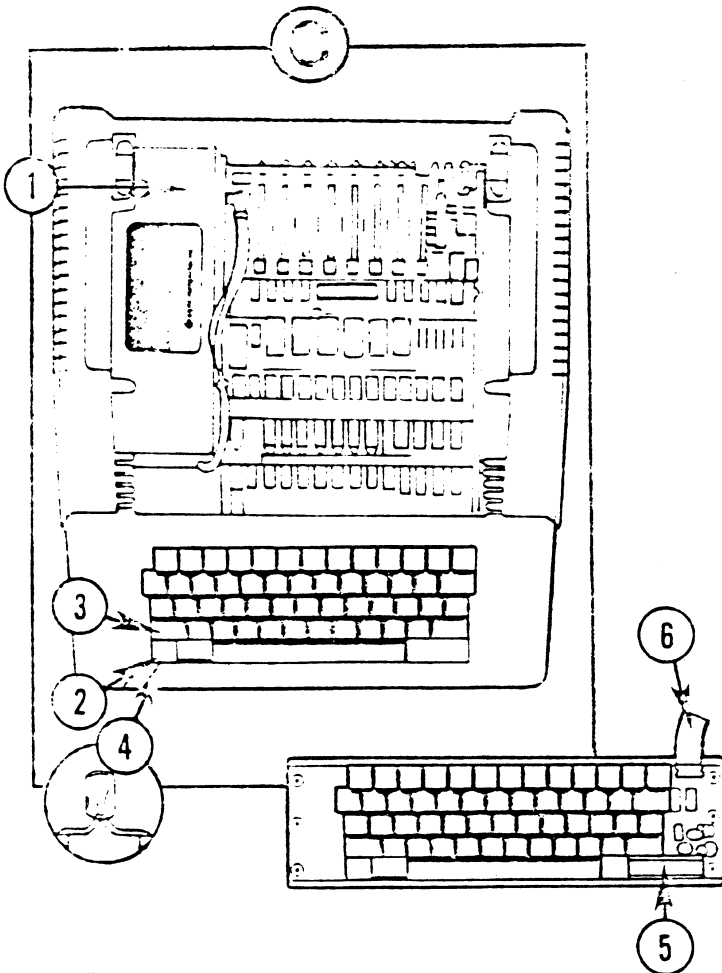
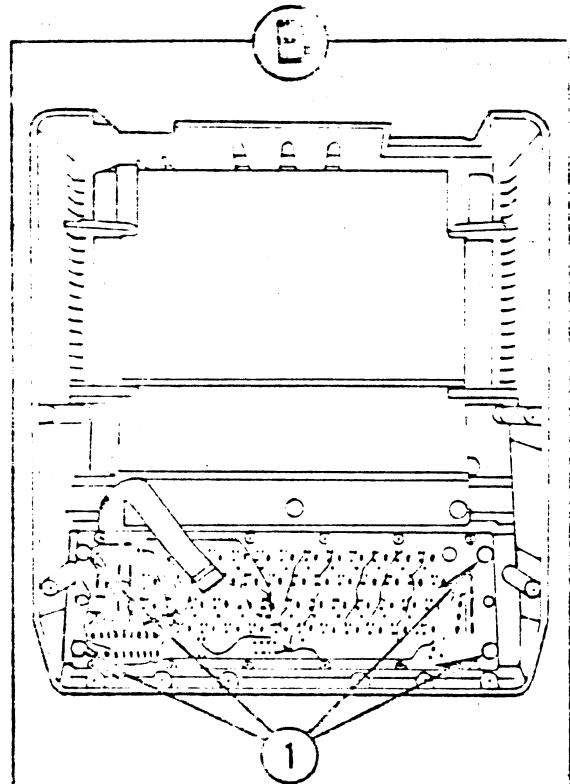
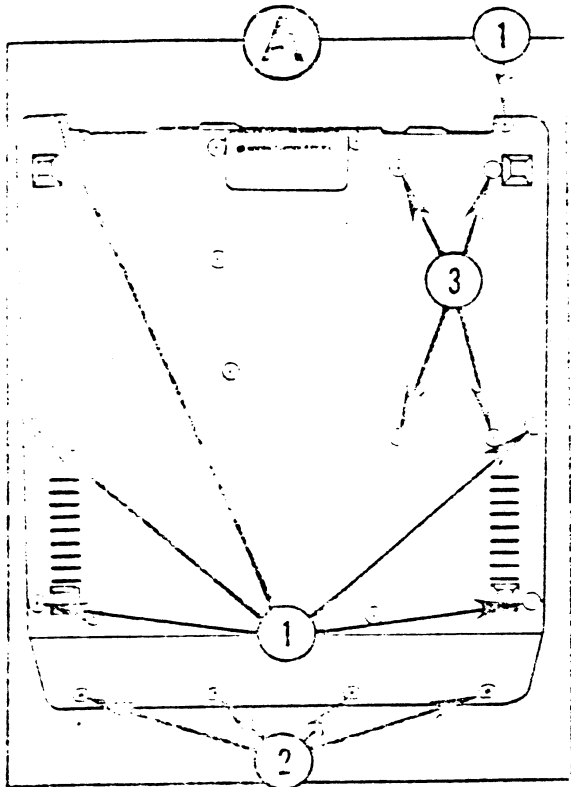


## REINSTALL KEYBOARD

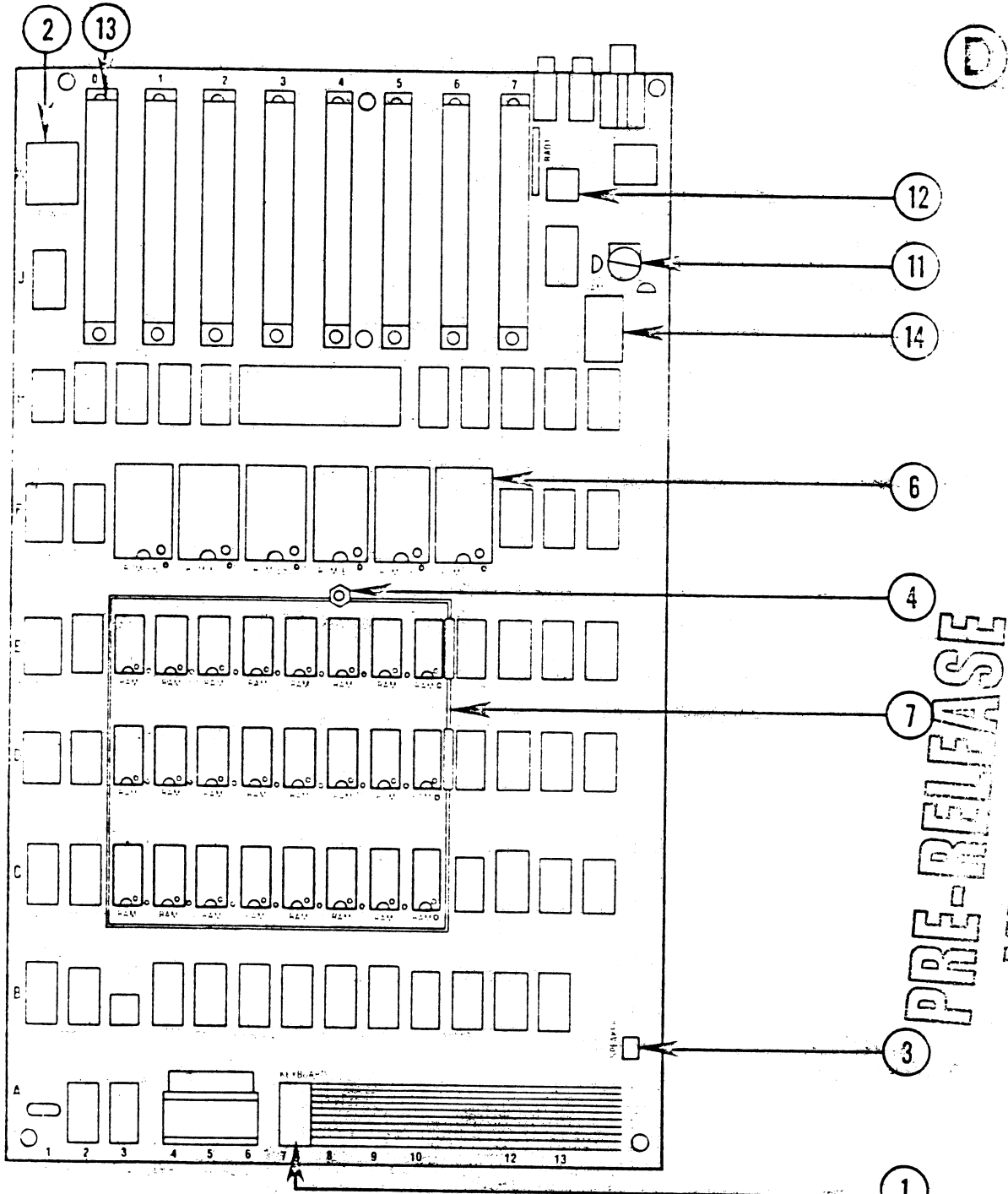
1. Reinstall keyboard in housing and tighten nuts with lock washers (or screws).
2. Lift housing and place on base.
3. Lift front of housing slightly off base and reinstall keyboard connector at location A7 (See D1).
4. Holding both base and housing, turn Apple upside down so keyboard rests on foam pad.
5. Install four lock washers and round-head screws at front of base (See A2).
6. Install six flat-head screws at three outside edges of Apple base (See A1).
7. To finish the procedure, complete these steps:
  - a. turn Apple right side up
  - b. reinstall Apple lid
  - c. reconnect power cord to Apple

NOTE: SEE SERVICE BULLETIN NUMBER 5 FOR NEW KEYBOARDS.

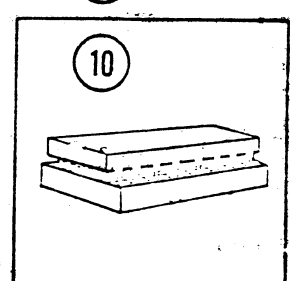
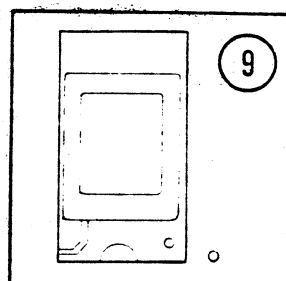
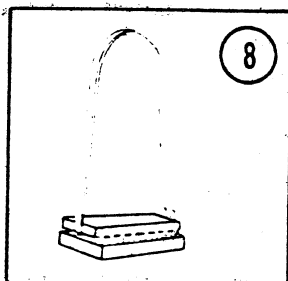
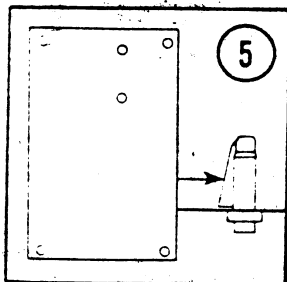
**PRE-RELEASE  
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PRE-RELEASE  
VERSION



**PRE-RELEASE  
VERSION**



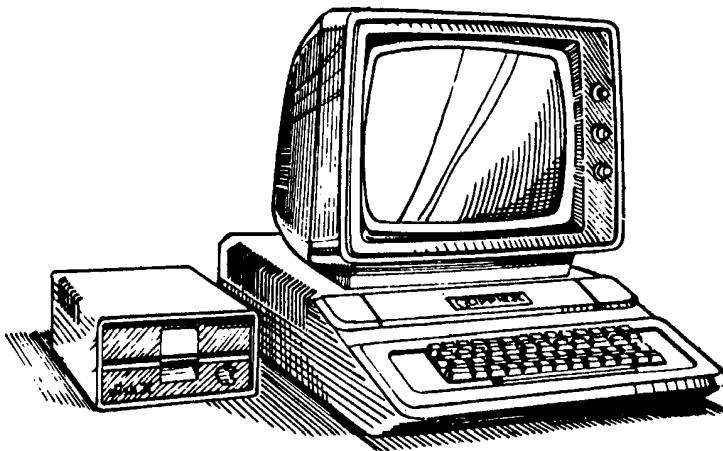


**Apple II Computer Technical Information**

**APPLE II / APPLE II-PLUS  
LEVEL II SERVICE REFERENCE MANUAL**

**Pre-Release Version**

**END OF MANUAL**



**Written by  
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1981**

( This page is not part of the original service manual )