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OP AMP APPLICATIONS

CHAPTER 7: HARDWARE AND HOUSEKEEPING TECHNIQUES

Walt Kester, James Bryant, Walt Jung, Joe Buxton, Wes Freeman

This chapter, one of the longer of those within the book, deals with topics just as important as all of those basic circuits immediately surrounding the op amp, discussed earlier. The chapter deals with various and sundry circuit/system issues which fall under the guise of system *hardware and housekeeping techniques*. In this context, the hardware and housekeeping may be all those support items surrounding an op amp, excluding the op amp itself. This includes issues of passive components, printed circuit design, power supply systems, protection of op amp devices against overvoltage and thermal effects, EMI/RFI issues, and finally, simulation, breadboarding and prototyping. Some of these topics aren't directly involved in the actual signal path of a design, but they are every bit as important as choosing the correct device and surrounding circuit values.

SECTION 7-1: PASSIVE COMPONENTS

James Bryant, Walt Jung, Walt Kester

Introduction

When designing with op amps and other precision analog devices, it is critical that users avoid the pitfall of poor passive component choice. In fact, the wrong passive component can derail even the best op amp or data converter application. This section includes discussion of some basic traps of choosing passive components for op amp applications.

So, you've spent good money for a precision op amp or data converter, only to find that, when plugged into your board, the device doesn't meet spec. Perhaps the circuit suffers from drift, poor frequency response, and oscillations— or simply doesn't achieve expected accuracy. Well, before you blame the device, you should closely examine your passive components— including capacitors, resistors, potentiometers, and yes, even the printed circuit boards. In these areas, subtle effects of tolerance, temperature, parasitics, aging, and user assembly procedures can unwittingly sink your circuit. And all too often these effects go unspecified (or underspecified) by passive component manufacturers.

In general, if you use data converters having 12 bits or more of resolution, or op amps that cost more than a few dollars, pay very close attention to passive components. Consider the case of a 12-bit DAC, where ½ LSB corresponds to 0.012% of full scale, or only 122 ppm. A host of passive component phenomena can accumulate errors far exceeding this! But, buying the most expensive passive components won't necessarily solve your problems either. Often, a *correct* 25-cent capacitor yields a better-performing, more cost-effective design than a premium-grade part. With a few basics, understanding and analyzing passive components may prove rewarding, albeit not easy.

Capacitors

Most designers are generally familiar with the range of capacitors available. But the mechanisms by which both static and dynamic errors can occur in precision circuit designs using capacitors are sometimes easy to forget, because of the tremendous variety of types available. These include dielectrics of glass, aluminum foil, solid tantalum and tantalum foil, silver mica, ceramic, Teflon, and the film capacitors, including polyester, polycarbonate, polystyrene, and polypropylene types. In addition to the traditional leaded packages, many of these are now also offered in surface mount styles.

Figure 7-1 is a workable model of a non-ideal capacitor. The nominal capacitance, C, is shunted by a resistance R_P, which represents *insulation resistance* or leakage. A second resistance, R_S, —*equivalent series resistance*, or ESR, —appears in series with the capacitor and represents the resistance of the capacitor leads and plates.

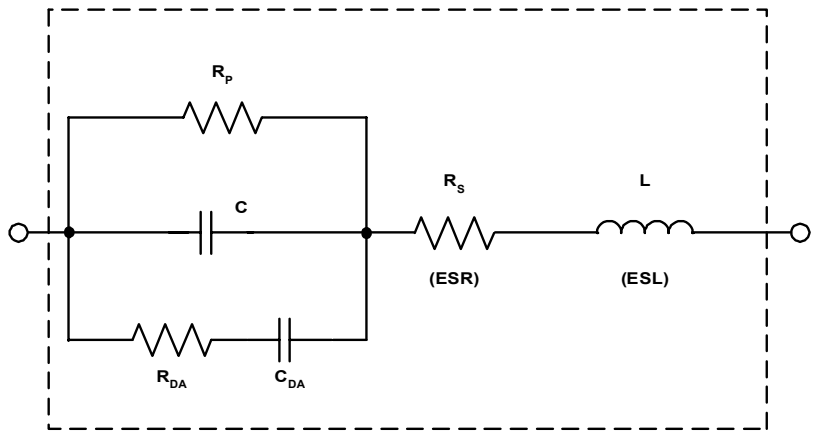


Figure 7-1: *A non-ideal capacitor equivalent circuit includes parasitic elements*

Note that capacitor phenomena aren't that easy to separate out. The matching of phenomena and models is for convenience in explanation. Inductance, L —the *equivalent series inductance*, or ESL, —models the inductance of the leads and plates. Finally, resistance R_{DA} and capacitance C_{DA} together form a simplified model of a phenomenon known as *dielectric absorption,* or DA. It can ruin fast and slow circuit dynamic performance. In a real capacitor R_{DA} and C_{DA} extend to include multiple parallel sets. These parasitic RC elements can act to degrade timing circuits substantially, and the phenomenon is discussed further below.

Dielectric Absorption

Dielectric absorption, which is also known as "soakage" and sometimes as "dielectric hysteresis" — is perhaps the least understood and potentially most damaging of various capacitor parasitic effects. Upon discharge, most capacitors are reluctant to give up all of their former charge, due to this memory consequence.

Figure 7-2 illustrates this effect. On the left of the diagram, after being charged to the source potential of V volts at time t_o, the capacitor is shorted by the switch S1 at time t_1, discharging it. At time t_2, the capacitor is then open-circuited; a residual voltage slowly

builds up across its terminals and reaches a nearly constant value. This error voltage is due to DA, and is shown in the right figure, a time/voltage representation of the charge/discharge/recovery sequence. Note that the recovered voltage error is proportional to both the original charging voltage V, as well as the rated DA for the capacitor in use.

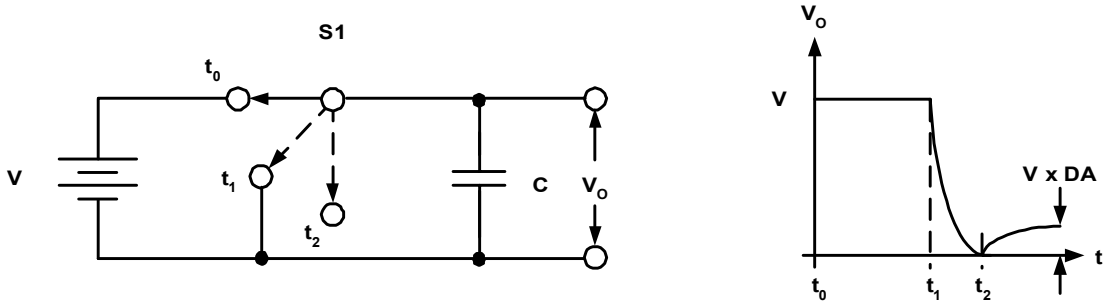


Figure 7-2: *A residual open-circuit voltage after charge/discharge characterizes capacitor dielectric absorption*

Standard techniques for specifying or measuring dielectric absorption are few and far between. Measured results are usually expressed as the percentage of the original charging voltage that reappears across the capacitor. Typically, the capacitor is charged for a long period, then shorted for a shorter established time. The capacitor is then allowed to recover for a specified period, and the residual voltage is then measured (see Reference 8 for details). While this explanation describes the basic phenomenon, it is important to note that real-world capacitors vary quite widely in their susceptibility to this error, with their rated DA ranging from well below to above 1%, the exact number being a function of the dielectric material used.

In practice, DA makes itself known in a variety of ways. Perhaps an integrator refuses to reset to zero, a voltage-to-frequency converter exhibits unexpected nonlinearity, or a sample-hold (SH) exhibits varying errors. This last manifestation can be particularly damaging in a data-acquisition system, where adjacent channels may be at voltages which differ by nearly full scale, as shown below.

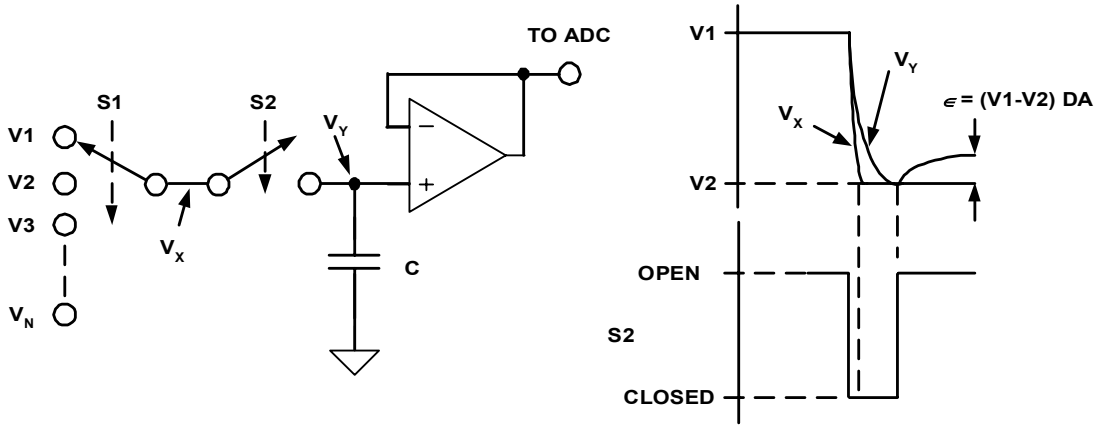


Figure 7-3: *Dielectric absorption induces errors in SH applications*

Figure 7-3 illustrates the case of DA error in a simple SH. On the left, switches S1 and S2 represent an input multiplexer and SH switch, respectively. The multiplexer output voltage is V_X, and the sampled voltage held on C is V_Y, which is buffered by the op amp for presentation to an ADC. As can be noted by the timing diagram on the right, a DA

error voltage, ϵ, appears in the hold mode, when the capacitor is effectively open circuit. This voltage is proportional to the difference of voltages V1 and V2, which, if at opposite extremes of the dynamic range, exacerbates the error. As a practical matter, the best solution for good performance in terms of DA in a SH is to use only the best capacitor.

The DA phenomenon is a characteristic of the dielectric material itself, although inferior manufacturing processes or electrode materials can also affect it. DA is specified as a percentage of the charging voltage. It can range from a low of 0.02% for Teflon, polystyrene, and polypropylene capacitors, up to a high of 10% or more for some electrolytics. For some time frames, the DA of polystyrene can be as low as 0.002%.

Common high-K ceramics and polycarbonate capacitor types display typical DA on the order of 0.2%, it should be noted this corresponds to ½ LSB at only 8 bits! Silver mica, glass, and tantalum capacitors typically exhibit even larger DA, ranging from 1.0% to 5.0%, with those of polyester devices failing in the vicinity of 0.5%. As a rule, if the capacitor spec sheet doesn't specifically discuss DA *within your time frame and voltage range*, exercise caution! Another type with lower *specified* DA is likely a better choice.

DA can produce long tails in the transient response of fast-settling circuits, such as those found in high-pass active filters or ac amplifiers. In some devices used for such applications, Figure 7-1's R_{DA}-C_{DA} model of DA can have a time constant of milliseconds. Much longer time constants are also quite usual. In fact, several paralleled R_{DA}-C_{DA} circuit sections with a wide range of time constants can model some devices. In fast-charge, fast-discharge applications, the behavior of the DA mechanism resembles "analog memory"; the capacitor in effect tries to remember its previous voltage.

In some designs, you can compensate for the effects of DA if it is simple and easily characterized, and you are willing to do custom tweaking. In an integrator, for instance, the output signal can be fed back through a suitable compensation network, tailored to cancel the circuit equivalent of the DA by placing a negative impedance effectively in parallel. Such compensation has been shown to improve SH circuit performance by factors of 10 or more (Reference 6).

Capacitor Parasitics and Dissipation Factor

In Figure 7-1, a capacitor's leakage resistance, R_P, the effective series resistance, R_S, and effective series inductance, L, act as parasitic elements, which can degrade an external circuit's performance. The effects of these elements are often lumped together and defined as a dissipation factor, or DF.

A capacitor's leakage is the small current that flows through the dielectric when a voltage is applied. Although modeled as a simple insulation resistance (R_P) in parallel with the capacitor, the leakage actually is nonlinear with voltage. Manufacturers often specify leakage as a megohm-microfarad product, which describes the dielectric's self-discharge time constant, in seconds. It ranges from a low of 1s or less for high-leakage capacitors, such as electrolytic devices, to the 100's of seconds for ceramic capacitors. Glass devices exhibit self-discharge time-constants of 1,000 or more; but the best leakage performance is shown by Teflon and the film devices (polystyrene, polypropylene), with time

constants exceeding 1,000,000 megohm-microfarads. For such a device, external leakage paths—created by surface contamination of the device's case or in the associated wiring or physical assembly—can overshadow the internal dielectric-related leakage.

Effective series inductance, ESL (Figure 7-1, again) arises from the inductance of the capacitor leads and plates, which, particularly at the higher frequencies, can turn a capacitor's normally capacitive reactance into an inductive reactance. Its magnitude strongly depends on construction details within the capacitor. Tubular wrapped-foil devices display significantly more lead inductance than molded radial-lead configurations. Multilayer ceramic and film-type devices typically exhibit the lowest series inductance, while ordinary tantalum and aluminum electrolytics typically exhibit the highest. Consequently, standard electrolytic types, if used alone, usually prove insufficient for *high-speed* local bypassing applications. Note however that there also are more specialized aluminum and tantalum electrolytics available, which may be suitable for higher speed uses. These are the types generally designed for use in switch-mode power supplies, which are covered more completely in a following section.

Manufacturers of capacitors often specify effective series impedance by means of impedance-versus-frequency plots. Not surprisingly, these curves show graphically a predominantly capacitive reactance at low frequencies, with rising impedance at higher frequencies because of the effect of series inductance.

Effective series resistance, ESR (resistor R_S of Figure 7-1), is made up of the resistance of the leads and plates. As noted, many manufacturers lump the effects of ESR, ESL, and leakage into a single parameter called *dissipation factor*, or DF. Dissipation factor measures the basic inefficiency of the capacitor. Manufacturers define it as the ratio of the energy lost to energy stored per cycle by the capacitor. The ratio of ESR to total capacitive reactance— at a specified frequency— approximates the dissipation factor, which turns out to be equivalent to the reciprocal of the figure of merit, Q. Stated as an approximation, $Q \approx 1/DF$ (with DF in numeric terms). For example, a DF of 0.1% is equivalent to a fraction of 0.001; thus the inverse in terms of Q would be 1000.

Dissipation factor often varies as a function of both temperature and frequency. Capacitors with mica and glass dielectrics generally have DF values from 0.03% to 1.0%. For ordinary ceramic devices, DF ranges from a low of 0.1 % to as high as 2.5 % at room temperature. And electrolytics usually exceed even this level. The film capacitors are the best as a group, with DFs of less than 0.1 %. Stable-dielectric ceramics, notably the NP0 (also called COG) types, have DF specs comparable to films (more below).

Tolerance, Temperature, and Other Effects

In general, precision capacitors are expensive and— even then— not necessarily easy to buy. In fact, choice of capacitance is limited both by the range of available values, and also by tolerances. In terms of size, the better performing capacitors in the film families tend to be limited in practical terms to 10μF or less (for dual reasons of size and expense). In terms of low value tolerance, ±1% is possible for NP0 ceramic and some film devices, but with possibly unacceptable delivery times. Many film capacitors can be made available with tolerances of less than ±1%, but on a special order basis only.

Most capacitors are sensitive to temperature variations. DF, DA, and capacitance value are all functions of temperature. For some capacitors, these parameters vary approximately linearly with temperature, in others they vary quite nonlinearly. Although it is usually not important for SH applications, an excessively large *temperature coefficient* (TC, measured in ppm/°C) can prove harmful to the performance of precision integrators, voltage-to-frequency converters, and oscillators. NP0 ceramic capacitors, with TCs as low as 30 ppm/°C, are the best for stability, with polystyrene and polypropylene next best, with TCs in the 100-200 ppm/°C range. On the other hand, when capacitance stability is important, one should stay away from types with TCs of more than a few hundred ppm/°C, or in fact any TC which is nonlinear.

A capacitor's maximum working temperature should also be considered, in light of the expected environment. Polystyrene capacitors, for instance, melt near 85°C, compared to Teflon's ability to survive temperatures up to 200°C.

Sensitivity of capacitance and DA to applied voltage, expressed as *voltage coefficient*, can also hurt capacitor performance within a circuit application. Although capacitor manufacturers don't always clearly specify voltage coefficients, the user should always consider the possible effects of such factors. For instance, when maximum voltages are applied, some high-K ceramic devices can experience a decrease in capacitance of 50% or more. This is an inherent distortion producer, making such types unsuitable for signal path filtering, for example, and better suited for supply bypassing. Interestingly, NP0 ceramics, the stable dielectric subset from the wide range of available ceramics, do offer good performance with respect to voltage coefficient.

Similarly, the capacitance, and dissipation factor of many types vary significantly with frequency, mainly as a result of a variation in dielectric constant. In this regard, the better dielectrics are polystyrene, polypropylene, and Teflon.

Assemble Critical Components Last

The designer's worries don't end with the design process. Some common printed circuit assembly techniques can prove ruinous to even the best designs. For instance, some commonly used cleaning solvents can infiltrate certain electrolytic capacitors— those with rubber end caps are particularly susceptible. Even worse, some of the film capacitors, polystyrene in particular, actually melt when contacted by some solvents. Rough handling of the leads can damage still other capacitors, creating random or even intermittent circuit problems. Etched-foil types are particularly delicate in this regard. To avoid these difficulties it may be advisable to mount especially critical components as the last step in the board assembly process— if possible.

Table 7-1 summarizes selection criteria for various capacitor types, arranged roughly in order of decreasing DA performance. In a selection process, the general information of this table should be supplemented by consultation of current vendor's catalog information (see References at end of section).

Table 7-1
Capacitor Comparison Chart

TYPE	TYPICAL DA	ADVANTAGES	DISADVANTAGES
Polystyrene	0.001% to 0.02%	Inexpensive Low DA Good stability (~120ppm/°C)	Damaged by temperature > +85°C Large High inductance Vendors limited
Polypropylene	0.001% to 0.02%	Inexpensive Low DA Stable (~200ppm/°C) Wide range of values	Damaged by temperature > +105°C Large High inductance
Teflon	0.003% to 0.02%	Low DA available Good stability Operational above +125 °C Wide range of values	Expensive Large High inductance
Polycarbonate	0.1%	Good stability Low cost Wide temperature range Wide range of values	Large DA limits to 8-bit applications High inductance
Polyester	0.3% to 0.5%	Moderate stability Low cost Wide temperature range Low inductance (stacked film)	Large DA limits to 8-bit applications High inductance (conventional)
NP0 Ceramic	<0.1%	Small case size Inexpensive, many vendors Good stability (30ppm/°C) 1% values available Low inductance (chip)	DA generally low (may not be specified) Low maximum values (≤ 10nF)
Monolithic Ceramic (High K)	>0.2%	Low inductance (chip) Wide range of values	Poor stability Poor DA High voltage coefficient
Mica	>0.003%	Low loss at HF Low inductance Good stability 1% values available	Quite large Low maximum values (≤ 10nF) Expensive
Aluminum Electrolytic	Very high	Large values High currents High voltages Small size	High leakage Usually polarized Poor stability, accuracy Inductive
Tantalum Electrolytic	Very high	Small size Large values Medium inductance	High leakage Usually polarized Expensive Poor stability, accuracy

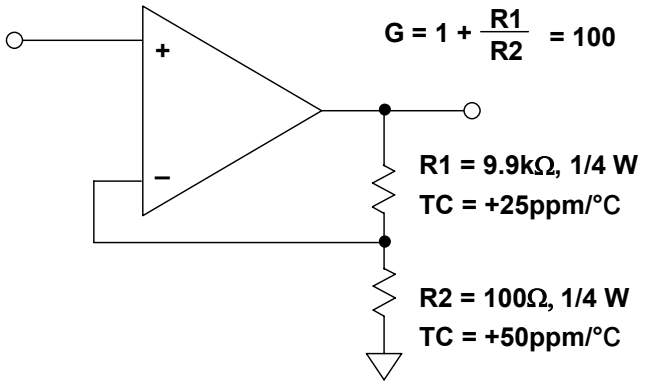
Designers should also consider the natural failure mechanisms of capacitors. Metallized film devices, for instance, often self-heal. They initially fail due to conductive bridges that develop through small perforations in the dielectric film. But, the resulting fault currents can generate sufficient heat to destroy the bridge, thus returning the capacitor to normal operation (at a slightly lower capacitance). Of course, applications in high-impedance circuits may not develop sufficient current to clear the bridge, so the designer must be wary here.

Tantalum capacitors also exhibit a degree, of self-healing, but— unlike film capacitors— the phenomenon depends on the temperature at the fault location rising slowly. Therefore, tantalum capacitors self-heal best in high impedance circuits which limit the surge in current through the capacitor's defect. Use caution therefore, when specifying tantalums for high-current applications.

Electrolytic capacitor life often depends on the rate at which capacitor fluids seep through end caps. Epoxy end seals perform better than rubber seals, but an epoxy sealed capacitor can explode under severe reverse-voltage or overvoltage conditions. Finally, *all* polarized capacitors must be protected from exposure to voltages outside their specifications.

Resistors and Potentiometers

Designers have a broad range of resistor technologies to choose from, including carbon composition, carbon film, bulk metal, metal film, and both inductive and non-inductive wire-wound types. As perhaps the most basic— and presumably most trouble-free— of components, resistors are often overlooked as error sources in high performance circuits.



- **Temperature change of 10°C causes gain change of 250ppm**
- **This is 1LSB in a 12-bit system and a disaster in a 16-bit system**

Figure 7-4: *Mismatched resistor TCs can induce temperature-related gain errors*

Yet, an improperly selected resistor can subvert the accuracy of a 12-bit design by developing errors well in excess of 122 ppm (½ LSB). When did you last read a resistor data sheet? You'd be surprised what can be learned from an informed review of data.

Consider the simple circuit of Figure 7-4, showing a non-inverting op amp where the 100x gain is set by R1 and R2. The TCs of these two resistors are a somewhat obvious source of error. Assume the op amp gain errors to be negligible, and that the resistors are

perfectly matched to a 99/1 ratio at +25ºC. If, as noted, the resistor TCs differ by only 25ppm/ºC, the gain of the amplifier changes by 250ppm for a 10ºC temperature change. This is about a 1 LSB error in a 12-bit system, and a major disaster in a 16-bit system. Temperature changes, however, can limit the accuracy of the Figure 7-4 amplifier in several ways. In this circuit (as well as many op amp circuits with component-ratio defined gains), the *absolute* TC of the resistors is less important— *as long as they track one another in ratio*. But even so, some resistor types simply aren't suitable for precise work. For example, *carbon composition* units—with TCs of approximately 1,500 ppm/°C, won't work. Even if the TCs could be matched to an unlikely 1%, the resulting 15 ppm/°C differential still proves inadequate— an 8°C shift creates a 120 ppm error.

Many manufacturers offer metal film and bulk metal resistors, with absolute TCs ranging between ±1 and ±100 ppm/°C. Beware, though; TCs can vary a great deal, particularly among discrete resistors from different batches. To avoid this problem, more expensive matched resistor pairs are offered by some manufacturers, with temperature coefficients that track one another to within 2 to 10 ppm/°C. Low-priced thin-film networks have good relative performance and are widely used.

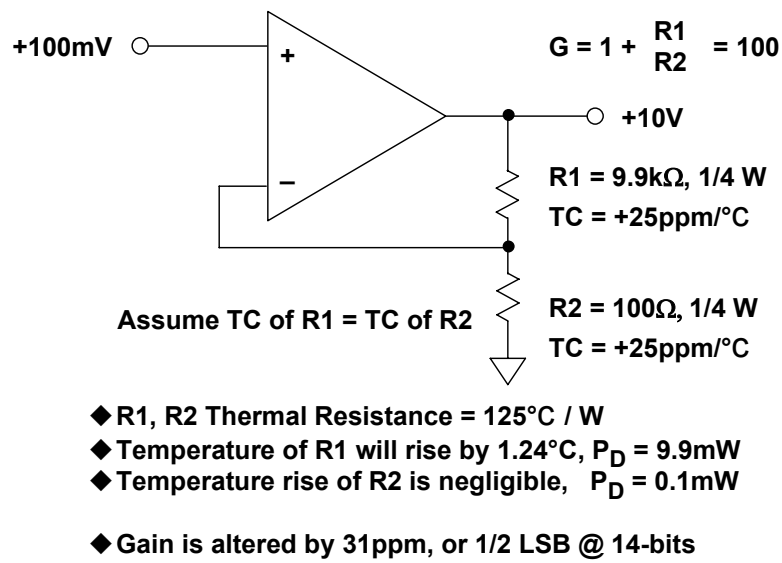


Figure 7-5: *Uneven power dissipation between resistors with identical TCs can also introduce temperature-related gain errors*

Suppose, as shown in Figure 7-5, R1 and R2 are ¼W resistors with identical 25ppm/ºC TCs. Even when the TCs are identical, there can still be significant errors! When the signal input is zero, the resistors dissipate no heat. But, if it is 100mV, there is 9.9V across R1, which then dissipates 9.9mW. It will experience a temperature rise of 1.24ºC (due to a 125ºC/W ¼W resistor thermal resistance). This 1.24ºC rise causes a resistance change of 31ppm, and thus a corresponding gain change. But R2, with only 100mV across it, is only heated a negligible 0.0125ºC. The resulting 31 ppm net gain error represents a fullscale error of ½ LSB at 14-bits, and is a disaster for a 16-bit system.

Even worse, the effects of this resistor self-heating also create easily calculable *nonlinearity errors*. In the Figure 7-5 example, with ½ the voltage input, the resulting self-heating error is only 15 ppm. In other words, the stage gain is not constant at ½ and

full scale (nor is it so at other points), as long as uneven temperature shifts exist between the gain-determining resistors. This is by no means a worst-case example; physically smaller resistors would give worse results, due to higher associated thermal resistance.

These, and similar errors, are avoided by selecting critical resistors that are accurately matched for both value and TC, are well derated for power, and have tight thermal coupling between those resistors were matching is important. This is best achieved by using a resistor network on a single substrate— such a network may either be within an IC, or it may be a separately packaged thin-film resistor network.

When the circuit resistances are very low (≤10Ω), *interconnection stability* also becomes important. For example, while often overlooked as an error, the resistance TC of typical copper wire or printed circuit traces can add errors. The TC of copper is typically ~3,900 ppm/°C. Thus a precision 10Ω, 10 ppm/°C wirewound resistor with 0. 1Ω of copper interconnect effectively becomes a 10.1Ω resistor with a TC of nearly 50 ppm/°C.

One final consideration applies mainly to designs that see widely varying ambient temperatures: a phenomenon known as *temperature retrace* describes the change in resistance which occurs after a specified number of cycles of exposure to low and high ambients with constant internal dissipation. Temperature retrace can exceed 10 ppm/°C, even for some of the better thin-film components.

- **Closely match resistance TCs.**
- **Use resistors with low absolute TCs.**
- **Use resistors with low thermal resistance (higher power ratings, larger cases).**
- **Tightly couple matched resistors thermally (use standard common-substrate networks).**
- **For large ratios consider using stepped attenuators.**

Figure 7-6: *A number of points are important towards minimizing temperature-related errors in resistors*

In summary, to design resistance-based circuits for minimum temperature-related errors, consider the points noted in Figure 7-6 (along with their cost):

Resistor Parasitics

Resistors can exhibit significant levels of parasitic inductance or capacitance, especially at high frequencies. Manufacturers often specify these parasitic effects as a reactance error, in % or ppm, based on the ratio of the difference between the impedance magnitude and the dc resistance, to the resistance, at one or more frequencies.

Wirewound resistors are especially susceptible to difficulties. Although resistor manufacturers offer wirewound components in either normal or noninductively wound form, even noninductively wound resistors create headaches for designers. These

resistors still appear slightly inductive (of the order of 20 μH) for values below 10kΩ. Above 10kΩ the same style resistors actually exhibit 5 pF of shunt capacitance.

These parasitic effects can raise havoc in dynamic circuit applications. Of particular concern are applications using wirewound resistors with values both greater than 10kΩ. Here it isn't uncommon to see peaking, or even oscillation. These effects become more evident at low-kHz frequency ranges.

Even in low-frequency circuit applications, parasitic effects in wirewound resistors can create difficulties. Exponential settling to 1 ppm may take 20 time constants or more. The parasitic effects associated with wirewound resistors can significantly increase net circuit settling time to beyond the length of the basic time constants.

Unacceptable amounts of parasitic reactance are often found even in resistors that aren't wirewound. For instance, some metal-film types have significant interlead capacitance, which shows up at high frequencies. In contrast, when considering this end-end capacitance, carbon resistors do the best at high frequencies.

Thermoelectric Effects

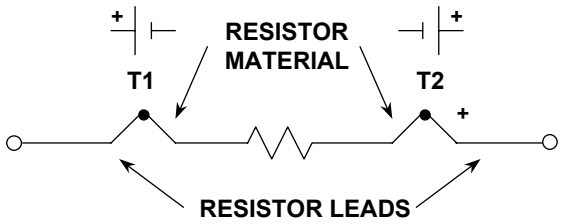
Another more subtle problem with resistors is the *thermocouple effect*, also sometimes referred to as *thermal EMF*. Wherever there is a junction between two different metallic conductors, a thermoelectric voltage results. The thermocouple effect is widely used to measure temperature, as described in detail within Chapter 4. However, in any low level precision op amp circuit it is also a potential source of inaccuracy, since wherever two different conductors meet, a thermocouple is formed (whether we like it or not). In fact, in many cases, it can easily produce the dominant error within an otherwise precision circuit design.

Parasitic thermocouples will cause errors when and if the various junctions forming the parasitic thermocouples are at different temperatures. With two junctions present on each side of the signal being processed within a circuit, by definition we have formed at least one thermocouple pair. If the two junctions of this thermocouple pair are at different temperatures, there will be a net temperature dependent error voltage produced. Conversely, if the two junctions of a parasitic thermocouple pair are kept at an identical temperature, then the net error produced will be zero, as the voltages of the two thermocouples effectively will be canceled.

This is a critically important point, since in practice we cannot avoid connecting dissimilar metals together to build an electronic circuit. But, what we can do is carefully control temperature differentials across the circuit, so such that the undesired thermocouple errors cancel one another.

The effect of such parasitics is very hard to avoid. To understand this, consider a case of making connections *with copper wire only*. In this case, even a junction formed by different copper wire alloys can have a thermoelectric voltage which is a small fraction of 1μV/ºC! And, taking things a step further, even such apparently benign components as resistors contain parasitic thermocouples, with potentially even stronger effects.

For example, consider the resistor model shown in Figure 7-7. The two connections between the resistor material and the leads form thermocouple junctions, T1 and T2. This thermocouple EMF can be as high as 400µV/ºC for some carbon composition resistors, and as low as 0.05µV/ºC for specially constructed resistors (see Reference 15). Ordinary metal film resistors (RN-types) are typically about 20µV/ºC.



TYPICAL RESISTOR THERMOCOUPLE EMFs

◆ CARBON COMPOSITION	≈ 400 µV/ °C
◆ METAL FILM	≈ 20 µV/ °C
◆ EVENOHM OR MANGANIN WIREWOUND	≈ 2 µV/ °C
◆ RCD Components HP-Series	≈ 0.05 µV/ °C

Figure 7-7: *Every resistor contains two thermocouples, formed between the leads and resistance element*

Note that these thermocouple effects are relatively unimportant for ac signals. Even for DC-only signals, they will nicely cancel one another, if, as noted above, the entire resistor is at a uniform temperature. However, if there is significant power dissipation in a resistor, or if its orientation with respect to a heat source is non-symmetrical, this can cause one of its ends to be warmer than the other, causing a net thermocouple error voltage. Using ordinary metal film resistors, an end-to-end temperature differential of 1ºC causes a thermocouple voltage of about 20µV. This error level is quite significant compared to the offset voltage drift of a precision op amp like the OP177, and extremely significant when compared to chopper-stabilized op amps, with their drifts of <1µV/°C.

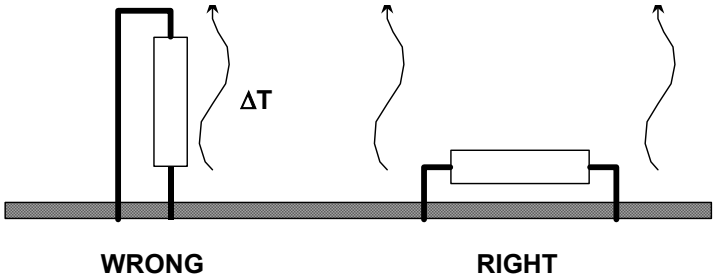


Figure 7-8: *The effects of thermocouple emfs generated by resistors can be minimized by orientation that normalizes the end temperatures*

Figure 7-8 shows how resistor orientation can make a difference in the net thermocouple voltage. In the left diagram, standing the resistor on end in order to conserve board space will invariably cause a temperature gradient across the resistor, especially if it is dissipating any significant power. In contrast, placing the resistor flat on the PC board as shown at the right will generally eliminate the gradient. An exception might occur, if

there is end-to-end resistor airflow. For such cases, orienting the resistor axis perpendicular to the airflow will minimize this source of error, since this tends to force the resistor ends to the same temperature.

Note that this line of thinking should be extended, to include orientation of resistors on a vertically mounted PC board. In such cases, natural convection air currents tend to flow upward across the board. Again, the resistor thermal axis should be perpendicular to convection, to minimize thermocouple effects. With tiny surface mount resistors, the thermocouple effects can be less problematic, due to tighter thermal coupling between the resistor ends.

In general, designers should strive to avoid thermal gradients on or around critical circuit boards. Often this means thermally isolating components that dissipate significant amounts of power. Thermal turbulence created by large temperature gradients can also result in dynamic noise-like low-frequency errors.

Voltage Sensitivity, Failure Mechanisms, and Aging

Resistors are also plagued by changes in value as a function of applied voltage. The deposited-oxide high-megohm type components are especially sensitive, with voltage coefficients ranging from 1 ppm/V to more than 200 ppm/V. This is another reason to exercise caution in such precision applications as high-voltage dividers.

The normal failure mechanism of a resistor can also create circuit difficulties, if not carefully considered beforehand. For example, carbon-composition resistors fail safely, by turning into open circuits. Consequently, in some applications, these components can play a useful secondary role, as a fuse. Replacing such a resistor with a carbon-film type can possibly lead to trouble, since carbon-films can fail as short circuits. (Metal-film components usually fail as open circuits.)

All resistors tend to change slightly in value with age. Manufacturers specify long-term stability in terms of change— ppm/year. Values of 50 or 75 ppm/year are not uncommon among metal film resistors. For critical applications, metal-film devices should be burned-in for at least one week at rated power. During burn-in, resistance values can shift by up to 100 or 200 ppm. Metal film resistors may need 4-5000 operational hours for full stabilization, especially if deprived of a burn-in period.

Resistor Excess Noise

Most designers have some familiarity with thermal, or Johnson noise, which occurs in resistors. But a less widely recognized secondary noise phenomenon is associated with resistors, and it is called *excess noise*. It can prove particularly troublesome in precision op amp and converter circuits, as it is evident only when current passes through a resistor.

To review briefly, thermal noise results from thermally induced random vibration of charge resistor carriers. Although the average current from the vibrations remains zero, instantaneous charge motions result in an instantaneous voltage across the terminals.

Excess noise on the other hand, occurs primarily when dc flows in a discontinuous medium— for example the conductive particles of a carbon composition resistor. The current flows unevenly through the compressed carbon granules, creating microscopic particle-to-particle "arcing". This phenomenon gives rise to a 1/f noise-power spectrum, in addition to the thermal noise spectrum. In other words, the excess spot noise voltage increases as the inverse square-root of frequency.

Excess noise often surprises the unwary designer. Resistor thermal noise and op amp input noise set the noise floor in typical op amp circuits. Only when voltages appear across input resistors and causes current to flow does the excess noise become a significant— and often dominant— factor. In general, carbon composition resistors generate the most excess noise. As the conductive medium becomes more uniform, excess noise becomes less significant. Carbon film resistors do better, with metal film, wirewound and bulk-metal-film resistors doing better yet.

Manufacturers specify excess noise in terms of a noise index— the number of microvolts of rms noise in the resistor in each decade of frequency per volt of dc drop across the resistor. The index can rise to 10dB (3 microvolts per dc volt per decade of bandwidth) or more. Excess noise is most significant at low frequencies, while above 100 kHz thermal noise predominates.

Potentiometers

Trimming potentiometers (trimpots) can suffer from most of the phenomena that plague fixed resistors. In addition, users must also remain vigilant against some hazards unique to these components.

For instance, many trimpots aren't sealed, and can be severely damaged by board washing solvents, and even by excessive humidity. Vibration— or simply extensive use— can damage the resistive element and wiper terminations. Contact noise, TCs, parasitic effects, and limitations on adjustable range can all hamper trimpot circuit operation. Furthermore, the limited resolution of wirewound types and the hidden limits to resolution in cermet and plastic types (hysteresis, incompatible material TCs, slack) make obtaining and maintaining precise circuit settings anything but an "infinite resolution" process. Given this background, two rules are suggested for the potential trimpot user. Rule 1: Use infinite care and infinitesimal adjustment range to avoid infinite frustration when applying manual trimpots. Rule 2: *Consider the elimination of manual trimming potentiometers altogether, if possible!* A number of digitally addressable potentiometers (RDACs) are now available for direct application in similar circuit functions as classic trimpots (See Reference 17). There are also many low cost multi-channel voltage output DACs expressly designed for system voltage trimming.

Table 7-2 summarizes selection criteria for various fixed resistor types, both in discrete form and as part of networks. In a selection process, the general information of this table should be supplemented by consultation of current vendor's catalog information (see References at end of section).

Table 7-2
Resistor Comparison Chart

	TYPE	ADVANTAGES	DISADVANTAGES
DISCRETE	Carbon Composition	Lowest Cost High Power/Small Case Size Wide Range of Values	Poor Tolerance (5%) Poor Temperature Coefficient (1500 ppm/°C)
	Wirewound	Excellent Tolerance (0.01%) Excellent TC (1ppm/°C) High Power	Reactance is a Problem Large Case Size Most Expensive
	Metal Film	Good Tolerance (0.1%) Good TC (<1 to 100ppm/°C) Moderate Cost Wide Range of Values Low Voltage Coefficient	Must be Stabilized with Burn-In Low Power
	Bulk Metal or Metal Foil	Excellent Tolerance (to 0.005%) Excellent TC (to <1ppm/°C) Low Reactance Low Voltage Coefficient	Low Power Very Expensive
	High Megohm	Very High Values (10^8 to $10^{14}\Omega$) Only Choice for Some Circuits	High Voltage Coefficient (200ppm/V) Fragile Glass Case (Needs Special Handling) Expensive
NETWORKS	Thick Film	Low Cost High Power Laser-Trimmable Readily Available	Fair Matching (0.1%) Poor TC (>100ppm/°C) Poor Tracking TC (10ppm/°C)
	Thin Film	Good Matching (<0.01%) Good TC (<100ppm/°C) Good Tracking TC (2ppm/°C) Moderate Cost Laser-Trimmable Low Capacitance Suitable for Hybrid IC Substrate	Often Large Geometry Limited Values and Configurations

Inductance

Stray Inductance

All conductors are inductive, and at high frequencies, the inductance of even quite short pieces of wire or printed circuit traces may be important. The inductance of a straight wire of length L mm and circular cross-section with radius R mm in free space is given by the first equation shown in Figure 7-9.

The inductance of a strip conductor (an approximation to a PC track) of width W mm and thickness H mm in free space is also given by the second equation in Figure 7-9.

In real systems, these formulas both turn out to be approximate, but they do give some idea of the order of magnitude of inductance involved. They tell us that 1cm of 0.5mm od wire has an inductance of 7.26nH, and 1cm of 0.25mm PC track has an inductance of 9.59nH - these figures are reasonably close to measured results.

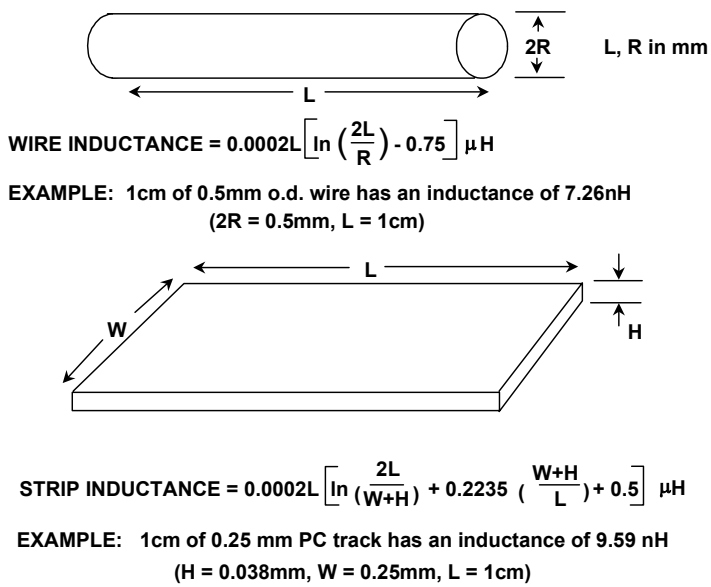


Figure 7-9: *Wire and strip inductance calculations*

At 10MHz, an inductance of 7.26nH has an impedance of 0.46 ohm, and so can give rise to 1% error in a 50 ohm system.

Mutual Inductance

Another consideration regarding inductance is the separation of outward and return currents. As we shall discuss in more detail later, Kirchoff's Law tells us that current flows in closed paths— there is always an outward and return path. The whole path forms a single-turn inductor.

This principle is illustrated by the contrasting signal trace routing arrangements of Figure 7-10 (opposite). If the area enclosed within the turn is relatively large, as in the upper "nonideal" picture, then the inductance (and hence the AC impedance) will also be large.

On the other hand, if the outward and return paths are closer together, as in the lower "improved" picture, the inductance will be much smaller.

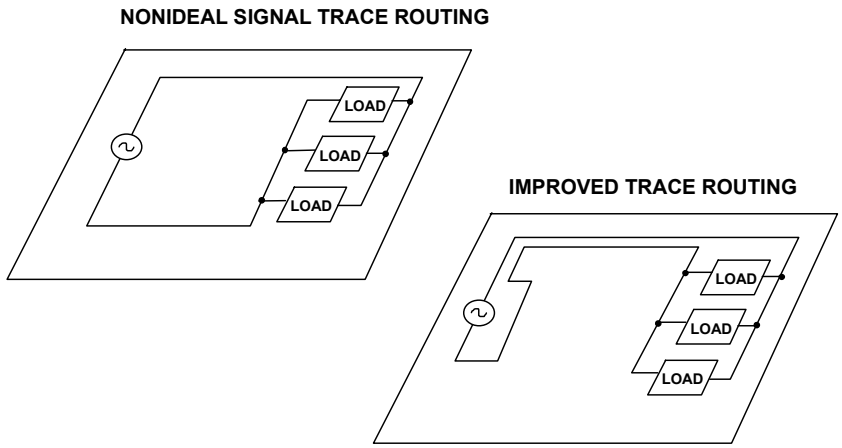
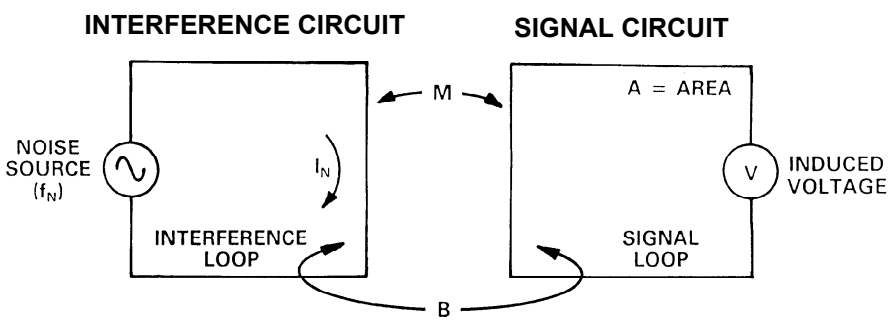


Figure 7-10: *Nonideal and improved signal trace routing*

Note that the nonideal signal routing case of Figure 7-10 has other drawbacks— the large area enclosed within the conductors produces extensive external magnetic fields, which may interact with other circuits, causing unwanted coupling. Similarly, the large area is more vulnerable to interaction with external magnetic fields, which can induce unwanted signals in the loop.



M = MUTUAL INDUCTANCE
B = MAGNETIC REFLUX DENSITY
A = AREA OF SIGNAL LOOP
$\omega_N = 2\pi f_N$ = FREQUENCY OF NOISE SOURCE

V = INDUCED VOLTAGE = $\omega_N M I_N = \omega AB$

Figure 7-11: *Basic principles of inductive coupling*

The basic principle is illustrated in Figure 7-11, and is a common mechanism for the transfer of unwanted signals (noise) between two circuits.

As with most other noise sources, as soon as we define the working principle, we can see ways of reducing the effect. In this case, reducing any or all of the terms in the equations in Figure 7-11 reduces the coupling. Reducing the frequency or amplitude of the current causing the interference may be impracticable, but it is frequently possible to reduce the

mutual inductance between the interfering and interfered with circuits by reducing loop areas on one or both sides and, possibly, increasing the distance between them.

A layout solution is illustrated by Figure 7-12. Here two circuits, shown as Z1 and Z2, are minimized for coupling by keeping each of the loop areas as small as is practical.

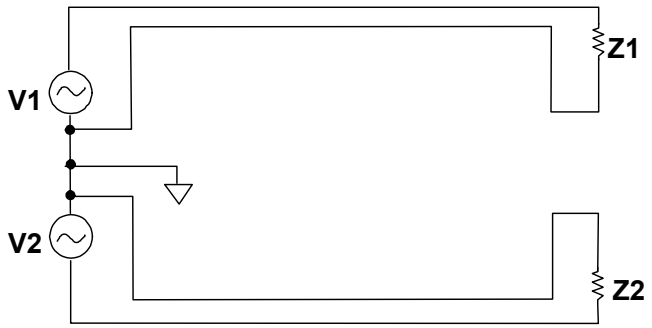


Figure 7-12: *Proper signal routing and layout can reduce inductive coupling*

As also illustrated in Figure 7-13, mutual inductance can be a problem in signals transmitted on cables. Mutual inductance is high in ribbon cables, especially when a single return is common to several signal circuits (top). Separate, dedicated signal and return lines for each signal circuit reduces the problem (middle). Using a cable with twisted pairs for each signal circuit as in the bottom picture is even better (but is more expensive and often unnecessary).

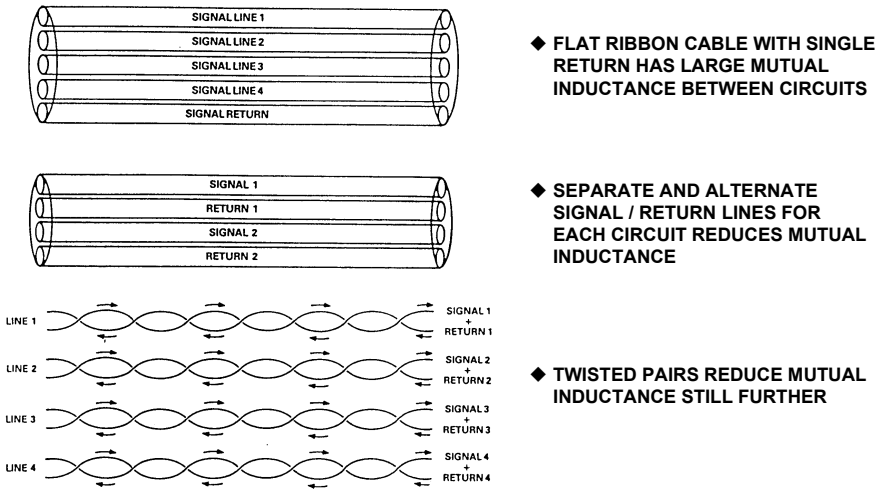


Figure 7-13: *Mutual inductance and coupling within signal cabling*

Shielding of magnetic fields to reduce mutual inductance is sometimes possible, but is by no means as easy as shielding an electric field with a Faraday shield (following section). HF magnetic fields are blocked by conductive material provided the skin depth in the conductor at the frequency to be screened is much less than the thickness of the conductor, and the screen has no holes (Faraday shields can tolerate small holes, magnetic screens cannot). LF and DC fields may be screened by a shield made of mu-metal sheet. Mu-metal is an alloy having very high permeability, but it is expensive, its magnetic properties are damaged by mechanical stress, and it will saturate if exposed to too high fields. Its use, therefore, should be avoided where possible.

Ringing

An inductor in series or parallel with a capacitor forms a resonant, or "tuned", circuit, whose key feature is that it shows marked change in impedance over a small range of frequency. Just how sharp the effect is depends on the relative Q of the tuned circuit. The effect is widely used to define the frequency response of narrow-band circuitry, but can also be a potential problem source.

If stray inductance and capacitance (which may or may not be stray) in a circuit should form a tuned circuit, then that tuned circuit may be excited by signals in the circuit, and ring at its resonant frequency.

An example is shown in Figure 7-14, where the resonant circuit formed by an inductive power line and its decoupling capacitor may possibly be excited by fast pulse currents drawn by the powered IC.

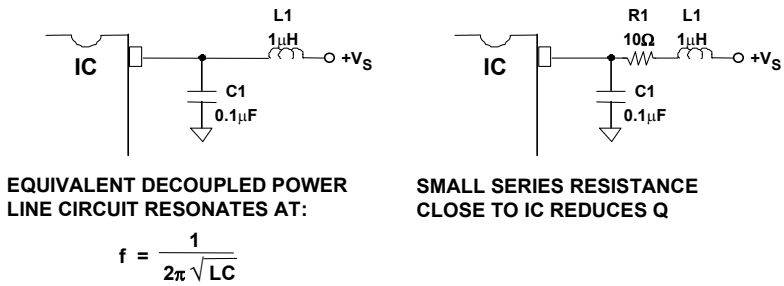


Figure 7-14: *Resonant circuit formed by power line decoupling*

While normal trace inductance and typical decoupling capacitances of 0.01 – 0.1μF will resonate well above a few MHz, an example 0.1μF capacitor and 1μH of inductance resonates at 500kHz. Left unchecked, this could present a resonance problem, as shown in the left case. Should an undesired power line resonance be present, the effect may be minimized by lowering the Q of the inductance. This is most easily done by inserting a small resistance (~10Ω) in the power line close to the IC, as shown in the right case.

Parasitic Effects in Inductors

Although inductance is one of the fundamental properties of an electronic circuit, inductors are far less common as components than are resistors and capacitors. As for precision components, they are even more rare. This is because they are harder to manufacture, less stable, and less physically robust than resistors and capacitors. It is relatively easy to manufacture stable precision inductors with inductances from nH to tens or hundreds of uH, but larger valued devices tend to be less stable, and large.

As we might expect in these circumstances, circuits are designed, where possible, to avoid the use of precision inductors. We find that stable precision inductors are relatively rarely used in precision analog circuitry, except in tuned circuits for high frequency narrow band applications.

Of course, they are widely used in power filters, switching power supplies and other applications where lack of precision is unimportant (more on this in a following section).

The important features of inductors used in such applications are their current carrying and saturation characteristics, and their Q. If an inductor consists of a coil of wire with an air core, its inductance will be essentially unaffected by the current it is carrying. On the other hand, if it is wound on a core of a magnetic material (magnetic alloy or ferrite), its inductance will be non-linear, since at high currents, the core will start to saturate. The effects of such saturation will reduce the efficiency of the circuitry employing the inductor and is liable to increase noise and harmonic generation.

As mentioned above, inductors and capacitors together form tuned circuits. Since all inductors will also have some stray capacity, all inductors will have a resonant frequency (which will normally be published on their data sheet), and should only be used as precision inductors at frequencies well below this.

Q or "Quality Factor"

The other characteristic of inductors is their Q (or "Quality Factor"), which is the ratio of the reactive impedance to the resistance, as indicated in Figure 7-15.

- **$Q = 2\pi f L/R$**
- **The Q of an inductor or resonant circuit is a measure of the ratio of its reactance to its resistance.**
- **The resistance is the HF and NOT the DC value.**
- **The 3 dB bandwidth of a single tuned circuit is Fc/Q where Fc is the center frequency.**

Figure 7-15: *Inductor Q or quality factor*

It is rarely possible to calculate the Q of an inductor from its DC resistance, since skin effect (and core losses if the inductor has a magnetic core) ensure that the Q of an inductor at high frequencies is always lower than that predicted from DC values.

Q is also a characteristic of tuned circuits (and of capacitors— but capacitors generally have such high Q values that it may be disregarded, in practice). The Q of a tuned circuit, which is generally very similar to the Q of its inductor (unless it is deliberately lowered by the use of an additional resistor), is a measure of its bandwidth around resonance. LC tuned circuits rarely have Q of much more than 100 (3dB bandwidth of 1%), but ceramic resonators may have a Q of thousands, and quartz crystals tens of thousands.

Don't Overlook Anything

Remember, if your precision op amp or data-converter-based design does not meet specification, try not to overlook anything in your efforts to find the error sources. Analyze both active *and* passive components, trying to identify and challenge any assumptions or preconceived notions that may blind you to the facts. Take nothing for granted.

For example, when not tied down to prevent motion, cable conductors, moving within their surrounding dielectrics, can create significant static charge buildups that cause errors, especially when connected to high-impedance circuits. Rigid cables, or even costly low-noise Teflon-insulated cables, are expensive alternative solutions.

As more and more high-precision op amps become available, and system designs call for higher speed and increased accuracy, a thorough understanding of the error sources described in this section (as well those following) becomes more important.

Some additional discussions of passive components within a succeeding power supply filtering section complements this one. In addition, the very next section on PCB design issues also complements many points within this section. Similar comments apply to the section on EMI/RFI.

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ACKNOWLEDGEMENTS:

Portions of this and the following section were adapted from Doug Grant and Scott Wurcer, "Avoiding Passive Component Pitfalls," originally published in **Analog Dialogue 17-2**, 1983.

NOTES:

SECTION 7-2: PCB DESIGN ISSUES

James Bryant

Printed circuit boards (PCBs) are by far the most common method of assembling modern electronic circuits. Comprised of a sandwich of insulating layer (or layers) and one or more copper conductor patterns, they can introduce various forms of errors into a circuit, particularly if the circuit is operating at either high precision or high speed. PCBs then, act as "unseen" components, wherever they are used in precision circuit designs. Since designers don't always consider the PCB electrical characteristics as additional components of their circuit, overall performance can easily end up worse than predicted. This general topic, manifested in many forms, is the focus of this section.

PCB effects that are harmful to precision circuit performance include leakage resistances, spurious voltage drops in trace foils, vias, and ground planes, the influence of stray capacitance, dielectric absorption (DA), and the related "hook". In addition, the tendency of PCBs to absorb atmospheric moisture, *hygroscopicity,* means that changes in humidity often cause the contributions of some parasitic effects to vary from day to day.

In general, PCB effects can be divided into two broad categories— those that most noticeably affect the static or dc operation of the circuit, and those that most noticeably affect dynamic or ac circuit operation.

Another very broad area of PCB design is the topic of grounding. Grounding is a problem area in itself for all analog designs, and it can be said that implementing a PCB based circuit doesn't change that fact. Fortunately, certain principles of quality grounding, namely the use of ground planes, are intrinsic to the PCB environment. This factor is one of the more significant advantages to PCB based analog designs, and appreciable discussion of this section is focused on this issue.

Some other aspects of grounding that must be managed include the control of spurious ground and signal return voltages that can degrade performance. These voltages can be due to external signal coupling, common currents, or simply excessive IR drops in ground conductors. Proper conductor routing and sizing, as well as differential signal handling and ground isolation techniques enables control of such parasitic voltages.

One final area of grounding to be discussed is grounding appropriate for a mixed-signal, analog/digital environment. Although this isn't the specific overall focus of the book, it is certainly true that interfacing with ADCs (or DACs) is a major task category of op amps, and thus it shouldn't be overlooked. Indeed, the single issue of quality grounding can drive the entire layout philosophy of a high performance mixed signal PCB design— as it well should.

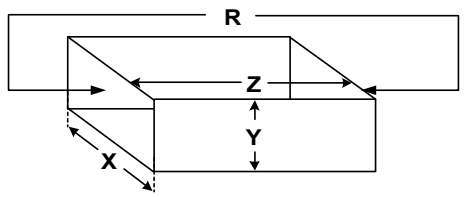
Resistance of Conductors

Every engineer is familiar with resistors— little cylinders with wire or tab ends— although perhaps fewer are aware of their idiosyncrasies, as generally covered in section 7-1. But far too few engineers consider that all the wires and PCB traces with which their systems and circuits are assembled are also resistors. In higher precision systems, even these trace resistances and simple wire interconnections can have degrading effects. Copper is *not* a superconductor— and too many engineers appear to think it is!

Figure 7-16 illustrates a method of calculating the sheet resistance R of a copper square, given the length Z, the width X, and the thickness Y.

$$R = \frac{\rho Z}{XY}$$

ρ = RESISTIVITY



SHEET RESISTANCE CALCULATION FOR
1 OZ. COPPER CONDUCTOR:

ρ = 1.724 X 10-6 Ωcm, Y = 0.0036cm

$$R = 0.48 \frac{Z}{X} m\Omega$$

$\frac{Z}{X}$ = NUMBER OF SQUARES

R = SHEET RESISTANCE OF 1 SQUARE (Z=X)
= 0.48mΩ/SQUARE

Figure 7-16: *Calculation of sheet resistance and linear resistance for standard copper PCB conductors*

At 25°C the resistivity of pure copper is 1.724E-6 ohm cm. The thickness of standard 1 ounce PCB copper foil is 0.036mm (0.0014"). Using the relations shown, the resistance of such a standard copper element is therefore 0.48mΩ /square. One can readily calculate the resistance of a linear trace, by effectively "stacking" a series of such squares end-end, to make up the line's length. The line length is Z and the width is X, so the line resistance R is simply a product of Z/X and the resistance of a single square, as noted in the figure.

For a given copper weight and trace width, a resistance/length calculation can be made. For example, the 0.25mm (10 mil) wide traces frequently used in PCB designs equates to a resistance/length of about 19mΩ/cm (48mΩ /inch), which is quite large. Moreover, the temperature coefficient of resistance for copper is about 0.4% /°C around room temperature. This is a factor that shouldn't be ignored, in particular within low impedance precision circuits, where the TC can shift the net impedance over temperature.

As shown in Figure 7-17, PCB trace resistance can be a serious error when conditions aren't favorable. Consider a 16-bit ADC with a 5kΩ input resistance, driven through 5cm of 0.25mm wide 1 oz. PCB track between it and its signal source. The track resistance of nearly 0.1Ω forms a divider with the 5kΩ load, creating an error. The resulting voltage drop is a gain error of 0.1/5k (~0.0019%), well over 1LSB (0.0015% for 16 bits).

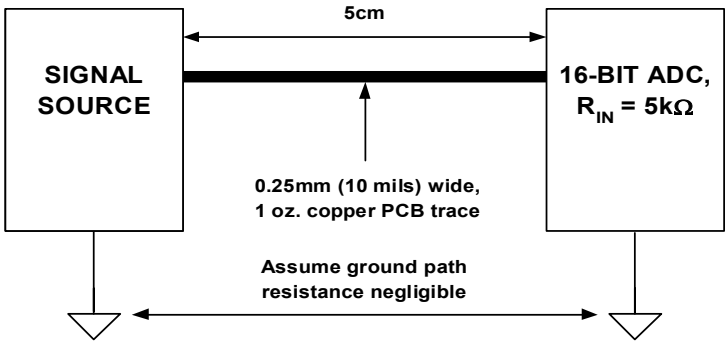


Figure 7-17: *Ohm's law predicts >1LSB of error due to drop in PCB conductor*

So, when dealing with precision circuits, the point is made that even simple design items such as PCB trace resistance cannot be dealt with casually. There are various solutions that can address this issue, such as wider traces (which may take up excessive space), the use of heavier copper (which may be too expensive), or simply choosing a high impedance converter. But, the most important thing is to think it all through, avoiding any tendency to overlook items appearing innocuous on the surface.

Voltage Drop in Signal Leads - "Kelvin" Feedback

The gain error resulting from resistive voltage drop in PCB signal leads is important only with high precision and/or at high resolutions (the Figure 7-17 example), or where large signal currents flow. Where load impedance is constant and resistive, adjusting overall system gain can compensate for the error. In other circumstances, it may often be removed by the use of "Kelvin" or "voltage sensing" feedback, as shown in Figure 7-18.

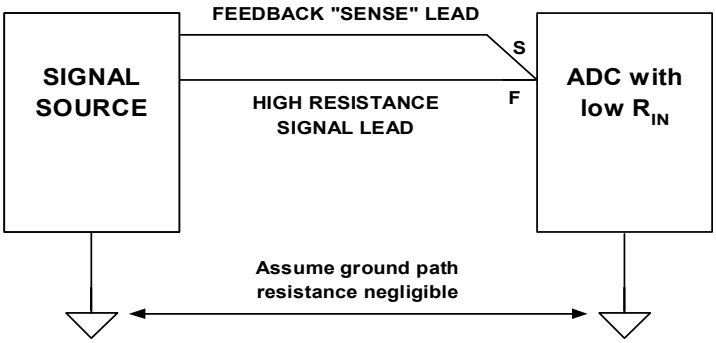


Figure 7-18: *Use of a sense connection moves accuracy to the load point*

In this modification to the case of Figure 7-17, a long resistive PCB trace is still used to drive the input of a high resolution ADC, with low input impedance. In this case however, the voltage drop in the signal lead does *not* give rise to an error, as feedback is taken directly from the input pin of the ADC, and returned to the driving source. This

scheme allows full accuracy to be achieved in the signal presented to the ADC, despite any voltage drop across the signal trace.

The use of separate force (F) and sense (S) connections at the load removes any errors resulting from voltage drops in the force lead, but, of course, may only be used in systems where there is negative feedback. It is also impossible to use such an arrangement to drive two or more loads with equal accuracy, since feedback may only be taken from one point. Also, in this much-simplified system, errors in the common lead source/load path are ignored, the assumption being that ground path voltages are negligible. In many systems this may not necessarily be the case, and additional steps may be needed, as noted below.

Signal Return Currents

Kirchoff's Law tells us that at any point in a circuit the algebraic sum of the currents is zero. This tells us that all currents flow in circles and, particularly, that the return current must always be considered when analyzing a circuit, as is illustrated in Figure 7-19 (see References 7 and 8).

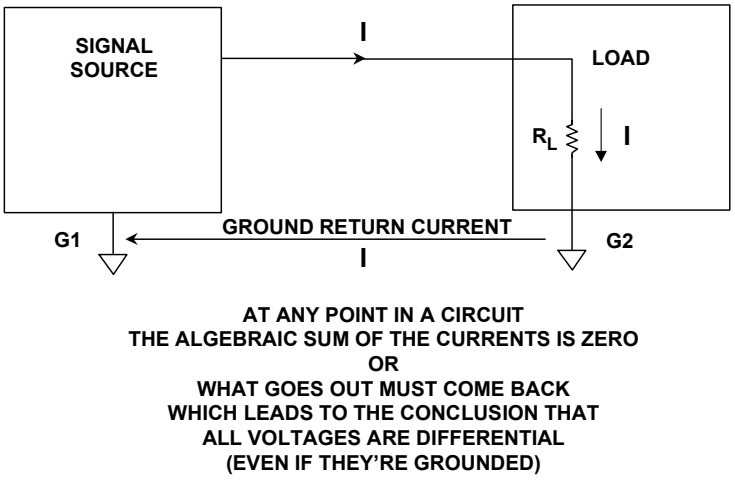


Figure 7-19: *Kirchoff's law helps in analyzing voltage drops around a complete source/load coupled circuit*

In dealing with grounding issues, common human tendencies provide some insight into how the correct thinking about the circuit can be helpful towards analysis. Most engineers readily consider the ground return current "I", *when they are considering a fully differential circuit*.

However, when considering the more usual circuit case, where a single-ended signal is referred to "ground", it is common to assume that all the points on the circuit diagram where ground symbols are found are at the same potential. Unfortunately, this happy circumstance just ain't necessarily so!

This overly optimistic approach is illustrated in Figure 7-20, where, if it really should exist, "infinite ground conductivity" would lead to zero ground voltage difference between source ground G1 and load ground G2. Unfortunately this approach isn't a wise practice, and when dealing with high precision circuits, it can lead to disasters.

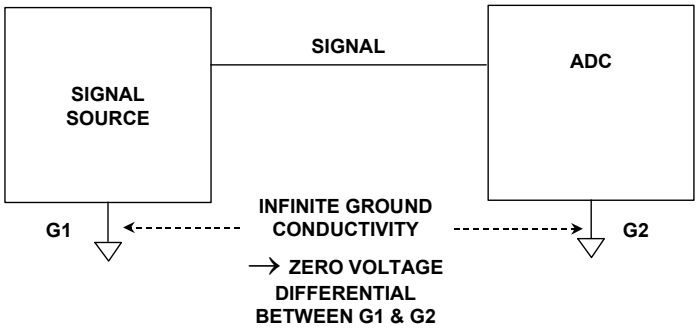


Figure 7-20: *Unlike this optimistic diagram, it is unrealistic to assume infinite conductivity between source/load grounds in a real-world system*

A more realistic approach to ground conductor integrity includes analysis of the impedance(s) involved, and careful attention to minimizing spurious noise voltages.

Ground Noise & Ground Loops

A more realistic model of a ground system is shown in Figure 7-21. The signal return current flows in the complex impedance existing between ground points G1 and G2 as shown, giving rise to a voltage drop ΔV in this path. But it is important to note that additional *external* currents, such as I_{EXT}, may also flow in this same path. It is critical to understand that such currents may generate uncorrelated noise voltages between G1 and G2 (dependent upon the current magnitude and relative ground impedance).

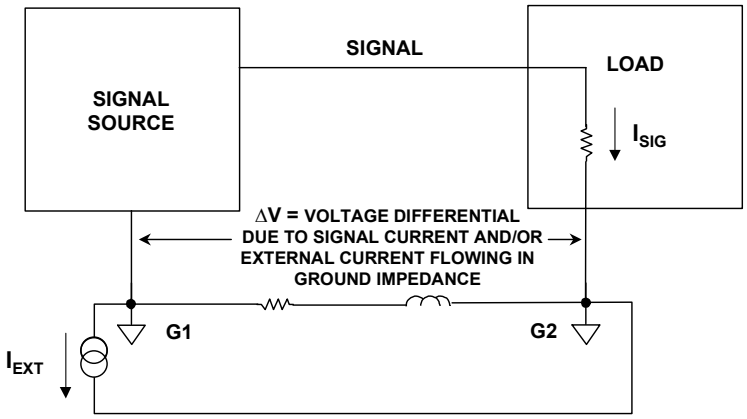


Figure 7-21: *A more realistic source-to-load grounding system view includes consideration of the impedance between G1-G2, plus the effect of any non-signal-related currents*

Some portion of these undesired voltages may end up being seen at the signal's load end, and they can have the potential to corrupt the signal being transmitted.

It is evident, of course, that other currents can only flow in the ground impedance, if there is a current path for them. In this case, severe problems can be caused by a high current circuit sharing an *unlooped* ground return with the signal source.

Figure 7-22 shows just such a common ground path, shared by the signal source and a high current circuit, which draws a large and varying current from its supply. This current flows in the common ground return, causing an error voltage ΔV to be developed.

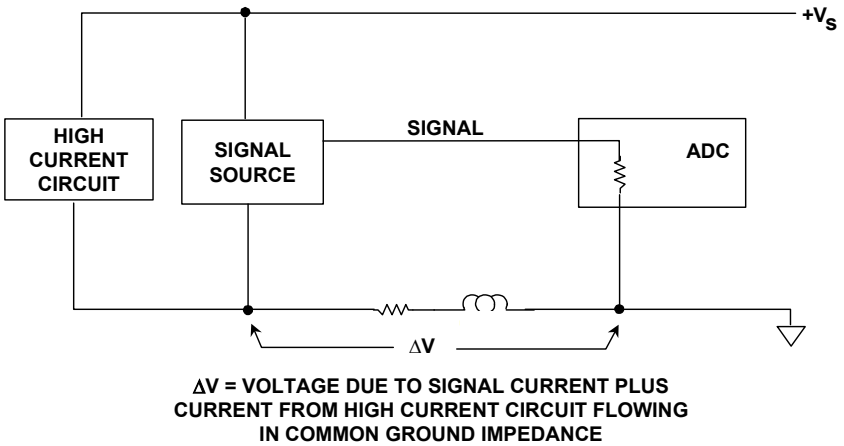


Figure 7-22: *Any current flowing through a common ground impedance can cause errors*

From Figure 7-23 below, it is also evident that if a ground network contains *loops,* or circular ground conductor patterns (with S1 closed), there is an even greater danger of it being vulnerable to EMFs induced by external magnetic fields. There is also a real danger of ground-current-related signals "escaping" from the high current areas, and causing noise in sensitive circuit regions elsewhere in the system.

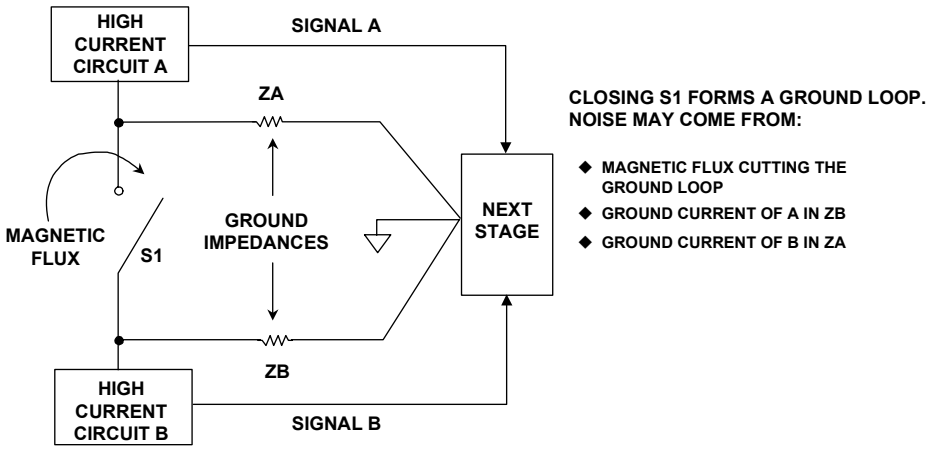


Figure 7-23: *A ground loop*

For these reasons ground loops are best avoided, by wiring all return paths within the circuit by separate paths back to a common point, i.e., the common ground point towards the mid-right of the diagram. This would be represented by the S1 open condition.

There are a number of possible ways of attacking the ground noise problem, apart from the presently impracticable one of using superconducting grounds. It is rare for any single method to be used to the exclusion of all others, and real systems generally contain a mixture. For descriptive purposes each approach is addressed separately.

Star Grounds

The "star" ground philosophy builds on the theory that there is one single ground point in a circuit to which all voltages are referred. This is known as the *star ground* point. It can be better understood by a visual analogy— the multiple conductors extending radially from the common schematic ground resemble a star. This can be appreciated by regarding Figure 7-23 again, considering many more ground returns from the common point. Note that the star point need not look like a star— it may be a point on a ground plane— but the key feature of the star ground system is that all voltages are measured with respect to a particular point in the ground network, not just to an undefined "ground" (i.e. wherever one can clip a probe). Figure 7-24 succinctly summarizes the philosophy.

- **IF ALL SIGNAL VOLTAGES WITHIN A SYSTEM ARE MEASURED WITH RESPECT TO A SINGLE POINT, THAT POINT IS SAID TO BE THE SYSTEM *STAR GROUND*.**

Figure 7-24: *The star ground concept*

This star grounding philosophy is reasonable theoretically, but can encounter practical difficulties. For example, if we design a star ground system, drawing out all signal paths to minimize signal interaction and the effects of high impedance signal or ground paths, we often find implementation problems. When the power supplies are added to the circuit diagram, they either add unwanted ground paths, or their supply currents flowing in the existing ground paths are sufficiently so large, or noisy (or both) so as to corrupt the signal transmission. This particular problem can often be avoided by having separate power supplies (and thus separate ground returns) for the various circuit portions. For example, separate analog and digital supplies with separate analog and digital grounds, joined at the star point, are common in mixed signal applications.

Separate Analog and Digital Grounds

As a fact of life, digital circuitry is noisy. Saturating logic draws large, fast current spikes from its supply during switching. However, logic stages, with hundreds of millivolts (or more) of noise immunity, usually have little need for high levels of supply decoupling. On the other hand, analog circuitry is quite vulnerable to noise on both power supply rails and grounds. So, it is very sensible to separate analog and digital circuitry, to prevent digital noise from corrupting analog performance. Such separation involves separation of both ground returns *and* power rails, which is inconvenient in a mixed signal system. Nevertheless, if a mixed signal system is to deliver full performance capability, it is often essential to have separate analog and digital grounds, and separate power supplies. The fact that some analog circuitry will "operate" (i.e., function) from a single +5V supply does *not* mean that it may safely be operated from the same noisy +5V supply as the microprocessor and dynamic RAM, the electric fan, and the solenoid jackhammer! What is required is that the analog portion *operate with full performance from such a low*

voltage supply, not just be functional. This distinction will by necessity require quite careful attention to both the supply rails and the ground interfacing.

Figures 7-25 and 7-26 summarize some analog and digital power supply and grounding concepts which are useful to bear in mind as systems are designed.

- **DIGITAL CIRCUITRY IS *NOISY***
- **ANALOG CIRCUITRY IS *QUIET***
- **CIRCUIT NOISE FROM DIGITAL CIRCUITRY CARRIED BY POWER AND GROUND LEADS CAN CORRUPT PRECISION ANALOG CIRCUITRY**
- **IT IS ADVISABLE TO SEPARATE THE POWER AND GROUND OF THE DIGITAL AND ANALOG PARTS OF A SYSTEM**
- **ANALOG AND DIGITAL GROUNDS MUST BE JOINED AT *ONE* POINT**

Figure 7-25: *Some power supply and ground noise concepts appropriate for mixed signal systems*

Note that, analog and digital ground in a system must be joined at some point, to allow signals to be referred to a common potential. This star point, or analog/digital common point, is chosen so that it does not introduce digital currents into the ground of the analog part of the system— it is often convenient to make the connection at the power supplies.

Note also that many ADCs and DACs have separate *analog ground* (AGND) and *digital ground* (DGND) pins. On the device data sheets, users are often advised to connect these pins together at the package. This seems to conflict with the advice to connect analog and digital ground at the power supplies, and, in systems with more than one converter, with the advice to join the analog and digital ground at a single point.

- **MONOLITHIC AND HYBRID ADCS FREQUENTLY HAVE SEPARATE *AGND* AND *DGND* PINS, WHICH MUST BE JOINED TOGETHER AT THE DEVICE.**
- **THIS ISN'T DONE TO BE DIFFICULT, BUT BECAUSE BONDWIRE VOLTAGE DROPS ARE TOO LARGE TO ALLOW INTERNAL CONNECTION.**
- **THE BEST SOLUTION TO THE GROUNDING PROBLEM ARISING FROM THIS REQUIREMENT IS TO CONNECT BOTH PINS TO SYSTEM "ANALOG GROUND."**
- **IT IS LIKELY THAT NEITHER THE DIGITAL NOISE SO INTRODUCED IN THE SYSTEM *AGND*, NOR THE SLIGHT LOSS OF DIGITAL NOISE IMMUNITY WILL SERIOUSLY AFFECT THE SYSTEM PERFORMANCE.**

Figure 7-26: *Treatment of analog and digital grounds with data converters of mixed signal systems*

There is, in fact, no conflict. The labels "analog ground" and "digital ground" on these pins refer to the parts of the converter to which the pins are connected, and not to the system grounds to which they must go. For example, with an ADC, generally these two pins should be joined together and to the *analog* ground of the system. It is not possible to join the two pins within the IC package, because the analog part of the converter

cannot tolerate the voltage drop resulting from the digital current flowing in the bond wire to the chip. But they can be so tied, *externally*.

Figure 7-27 illustrates this concept of ground connections for an ADC. If these pins are connected in this way, the digital noise immunity of the converter is diminished somewhat, by the amount of common-mode noise between the digital and analog system grounds. However, since digital noise immunity is of the order of hundreds or thousands of millivolts, this factor is unlikely to be important.

The analog noise immunity is diminished only by the external digital currents of the converter itself flowing in the analog ground. These currents should be kept quite small, and this can be minimized by ensuring that the converter outputs don't see heavy loads. A good solution towards this is to use a low input current buffer at the ADC output, such as a CMOS buffer-register IC.

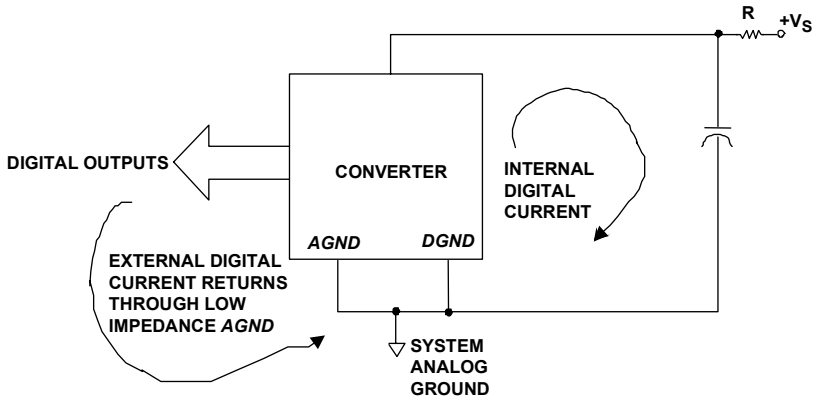


Figure 7-27: *Analog (AGND) and digital ground (DGND) pins of a data converter should be returned to system* analog *ground*

If the logic supply to the converter is isolated with a small resistance and decoupled to analog ground with a local 0.1µF capacitor, all the fast-edge digital currents of the converter will return to ground through the capacitor, and will not appear in the external ground circuit. If the analog ground impedance is maintained low, as it should be for adequate analog performance, additional noise due to the external digital ground current should rarely present a problem.

Ground planes

Related to the star ground system discussed earlier is the use of a *ground plane*. To implement a ground plane, one side of a double-sided PCB (or one layer of a multi-layer one) is made of continuous copper and used as ground. The theory behind this is that the large amount of metal will have as low a resistance as is possible. It will, because of the large flattened conductor pattern, also have as low an inductance as possible. It then offers the best possible conduction, in terms of minimizing spurious ground difference voltages across the conducting plane.

Note that ground plane concept can also be extended to include *voltage planes.* A voltage plane offers advantages similar to a ground plane, i.e., a very low impedance conductor, but is dedicated to a one (or more) of the system supply voltages. Thus a system can have more than one voltage plane, as well as a ground plane.

It has been sometimes argued that ground planes shouldn't be used, as they are liable to introduce manufacture and assembly problems. Such an argument may have had limited validity some years ago when PCB adhesives were less well developed, wave-soldering less reliable, and solder resist techniques less well understood, but not today.

A summary of key points related to the construction and operation of ground planes is contained in Figure 7-28.

- ONE ENTIRE PCB SIDE (OR LAYER) IS A CONTINUOUS GROUNDED CONDUCTOR.
- THIS GIVES MINIMUM GROUND RESISTANCE AND INDUCTANCE, BUT ISN'T ALWAYS SUFFICIENT TO SOLVE ALL GROUNDING PROBLEMS.
- BREAKS IN GROUND PLANES CAN IMPROVE OR DEGRADE CIRCUIT PERFORMANCE — THERE IS NO GENERAL RULE.
- YEARS AGO GROUND PLANES WERE DIFFICULT TO FABRICATE. TODAY THEY AREN'T.
- MULTI-LAYER, GROUND AND VOLTAGE PLANE PCB DESIGNS ARE STANDARD

Figure 7-28: *Characteristics of ground planes*

While ground planes solve many ground impedance problems, it should still be understood they aren't a panacea. Even a continuous sheet of copper foil has residual resistance and inductance, and in some circumstances, these can be enough to prevent proper circuit function. Designers should be wary of injecting very high currents in a ground plane, as they can produce voltage drops that interfere with sensitive circuitry.

Skin Effect

At high frequencies, also consider *skin effect*, where inductive effects cause currents to flow only in the outer surface of conductors. Note that this is in contrast to the earlier discussions of this section on dc resistance of conductors.

The skin effect has the consequence of increasing the resistance of a conductor at high frequencies. Note also that this effect is separate from the increase in impedance due to the effects of the self-inductance of conductors as frequency is increased.

Skin effect is quite a complex phenomenon, and detailed calculations are beyond the scope of this discussion. However, a good approximation for copper is that the skin depth in centimeters is $6.61/\sqrt{f}$, (f in Hz).

A summary of the skin effect within a typical PCB conductor foil is shown in Figure 7-29. Note that this copper conductor cross-sectional view assumes looking into the *side* of the conducting trace.

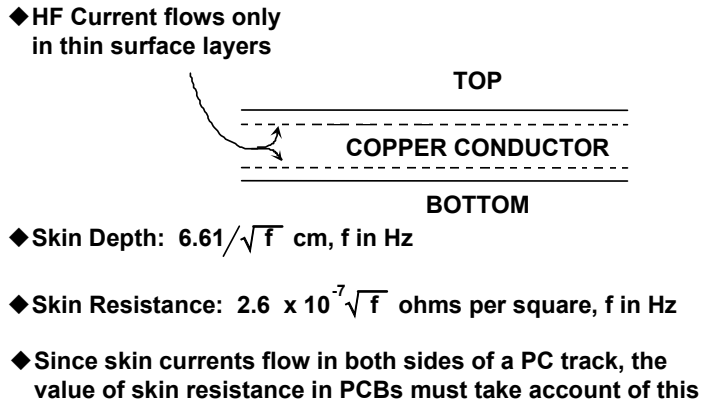


Figure 7-29: *Skin depth in a PC conductor*

Assuming that skin effects become important when the skin depth is less than 50% of the thickness of the conductor, this tells us that for a typical PC foil, we must be concerned about skin effects at frequencies above approximately 12MHz.

Where skin effect is important, the resistance for copper is $2.6 \times 10^{-7} \sqrt{f}$ Ohms per square, (f in Hz). This formula is invalid if the skin thickness is greater than the conductor thickness (i.e. at DC or LF).

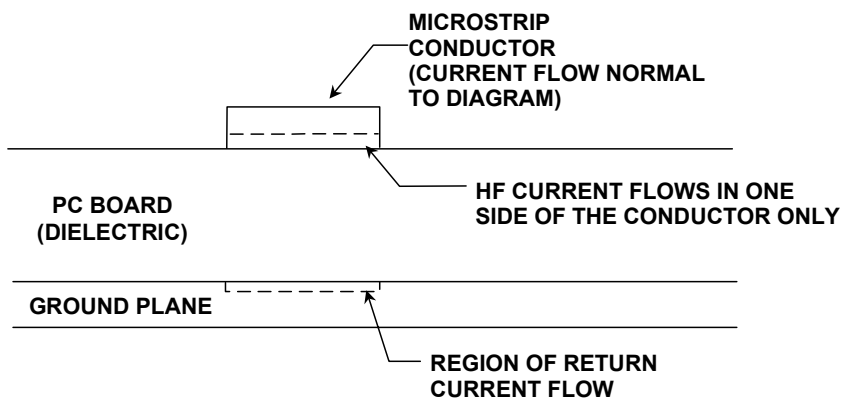


Figure 7-30: *Skin effect with PC conductor and ground plane*

Figure 7-30 illustrates a case of a PCB conductor with current flow, as separated from the ground plane underneath.

In this diagram, note the (dotted) regions of HF current flow, as reduced by the skin effect. When calculating skin effect in PCBs, it is important to remember that current generally flows in both sides of the PC foil (this is not necessarily the case in microstrip lines, see below), so the resistance per square of PC foil may be half the above value.

Transmission Lines

We earlier considered the benefits of outward and return signal paths being close together so that inductance is minimized. As shown previously in Figure 7-30, when an HF signal flows in a PC track running over a ground plane, the arrangement functions as a *microstrip* transmission line, and the majority of the return current flows in the ground plane underneath the line.

Figure 7-31 shows the general parameters for a microstrip transmission line, given the conductor width, w, dielectric thickness, h, and the dielectric constant, E_r.

The characteristic impedance of such a microstrip line will depend upon the width of the track and the thickness and dielectric constant of the PCB material. Designs of microstrip lines are covered in more detail within section six of this chapter.

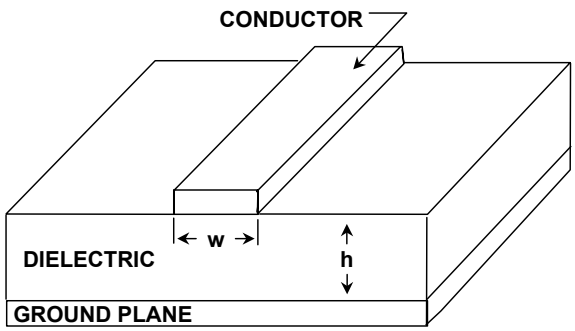


Figure 7-31: *A PCB microstrip transmission line is an example of a controlled impedance conductor pair*

For most dc and lower frequency applications, the characteristic impedance of PCB traces will be relatively unimportant. Even at frequencies where a track over a ground plane behaves as a transmission line, it is not necessary to worry about its characteristic impedance or proper termination if the free space wavelengths of the frequencies of interest are greater than ten times the length of the line.

However, at VHF and higher frequencies it is possible to use PCB tracks as microstrip lines within properly terminated transmission systems. Typically the microstrip will be designed to match standard coaxial cable impedances, such as 50, 75 or 100Ω, simplifying interfacing.

Note that if losses in such systems are to be minimized, the PCB material must be chosen for low high frequency losses. This usually means the use of Teflon or some other comparably low-loss PCB material. Often, though, the losses in short lines on cheap glass-fibre board are small enough to be quite acceptable.

Be Careful With Ground Plane Breaks

Wherever there is a break in the ground plane beneath a conductor, the ground plane return current must by necessity flow *around* the break. As a result, both the inductance and the vulnerability of the circuit to external fields are increased. This situation is diagrammed in Figure 7-32, where conductors A and B must cross one another.

Where such a break is made to allow a crossover of two perpendicular conductors, it would be far better if the second signal were carried across both the first and the ground plane by means of a piece of wire. The ground plane then acts as a shield between the two signal conductors, and the two ground return currents, flowing in opposite sides of the ground plane as a result of skin effects, do not interact.

With a multi-layer board, both the crossover and the continuous ground plane can be accommodated without the need for a wire link. Multi-layer PCBs are expensive and harder to trouble-shoot than more simple double-sided boards, but do offer even better shielding and signal routing. The principles involved remain unchanged but the range of layout options is increased.

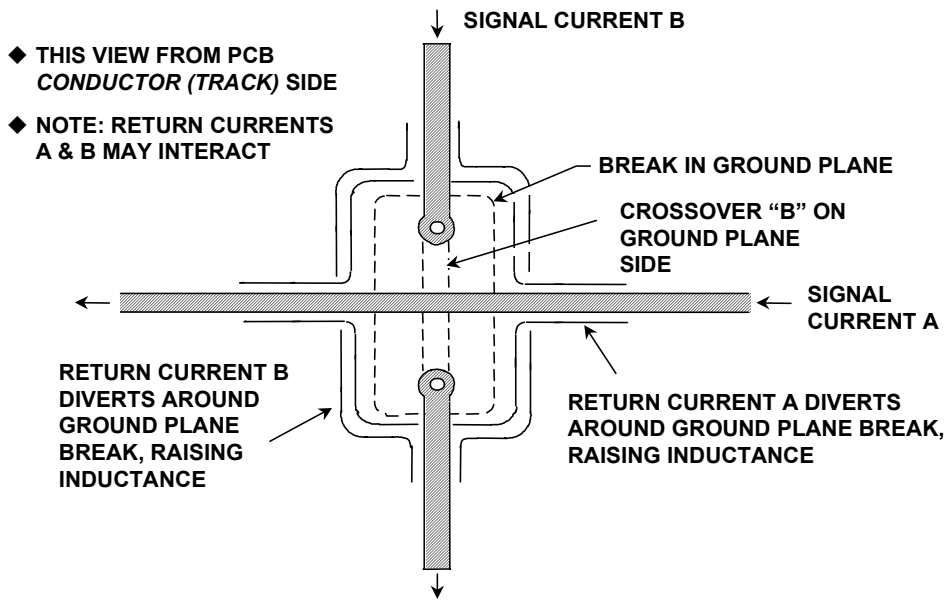


Figure 7-32: *A ground plane break raises circuit inductance, and increases vulnerability to external fields*

The use of double-sided or multi-layer PCBs with at least one continuous ground plane is undoubtedly one of the most successful design approaches for high performance mixed signal circuitry. Often the impedance of such a ground plane is sufficiently low to permit the use of a single ground plane for both analog and digital parts of the system. However, whether or not this is possible does depend upon the resolution and bandwidth required, and the amount of digital noise present in the system.

Ground Isolation Techniques

While the use of ground planes does lower impedance and helps greatly in lowering ground noise, there may still be situations where a prohibitive level of noise exists. In such cases, the use of ground error minimization and isolation techniques can be helpful.

Another illustration of a common-ground impedance coupling problem is shown in Figure 7-33. In this circuit a precision gain-of-100 preamp amplifies a low-level signal V_{IN}, using an AD8551 chopper-stabilized amplifier for best dc accuracy. At the load end, the signal V_{OUT} is measured with respect to G2, the local ground. Because of the small 700µA I_{SUPPLY} of the AD8551 flowing between G1 and G2, there is a 7µV ground error— about 7 times the typical input offset expected from the op amp!

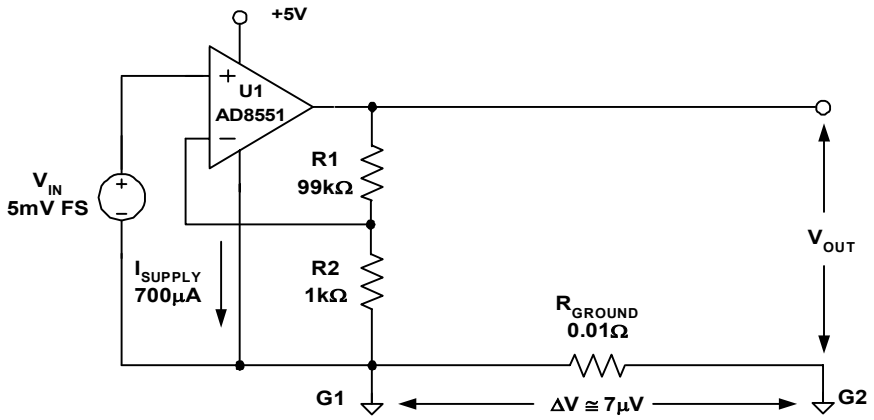


Figure 7-33: *Unless care is taken, even small common ground currents can degrade precision amplifier accuracy*

This error can be avoided simply by routing the negative supply pin current of the op amp back to star ground G2 as opposed to ground G1, by using a separate trace. This step eliminates the G1-G2 path power supply current, and so minimizes the ground leg voltage error. Note that there will be little error developed in the "hot" V_{OUT} lead, so long as the current drain at the load end is small.

In some cases, there may be simply unavoidable ground voltage differences between a source signal and the load point where it is to be measured. Within the context of this "same-board" discussion, this might require rejecting ground error voltages of several tens-of-mV. Or, should the source signal originate from an "off-board" source, then the magnitude of the common-mode voltages to be rejected can easily rise into a several volt range (or even tens-of-volts).

Fortunately, full signal transmission accuracy can still be accomplished in the face of such high noise voltages, by employing a principle discussed earlier. This is the use of a differential-input, *ground isolation* amplifier. The ground isolation amplifier minimizes the effect of ground error voltages between stages by processing the signal in differential fashion, thereby rejecting CM voltages by a substantial margin (typically 60dB or more).

Two ground isolation amplifier solutions are shown in Figure 7-34. This diagram can alternately employ either the AD629 to handle CM voltages up to ±270V, or the AMP03, which is suitable for CM voltages up to ±20V.

In the circuit, input voltage V_{IN} is referred to G1, but must be measured with respect to G2. With the use of a high CMR unity-gain difference amplifier, the noise voltage ΔV existing between these two grounds is easily rejected. The AD629 offers a typical CMR of 88dB, while the AMP03 typically achieves 100dB. In the AD629, the high CMV rating is done by a combination of high CM attenuation, followed by differential gain, realizing a net differential gain of unity. The AD629 uses the first listed value resistors noted in the figure for R1-R5. The AMP03 operates as a precision four-resistor differential amplifier, using the 25kΩ value R1-R4 resistors noted. Both devices are complete, one package solutions to the ground-isolation amplifier.

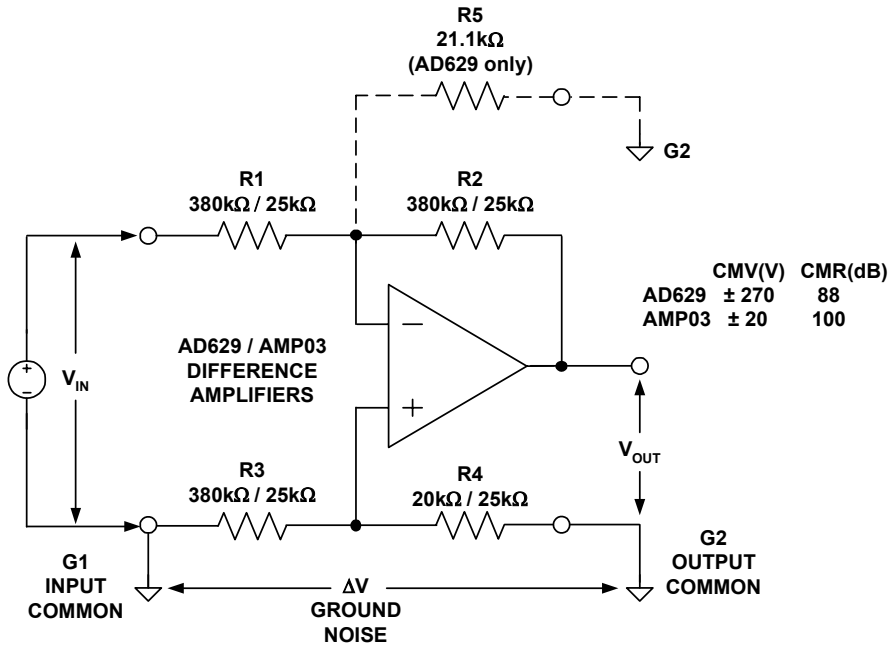


Figure 7-34: *A differential input ground isolating amplifier allows high transmission accuracy by rejecting ground noise voltage between source (G1) and measurement (G2) grounds*

This scheme allows relative freedom from tightly controlling ground drop voltages, or running additional and/or larger PCB traces to minimize such error voltages. Note that it can be implemented either with the fixed gain difference amplifiers shown, or also with a standard in-amp IC, configured for unity gain. The AD623, for example, also allows single-supply use. In any case, signal polarity is also controllable, by simple reversal of the difference amplifier inputs.

In general terms, transmitting a signal from one point on a PCB to another for measurement or further processing can be optimized by two key interrelated techniques. These are the use of high-impedance, differential signal-handling techniques. The high impedance loading of an in-amp minimizes voltage drops, and differential sensing of the remote voltage minimizes sensitivity to ground noise.

When the further signal processing is A/D conversion, these transmission criteria can be implemented *without* adding a differential ground isolation amplifier stage. Simply select an ADC which operates differentially. The high input impedance of the ADC minimizes load sensitivity to the PCB wiring resistance. In addition, the differential input feature allows the output of the source to be sensed directly at the source output terminals (even if single-ended). The CMR of the ADC then eliminates sensitivity to noise voltages between the ADC and source grounds.

An illustration of this concept using an ADC with high impedance differential inputs is shown in Figure 7-35. Note that the general concept can be extended to virtually any signal source, driving any load. All loads, even single-ended ones, become differential-input by adding an appropriate differential input stage.

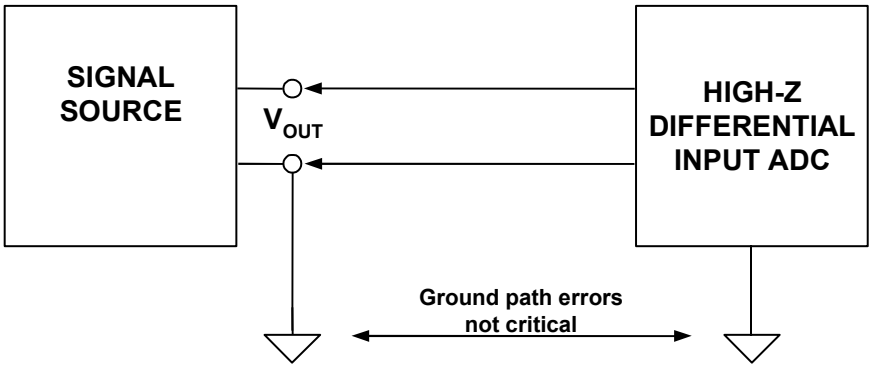


Figure 7-35: *A high-impedance differential input ADC also allows high transmission accuracy between source and load*

The differential input can be provided by either a fully developed high-Z in-amp, or in many cases it can be a simple subtractor stage op amp, such as Figure 7-34.

Static PCB Effects

Leakage resistance is the dominant static circuit board effect. Contamination of the PCB surface by flux residues, deposited salts, and other debris can create leakage paths between circuit nodes. Even on well-cleaned boards, it is not unusual to find 10 nA or more of leakage to nearby nodes from 15-volt supply rails. Nanoamperes of leakage current into the wrong nodes often cause volts of error at a circuit's output; for example, 10 nA into a 10 megohm resistance causes 0.1 V of error. Unfortunately, the standard op amp pinout places the $-V_S$ supply pin next to the + input, which is often hoped to be at high impedance! To help identify nodes sensitive to the effects of leakage currents ask the simple question: If a spurious current of a few nanoamperes or more were injected into this node, would it matter?

If the circuit is already built, you can localize moisture sensitivity to a suspect node with a classic test. While observing circuit operation, blow on potential trouble spots through a simple soda straw. The straw focuses the breath's moisture, which, with the board's salt content in susceptible portions of the design, disrupts circuit operation upon contact.

There are several means of eliminating simple surface leakage problems. Thorough washing of circuit boards to remove residues helps considerably. A simple procedure includes vigorously brushing the boards with isopropyl alcohol, followed by thorough washing with deionized water and an 85°C bakeout for a few hours. Be careful when selecting board-washing solvents, though. When cleaned with certain solvents, some water-soluble fluxes create salt deposits, exacerbating the leakage problem.

Unfortunately, if a circuit displays sensitivity to leakage, even the most rigorous cleaning can offer only a temporary solution. Problems soon return upon handling, or exposure to foul atmospheres, and high humidity. Some additional means must be sought to stabilize circuit behavior, such as conformal surface coating.

Fortunately, there is an answer to this, namely *guarding*, which offers a fairly reliable and permanent solution to the problem of surface leakage. Well-designed guards can eliminate leakage problems, even for circuits exposed to harsh industrial environments. Two schematics illustrate the basic guarding principle, as applied to typical inverting and non-inverting op amp circuits.

Figure 7-36 illustrates an inverting mode guard application. In this case, the op amp reference input is grounded, so the guard is a grounded ring surrounding all leads to the inverting input, as noted by the dotted line.

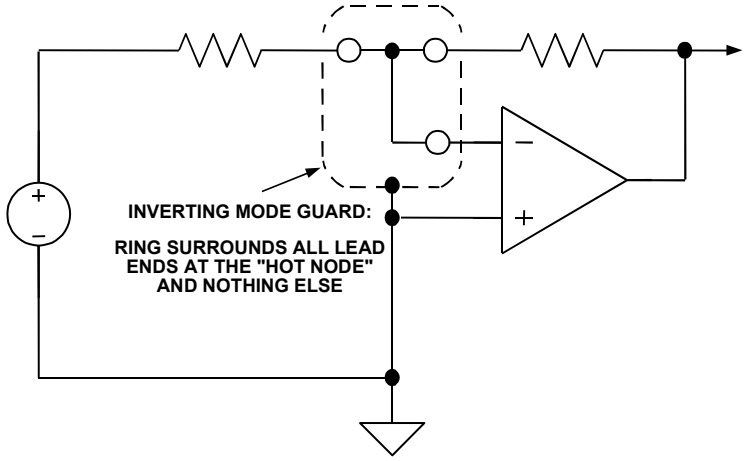


Figure 7-36: *Inverting mode guard encloses all op amp inverting input connections within a grounded guard ring*

Guarding basic principles are simple: *Completely* surround sensitive nodes with conductors that can readily sink stray currents, and maintain the guard conductors at the exact potential of the sensitive node (as otherwise the guard will serve as a leakage source rather than a leakage sink). For example, to keep leakage into a node below 1 pA (assuming 1000-megohm leakage resistance) the guard and guarded node must be within 1 mV. Generally, the low offset of a modern op amp is sufficient to meet this criterion.

There are important caveats to be noted with implementing a true high-quality guard. For traditional through-hole PCB connections, the guard pattern should appear on *both* sides of the circuit board, to be most effective. And, it should also be connected along its length by several vias. Finally, when either justified or required by the system design

parameters, do make an effort to include guards in the PCB design process from the outset— there is little likelihood that a proper guard can be added as an afterthought.

Figure 7-37 illustrates the case for a non-inverting guard. In this instance the op amp reference input is directly driven by the source, which complicates matters considerably. Again, the guard ring completely surrounds all of the input nodal connections. In this instance however, the guard is driven from the low impedance feedback divider connected to the inverting input.

Usually the guard-to-divider junction will be a direct connection, but in some cases a unity gain buffer might be used at "X" to drive a cable shield, or also to maintain the lowest possible impedance at the guard ring.

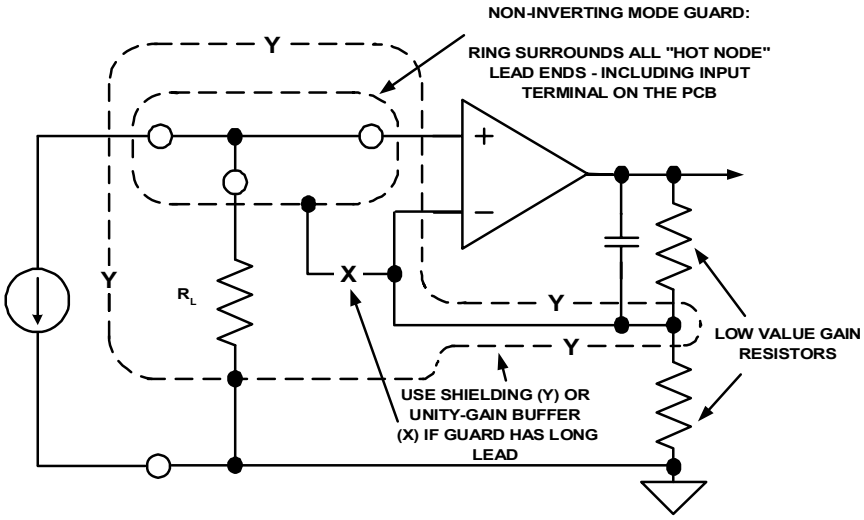


Figure 7-37: *Non-inverting mode guard encloses all op amp non-inverting input connections within a low impedance, driven guard ring*

In lieu of the buffer, another useful step is to use an additional, directly grounded screen ring, "Y", which surrounds the inner guard and the feedback nodes as shown. This step costs nothing except some added layout time, and will greatly help buffer leakage effects into the higher impedance inner guard ring.

Of course what hasn't been addressed to this point is just how the op amp itself gets connected into these guarded islands without compromising performance. The traditional method using a TO-99 metal can package device was to employ double-sided PCB guard rings, with both op amp inputs terminated within the guarded ring.

The high impedance sensor discussions in Chapter 4 use the above-described method. The section immediately following illustrates how more modern IC packages can be mounted to PCB patterns, and take advantage of guarding and low-leakage operation.

Sample MINIDIP and SOIC op amp PCB guard layouts

Modern assembly practices have favored smaller plastic packages such as 8 pin MINIDIP and SOIC types. Some suggested partial layouts for guard circuits using these packages is shown in the next two figures. While guard traces may also be possible with even more tiny op amp footprints, such as SOT23 etc., the required trace separations become even more confining, challenging the layout designer as well as the manufacturing processes.

For the ADI "N" style MINIDIP package, Figure 7-38 illustrates how guarding can be accomplished for inverting (left) and non-inverting (right) operating modes. This setup would also be applicable to other op amp devices where relatively high voltages occur at pin 1 or 4. Using a standard 8 pin DIP outline, it can be noted that this package's 0.1" pin spacing allows a PC trace (here, the guard trace) to pass between adjacent pins. This is the key to implementing effective DIP package guarding, as it can adequately prevent a leakage path from the $-V_S$ supply at pin 4, or from similar high potentials at pin 1.

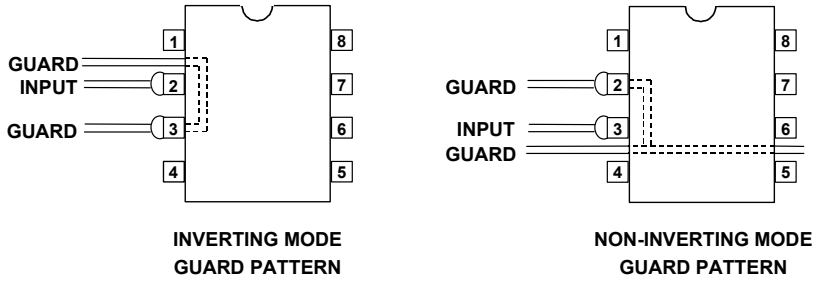


Figure 7-38: *PCB guard patterns for inverting and non-inverting mode op amps using 8 pin MINIDIP (N) package*

For the left-side inverting mode, note that the pin 3 connected and grounded guard traces surround the op amp inverting input (pin 2), and run parallel to the input trace. This guard would be continued out to and around the source and feedback connections of Figure 7-36 (or other similar circuit), including an input pad in the case of a cable. In the right-side non-inverting mode, the guard voltage is the feedback divider voltage to pin 2. This corresponds to the inverting input node of the amplifier, from Figure 7-37.

Note that in both of the cases of Figure 7-38, the guard physical connections shown are only partial— an actual layout would include all sensitive nodes within the circuit. In both the inverting and the non-inverting modes using the MINIDIP or other through-hole style package, the PCB guard traces should be located on both sides of the board, with top and bottom traces connected with several vias.

Things become slightly more complicated when using guarding techniques with the SOIC surface mount ("R") package, as the 0.05" pin spacing doesn't easily allow routing of PCB traces between the pins. But, there is still an effective guarding answer, at least for the inverting case. Figure 7-39 shows guards for the ADI "R" style SOIC package.

Note that for many single op amp devices in this SOIC "R" package, pins 1, 5, and 8 are "no connect" pins. For such instances, this means that these locations can be employed in the layout to route guard traces. In the case of the inverting mode (left), the guarding is still completely effective, with the dummy pin 1 and pin 3 serving as the grounded guard trace. This is a fully effective guard without compromise. Also, with SOIC op amps, much of the circuitry around the device will not use through-hole components. So, the guard ring may only be necessary on the op amp PCB side.

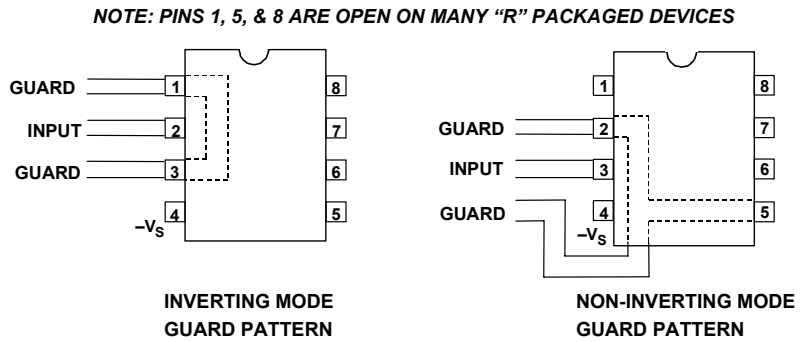


Figure 7-39: *PCB guard patterns for inverting and non-inverting mode op amps using 8 pin SOIC (R) package*

In the case of the follower stage (right), the guard trace must be routed around the negative supply at pin 4, and thus pin 4 to pin 3 leakage isn't fully guarded. For this reason, a precision high impedance follower stage using an SOIC package op amp isn't generally recommended, as guarding isn't possible for dual supply connected devices.

However, an exception to this caveat does apply to the use of a *single-supply* op amp as a non-inverting stage. For example, if the AD8551 is used, pin 4 becomes ground, and some degree of intrinsic guarding is then established by default.

Dynamic PCB Effects

Although static PCB effects can come and go with changes in humidity or board contamination, problems that most noticeably affect the dynamic performance of a circuit usually remain relatively constant. Short of a new design, washing or any other simple fixes can't fix them. As such, they can permanently and adversely affect a design's specifications and performance. The problems of stray capacitance, linked to lead and component placement, are reasonably well known to most circuit designers. Since lead placement can be permanently dealt with by correct layout, any remaining difficulty is solved by training assembly personnel to orient components or bend leads optimally.

Dielectric absorption (DA), on the other hand, represents a more troublesome and still poorly understood circuit-board phenomenon. Like DA in discrete capacitors, DA in a printed-circuit board can be modeled by a series resistor and capacitor connecting two closely spaced nodes. Its effect is inverse with spacing and linear with length.

As shown in Figure 7-40, the RC model for this effective capacitance ranges from 0.1 to 2.0 pF, with the resistance ranging from 50 to 500 MΩ. Values of 0.5 pF and 100 MΩ are most common. Consequently, circuit-board DA interacts most strongly with high-impedance circuits.

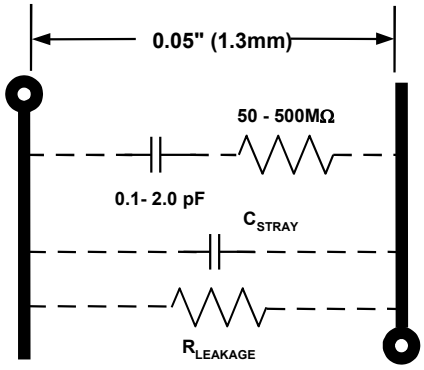


Figure 7-40: *DA plagues dynamic response of PCB-based circuits*

PCB DA most noticeably influences dynamic circuit response, for example, settling time. Unlike circuit leakage, the effects aren't usually linked to humidity or other environmental conditions, but rather, are a function of the board's dielectric properties. The chemistry involved in producing plated-through holes seems to exacerbate the problem. If your circuits don't meet expected transient response specs, you should consider PCB DA as a possible cause.

Fortunately, there are solutions. As in the case of capacitor DA, external components can be used to compensate for the effect. More importantly, surface guards that totally isolate sensitive nodes from parasitic coupling often eliminate the problem (note that these guards should be duplicated on both sides of the board, in cases of through-hole components). As noted previously, low-loss PCB dielectrics are also available.

PCB "hook", similar if not identical to DA, is characterized by variation in effective circuit-board capacitance with frequency (see Reference 1). In general, it affects high-impedance circuit transient response where board capacitance is an appreciable portion of the total in the circuit. Circuits operating at frequencies below 10 kHz are the most susceptible. As in circuit board DA, the board's chemical makeup very much influences its effects.

Stray Capacitance

When two conductors aren't short-circuited together, or totally screened from each other by a conducting (Faraday) screen, there is a capacitance between them. So, on any PCB, there will be a large number of capacitors associated with any circuit (which may or may not be considered in models of the circuit). Where high frequency performance matters (and even dc and VLF circuits may use devices with high Ft and therefore be vulnerable to HF instability), it is very important to consider the effects of this stray capacitance.

Any basic textbook will provide formulas for the capacitance of parallel wires and other geometric configurations (see References 9 and 10). The example we need consider in this discussion is the parallel plate capacitor, often formed by conductors on opposite sides of a PCB. The basic diagram describing this capacitance is shown in Figure 7-41.

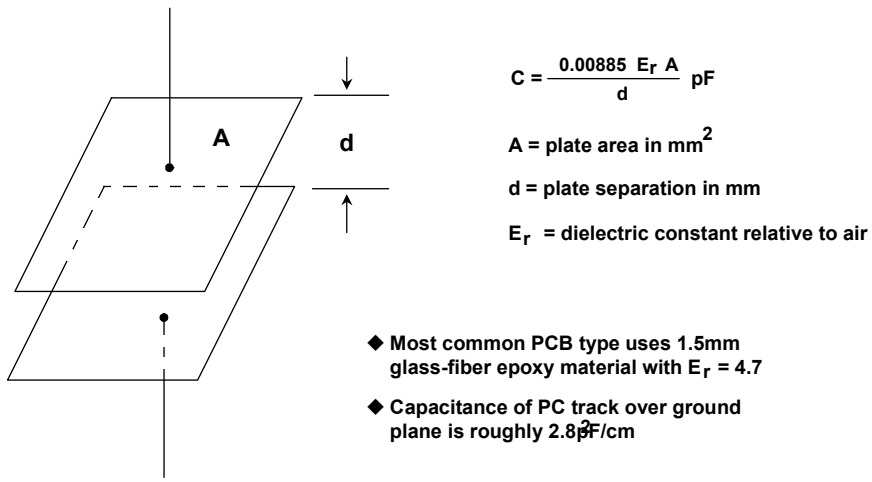


Figure 7-41: *Capacitance of two parallel plates*

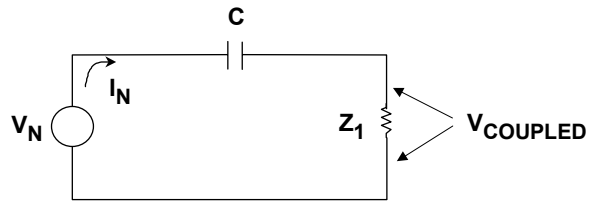
Neglecting edge effects, the capacitance of two parallel plates of area A mm^2 and separation d mm in a medium of dielectric constant E_r relative to air is $0.00885\ E_r A/d$ pF.

From this formula, we can calculate that for general purpose PCB material ($E_r = 4.7$, d = 1.5mm), the capacitance between conductors on opposite sides of the board is just under $3pF/cm^2$. In general, such capacitance will be parasitic, and circuits must be designed so that it does not affect their performance.

While it is possible to use PCB capacitance in place of small discrete capacitors, the dielectric properties of common PCB substrate materials cause such capacitors to behave poorly. They have a rather high temperature coefficient and poor Q at high frequencies, which makes them unsuitable for many applications. Boards made with lower-loss dielectrics such as Teflon are expensive exceptions to this rule.

Capacitive Noise & Faraday Shields

There is a capacitance between any two conductors separated by a dielectric (air or vacuum are dielectrics). If there is a change of voltage on one, there will be a movement of charge on the other. A basic model for this is shown in Figure 7-42.



Z_1 = CIRCUIT IMPEDANCE
Z2 = 1/jωC

$$V_{COUPLED} = V_N \left(\frac{Z_1}{Z_1 + Z_2} \right)$$

Figure 7-42: *Capacitive coupling equivalent circuit model*

It is evident that the noise voltage, $V_{COUPLED}$ appearing across Z_1, may be reduced by several means, all of which reduce noise current in Z_1. They are reduction of the signal voltage V_N, reduction of the frequency involved, reduction of the capacitance, or reduction of Z_1 itself. Unfortunately however, often none of these circuit parameters can be freely changed, and an alternate method is needed to minimize the interference. The best solution towards reducing the noise coupling effect of C is to insert a grounded conductor, also known as a *Faraday shield*, between the noise source and the affected circuit. This has the desirable effect of reducing Z_1 noise current, thus reducing $V_{COUPLED}$.

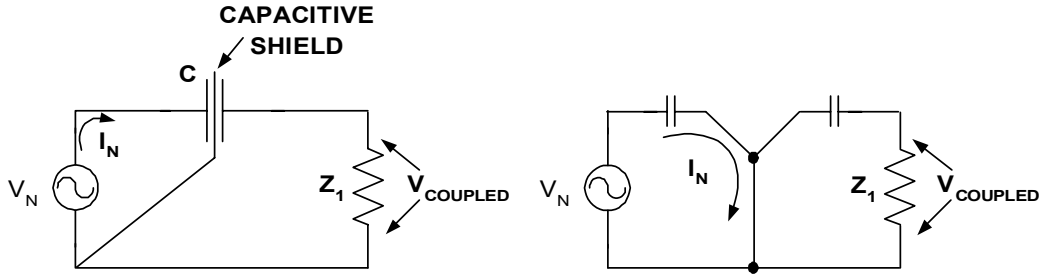


Figure 7-43: *An operational model of a Faraday shield*

A Faraday shield model is shown by Figure 7-43. In the left picture, the function of the shield is noted by how it effectively divides the coupling capacitance, C. In the right picture the net effect on the coupled voltage across Z_1 is shown. Although the noise current I_N still flows in the shield, most of it is now diverted away from Z_1. As a result, the coupled noise voltage $V_{COUPLED}$ across Z_1 is reduced.

A Faraday shield is easily implemented and almost always successful. Thus capacitively coupled noise is rarely an intractable problem. However, to be fully effective, a Faraday shield must completely block the electric field between the noise source and the shielded circuit. It must also be connected so that the displacement current returns to its source, without flowing in any part of the circuit where it can introduce conducted noise.

The Floating Shield Problem

And, it is quite important to note here— *a conductor that is intended to function as a Faraday shield must never be left floating, as this almost always increases capacity and exacerbates the noise problem*!

An example of this "floating shield" problem is seen in side-brazed ceramic IC packages. These DIP packages have a small square conducting Kovar lid soldered onto a metallized rim on the ceramic package top. Package manufacturers offer only two options: the metallized rim may be connected to one of the corner pins of the package, or it may be left unconnected.

Most logic circuits have a ground pin at one of the package corners, and therefore the lid is grounded. Alas, many analog circuits don't have a ground pin at a package corner, and the lid is left floating— acting as an antenna for noise. Such circuits turn out to be far more vulnerable to electric field noise than the same chip in a plastic DIP package, where the chip is completely unshielded.

Whenever practical, it is good practice for the user to ground the lid of any side brazed ceramic IC where the lid is not grounded by the manufacturer, thus implementing an *effective* Faraday shield. This can be done with a wire soldered to the lid (this will not damage the device, as the chip is thermally and electrically isolated from the lid). If soldering to the lid is unacceptable, a grounded phosphor-bronze clip may be used to make the ground connection, or conductive paint from the lid to the ground pin.

A safety note is appropriate at this point. Never attempt to ground such a lid without first verifying that it is unconnected. Occasionally device types are found with the lid connected to a power supply rather than to ground!

A case where a Faraday shield is impracticable is between IC chip bondwires, which has important consequences. The stray capacitance between chip bondwires and associated leadframes is typically ≈ 0.2pF, with observed values generally between 0.05 and 0.6pF.)

Buffering ADCs Against Logic Noise

If we have a high resolution data converter (ADC or DAC) connected to a high speed data bus which carries logic noise with a 2-5 V/ns edge rate, this noise is easily connected to the converter analog port via stray capacitance across the device. Whenever the data bus is active, intolerable amounts of noise are capacitively coupled into the analog port, thus seriously degrading performance.

This particular effect is illustrated by the diagram of Figure 7-44, where multiple package capacitors couple noisy edge signals from the data bus into the analog input of an ADC.

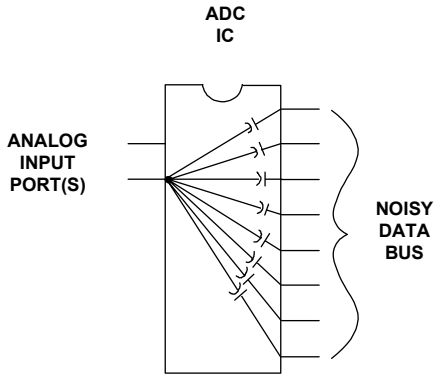


Figure 7-44: *A high speed ADC IC sitting on a fast data bus couples digital noise into the analog port, thus limiting performance*

Present technology offers no cure for this problem, within the affected IC device itself. The problem also limits performance possible from other broadband monolithic mixed signal ICs with single-chip analog and digital circuits. Fortunately, this coupled noise problem can be simply avoided, by *not* connecting the data bus directly to the converter.

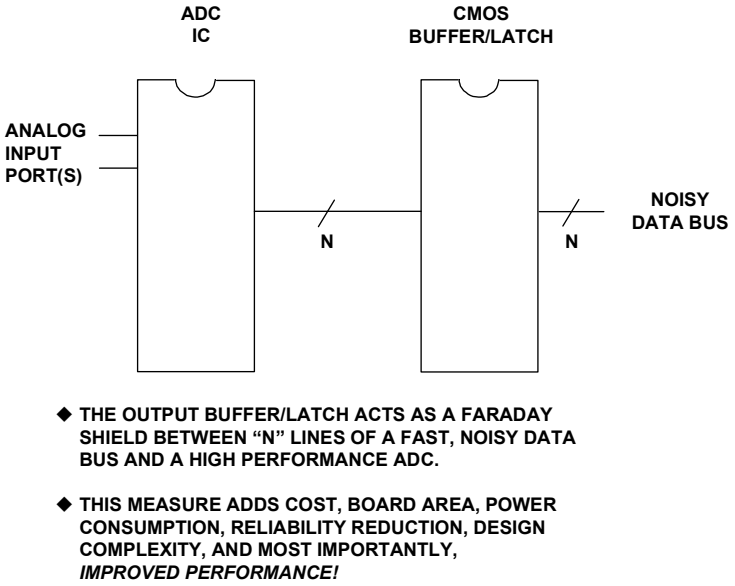


Figure 7-45: *A high speed ADC IC using a CMOS buffer/latch at the output shows enhanced immunity of digital data bus noise*

Instead, *use a CMOS latched buffer as a converter-to-bus interface*, as shown by Figure 7-45. Now the CMOS buffer IC acts as a Faraday shield, and dramatically reduces noise coupling from the digital bus. This solution costs money, occupies board area, reduces reliability (very slightly), consumes power, and it complicates the design— but it does improve the signal-to-noise ratio of the converter! The designer must decide whether it is worthwhile for individual cases, but in general it is highly recommended.

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ACKNOWLEDGEMENTS:

Portions of this section were adapted from Doug Grant and Scott Wurcer, "Avoiding Passive Component Pitfalls", originally published in **Analog Dialogue 17-2**, 1983.

SECTION 7-3: OP AMP POWER SUPPLY SYSTEMS

Walt Jung, Walt Kester

Op amp circuits have traditionally been powered from well-regulated, low noise linear power supplies. This type of power system is typically characterized by medium-to-low power conversion efficiency. Such linear regulators usually excel in terms of self-generated and radiated noise components. If the designer's life were truly simple, it might continue with such familiar designs offering good performance and minimal side effects.

But, the designer's life is hardly so simple. Modern systems may allow using linear regulators, but multiple output levels and/or polarities are often required. There may also be some additional requirements set for efficiency, which may dictate the use of dc-dc conversion techniques, and, unfortunately, their higher associated noise output.

This section addresses power supply design issues for op amp systems, taking into account the regulator types most likely to be used. The primary dc power sources are assumed to be either rectified and smoothed ac sources (i.e., mains derived), a battery stack, or a switching regulator output. The latter example could be fed from either a battery or a mains-derived dc source.

As noted in Figure 7-46, linear mode regulation is generally recommended as an optimum starting point in all instances (first bullet). Nevertheless, in some cases, a degree of hybridization between fully linear and switching mode regulation may be required (second bullet). This could be either for efficiency or other diverse reasons.

- **High performance analog power systems use *linear regulators*, with primary power derived from:**
  - **AC line power**
  - **Battery power systems**
  - **DC- DC power conversion systems**
- ***Switching regulators* should be avoided if at all possible, but if not…**
  - **Apply noise control techniques**
  - **Use quality layout and grounding**
  - **Be aware of EMI**

Figure 7-46: *Regulation priorities for op amp power supply systems*

Whenever switching-type regulators are involved in powering precision analog circuits, noise control is very likely to be a design issue. Therefore some focus of this section is on minimizing noise when using switching regulators.

Linear IC Regulation

Linear IC voltage regulators have long been standard power system building blocks. After an initial introduction in 5V logic voltage regulator form, they have since expanded into other standard voltage levels spanning from 3 to 24V, handling output currents from as low as 100mA (or less) to as high as 5A (or more). For several good reasons, linear style IC voltage regulators have been valuable system components since the early days. As mentioned above, a basic reason is the relatively low noise characteristic vis-à-vis the switching type of regulator. Others are a low parts count and overall simplicity compared to discrete solutions. But, because of their power losses, these linear regulators have also been known for being relatively inefficient. Early generation devices (of which many are still available) required 2V or more of unregulated input above the regulated output voltage, making them lossy in power terms.

More recently however, linear IC regulators have been developed with more liberal (i.e., lower) limits on minimum input-output voltage. This voltage, known more commonly as *dropout* voltage, has led to what is termed the *Low DropOut* regulator, or more simply, the LDO. Dropout voltage (V_{MIN}) is defined simply as that minimum input-output differential where the regulator undergoes a 2% reduction in output voltage. For example, if a nominal 5.0V LDO output drops to 4.9V (-2%) under conditions of an input-output differential of 0.5V, by this definition the LDO's dropout voltage is 0.5V.

Dropout voltage is extremely critical to a linear regulator's power efficiency. The lower the voltage allowable across a regulator while still maintaining a regulated output, the less power the regulator dissipates as a result. A low regulator dropout voltage is the key to this, as it takes a lower dropout to maintain regulation as the input voltage lowers. In performance terms, the bottom line for LDOs is simply that more useful power is delivered to the load and less heat is generated in the regulator. LDOs are key elements of power systems providing stable voltages from batteries, such as portable computers, cellular phones, etc. This is because they maintain a regulated output down to lower points on the battery's discharge curve. Or, within classic mains-powered raw DC supplies, LDOs allow lower transformer secondary voltages, reducing system shutdowns under brownout conditions, as well as allowing cooler operation.

Some Linear Voltage Regulator Basics

A brief review of three terminal linear IC regulator fundamentals is necessary before understanding the LDO variety. Most (but not all) of the general three terminal regulator types available today are *positive leg, series style* regulators. This simply means that they control the regulated voltage output by means of a pass element in series with the positive unregulated input. And, although they are fewer in number, there are also *negative leg* series style regulators, which operate in a fashion complementary to the positive units.

A basic hookup diagram of a three terminal regulator is shown in Figure 7-47. In terms of basic functionality, many standard voltage regulators operate in a series mode, three-terminal form, just as shown here. As can be noted from this figure, the three I/O terminals are V_{IN}, GND (or Common), and V_{OUT}. Note also that this regulator block, in

the absence of any assigned voltage polarity, could in principle be a positive type regulator. Or, it might also be a negative style of voltage regulator— the principle is the same for both— a common terminal, as well as input and output terminals.

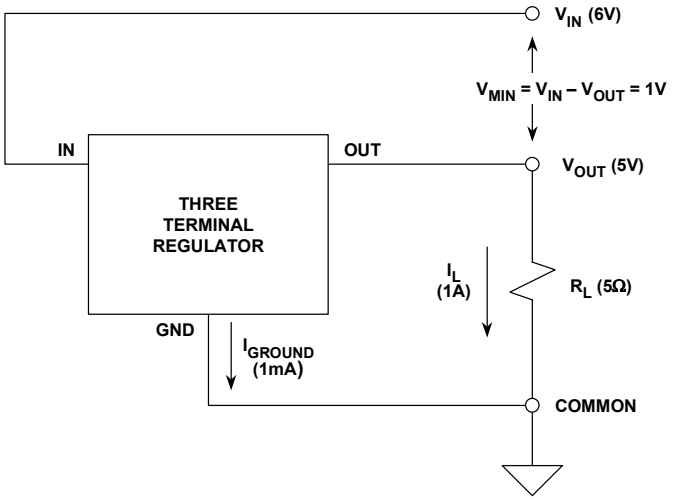

Figure 7-47: *A basic three terminal regulator hookup (either positive or negative)*

In operation, there are two power components which get dissipated in the regulator, one a function of $V_{IN} - V_{OUT}$ and I_L, plus a second which is a function of V_{IN} and Iground. The first of these is usually dominant. Analysis of the situation will reveal that as the dropout voltage V_{MIN} is reduced, the regulator is able to deliver a higher percentage of the input power to the load, and is thus more efficient, running cooler and saving power. This is the core appeal of the modern LDO type of regulator (see Reference 1).

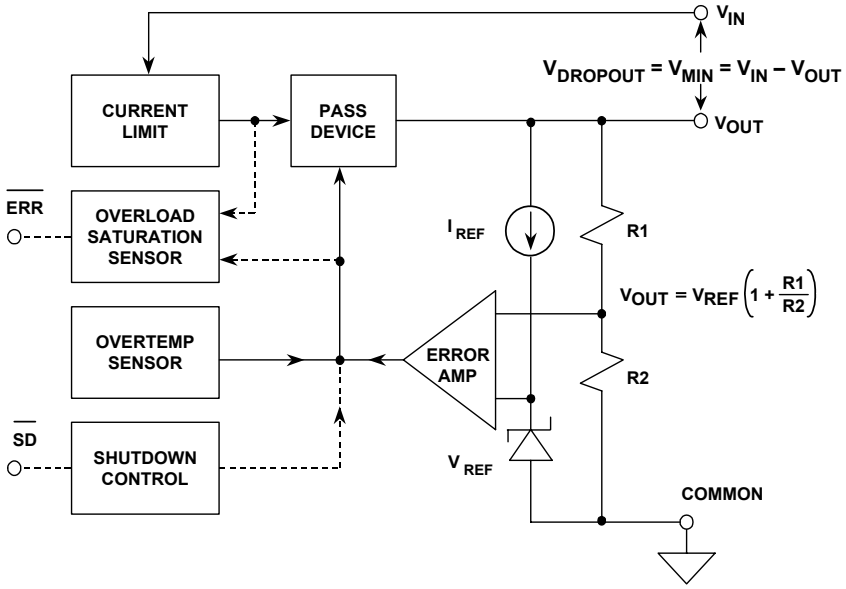

Figure 7-48: *Functional diagram of a typical voltage regulator*

A more detailed look within a typical regulator block diagram reveals a variety of elements, as is shown in Figure 7-48. Note that all regulators will contain those functional components connected via solid lines. The connections shown dotted indicate options, which might be available when more than three I/O pins are available.

In operation, a voltage reference block produces a stable voltage V_{REF}, which is almost always a voltage based on the bandgap voltage of silicon, typically ~1.2V (see Reference 2). This allows output voltages of 3V or more from supplies as low as 5V. This voltage drives one input of an error amplifier, with the second input connected to the divider, R1-R2. The error amplifier drives the pass device, which in turn controls the output. The resulting regulated voltage is then simply:

$$V_{OUT} = V_{REF}\left(1 + \frac{R1}{R2}\right) \qquad \text{Eq. 7-1}$$

Pass Devices

The pass device is a foremost regulator part, and the type chosen here has a major influence on almost all regulator performance issues. Most notable among these is dropout voltage, V_{MIN}. Analysis shows the use of an *inverting* mode pass transistor allows the pass device to be effectively saturated, thus minimizing the associated voltage losses. Therefore this factor makes the two most desirable pass devices for LDO use a PNP bipolar, or a PMOS transistor. These device types achieve the lowest levels of V_{IN}-V_{OUT} required for LDO operation. In contrast, NPN bipolars are poor as pass devices in terms of low dropout, particularly when they are Darlington connected.

Standard fixed-voltage IC regulator architectures illustrate this point on regarding pass devices. For example, the fixed-voltage LM309 5V regulators and family derivatives such as the 7805, 7815 et al, (and their various low and medium current alternates) are poor in terms of dropout voltage. These designs use a Darlington pass connection, not known for low dropout (~1.5V typical), or for low quiescent current (~5mA).

±15V regulator using adjustable voltage ICs

Later developments in references and three-terminal regulation techniques led to the development of the *voltage-adjustable* regulator. The original IC to employ this concept was the LM317, a positive regulator. The device produces a fixed reference voltage of 1.25V, appearing between the V_{OUT} and ADJ pins of the IC. External scaling resistors set up the desired output voltage, adjustable in the range of 1.25 – 30V. A complementary device, the LM337, operates in similar fashion, regulating negative voltages.

An application example using standard *adjustable* three terminal regulators to implement a ±15V linear power supply is shown in Figure 7-49. This is a circuit as might be used for powering traditional op amp supply rails. It is capable of better line regulation performance than would an otherwise similar circuit, using standard fixed-voltage regulator devices, such as for example 7815 and 7915 ICs. However, in terms of power efficiency it isn't outstanding, due to the use of the chosen ICs, which require 2V or more of headroom for operation.

In the upper portion of this circuit an LM317 adjustable regulator is used, with R2 and R1 chosen to provide a 15V output at the upper output terminal. If desired, R2 can easily be adjusted for other output levels, according to the figure's V_{OUT} expression. Resistor R1 should be left fixed, as it sets the minimum regulator drain of 10mA or more.

In this circuit, capacitors C1 and C2 should be tantalum types, and R1-R2 metal films. C3 is optional, but is highly recommended if the lowest level of output noise is desired. The normally reverse biased diode D1 provides a protective output clamp, for system cases where the output voltage would tend to reverse, if one supply should fail. The circuit operates from a rectified and filtered ac supply at V_{IN}, polarized as shown. The output current is determined by choosing the regulator IC for appropriate current capability.

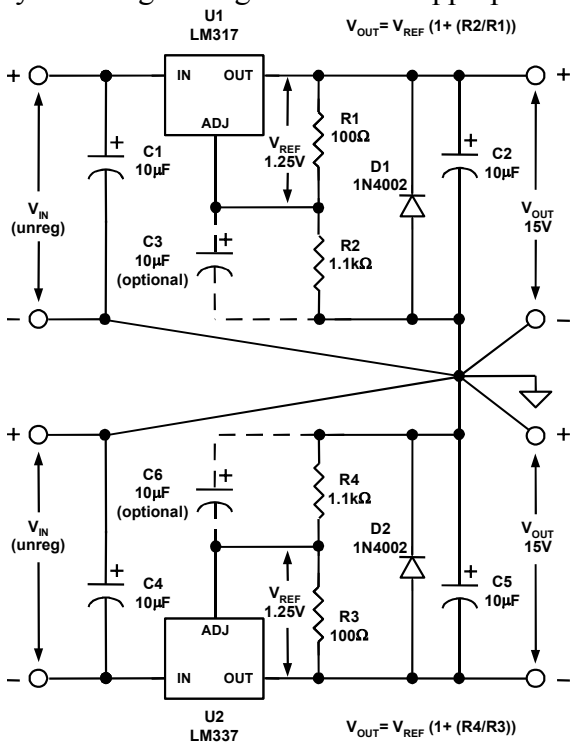

Figure 7-49: *A classic ±15V, 1A linear supply regulator using adjustable voltage regulator ICs*

To implement the negative supply portion, the sister device to the LM317 is used, the LM337. The bottom circuit section thus mirrors the operation of the upper, delivering a negative 15V at the lowest output terminal. Programming of the LM337 for output voltage is similar to that of the LM317, but uses resistors R4 and R3. R4 should be used to adjust the voltage, with R3 remaining fixed. C6 is again optional, but is recommended for reasons of lowest noise.

Low Dropout Regulator Architectures

In contrast to traditional three terminal regulators with Darlington or single-NPN pass devices, low dropout regulators employ lower voltage threshold pass devices. This basic operational difference allows them to operate effectively down to a range of 100-200mV in terms of their specified V_{MIN}. In terms of use within a system, this factor can have fairly significant operational advantages.

An effective implementation of some key LDO features is contained in the Analog Devices series of anyCAP™ LDO regulators. Devices of this ADP330X series are so named for their relative insensitivity to the output capacitor, in terms of both its size and ESR. Available in power efficient packages such as the ADI Thermal Coastline (and

other thermally enhanced packages), they come in both stand-alone LDO and LDO controller forms (used with an external PMOS FET). They also offer a wide span of fixed output voltages from 1.8 to 5V, with rated current outputs up to 500mA. User-adjustable output voltage versions are also available. A basic simplified diagram for the family is shown schematically in Figure 7-50.

One of the key differences in the ADP330X LDO series is the use of a high gain vertical PNP pass device, Q1, allowing typical dropout voltages for the series to be on the order of 1mV/mA for currents of 200mA or less.

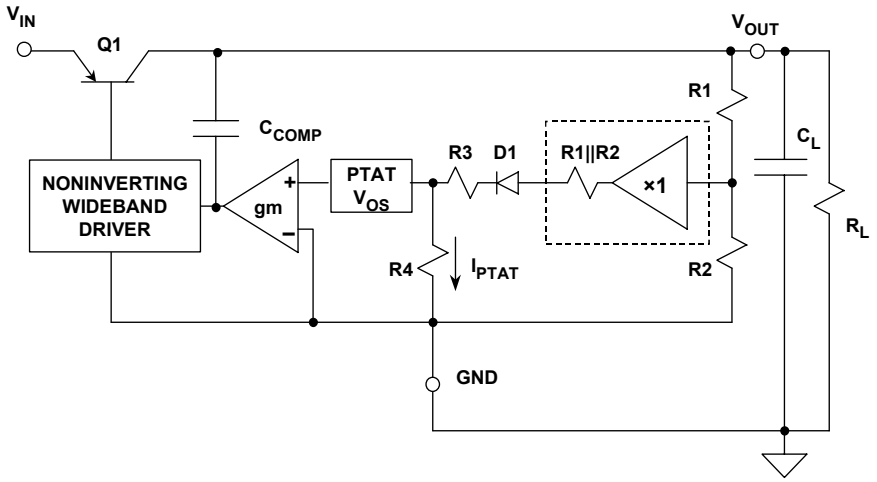

Figure 7-50: *The ADP330X anyCAP™ LDO architecture has both dc and ac performance advantages*

In circuit operation, V_{REF} is defined as a reference voltage existing at the output of a zero impedance divider of ratio R1/R2. In the figure, this is depicted symbolically by the (dotted) unity gain buffer amplifier fed by R1/R2, which has an output of V_{REF}. This reference voltage feeds into a series connection of (dotted) R1||R2, then actual components D1, R3, R4, etc. The regulator output voltage is:

$$V_{OUT} = V_{REF}\left(1 + \frac{R1}{R2}\right) \qquad \text{Eq. 7-2}$$

In the various devices of the ADP330X series, the R1-R2 divider is adjusted to produce standard output voltages of 1.8, 2.5, 2.7, 3.0, 3.2, 3.3, and 5.0V. The regulator behaves as if the entire error amplifier has simply an offset voltage of V_{REF} volts, as seen at the output of a conventional R1-R2 divider.

While the above described dc performance enhancements of the ADP330X series are worthwhile, more dramatic improvements come in areas of ac-related performance. Capacitive loading and the potential instability it brings is a major deterrent to easy LDO applications. One method of providing some measure of immunity to variation in an amplifier response pole is the use of a frequency compensation technique called *pole splitting*. In the Figure 7-50 circuit, C_{COMP} functions as the pole splitting capacitor, and provides benefits of a buffered, C_L independent single-pole response. As a

result, frequency response is dominated by the regulator's internal compensation, and becomes relatively immune to the value and ESR of load capacitor C_L.

This feature makes the design tolerant of virtually any output capacitor type. C_L, the load capacitor, can be as low as 0.47µF, and it can also be a multi-layer ceramic capacitor (MLCC) type, allowing a very small physical size for the entire regulation function.

Fixed Voltage, 50/100/200/500 mA LDO Regulators

A basic regulator application diagram common to various fixed voltage devices of the ADP330X device series is shown by Figure 7-51. Operation of the various pins and internal functions is discussed below. To adapt this general diagram to a specific current and voltage requirement, select a basic device for output current from the table in the diagram. Then select the output voltage by the part # suffix, consistent with the table.

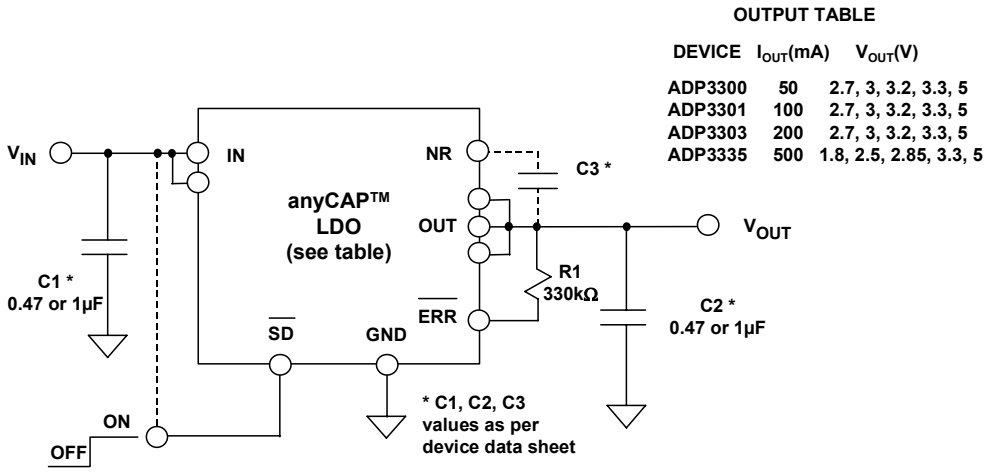

Figure 7-51: *A basic LDO regulator hookup useful by device selection from 50 to 500mA, at fixed voltages per table*

This circuit is a general one, illustrating common points. For example, the ADP3300 is a 50mA basic LDO regulator device, designed for those fixed output voltages as noted. An actual ADP3300 device ordered would be ADP3300ART-YY, where the "YY" is a voltage designator suffix such as 2.7, 3, 3.2, 3.3, or 5, for the respective table voltages. The "ART" portion of the part number designates the package (SOT23 6-lead). To produce 5V from the circuit, use the ADP3300ART-5. Similar comments apply to the other devices, insofar as part numbering. For example, an ADP3301AR-5 depicts an SO-8 packaged 100mA device, producing 5V output.

In operation, the circuit produces rated output voltage for loads under the max current limit, for input voltages above $V_{OUT} + V_{MIN}$ (where V_{MIN} is the dropout voltage for the specific device used, at rated current). The circuit is ON when the shutdown input is in a HIGH state, either by a logic HIGH control input to the $\overline{SD}$ pin, or by simply tying this pin to V_{IN} (shown dotted). When $\overline{SD}$ is LOW or grounded, the regulator shuts down, and draws a minimum quiescent current.

The anyCAP™ regulator devices maintain regulation over a wide range of load, input voltage and temperature conditions. Most devices have a combined error band of ±1.4%

(or less). When an overload condition is detected, the open collector $\overline{ERR}$ goes to a LOW state. R1 is a pullup resistor for the $\overline{ERR}$ output. This resistor can be eliminated if the load provides a pullup current.

C3, connected between the OUT and NR pins, can be used for an optional noise reduction (NR) feature. This is accomplished by bypassing a portion of the internal resistive divider, which reduces output noise ~10 dB. When exercised, only the recommended low leakage capacitors as specific to a particular part should be used. The C1 input and C2 output capacitors should be selected as either 0.47 or 1µF values respectively, again, as per the particular device used. For most devices of the series 0.47µF suffices, but the ADP3335 uses the 1µF values. Larger capacitors can also be used, and will provide better transient performance.

Heat sinking of device packages with more than 5 pins is enhanced, by use of multiple IN and OUT pins. All of the pins available should therefore be used in the PCB design, to minimize layout thermal resistance.

Adjustable Voltage, 200mA LDO Regulator

In addition to the fixed output voltage LDO devices discussed above, adjustable versions are also available, to realize non-standard voltages. The ADP3331 is one such device, and it is shown in Figure 7-52, configured as a 2.8V output, 200mA LDO application.

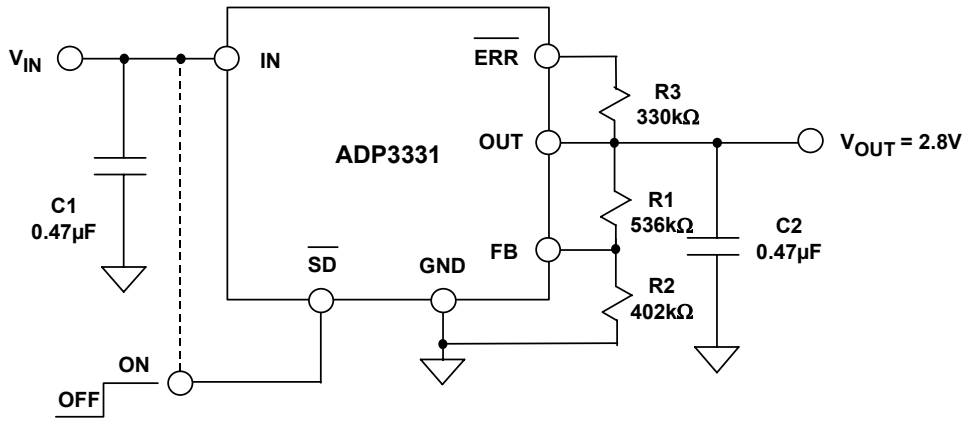

Figure 7-52: *An adjustable 200mA LDO regulator set up for a 2.8V output*

The ADP3331 is generally similar to other anyCAP™ LDO parts, with two notable exceptions. It has a lower quiescent current (~34µA when lightly loaded) and most importantly, the output voltage is user-adjustable. As noted in the circuit, R1 and R2 are external precision resistors used to define the regulator operating voltage.

The output of this regulator is V_{OUT}, which is related to feedback pin FB voltage V_{FB} as:

$$V_{OUT} = V_{FB}\left(1 + \frac{R1}{R2}\right) \qquad \text{Eq. 7-3}$$

where V_{FB} is 1.204V. Resistors R1 and R2 program V_{OUT}, and their parallel equivalent should be kept close to 230kΩ for best stability.

To select R1 and R2, first calculate their ideal values, according to the following two expressions:

$$R1 = 230\left(\frac{V_{OUT}}{V_{FB}}\right)k\Omega \qquad \text{Eq. 7-4}$$

$$R2 = \frac{230}{\left(1 + \frac{V_{FB}}{V_{OUT}}\right)}k\Omega \qquad \text{Eq. 7-5}$$

In the example circuit, V_{OUT} is 2.8V, which yields R1 = 534.9kΩ, and R2 = 403.5kΩ. As noted in the figure, closest standard 1% values are used, which provides an output of 2.8093V (perfect resistors assumed). In practice, the resistor tolerances should be added to the ±1.4% tolerance of the ADP3331 for an estimation of overall error.

To complement the above-discussed anyCAP™ series of standalone LDO regulators, there is the LDO *regulator controller*. The regulator controller IC picks up where the standalone regulator stops for either load current or power dissipation, using an external PMOS FET pass device. As such, the current capability of the LDO can be extended to several amps. An LDO regulator controller application is shown later in this discussion.

These application examples above illustrate a subset of the entire anyCAP™ family of LDOs. Further information on this series of standalone and regulator controller LDO devices can be found in the references at the end of the section.

Charge-Pump Voltage Converters

Another method for developing supply voltage for op amp systems employs what is known as a *charge-pump* circuit (also called switched capacitor voltage conversion). Charge-pump voltage converters accomplish energy transfer and voltage conversion using charges stored on capacitors, thus the name, charge-pump.

Using switching techniques, charge-pumps convert supply voltage of one polarity to a higher or lower voltage, or to an alternate polarity (at either higher or lower voltage). This is accomplished with only an array of low resistance switches, a clock for timing, and a few external storage capacitors to hold the charges being transferred in the voltage conversion process. No inductive components are used, thus EMI generation is kept to a minimum. Although relatively high currents are switched internally, the high current switching is localized, and therefore the generated noise is not as great as in inductive type switchers. With due consideration towards component selection, charge-pump converters can be implemented with reasonable noise performance.

The two common charge-pump voltage converters are the *voltage inverter* and the *voltage doubler* circuits. In a voltage inverter, a charge pump capacitor is charged to the input voltage during the first half of the switching cycle. During the second half of the switching cycle the input voltage stored on the charge pump capacitor is inverted, and is applied to an output capacitor and the load. Thus the output voltage is essentially the negative of the input voltage, and the average input current is approximately equal to the

output current. The switching frequency impacts the size of the external capacitors required, and higher switching frequencies allow the use of smaller capacitors. The duty cycle— defined as the ratio of charge pump charging time to the entire switching cycle time— is usually 50%, which yields optimal transfer efficiency.

A voltage doubler works similarly to the inverter. In this case the pump capacitor accomplishes a voltage doubling function. In the first phase it is charged from the input, but in the second phase of the cycle it appears in series with the output capacitor. Over time, this has the effect of doubling the magnitude of the input voltage across the output capacitor and load. Both the inverter and voltage doubler circuits provide no voltage regulation in basic form. However, techniques exist to add regulation (discussed below).

There are advantages and disadvantages to using charge-pump techniques, compared to inductor-based switching regulators. An obvious key advantage is the elimination of the inductor and the related magnetic design issues. In addition, charge-pump converters typically have relatively low noise and minimal radiated EMI. Application circuits are simple, and usually only two or three external capacitors are required. Because there are no inductors, the final PCB height can generally be made smaller than a comparable inductance-based switching regulator. Charge-pump inverters are also low in cost, compact, and capable of efficiencies greater than 90%. Obviously, current output is limited by the capacitor size and the switch capacity. Typical IC charge-pump inverters have 150mA maximum outputs.

- **No Inductors!**
- **Minimal Radiated EMI**
- **Simple Implementation: 2 External Capacitors (Plus an Input Capacitor)**
- **Efficiency > 90% Achievable**
- **Low Cost, Compact, Low Profile (Height)**
- **Optimized for Doubling or Inverting Supply Voltage: -- ADM660 or ADM8660**
- **Voltage Regulated Output Devices Available: -- ADP3603/ADP3604/ADP3605/ADP3607**

Figure 7-53: *Some general charge-pump characteristics*

On their downside, charge-pump converters don't maintain high efficiency for a wide voltage range of input to output, unlike inductive switching regulators. Nevertheless, they are still often suitable for lower current loads where any efficiency disadvantages are a small portion of a larger system power budget. A summary of general charge-pump operating characteristics is shown in Figure 7-53.

An example of charge-pump applicability is the voltage inverter function. Inverters are often useful where a relatively low current negative voltage (i.e., -3V) is required, in addition to a primary positive voltage (such as 5V). This may occur in a single supply system, where only a few high performance parts require the negative voltage. Similarly, voltage doublers are useful in low current applications, where a voltage greater than a primary supply voltage is required.

Unregulated inverter and doubler charge-pumps

Illustrating these principles are a pair of basic charge-pump ICs from Analog Devices, shown in Figure 7-54. The ADM660 is a popular charge-pump IC, and is shown here operating as both a voltage inverter (left) and the doubler (right) functions. Switching frequency of this IC is selectable between 25kHz and 120kHz using the FC input pin. With the FC input is open as shown, the switching frequency is 25kHz; with it connected to the V+ pin, frequency increases to 120kHz. Generally, efficiency is greater when operating at the higher frequency. Only two external electrolytic capacitors are required for operation, C1 and C2 (ESR should be <200mΩ). The value of these capacitors is flexible. For a 25kHz switching frequency 10µF tantalum types are recommended; for 120kHz operation 2.2µF provides comparable performance. Larger values can also be used, and will provide lower output ripple (at the expense of greater size and cost).

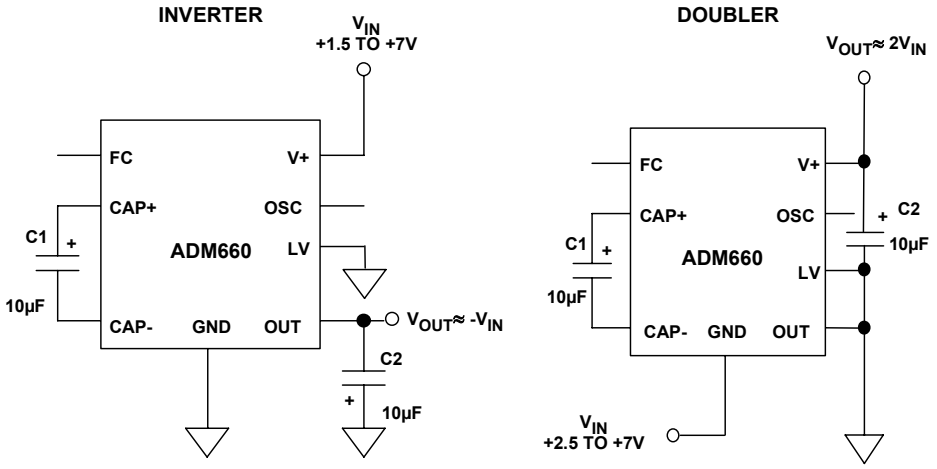

Figure 7-54: *ADM660 IC functions as a supply inverter (left) or doubler (right)*

These circuits accept V_{IN} inputs over the ranges noted, and deliver a nominal voltage output tracking the input voltage in magnitude, as noted in the output expressions. Although the output voltage is not regulated in these basic designs, it is still relatively low in impedance, due to the nominal 9Ω resistance of the IC switches.

Efficiency of these circuits using the ADM660/ADM8660 can be 90% or more, for output currents up to 50mA at a 120kHz frequency. The ADM8660 is a device similar to the ADM660, however it is optimized for inverter operation, and includes a shutdown feature which reduces the quiescent current to 5µA.

Regulated Output Charge-Pump Voltage Converters

Adding regulation to a simple charge-pump voltage converter function greatly enhances its usefulness for most applications. There are several techniques for adding regulation to a charge-pump converter. The most straightforward is to follow the charge-pump inverter/doubler with an LDO regulator. The LDO provides the regulated output, and can also reduce the charge-pump converter's ripple. This approach, however, adds complexity and reduces the available output voltage by the dropout voltage of the LDO (~200mV). These factors may or may not be a disadvantage.

By far the simplest and most effective method for achieving regulation in a charge-pump voltage converter is to simply use a charge-pump design with an internal error amplifier, to control the on-resistance of one of the switches.

This method is used in the ADP3603/3604/3605 voltage inverters, devices offering regulated outputs for positive input voltage ranges. The output is sensed and fed back into the device via a sensing pin, V_{SENSE}. Key features of the series are good output regulation, 3% in the ADP3605, and a high switching frequency of 250kHz, good for both high efficiency and small component size.

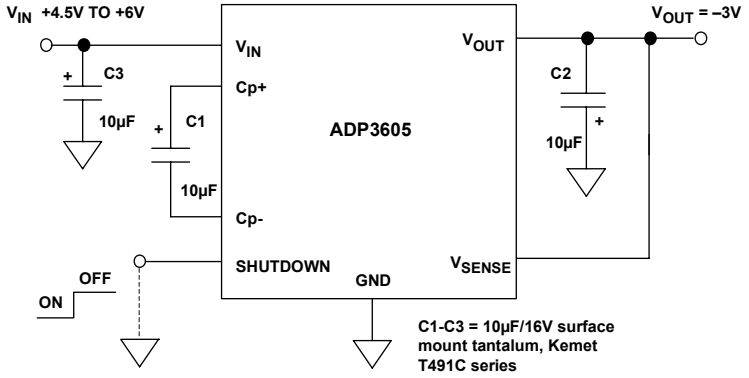

Figure 7-55: *ADP3605 5V to –3V, 60mA regulated supply inverter*

An example circuit for the ADP3605 IC from this series is shown in Figure 7-55. The application is a 5V to –3V inverter, with the output regulated ±3% for currents up to 60mA. In normal operation, the SHUTDOWN pin is connected to ground (as shown dotted). Alternately, a logic HIGH at this pin shuts the device down to a standby current of 2µA.

The 10µF capacitors for C1-C3 should have ESRs of less than 150mΩ (4.7µF can be used at the expense of slightly higher output ripple voltage). C1 is the most critical of the 3, because of its higher current flow. The tantalum type listed is recommended for lowest output ripple.

With values as shown, typical output ripple voltage ranges up to approximately 60mV as the output current varies over the 60mA range. Although output is regulated for currents up to 60mA, higher currents of up to 100mA are also possible with further voltage deviation, and proportionally greater ripple.

These application examples illustrate a subset of the entire charge-pump IC family. Further information on these devices can be found in the end-of-section references.

Linear post regulator for switching supplies

Another powerful noise reduction option which can be utilized in conjunction with a switching type supply is the option of a *linear post regulator* stage. This is at best an LDO type of regulator, chosen for the desired clean analog voltage level and current. It is preceded by a switching stage, which might be a buck or boost type inductor-based design, or it may also be a charge-pump. The switching converter allows the overall design to be more power-efficient, and the linear post regulator provides clean regulation at the load, reducing the noise of the switcher. This type of regulator can also be termed *hybrid regulation*, since it combines both switching and linear regulation concepts.

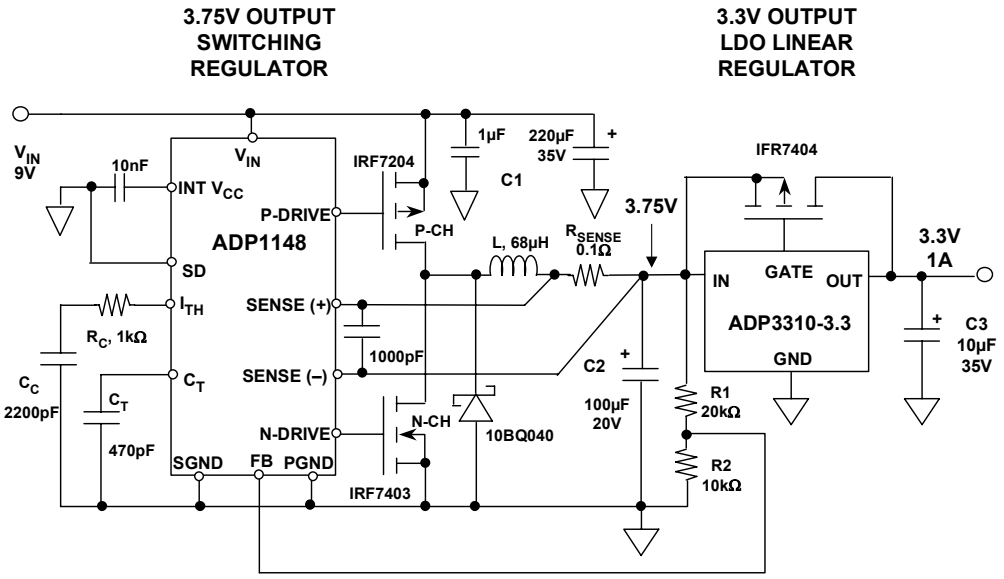

Figure 7-56: *A linear post-regulator operating after a switching/linear regulator is capable of low noise, as well as good DC efficiency*

An example circuit is shown in Figure 7-56, which features a 3.3V/1A low noise, analog-compatible regulator. It operates from a nominal 9V supply, using a buck or step-down type of switching regulator, as the first stage at the left. The switcher output is set for a few hundred mV above the desired final voltage output, minimizing power in the LDO stage at the right. This feature can eliminate need for a heat sink on the LDO pass device.

In this example the ADP1148 IC switcher is set up for a 3.75V output by R1-R2, but in principle, this voltage can be anything suitable to match the headroom of the companion LDO (within specification limits, of course). In addition, the principle extends to any LDO devices and other current levels, and other switching regulators. The ADP3310-3.3 is a fixed-voltage LDO controller, driving a PMOS FET pass device, with a 3.3V output.

The linear post regulation stage provides both noise-reduction (in this case about 14dB), as well as good dc regulation. To realize best results, good grounding practices must be followed. In tests, noise at the 3.3V output was about 5mVp-p at the 150kHz switcher frequency. Note that the LDO noise rejection for such relatively high frequencies is much less than at 100/120Hz. Note also that C2's ESR will indirectly control the final noise output. The ripple figures given are for a general-purpose C2 part, and can be improved.

Power Supply Noise Reduction and Filtering

During the last decade or so, switching power supplies have become much more common in electronic systems. As a consequence, they also are being used for analog supplies. Good reasons for the general popularity include their high efficiency, low temperature rise, small size, and light weight.

In spite of these benefits, switchers *do* have drawbacks, most notably high output noise. This noise generally extends over a broad band of frequencies, resulting in both conducted and radiated noise, as well as unwanted electric and magnetic fields. Voltage output noise of switching supplies are short-duration voltage transients, or spikes. Although the fundamental switching frequency can range from 20kHz to 1MHz, the spikes can contain frequency components extending to 100MHz or more. While specifying switching supplies in terms of RMS noise is common vendor practice, as a user you should also specify the *peak* (or p-p) amplitudes of the switching spikes, with the output loading of your system.

This section discusses filter techniques for rendering a switching regulator output *analog ready*, that is sufficiently quiet to power precision op amp and other analog circuitry with relatively small loss of DC terminal voltage. The filter solutions presented are generally applicable to all power supply types incorporating switching element(s) in their energy path. This includes charge-pump as well as other switching type converters and supplies. This section focuses on reducing *conducted type* switching power supply noise with external post filters, as opposed to radiated type noise.

- **Capacitors**
- **Inductors**
- **Ferrites**
- **Resistors**
- **Linear Post Regulation**
- **Proper Layout and Grounding**
- **Physical Separation!**

Figure 7-57: *Tools useful in reducing power supply noise*

Tools useful for combating high frequency switcher noise are shown by Figure 7-57. These differ in electrical characteristics as well as practicality towards noise reduction, and are listed roughly in an order of priorities. Of these tools, L and C are the most powerful filter elements, and are the most cost-effective, as well as small in size.

Capacitors

Capacitors are probably the single most important filter component for reducing switching-related noise. As noted in the first section of this chapter, there are many different types of capacitors. It is also quite true that understanding of their individual characteristics is absolutely mandatory to the design of effective and practical power supply filters. There are generally three classes of capacitors useful in 10kHz-100MHz

filters, broadly distinguished as the generic dielectric types; *electrolytic*, *film*, and *ceramic*. These discussions complement earlier ones, focusing on power-related concepts.

With any dielectric, a major potential filter loss element is ESR (equivalent series resistance), the net parasitic resistance of the capacitor. ESR provides an ultimate limit to filter performance, and requires more than casual consideration, because it can vary both with frequency and temperature in some types. Another capacitor loss element is ESL (equivalent series inductance). ESL determines the frequency where the net impedance characteristic switches from capacitive to inductive. This varies from as low as 10kHz in some electrolytics to as high as 100MHz or more in chip ceramic types. Both ESR and ESL are minimized when a leadless package is used. All capacitor types mentioned are available in surface mount packages, preferable for high speed uses.

The *electrolytic* family provides an excellent, cost-effective low-frequency filter component, because of the wide range of values, a high capacitance-to-volume ratio, and a broad range of working voltages. It includes *general purpose aluminum electrolytic* types, available in working voltages from below 10V up to about 500V, and in size from 1 to several thousand μF (with proportional case sizes). All electrolytic capacitors are polarized, and cannot withstand more than a volt or so of reverse bias without damage.

A subset of the general electrolytic family includes *tantalum* types, generally limited to voltages of 100V or less, with capacitance of 500μF or less (see Reference 7). In a given size, tantalums exhibit a higher capacitance-to-volume ratios than do general purpose electrolytics, and have both a higher frequency range and lower ESR. They are generally more expensive than standard electrolytics, and must be carefully applied with respect to surge and ripple currents.

A subset of aluminum electrolytic capacitors is the *switching* type, designed for handling high pulse currents at frequencies up to several hundred kHz with low losses (see Reference 8). This capacitor type can compete with tantalums in high frequency filtering applications, with the advantage of a broader range of values.

A more specialized high performance aluminum electrolytic capacitor type uses an organic semiconductor electrolyte (see Reference 9). The *OS-CON* capacitors feature appreciably lower ESR and higher frequency range than do other electrolytic types, with an additional feature of minimal low-temperature ESR degradation.

Film capacitors are available in very broad value ranges and an array of dielectrics, including polyester, polycarbonate, polypropylene, and polystyrene. Because of the low dielectric constant of these films, their volumetric efficiency is quite low, and a 10μF/50V polyester capacitor (for example) is actually a handful. Metalized (as opposed to foil) electrodes does help to reduce size, but even the highest dielectric constant units among film types (polyester, polycarbonate) are still larger than any electrolytic, even using the thinnest films with the lowest voltage ratings (50V). Where film types excel is in their low dielectric losses, a factor which may not necessarily be a practical advantage for filtering switchers. For example, ESR in film capacitors can be as low as 10mΩ or less, and the behavior of films generally is very high in terms of Q. In fact, this can cause problems of spurious resonance in filters, requiring damping components.

As typically constructed using wound layers, film capacitors can be inductive, which limits their effectiveness for high frequency filtering. Obviously, only non-inductively made film caps are useful for switching regulator filters. One specific style which is non-inductive is the *stacked-film* type, where the capacitor plates are cut as small overlapping linear sheet sections from a much larger wound drum of dielectric/plate material. This technique offers the low inductance attractiveness of a plate sheet style capacitor with conventional leads (see References 8 and 10). Obviously, minimal lead length should be used for best high frequency effectiveness. Very high current polycarbonate film types are also available, specifically designed for switching power supplies, with a variety of low inductance terminations to minimize ESL (see Reference 11). Dependent upon their electrical and physical size, film capacitors can be useful at frequencies to above 10MHz. At the highest frequencies, only stacked film types should be considered. Leadless surface mount packages are now available for film types, minimizing inductance.

Ceramic is often the capacitor material of choice above a few MHz, due to its compact size, low loss, and availability up to several µF in the high-K dielectric formulations (X7R and Z5U), at voltage ratings up to 200V (see ceramic families of Reference 7).

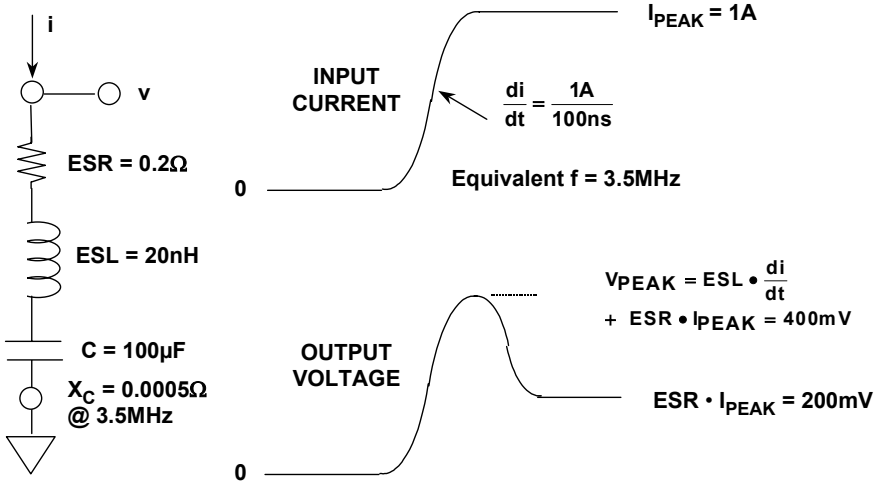

Figure 7-58: *Capacitor equivalent circuit and response to input current pulse*

Multilayer ceramic "chip caps" are very popular for bypassing and/or filtering at 10MHz or more, simply because their very low inductance design allows near optimum RF bypassing. For smaller values, ceramic chip caps have an operating frequency range to 1GHz. For high frequency applications, a useful selection can be ensured by selecting a value which has a self-resonant frequency *above* the highest frequency of interest.

The capacitor model and waveforms of Figure 7-58 illustrate how the various parasitic model elements become dominant, dependent upon the operating frequency. Assume an input current pulse changing from 0 to 1A in 100ns, as noted in the figure, and consider what voltage will be developed across the capacitor.

The fast-rising edge of the current waveform shown results in an initial voltage peak across the capacitor, which is proportional to the ESL. After the initial transient, the voltage settles down to a longer duration level which is proportional to the ESR of the

capacitor. Thus the ESL determines how effective a filter the capacitor is for the fastest components of the current signal, and the ESR is important for longer time frame components. Note that an overall time frame of a few microseconds (or even less) is relevant here. As things turn out, this means switching frequencies in the 100kHz to 1MHz range. Unfortunately however, this happens to be the region where most electrolytic types begin to perform poorly.

All electrolytics will display impedance curves similar in general shape to that of Figure 7-59. In a practical capacitor, at frequencies below about 10kHz the net impedance seen at the terminals is almost purely capacitive (C region). At intermediate frequencies, the net impedance is determined by ESR, for example about 0.1 to 0.5Ω at ~125kHz, for several types (ESR region). Above about several hundred kHz to 1MHz these capacitor types become inductive, with net impedance rising (ESL region).

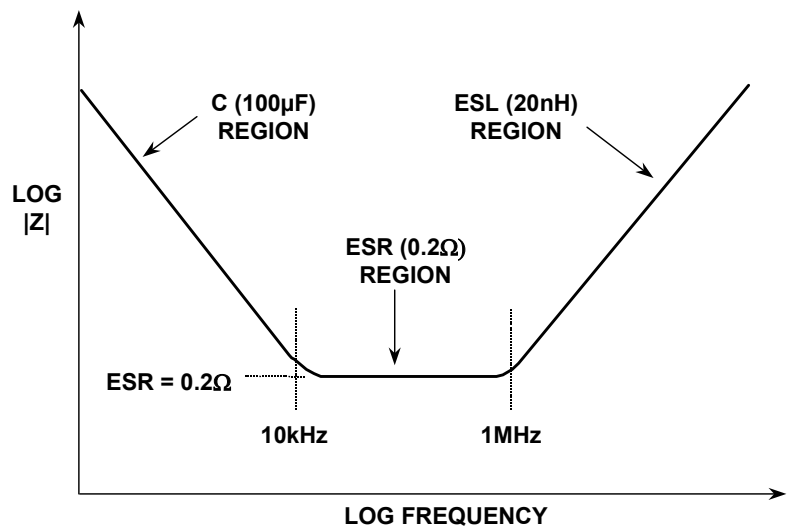

Figure 7-59: *Electrolytic capacitor impedance versus frequency*

The minimum impedance within the 10kHz – 1MHz range will vary with the magnitude of the capacitor's ESR. This is the primary reason why ESR is the most critical item in determining a given capacitor's effectiveness as a switching supply filter element. Higher up in frequency, the inductive region will vary with ESL (which in turn is also strongly effected by package style). It should go without saying that a wideband impedance plot for a capacitor being considered for a filter application will go a long way towards predicting its potential value, as well as for comparing one type against another.

It should be understood that all real world capacitors have some finite ESR. While it is usually desirable for filter capacitors to possess low ESR, this isn't always so. In some cases, the ESR may actually be helpful in reducing resonance peaks in filters, by supplying "free" damping. For example, in most electrolytic types, a nominally flat broad series resonance region can be noted in an impedance vs. frequency plot. This occurs where |Z| falls to a minimum level, nominally equal to the capacitor's ESR at that frequency. This low Q resonance can generally be noted to cover a relatively wide frequency range of several octaves. Contrasted to the high Q sharp resonances of film and ceramic caps, electrolytic's low Q behavior can be useful in controlling resonant peaks.

Ferrites

A second important filter element is the inductor, available in various forms. The use of *ferrite* core materials is prevalent in inductors most practical for power supply filtering.

Regarding inductors, ferrites, which are non-conductive ceramics manufactured from the oxides of nickel, zinc, manganese, etc., are extremely useful in power supply filters (see Reference 12). Ferrites can act as either inductors or resistors, dependent upon their construction and the frequency range. At low frequencies (<100kHz), inductive ferrites are useful in low-pass LC filters. At higher frequencies, ferrites become resistive, which can be an important characteristic in high-frequency filters. Again, exact behavior is a function of the specifics. Ferrite impedance depends on material, operating frequency range, DC bias current, number of turns, size, shape, and temperature. Figure 7-60 summarizes a number of ferrite characteristics.

- **Ferrites Good for Frequencies Above 25kHz**
- **Many Sizes / Shapes Available Including Leaded "Resistor Style"**
- **Ferrite Impedance at High Frequencies Primarily Resistive -- Ideal for HF Filtering**
- **Low DC Loss: Resistance of Wire Passing Through Ferrite is Very Low**
- **High Saturation Current Versions Available**
- **Choice Depends Upon:**
  - **Source and Frequency of Interference**
  - **Impedance Required at Interference Frequency**
  - **Environmental: Temperature, AC and DC Field Strength, Size and Space Available**
- **Always Test the Design!**

Figure 7-60: *A summary of ferrite characteristics*

Several ferrite manufacturers offer a wide selection of ferrite materials from which to choose, as well as a variety of packaging styles for the finished network (see References 13 and 14). A simple form is the *bead* of ferrite material, a cylinder of the ferrite which is simply slipped over the power supply lead to the decoupled stage. Alternately, the *leaded ferrite bead* is the same bead, pre-mounted on a length of wire and used as a component (see Reference 14). More complex beads offer multiple holes through the cylinder for increased decoupling, plus other variations. Surface mount beads are also available. PSpice models of Fair-Rite ferrites are available, allowing ferrite impedance estimations (see Reference 15). The models match measured rather than theoretical impedances.

A ferrite's impedance is dependent upon a number of inter-dependent variables, and is difficult to quantify analytically, thus selecting the proper ferrite is not straightforward. However, knowing the following system characteristics will make selection easier. First, determine the frequency range of the noise to be filtered. Second, the expected temperature range of the filter should be known, as ferrite impedance varies with temperature. Third, the DC current flowing through the ferrite must be known, to ensure that the ferrite does not saturate. Although models and other analytical tools may prove useful, the general guidelines given above, coupled with actual filter experimentation connected under system load conditions, should lead to a proper ferrite selection.

Card Entry Filter

Using proper component selection, low and high frequency band filters can be designed to smooth a noisy switching supply output so as to produce an *analog ready* supply. It is most practical to do this over two (and sometimes more) stages, each stage optimized for a range of frequencies.

A basic stage can be used to carry the entire load current, and filter noise by 60dB or more up to a 1-10MHz range. Figure 7-61 illustrates this type of filter, which is used as a *card entry filter,* providing broadband filtering for all power entering a PC card.

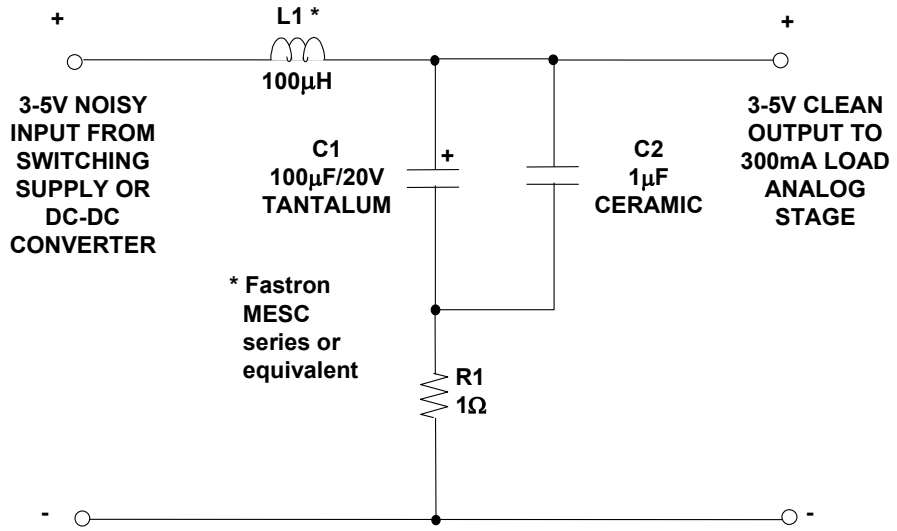

Figure 7-61: *A card-entry filter is useful for low-medium frequency power line noise filtering in analog systems*

In this filter, L1 and C1 perform the primary filtering, which provides a corner frequency of about 1.6kHz. With the corner thus placed well below typical switching frequencies, the circuit can have good attenuation up to 1MHZ, where the typical attenuation is on the order of 60dB. At higher frequencies parasitics limit performance, and a second filter stage will be more useful.

The ultimate level of performance available from this filter will be related to the components used within it. L1 should be derated for the operating current, thus for 300mA loads it is a 1A type. The specified L1 choke has a typical DCR of 0.65Ω, for low drop across the filter (see Reference 16). C1 can be either a tantalum or an aluminum electrolytic, with moderately low ESR. For current levels lower than 300mA, L1 can be proportionally downsized, saving space. The resistor R1 provides damping for the LC filter, to prevent possible ringing. R1 can be reduced or even possibly eliminated, if the ESR of C1 provides a comparable impedance.

While the example shown is a single-supply configuration, obviously the same filter concepts apply for dual supplies.

Rail bypass/distribution filter

A complement to the card-entry filter is the rail-bypass filter scheme of Figure 7-62. When operating from relatively clean power supplies, the heavy noise filtering of the card entry filter may not be necessary. However, some sort of low frequency bypassing with appreciable energy storage is almost always good, and this is especially true if high currents are being delivered by the stages under power.

In such cases, some lumped low frequency bypassing is appropriate on the card. Although these energy storage filters need not be immediately adjacent to the ICs they serve, they should be within a few inches. This type of bypassing scheme should be considered a minimum for powering any analog circuit. The exact capacitor values aren't critical, and can vary appreciably. The most important thing is to avoid leaving them out!

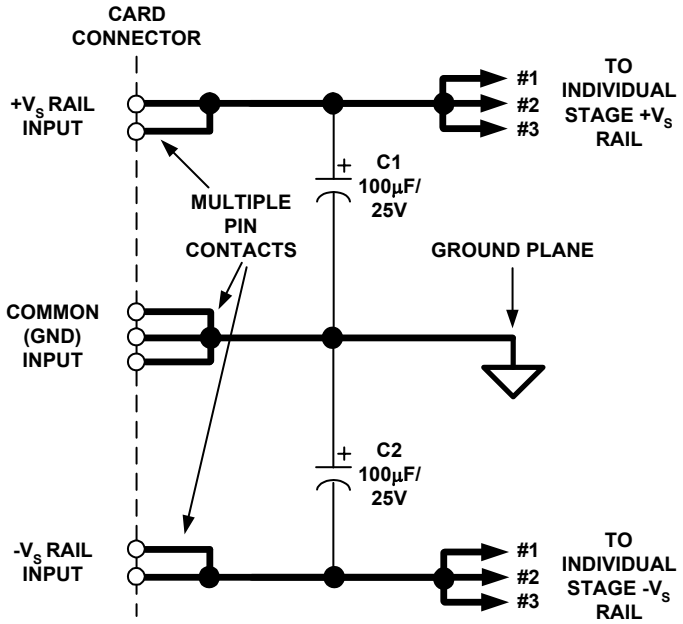

Figure 7-62: *Dual-supply low frequency rail bypass/distribution filter*

The circuit shown uses C1 and C2 as these bypasses in a dual-rail system. Note that multiple card contacts are recommended for the I/O pins, especially ground connection. From the capacitors outward, supply rail traces are distributed to each stage as shown, in "star" distribution fashion. Note— while this is the optimum method to minimize inter-stage crosstalk, in practice some degree of "daisy chaining" is often difficult to avoid. A prudent designer should therefore carefully consider common supply currents effects in designing these PCB distribution paths.

Wider than normal traces are recommended for these supply rails, especially those carrying appreciable current. If the current levels are in the ampere region, then star-type supply distribution with ultra-wide traces should be considered mandatory. In extreme cases, a dedicated power plane can be used. The impedance of the ground return path is minimized by the use of a ground plane.

Local high frequency bypass/decoupling

At each individual analog stage, further local, high-frequency-only filtering is used. With this technique, used in conjunction with either the card-entry filter or the low frequency bypassing network, such smaller and simpler local filter stages provide optimum high frequency decoupling. *These stages are provided directly at the power pins, of* all *individual analog stages*.

Figure 7-63 shows this technique, in both correct (left) as well as incorrect example implementations (right). In the left example, a typical 0.1µF chip ceramic capacitor goes directly to the opposite PCB side ground plane, by virtue of the via, and on to the IC's GND pin by a second via. In contrast, the less desirable setup at the right adds additional PCB trace inductance in the ground path of the decoupling cap, reducing effectiveness.

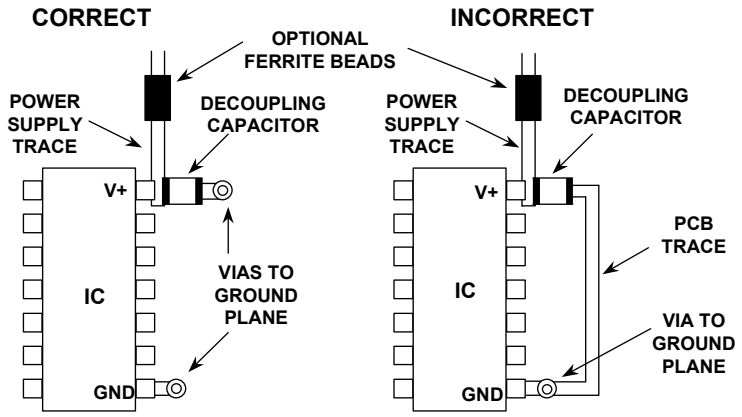

Figure 7-63: *Localized high frequency supply filter(s) provides optimum filtering and decoupling via short low-inductance path (ground plane)*

The general technique is shown here as suitable for a single-rail power supply, but the concept obviously extends to dual rail systems. Note— if the decoupled IC in question is an op amp, the GND pin shown is the $-V_S$ pin. For dual supply op amp uses, there is no op amp GND pin per se, so the dual decoupling networks should go directly to the ground plane when used, or other local ground.

All high frequency (i.e., ≥10MHz) ICs should use a bypassing scheme similar to Figure 7-63 for best performance. Trying to operate op amps and other high performance ICs without local bypassing is almost always folly. It *may* be possible in a few circumstances, *if* the circuitry is strictly micropower in nature, and the gain-bandwidth in the kHz range. To put things into an overall perspective however, note that a pair of 0.1µF ceramic bypass caps cost less than 25 cents. Hardly a worthy saving compared to the potential grief and lost time of troubleshooting a system without bypassing!

In contrast, the ferrite beads aren't 100% necessary, but they will add extra HF noise isolation and decoupling, which is often desirable. Possible caveats here would be to verify that the beads never saturate, when the op amps are handling high currents.

Note that with some ferrites, even before full saturation occurs, some beads can be non-linear, so if a power stage is required to operate with a low distortion output, this should also be lab checked.

Figure 7-64 summarizes the previous points of this section regarding power supply conditioning techniques for op amp circuitry.

- **Use Proper Layout and Grounding Techniques!**
- **At HF Local Decoupling at IC Power Pins is Mandatory**
- **At HF Ground Planes are Mandatory**
- **External LC Filters Very Effective in Reducing Ripple**
- **Low ESR/ESL Capacitors Give Best Results**
- **Parallel Caps Lower ESR/ESL and Increase C**
- **Linear Post Regulation Effective for Noise Reduction and Best Regulation**
- **Completely Analytical Approach Difficult**
  -- Prototyping Required for Optimum Results
- **Once Design is Final, Don't Switch Vendors or Substitute Parts**
  -- Without First Verifying Performance Within the Circuit!

Figure 7-64: *A summary of power supply conditioning techniques for high performance op amp circuitry*

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NOTES:

SECTION 7-4: OP AMP PROTECTION

Walt Jung, Walt Kester, James Bryant, Joe Buxton, Wes Freeman

Frequently, op amps and other analog ICs require protection against destructive potentials at their input and output terminals. One basic reason behind this is that these ICs are by nature relatively fragile components. Although designed to be as robust as possible *for normal signals*, there are nevertheless certain application and/or handling conditions where they can see voltage transients beyond their ratings. This situation can occur for either of two instances. The first of these is *in-circuit,* that is, operating within an application circuit. The second instance is *out-of-circuit,* which might be at anytime after receipt from a supplier, but prior to final assembly and mounting of the IC. In either case, under over-voltage conditions, it is a basic fact-of-life that unless the designer limits the fault currents at the input (or possibly output) of the IC, it can be damaged or destroyed.

So, obviously the designer should fully understand all of the fault mechanisms internal to those ICs that may require protection. This then allows design of networks that can protect the in-circuit IC throughout its lifetime, without undue compromise of speed, precision, etc. Or, for the out-of-circuit IC, it can help define proper protective handling procedures until it reaches its final destination. This section of the chapter examines a variety of protection schemes to ensure adequate protection for op amps and other analog ICs for in-circuit applications, as well as for out-of-circuit environments.

In-Circuit Over-Voltage Protection

There are many common cases that stress op amps and other analog ICs at the input, while operating within an application, i.e., in-circuit. Since these ICs must often interface to the outside world, this may entail handling voltages exceeding their absolute maximum ratings. For example, sensors are often placed in environments where a fault condition can expose the circuit to a dangerously high voltage. With the sensor connected to a signal processing amplifier, the input then sees excessive voltages during a fault.

General Input Common Mode Limitations

Whenever an op amp input common mode (CM) voltage goes outside its supply range, the op amp can be damaged, even if the supplies are turned off. Accordingly, the absolute maximum input ratings of almost all op amps limits the greatest applied voltage to a level equal to the positive and negative supply voltage, plus about 0.3V beyond these voltages (i.e., $+V_S + 0.3V$, or $-V_S - 0.3V$). While some exceptions to this general rule might exist it is important to note this: *Most IC op amps require input protection when over-voltage of more than 0.3V beyond the rails occurs.*

A safe operating rule is to always keep the applied op amp CM voltage between the rail limits. Here, "safe" implies prevention of outright IC destruction. As will be seen later, there are also intermediate "danger-zone" CM conditions between the rails with certain op amps, which can invoke dangerous (but not necessarily destructive) behavior.

Speaking generally, it is important to note that almost *any* op amp input will break down, given sufficient over-voltage to the positive or negative rail. Under breakdown conditions high and uncontrolled current can flow, so the danger is obvious. The exact breakdown voltage is entirely dependent on the individual op amp input stage. It may be a 0.6V diode drop, or a process-related breakdown of 50V or more. In many cases, over-voltage stress can result in currents over 100mA, which destroys a part almost instantly.

Therefore, unless otherwise stated on the data sheet, op amp input fault current should be limited to ≤5mA to avoid damage. This is a conservative rule of thumb, based on metal trace widths in a typical op amp input. Higher levels of current can cause *metal migration*, a cumulative effect, which, if sustained, eventually leads to an open trace. Should a migration situation be present, failure may only appear after a long time due to multiple over-voltages, a very difficult failure to identify. So, even though an amplifier may appear to withstand over-voltage currents well above 5mA for a short time period, it is important to limit the current to 5mA (or preferably less) for long term reliability.

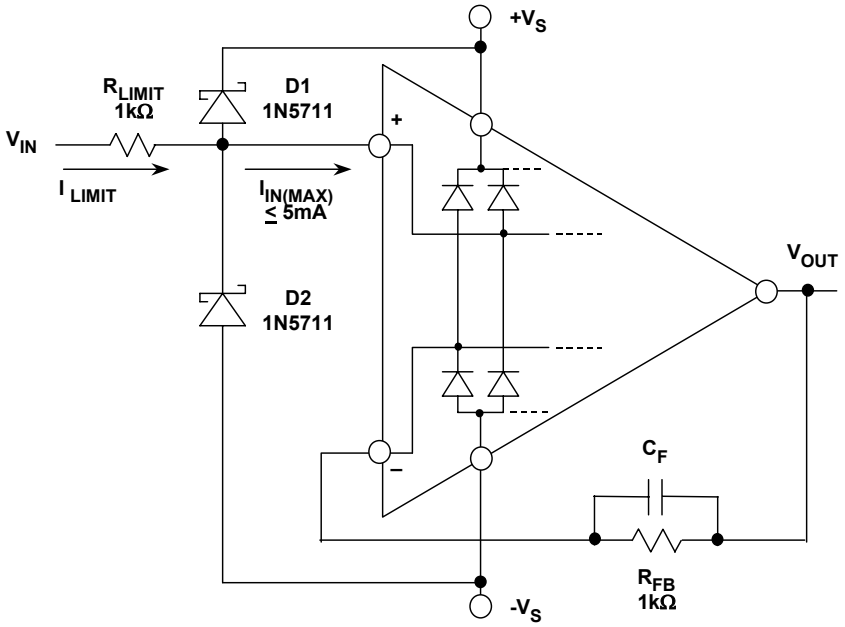


Figure 7-65: *A general-purpose op amp CM over-voltage protection network using Schottky clamp diodes with current limit resistance*

Figure 7-65 illustrates an external, general-purpose op amp CM protection circuit. The basis of this scheme is the use of Schottky diodes D1 and D2, plus an external current limiting resistor, R_{LIMIT}. With appropriate selection of these parts, input protection for a great many op amps can be ensured. Note that an op amp may also have *internal* protection diodes to the supplies (as shown) which conduct at about 0.6V forward drop above or below the respective rails. In this case however, the external Schottky diodes effectively parallel any internal diodes, so the internal units never reach their threshold. Diverting fault currents externally eliminates potential stress, protecting the op amp.

The external diodes also allow other degrees of freedom, some not so obvious. For example, if fault current is allowed to flow in the op amp, R_{LIMIT} must then be chosen so that the maximum current is no more than 5mA for the worst case V_{IN}. This criterion can

result in rather large R_{LIMIT} values, and the associated increase in noise and offset voltage may not be acceptable. For instance, to protect against a V_{IN} of 100V with the 5mA criterion, R_{LIMIT} must be ≥20kΩ. However with external Schottky clamping diodes, this allows R_{LIMIT} to be governed by the maximum allowable D1-D2 current, which can be larger than 5mA. However, care must be used here, for at very high currents the Schottky diode drop may exceed 0.6V, possibly activating internal op amp diodes.

It is very useful to keep the R_{LIMIT} value as low as possible, to minimize offset and noise errors. R_{LIMIT}, in series with the op amp input, produces a bias-current-proportional voltage drop. Left uncorrected, this voltage appears as an increase in the circuit's ffset voltage. Thus for op amps where the bias currents are moderate and approximately equal (most bipolar types) compensation resistor R_{FB} balances the dc effect, and minimizes this error. For low bias current op amps (Ib ≤10nA, or FET types) it is likely R_{FB} won't be necessary. To minimize noise associated with R_{FB}, bypass it with a capacitor, C_F.

Clamping Diode Leakage

For obvious reasons, it is critical that diodes used for protective clamping at an op amp input have a leakage sufficiently low to not interfere with the bias level of the application.

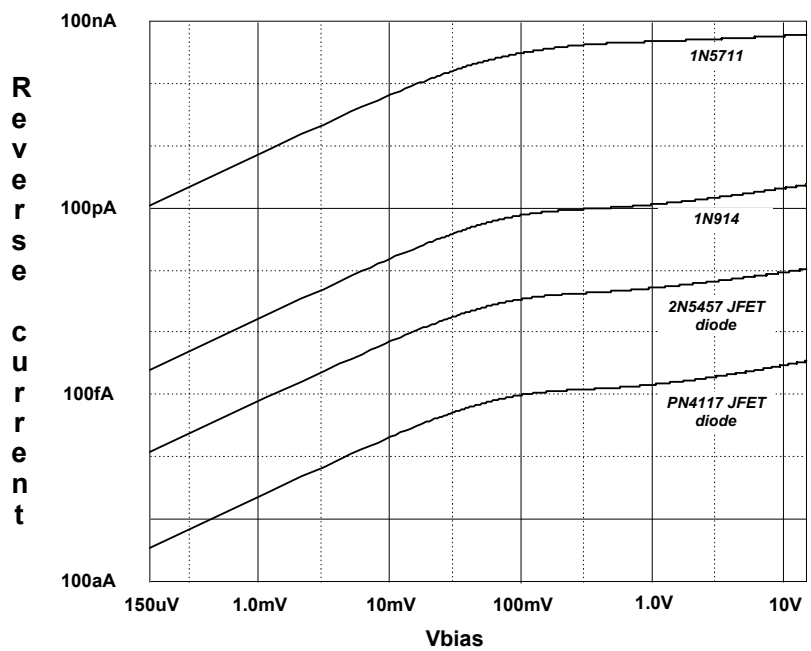


Figure 7-66: *Reverse bias current characteristics for diodes useful in protective clamping networks (PSpice simulation)*

Figure 7-66 illustrates how some well-known diodes differ in terms of leakage current, as a function of the reverse bias voltage, Vbias.

In this chart, a 25°C simulation using PSpice diode models, it is easy to see that not only is the diode type critical, so is the reverse bias. The 1N5711 Schottky type for example, has a leakage of nearly 100nA at a reverse bias of 15V, as it would typically be used with a ±15V powered op amp. With this level of leakage, such diodes will only be useful with

op amps with bias currents of several μA. For protection of appreciably lower bias current op amps (particularly most FET input devices) much lower leakage is necessary.

As the data of Figure 7-66 shows, not only does selecting a better diode help control leakage current, but operating it at a low bias voltage condition reduces leakage substantially. For example, while an ordinary 1N914 or 1N4148 diode may have 200pA of leakage at 15V, this is reduced to slightly more than a pA with bias controlled to 1mV. But there is a caveat here! When used in a high impedance clamp circuit, glass diodes such as the 1N914/1N4148 families should either be shielded from incident light, or use opaque packages. This is necessary to minimize parasitic photocurrent from the surrounding light, which effectively appears as diode leakage current.

Specialty diodes with much lower leakage are also available, such as diode-connected FET devices characterized as protection diodes (see DPAD series of Reference 2). Within the data of Figure 7-66, the 2N5457 is a general purpose JFET, and the 2N4117/PN4117 family consists of parts designed for low current levels. Other low leakage and specialty diodes are described in References 3 and 4.

A Flexible Voltage Follower Protection Circuit

Of course, it isn't a simple matter to effectively apply protective clamping to op amp inputs, while reducing diode bias level to a sub-mV level.

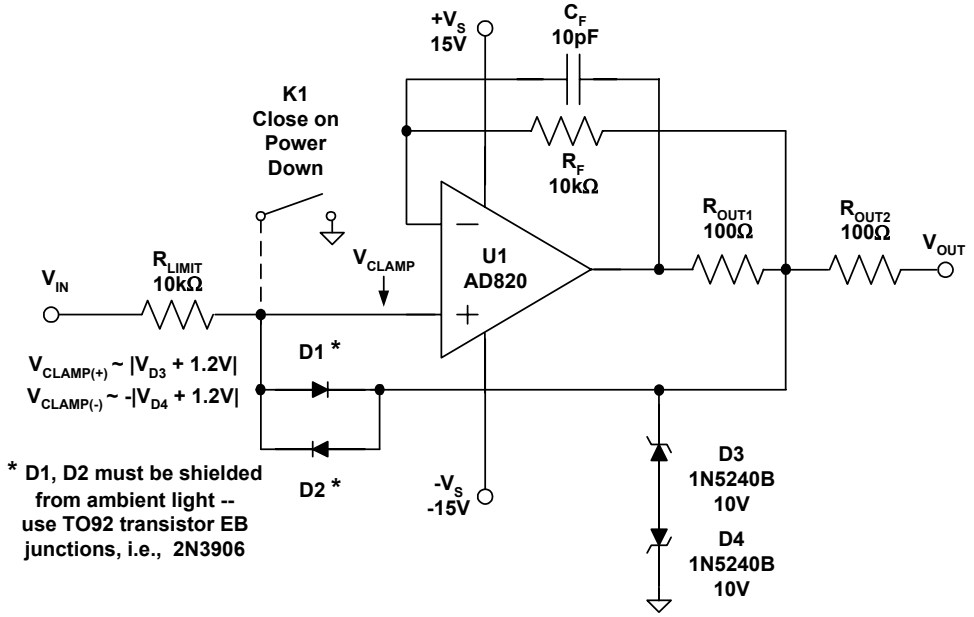


Figure 7-67: *Bootstrapping the D1-D2 protection network reduces diode leakage to negligible levels, and is voltage-programmable for clamp level.*

The circuit of Figure 7-67 shows low-leakage input clamping and other means used with a follower connected FET op amp, with protection at input and output, for both power on or off conditions.

Disregarding the various diodes momentarily, this circuit is an output-current-limited voltage follower. With the addition of diodes D1-D2 and D3-D4, it has both a voltage-

limited output, and an over-voltage protected input. Operating below the voltage threshold of output series-connected zener diodes D3-D4, the circuit behaves as a precision voltage follower. Under normal follower operation, that is at input/output voltages < | V_Z + 0.6 | volts (where V_Z is the breakdown voltage of D3 or D4), diodes D1-D2 see only the combined offset and CM voltage errors of U1 as bias voltage. This reduces the D1-D2 leakage to very low levels, consistent with the pA level bias current of a FET input op amp. Note that D1-D2 *must* be prevented from photo-conduction, and one direct means of this is to use opaque package diodes, such as the 2N3906 EB junctions discussed by Pease (see References 3 and 4). If 1N914s are used they must be light shielded. In either case, bootstrapping greatly reduces the effective D1-D2 leakage.

For input/output voltage levels greater than V_Z + 0.6V, zener diodes D3-D4 breakdown. This action clamps both the V_{OUT} output node and the V_{CLAMP} node via D1-D2. The input of the op amp is clamped to either polarity of the two input levels of V_{CLAMP}, as indicated within the figure. Under clamp conditions, input voltage V_{IN} can rise to levels beyond the supply rails of U1 without harm, with excess current limited by R_{LIMIT}. If sustained high-level (~100V) inputs will be applied, R_{LIMIT} should be rated as a 1-2W (or fusible) type.

This circuit has very good DC characteristics, due to the fact that the clamping network is bootstrapped. This produces very low input/output errors below the V_{CLAMP} threshold (consistent with the op amp specifications, of course). Note that this bootstrapping has ac benefits as well, as it reduces the D1-D2 capacitance seen by the source. While the ~100pF capacitance of D3-D4 might cause a loading problem with some op amps, this is mitigated by the isolating effect of R_{OUT1}, plus the feedback compensation of C_F. Both R_{OUT1} and R_{OUT2} protect the op amp output.

The input voltage clamping level is also programmable, and is set by the choice of zener voltage V_Z. This voltage plus 1.2V should be greater than the maximum input, but below the rail voltage, as summarized in the figure. The example uses 10V±5% zener diodes, so input clamping typically will occur at ±11.2V, allowing ±10V swings.

An important caveat to the above is that it applies for *power on* conditions. With *power off*, D1-D4 still clamp to the noted levels, but this now produces a condition whereby the U1 input and output voltage can exceed the rails.

Note that this could be dangerous, for a given U1 device. If so, an optional and simple means towards providing a lower, safe clamping level for power off conditions is to use a relay at the V_{CLAMP} node. The contacts are open with power applied, and closed with power absent. With attention paid to an overall PCB layout, this can preserve a pA level bias current of FET op amps used for U1.

CM Over-Voltage Protection Using CMOS Channel Protectors

A much simpler alternative for over-voltage protection is the CMOS *channel protector*. A channel protector is a device in series with the signal path, for example preceding an op amp input. It provides over-voltage protection by dynamically altering its resistance under fault conditions. Functionally, it has the distinct advantage of affording protection for sensitive components from voltage transients, whether the power supplies are present or not. Representative devices are the ADG465/ADG466/ADG467, which are channel protectors with single, triple, and octal channel options. Because this form of protection works whether supplies are present or not, the devices are ideal for use in applications where input over-voltages are common, or where correct power sequencing can't always be guaranteed. One such example is within hot-insertion rack systems.

An application of a channel protector for over-voltage protection of a precision buffer circuit is shown in Figure 7-68. A single channel device, the ADG465 at U2, is used here at the input of the U1 precision op amp buffer, an OP777.

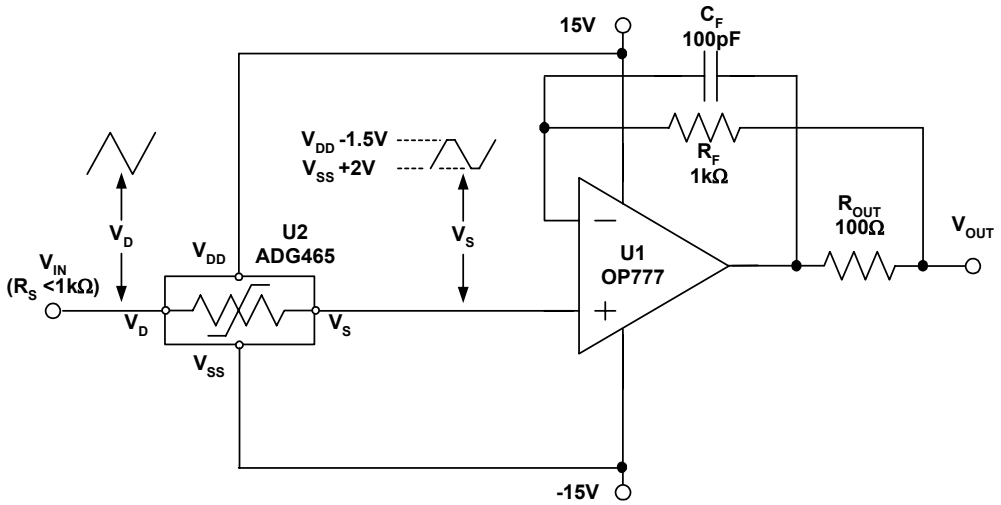


Figure 7-68: *Using an ADG465 channel protector IC with a precision buffer offers great simplicity of protection and fail-safe operation during power off.*

In operation, a channel protector behaves just like a series resistor of 60Ω to 80Ω in normal operation (i.e., non-fault conditions). Consisting of a series connection of multiple P and N MOSFETs, the protector dynamically adjusts channel resistance according to the voltage seen at the V_D terminal. Normal conduction occurs with V_D more than a threshold level above or below the rails, i.e., $(V_{SS} + 2V) < V_D < (V_{DD} – 1.5V)$. For fault conditions the analog input voltage exceeds this range, causing one of the series MOSFETs to switch off, thus raising the channel resistance to a high level. This clamps the V_S output at one extreme range, either $V_{SS} + 2V$ or $V_{DD} – 1.5V$, as shown in Figure 7-68.

A major channel protector advantage is the fact that both circuit and signal source protection are provided, in the event of over-voltage or power loss. Although shown here operating from op amp ±15V supplies, these channel protectors can handle total supplies of up to 40V. They also can withstand over-voltage inputs from $V_{SS} – 20V$ to $V_{DD} + 20V$ with power on (or ±35V in the circuit shown). With power off ($V_{DD} = V_{SS} = 0V$),

maximum input voltage is ±35V. Maximum room temperature channel leakage is 1nA, making them suitable for op amps and in-amps with bias currents of several nA and up.

Related to the ADG46X series of channel protectors are several *fault-protected multiplexers*, for example the ADG508F/509F, and the ADG438F/439F families. Both the channel protectors and the fault-protected multiplexers are low power devices, and even under fault conditions, their supply current is limited to sub microampere levels. A further advantage of the fault-protected multiplexer devices is that they retain proper channel isolation, even for input conditions of one channel seeing an over-voltage, that is the remaining channels still function.

CM Over-Voltage Protection Using High CM Voltage In-Amp

The ultimate simplicity for analog channel over-voltage protection is achieved with resistive input attenuation ahead of a precision op amp. This combination equates to a high voltage capable in-amp, such as the AD629, which is able to linearly process differential signals riding upon CM voltages of up to ±270V. Further, and most important to over-voltage protection considerations, the on-chip resistors afford protection for either common mode or differential voltages of up to ±500V. All of this is achieved by virtue of a precision laser-trimmed thin-film resistor array and op amp, as shown in Figure 7-69.

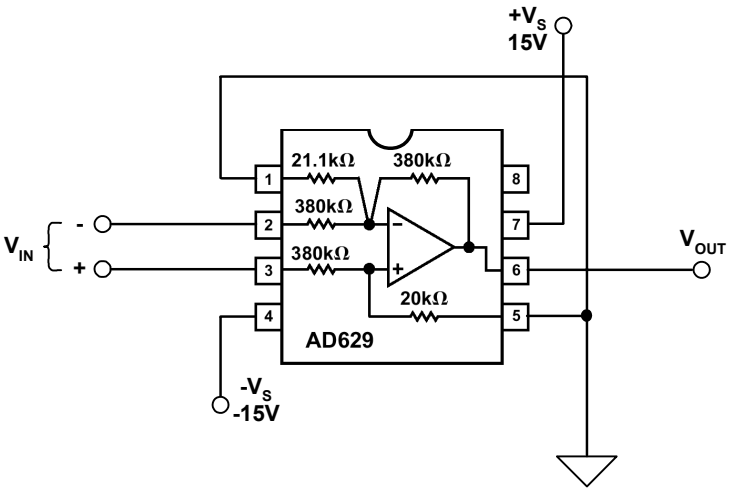


Figure 7-69: *The AD629 high voltage in-amp IC offers ± 500V input over-voltage protection, one-component simplicity, and fail-safe power off operation*

Examination of this topology shows that the resistive network around the AD629's precision op amp acts to divide down the applied CM voltage at V_{IN} by a factor of 20/1. The AD629 simultaneously processes the input differential mode signal V_{IN} to a single-ended output referred to a local ground, at a gain factor of unity. Gain errors are no more than ±0.03 or 0.05%, while offset voltage is no more than 0.5 or 1mV (grade dependent). The AD629 operates over a supply range of ±2.5 to ±18V.

These factors combine to make the AD629 a simple, one-component choice for the protection of off-card analog inputs that can potentially see dangerous transient voltages. Due to the relatively high resistor values used, protection of the device is also inherent with no power applied, since the input resistors safely limit fault currents. In addition, it

offers those operating advantages inherent to an in-amp: high CMR (86dB minimum at 500Hz), excellent overall dc precision, and the flexibility of simple polarity changes.

On the flip side of performance issues, several factors make the AD629's output noise and drift relatively high, if compared to a lower gain in-amp configuration such as the AMP03. These are the Johnson noise of the high value resistors, and the high noise gain of the topology (21x). These factors raise the op amp noise and drift along with the resistor noise by a factor higher than typical. Of course, whether or not this is an issue relevant to an individual application will require evaluation on a case-by-case basis.

Inverting mode op amp protection schemes

There are some special cases of over-voltage protection requirements that don't fit into the more general CM protection schemes above. Figure 7-70 is one such example, a low bias current FET input op amp I/V converter.

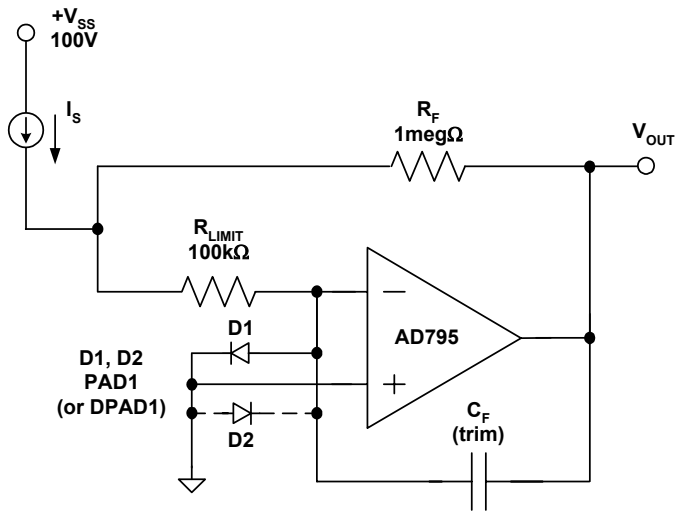


Figure 7-70: *A low bias current FET input op amp I/V converter with over-voltage protection network R_{LIMIT} and D1*

In this circuit the AD795 1pA bias current op amp is used as a precision inverter. Some current-source nature signals can originate from a high voltage potential, such as the 100V V_{SS} level shown. As such, they have the potential of developing fault voltage levels beyond the op amp rails, producing fault current into the op amp well above safe levels. To prevent this, protection resistor R_{LIMIT} is used inside the feedback loop as shown, along with voltage clamp D1 (D2).

For normal signal condition (i.e., $I_S \leq 10uA$) the op amp's inverting node is very close to ground, with just a tiny voltage drop across R_{LIMIT}. Normal I/V conversion takes place, with gain set by R_F. For protection, D1 is a special low leakage diode, clamping any excess voltage at the (-) node to ~0.6V, thus protecting the op amp. The value of R_{LIMIT} is chosen to allow a 1mA max current under fault conditions. Bootstrapping the D1 (and/or D2) clamp diodes as shown minimizes the normal operating voltage across the inverting node, keeping the diode leakage low (see Figure 7-66, again). Note that for a positive source voltage as shown, only positive clamping is needed, so just one diode suffices.

Only the lowest leakage diodes (≤1pA) such as the PAD1 (or the DPAD1 dual) should be used in this circuit. As noted previously, any clamping diode used here should either be shielded from light (or use opaque packaging), to minimize photocurrent from ambient light. Even so, the diode(s) will increase the net input current and shunt capacitance, and feedback compensation C_F will likely be necessary to control response peaking. C_F should be a very low leakage type. Also, with the use of very low input bias current devices such as the AD795, it isn't possible to use the same level of internal protection circuitry as with other ADI op amps. This factor makes the AD795 more sensitive to handling, so ESD precautions should be taken.

Amplifier Output Voltage Phase-Reversal

As alluded to above, there are "gray-area" op amp groups that have anomalous CM voltage zones, falling between the supply rails. As such, protection for these devices cannot be guaranteed by simply ensuring that the inputs stay between the rails— they must additionally stay *entirely* within their rated CM range, for consistent behavior.

Peculiar to some op amps, this misbehavior phenomenon is called *output voltage phase-reversal.* It is seen when one or both of the op amp inputs exceeds their allowable input CM voltage range. Note that the inputs may still be well within the extremes of rail voltage, but simply below one specified CM limit. Typically, this is towards the negative range. Phase-reversal is most often associated with JFET and/or BiFET amplifiers, but some bipolar single-supply amplifiers are also susceptible to it.

The Figure 7-71 waveforms illustrates this general phenomenon, with an overdriven voltage follower input on the left, and the resulting output phase-reversal at the right.

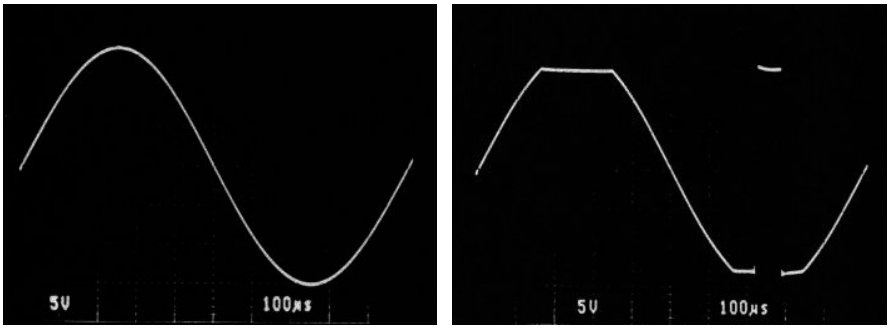


Figure 7-71: *An illustration of input overdriving waveform (left) and the resulting output phase-reversal (right), using a JFET input op amp*

While the specific details of the internal mechanism may vary with individual op amps, it suffices to say that the output phase-reversal occurs when a critical section of the amplifier front end saturates, causing the input-output sign relationship to temporarily reverse. Under this condition, when the CM range is exceeded, the negative going input waveform in Figure 7-71 (left) does not continue going more negative in the output waveform, Figure 7-71 (right). Instead, the input-output relationship *phase-reverses*, with the output suddenly going positive, i.e., the spike. It is important to note that this is *not* a latching form of phase-reversal, as the output will once again continue to properly track

the input, when the input returns to the CM range. In Figure 7-71, this can be seen in the continuance of the output sine wave, after the positive-going phase-reversal spike settles.

In most applications, this output voltage phase-reversal does no harm to the op amp, nor to the circuit where it is used. Indeed, since it is triggered when the CM limit is exceeded, non-inverting stages with appreciable signal gain never see it, since their applied CM voltage is too small.

Note that with inverting applications the output phase-reversal problem is non-existent, as the CM range isn't exercised. So, although a number of (mostly older) op amps suffer from phase-reversal, it still is rarely a serious problem in system design.

Nevertheless, when and if a phase-reversal susceptible amplifier used in a servo loop application sees excess CM voltage, the effect can be disastrous— it goes **Bang!** So, the best advice is to be forewarned.

An Output Phase-Reversal Do-it-Yourself Test

Since output phase-reversal may not always be fully described on a data sheet, it is quite useful to test for it. This is easily done in the lab, by driving a questionable op amp as a unity-gain follower, from a source impedance (R_{LIMIT}) of ~1kΩ. It is helpful to make this a variable, 1-100kΩ range resistance.

With a low resistance setting (1kΩ), while bringing the driving signal level slowly up towards the rail limits, observe the amplifier output. If a phase-reversal mechanism is present, when the CM limit of the op amp is exceeded, the output will suddenly reverse (see Figure 7-71, right, again). If there is no phase-reversal present in an amplifier, the output waveform will simply clip at the limits of its swing. It may prove helpful to have a well-behaved op amp available for this test, to serve as a performance reference. One such device is the AD8610.

Note that in general, some care should be used with this test. Without a series current-limit resistor, if the generator impedance is too low (or level too high), it could possibly damage an internal junction of the op amp under test. So, obviously, caution is best for such cases.

Once a suitable R_{LIMIT} resistance value is found, well-behaved op amps will simply show a smooth, bipolar range, clipped output waveform when overdriven. This clipping will appear more like the *upper (positive swing)* portion of the waveform within Fig. 7-71, right (again).

Fixes For Output Phase–Reversal

An op amp manufacturer might not always give the R_{LIMIT} resistance value appropriate to prevent output phase-reversal. But, the value can be determined empirically with the driving method mentioned above. Most often, the R_{LIMIT} resistor value providing protection against phase-reversal will also safely limit fault current through any input CM clamping diodes. If in doubt, a nominal value of 1kΩ is a good starting point for testing.

Typically, FET input op amps will need only the current limiting series resistor for protection, but bipolar input devices are best protected with this same limiting resistor, *along with a Schottky diode* (i.e., R_{LIMIT} and D2, of Figure 7-65, again).

For a more detailed description of the output voltage phase-reversal effect, see References 7 and 8. Figure 7-72 summarizes a number of the key points relating to output voltage phase-reversal.

Alternately, any of the several previously mentioned CM clamping schemes can be used to prevent output phase-reversal, by setting the clamp voltage to be less than the amplifier CM range limit where phase-reversal occurs. For example, Figure 7-67 would operate to prevent phase-reversal in FET amplifiers susceptible to it, if the negative clamp limit is set so that $V_{CLAMP(-)}$ never exceeds the typical negative CM range of –11V on a –15V rail.

- ***Non-Latching* Inversion of Transfer Function, Triggered by Exceeding Common Mode Limit**
- **Sometimes Occurs in FET and Bipolar (Single-Supply) Op Amps**
- **Doesn't Harm Amplifier… but *Disastrous* for Servo Systems!**
- **Not Usually Specified on Data Sheet, so Amplifier Must be Checked**
- **Easily Prevented:**
  - **All op amps: Limit applied CM voltage by clamping or other means**
  - **BiFETs: Add series input resistance, R_{LIMIT}**
  - **Bipolars: R_{LIMIT} and Schottky clamp diode to rail**

Figure 7-72: *A summary of key points regarding output phase-reversal in FET and bipolar input op amps*

For validation of this or any of the previous over-voltage protection schemes, the circuit should be verified on a number of op amps, over a range of conditions as suitable to the final application environment.

Input Differential Protection

The discussions thus far have been on over-voltage common-mode conditions, which is typically associated with forward biasing of PN junctions inherent in the structure of the input stage. There is another equally important aspect of protection against over-voltage, which is that due to excess *differential* voltages. Excessive differential voltage, when applied to certain op amps, can lead to degradation of their operating characteristics.

This degradation is brought about by *reverse junction breakdown,* a second case of undesirable input stage conduction, occurring under conditions of *differential* over-voltage. However, in the case of reverse breakdown of a PN junction, the problem can be more subtle in nature. It is illustrated by the partial op amp input stage in Figure 7-73.

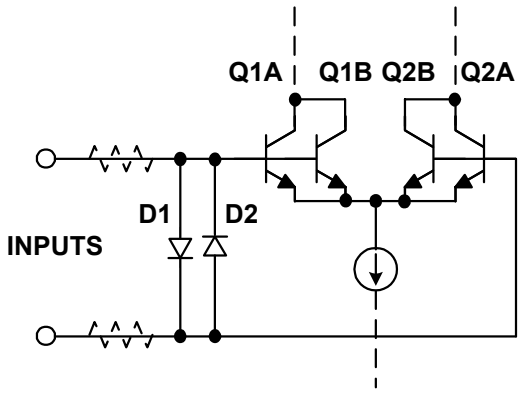


Figure 7-73: *An op amp input stage with D1-D2 input differential over-voltage protection network*

This circuit, applicable to a low noise op amp such as the OP27, is also typical of many others using low noise bipolar transistors for differential pair Q1-Q2. In the absence of any protection, it can be shown that voltages above about 7V between the two inputs will cause a reverse junction breakdown of either Q2 or Q1 (dependent upon relative polarity). Note that, in cases of E-B breakdown, even small reverse currents can cause degradation in both transistor gain and noise (see Reference 6). After E-B breakdown occurs, op amp parameters such as the bias currents and noise may well be out of specification. This is usually permanent, and it can occur gradually and quite subtly, particularly if triggered by transients. For these reasons, virtually all low-noise op amps, whether NPN or PNP based, utilize protection diodes such as D1-D2 across the inputs. These diodes conduct for applied voltages greater than ±0.6V, protecting the transistors.

The dotted series resistors function as current limiters (protection for the protection diodes) but aren't used in all cases. For example, the AD797 doesn't have the resistors, simply because they would degrade the part's specified noise of 1nV/√Hz. Note— when the resistors are absent internally, some means of external current limiting must be provided, when and if differential over-voltage conditions do occur. Obviously, this is a tradeoff situation, so the confidence of full protection must be weighed against the noise degradation. Note that an application circuit itself may provide sufficient resistance in the op amp inputs, such that additional resistance isn't needed.

In applying a low noise bipolar input stage op amp, first check the chosen part's data sheet for internal protection. When necessary, protection diodes D1-D2, if not internal to the op amp, should be added to guarantee prevention of Q1-Q2 E-B breakdown. If differential transients of more than 5V can be seen by the op amp in the application, the diodes are in order. Ordinary low capacitance diodes will suffice, such as the 1N4148 family. Add current limiting resistors as necessary, to limit diode current to safe levels.

Other IC device junctions, such as base-collector and JFET gate-source junctions don't exhibit the same degradation in performance upon break down, and for these the input current should be limited to 5mA, unless the data sheet specifies a different value.

Protecting In-Amps Against Over-Voltage

From a protection standpoint, instrumentation amplifiers (in-amps) are similar in many ways to op amps. Like op amps, their absolute maximum ratings must be observed for both common and differential mode input voltages.

A much simplified schematic of the AD620 in-amp is shown in Figure 7-74, showing the input differential transistors and their associated protection parts.

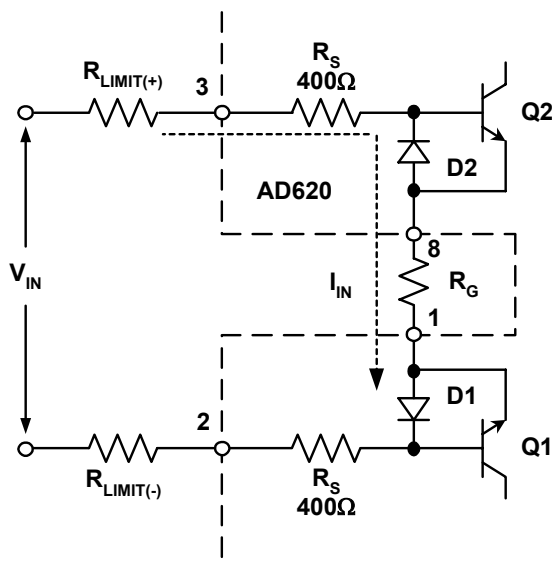


Figure 7-74: *The AD620 in-amp input internally uses D1-D2 and series resistors R_S for protection (additional protection can be added externally)*

An important point, unique to the AD620 device, is the fact that the 400Ω internal R_S protection resistors are *thin-film types*. Therefore these resistors don't show symptoms of diode-like conduction to the IC substrate (as would be the case were they diffused resistors). Practically, this means that the input ends of these resistors (pins 3 and 2) can go above or below the supplies. Differential fault currents will be limited by the combination of twice the internal R_S plus the external gain resistance, R_G. Excess applied CM voltages will show current limited by R_S.

In more detail, it can be noted that input transistors Q1 and Q2 have protection diodes D1 and D2 across their base-emitter junctions, to prevent reverse breakdown. For differential voltages, analysis of shows that a fault current, I_{IN}, flows through the external R_{LIMIT}

resistors (if present), the internal R_S resistors, the gain-setting resistor R_G, and two diode drops (Q2, D1). For the AD620 topology, R_G varies inversely with gain, and a worst case (lowest resistance) occurs with the maximum gain of 1000, when R_G is 49.9Ω. Therefore the lowest total internal path series resistance is about 850Ω.

For the AD620, any combination of CM and differential input voltages should be limited to levels that limit the input fault current to 20mA, maximum. A purely differential voltage of 17V would result in this current level, for the lowest resistance case. For CM voltages which may go beyond either rail, an internal diode not shown in Fig. 7-74 conducts, effectively clamping the driven input to either $+V_S$ or $-V_S$ at the R_S inner end. For this over-voltage CM condition, the 400Ω value of R_S and the excess voltage beyond the rail determines the current level. If for example V_{IN} is 23V with $+V_S$ at 15V, 8V appears across R_S, and the 20mA current rating is reached. Higher fault voltages can be dealt with by adding R_{LIMIT} resistance, to maintain fault current at 20mA or less.

A more generalized external voltage protection circuit for an in-amp like the AD620 is shown in Figure 7-75.

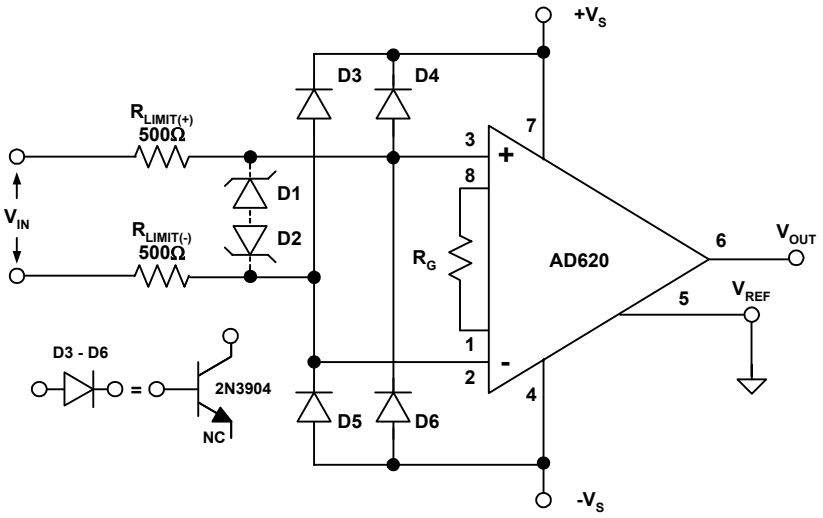


Figure 7-75: *A generalized diode protection circuit for the AD620 and other in-amps uses D3-D6 for CM clamping and series resistors R_{LIMIT} for protection*

In this circuit, low-leakage diodes D3-D6 are used as CM clamps. Since the in-amp bias current may be only 1nA or so (for the AD620), a low-leakage diode type is mandatory. As can be noted from the topology, diode bootstrapping isn't possible with this configuration.

It should be noted that not only must the diodes have basically low leakage, they must also maintain low leakage at the highest expected temperature. This suggests either FET type diodes (see Fig. 7-66, again), or the transistor C-B types shown. The R_{LIMIT} resistors are chosen to limit the maximum diode current under fault conditions. If additional *differential* protection is used, either back-back zener or Transzorb clamps can be used, shown as D1-D2. If this is done, leakage of these diodes should be carefully considered.

The protection scheme of Figure 7-75, while effective using appropriate parts, has the downside of being busy for components. A much more simple in-amp protection using fault protected devices is shown in Figure 7-76. Although shown with an AD620, this circuit is useful with many other dual-supply in-amps with bias currents of 1nA or more. It uses two-thirds of a triple ADG466 channel-protector for the in-amp differential inputs.

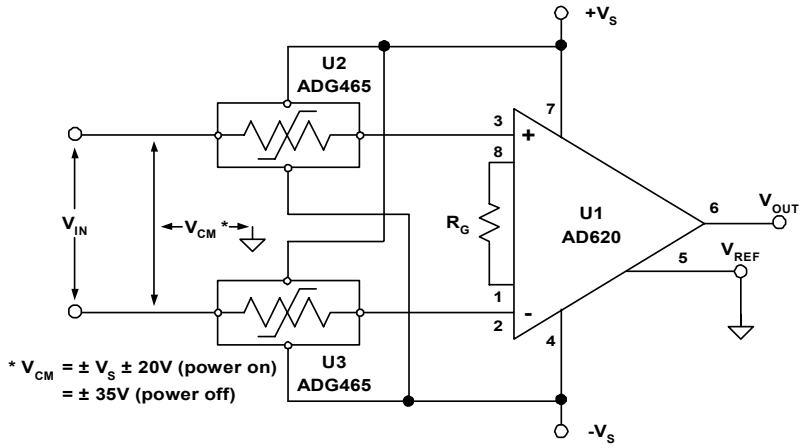


Figure 7-76: *A channel protector device (or fault-protected multiplexer) provides protection for dual-supply in-amps with a minimum of extra parts*

Because the nature of a channel protection device is to turn off as V_{IN} approaches either rail, the scheme of Figure 7-76 doesn't function with rail sensing single-supply in-amps. If near-rail operation and protection is required in an in-amp application, an alternative method is necessary. Many single-supply in-amps are topologically similar to the two-amplifier in-amp circuit which is shown within the dotted box of Figure 7-77.

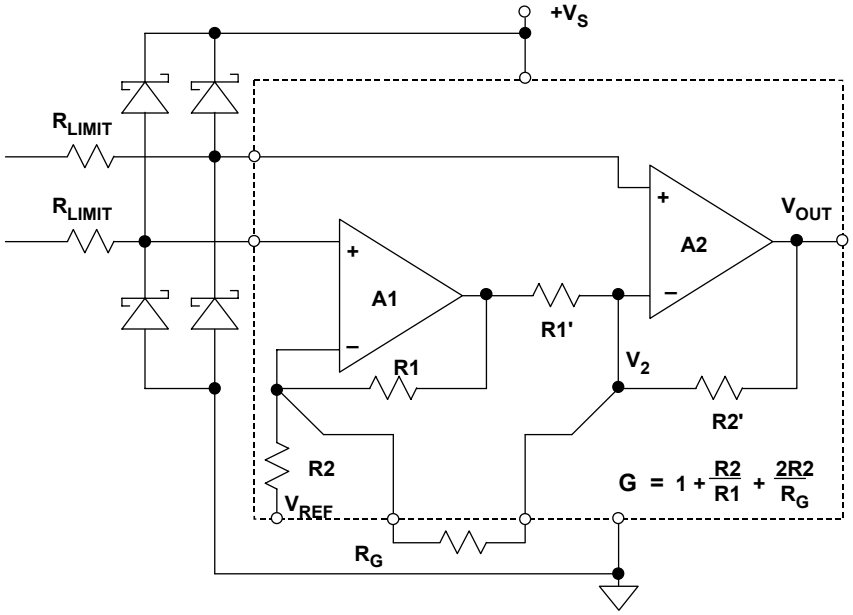


Figure 7-77: *Single-supply in-amps may or may not require external protection in the form of resistors and clamp diodes— if so, they can be added as shown*

In terms of the necessity for externally added protection components, a given in-amp may or may not require them. Each case needs to be considered individually. For example,

some in-amps have clamp diodes as shown, but *internal to the device*. The AD623 is such a part, but it lacks the series resistors, which can be added externally when and if necessary. Note that this approach allows the R_{LIMIT} value to be optimized for protection, with negligible impact on noise for those applications not needing the protection.

Also, some in-amp devices have both internal protection resistors *and* clamping diodes, an example here is the AD627. In this device, the internal protection is adequate for transients up to 40V beyond the supplies (a 20mA fault current in the internal resistors). For over-voltage levels higher than this, external R_{LIMIT} resistors can be added.

The use of the Schottky diodes as shown at the two inputs is an option for in-amp protection. If no clamping is specifically provided internally, then they are applicable. Their use is generally similar to the op amp protection case of Figure 7-65, with comparable caveats as far as leakage. Note that in many cases, due to internal protection networks of modern in-amps, these diodes just won't be necessary. But again, there aren't hard rules on this, so always check the data sheet before finalizing an application.

To summarize, Figure 7-78 reviews the major points of the in-circuit over-voltage issues discussed in this section.

- **INPUT VOLTAGES MUST NOT EXCEED ABSOLUTE MAXIMUM RATINGS (Usually Specified With Respect to Supply Voltages)**
- **Requires $V_{IN(CM)}$ Stay Within a Range Extending to ≤0.3V Beyond Rails ($-V_S-0.3V \geq V_{IN} \leq +V_S+0.3V$)**
- **IC Input Stage Fault Currents *Must* Be Limited (≤ 5mA Unless Otherwise Specified)**
- **Avoid Reverse-Bias Breakdown in Input Stage Junctions!**
- **Differential and Common Mode Ratings Often Differ**
- **No Two Amplifiers are Exactly the Same**
- **Watch Out for Output Phase-Reversal in JFET and SS Bipolar Op Amps!**
- **Some ICs Contain *Internal* Input Protection**
  - **Diode Voltage Clamps, Current Limiting Resistors (or both)**
  - **Absolute Maximum Ratings Must Still Be Observed**

Figure 7-78: *A summary of in-circuit over-voltage points*

If these varied over-voltage precautions for op amps and in-amps seem complex, yes indeed, they are! Whenever op amp (or in-amp) inputs (and outputs) go outside equipment boundaries, dangerous or destructive things can happen to them. Obviously, these potentially hazardous situations should be anticipated, for highest reliability.

Fortunately, most applications are contained entirely within the equipment, and usually see inputs and outputs to/from other ICs on the same power system. Therefore clamping and protection schemes typically aren't necessary for these cases.

Out-of-Circuit Over-Voltage Protection

Linear ICs such as op amps and in-amps must also be protected prior to the time that they are mounted to a printed circuit board, that is an *out-of-circuit* state. In such a condition, ICs are completely at the mercy of their environment as to what stressful voltage surges they may see. Most often the harmful voltage surges come from *electrostatic discharge,* or, as more commonly referenced, ESD. This is a single, fast, high current transfer of electrostatic charge resulting from one of two conditions. These conditions are:

1) *Direct contact transfer between two objects at different potentials (sometimes called contact discharge)*

2) *A high electrostatic field between two objects when they are in close proximity (sometimes called air discharge)*

The prime sources of static electricity are mostly insulators and are typically synthetic materials, e.g., vinyl or plastic work surfaces, insulated shoes, finished wood chairs, Scotch tape, bubble pack, soldering irons with ungrounded tips, etc. Voltage levels generated by these sources can be extremely high since their charge is not readily distributed over their surfaces or conducted to other objects.

- **Walking Across a Carpet**
  1000V - 1500V
- **Walking Across a Vinyl Floor**
  150V - 250V
- **Handling Material Protected by Clear Plastic Covers**
  400V - 600V
- **Handling Polyethylene Bags**
  1000V - 2000V
- **Pouring Polyurethane Foam Into a Box**
  1200V - 1500V
- **Note: Above Assumes 60% RH. For Low RH (30%), Voltages Can Be > 10 Times**

Figure 7-79: *ESD voltages generated by various ordinary circumstances*

The generation of static electricity caused by rubbing two substances together is called the *triboelectric* effect. Some common examples of ordinary acts producing significant ESD voltages are shown in Figure 7-79.

ICs can be damaged by the high voltages and high peak currents generated by ESD. Precision analog circuits, often featuring very low bias currents, are more susceptible to damage than common digital circuits, because traditional input-protection structures which protect against ESD damage increase input leakage— and thus can't be used.

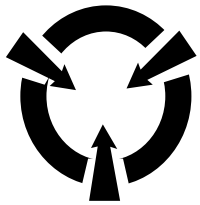
For the design engineer or technician, the most common manifestation of ESD damage is a catastrophic failure of the IC. However, exposure to ESD can also cause increased leakage or degrade other parameters. If a device appears to not meet a data sheet specification during evaluation, the possibility of ESD damage should be considered. Figure 7-80 outlines some relevant points on ESD induced failures.

- **ESD Failure Mechanisms:**
  - **Dielectric or junction damage**
  - **Surface charge accumulation**
  - **Conductor fusing**
- **ESD Damage Can Cause:**
  - **Increased leakage**
  - **Degradation in performance**
  - **Functional failures of ICs**
- **ESD Damage is often Cumulative:**
  - **For example, each ESD "zap" may increase junction damage until, finally, the device fails.**

Figure 7-80: *Understanding ESD damage*

All ESD-sensitive devices are shipped in protective packaging. ICs are usually contained in either conductive foam or antistatic shipping tubes, and the container is then sealed in a static-dissipative plastic bag. The sealed bag is marked with a distinctive sticker, such as in Figure 7-81, which outlines the appropriate handling procedures.

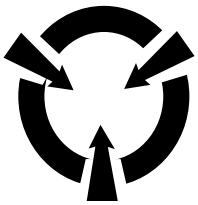
All static sensitive devices are sealed in protective packaging and marked with special handling instructions



CAUTION

SENSITIVE ELECTRONIC DEVICES

DO NOT SHIP OR STORE NEAR STRONG ELECTROSTATIC, ELECTROMAGNETIC, MAGNETIC, OR RADIOACTIVE FIELDS



CAUTION

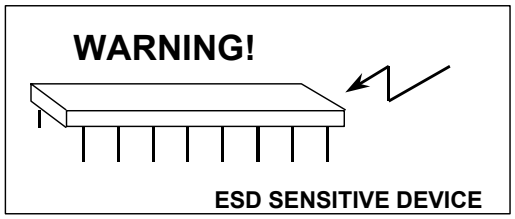
SENSITIVE ELECTRONIC DEVICES

DO NOT OPEN EXCEPT AT APPROVED FIELD FORCE PROTECTIVE WORK STATION

Figure 7-81: *Recognizing ESD-sensitive devices by package and labeling*

The presence of outside package notices such as those shown in Figure 7-81 is notice to the user that device handling procedures appropriate for ESD protection are necessary.

In addition, data sheets for ESD-sensitive ICs generally have a bold statement to that effect, as shown in Figure 7-82.



CAUTION

ESD (Electrostatic Discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADXXX features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

Figure 7-82: *ESD data sheet statement for linear ICs*

Once ESD-sensitive devices are identified, protection is relatively easy. Obviously, keeping ICs in their original protective packages as long as possible is a first step. A second step is discharging potentially damaging ESD sources before IC damage occurs. Discharging such voltages can be done quickly and safely, through a high impedance.

A key component required for ESD-safe IC handling is a workbench with a static-dissipative surface, shown in the workstation of Figure 7-83. The surface is connected to ground through a 1MΩ resistor, which dissipates any static charge, while protecting the user from electrical ground fault shock hazards. If existing bench tops are nonconductive, a static-dissipative mat should be added, along with the discharge resistor.

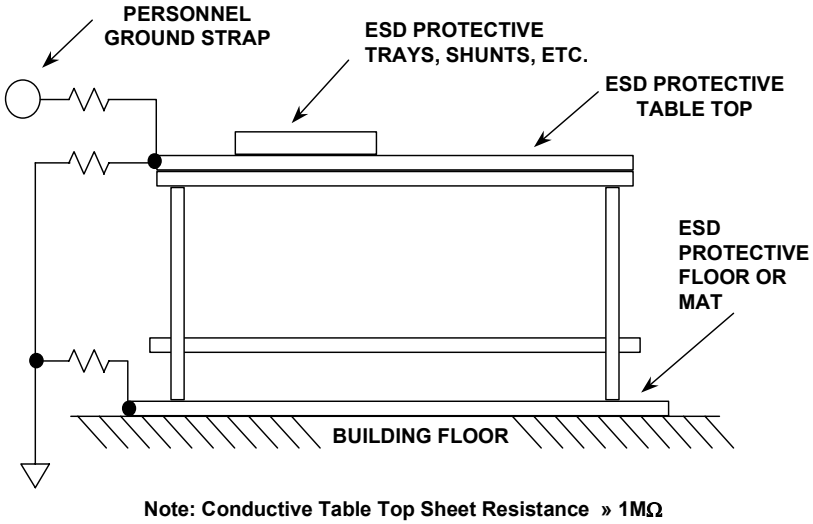


Figure 7-83: *A workstation environment suitable for handling ESD-sensitive ICs*

Note that the surface of the workbench has a moderately high sheet resistance. It is neither necessary nor desirable to use a low-resistance surface (such as a sheet of copper-clad PC board) for the work surface. Remember, a high peak current may flow if a charged IC is discharged through a low impedance. This is precisely what happens when

a charged IC contacts a grounded copper clad board. When the same charged IC is placed on the high impedance surface of Figure 7-83 however, the peak current isn't high enough to damage the device.

Several personnel handling techniques are keys to minimizing ESD-related damage. At the workstation, a conductive wrist strap is recommended while handling ESD-sensitive devices. The wrist strap ensures that normal tasks, such as peeling tape from packages, won't cause IC damage. Again, a 1MΩ resistor, from the wrist strap to ground, is required for safety. When building prototype breadboards or assembling PC boards which contain ESD-sensitive ICs, all passive components should be inserted and soldered before the ICs. This minimizes the ESD exposure of the sensitive devices. The soldering iron must, of course, have a grounded tip.

Protecting ICs from ESD requires the participation of both the IC manufacturer and the customer. IC manufacturers have a vested interest in providing the highest possible level of ESD protection for their products. IC circuit designers, process engineers, packaging specialists and others are constantly looking for new and improved circuit designs, processes, and packaging methods to withstand or shunt ESD energy.

ANALOG DEVICES:

- **Circuit Design and Fabrication -**
  ↓ **Design and manufacture products with the highest level of ESD**
  ↓ **protection consistent with required analog and digital performance.**
- **Pack and Ship -**
  ↓ **Pack in static dissipative material. Mark packages with ESD warning.**

CUSTOMERS:

- **Incoming Inspection -**
  ↓ **Inspect at grounded workstation. Minimize handling.**
- **Inventory Control -**
  ↓ **Store in original ESD-safe packaging. Minimize handling.**
- **Manufacturing -**
  ↓ **Deliver to work area in original ESD-safe packaging. Open packages only at**
  ↓ **grounded workstation. Package subassemblies in static dissipative packaging.**
- **Pack and Ship -**
  Pack in static dissipative material if required. Replacement or optional boards may require special attention.

Figure 7-84: *ESD protection requires a partner relationship between ADI and the end customer with control at key points*

A complete ESD protection plan, however, requires more than building ESD protection into ICs. The users of ICs must also provide their employees with the necessary knowledge of and training in ESD handling procedures, so that protection can be built in at all key points along the way, as outlined in Figure 7-84.

Special care should be taken when breadboarding and evaluating ICs. The effects of ESD damage can be cumulative, so repeated mishandling of a device can eventually cause a failure. Inserting and removing ICs from a test socket, storing devices during evaluation, and adding or removing external components on the breadboard should all be done while

observing proper ESD precautions. Again, if a device fails during a prototype system development, repeated ESD stress may be the cause.

The key word to remember with respect to ESD is *prevention*. There is no way to undo ESD damage, or to compensate for its effects.

ESD Models and Testing

Some applications have higher sensitivity to ESD than others. ICs which are located on a PC board surrounded by other circuits are generally much less susceptible to ESD damage than circuits which must interface with other PC boards or the outside world. These ICs are generally not specified or guaranteed to meet any particular ESD specification (with the exception of MIL-STD-883 Method 3015 classified devices). A good example of an ESD-sensitive interface is the RS-232 interface port ICs on a computer, which can easily be exposed to excess voltages. In order to guarantee ESD performance for such devices, the test methods and limits must be specified.

A host of test waveforms and specifications have been developed to evaluate the susceptibility of devices to ESD. The three most prominent of these waveforms currently in use for semiconductor or discrete devices are: The Human Body Model (HBM), the Machine Model (MM), and the Charged Device Model (CDM). Each of these models represents a fundamentally different ESD event, consequently, correlation between the test results for these models is minimal.

- **IEC1000-4 Electromagnetic Compatibility EMC**
- **IEC1000-4-1 Overview of Immunity Tests**
- **IEC1000-4-2 Electrostatic Discharge Immunity (ESD)**
- **IEC1000-4-3 Radiated Radio-Frequency Electromagnetic Field Immunity**
- **IEC1000-4-4 Electrical Fast Transients (EFT)**
- **IEC1000-4-5 Lightening Surges**
- **IEC1000-4-6 Conducted Radio Frequency Disturbances above 9kHz**
- **Compliance Marking: CE**

Figure 7-85: *A listing of the IEC standards applicable to ESD specifications and testing procedures*

Since 1996, all electronic equipment sold to or within the European Community must meet Electromechanical Compatibility (EMC) levels as defined in specification IEC1000-4-x. Note that this does not apply to individual ICs, *but to the end equipment.* These standards are defined along with test methods in the various IEC1000 specifications, and are listed in Figure 7-85.

IEC1000-4-2 specifies compliance testing using two coupling methods, *contact discharge* and *air-gap discharge*.

Contact discharge calls for a direct connection to the unit being tested. Air-gap discharge uses a higher test voltage, but does not make direct contact with the unit under test. With air discharge, the discharge gun is moved toward the unit under test, developing an arc across the air gap, hence the term air discharge. This method is influenced by humidity, temperature, barometric pressure, distance and rate of closure of the discharge gun. The contact-discharge method, while less realistic, is more repeatable and is gaining acceptance in preference to the air-gap method.

Although very little energy is contained within an ESD pulse, the extremely fast risetime coupled with high voltages can cause failures in unprotected ICs. Catastrophic destruction can occur immediately as a result of arcing or heating. Even if catastrophic failure does not occur immediately, the device may suffer from parametric degradation, which may result in degraded performance. The cumulative effects of continuous exposure can eventually lead to complete failure.

I-O lines are particularly vulnerable to ESD damage. Simply touching or plugging in an I-O cable can result in a static discharge that can damage or completely destroy the interface product connected to the I-O port (such as RS-232 line drivers and receivers).

Traditional ESD test methods such as MIL-STD-883B Method 3015.7 do not fully test a product's susceptibility to this type of discharge. This test was intended to test a product's susceptibility to ESD damage during handling. Each pin is tested with respect to all other pins. There are some important differences between the MIL-STD-883B Method 3015.7 test and the IEC test, noted as follows:

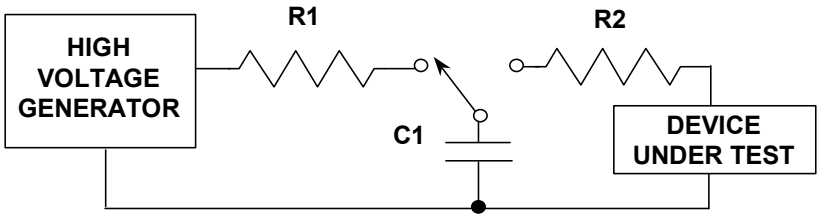
1) The IEC test is much more stringent in terms of discharge energy. The peak current injected is over four times greater.

2) The current risetime is significantly faster in the IEC test.

3) The IEC test is carried out while power is applied to the device.

It is possible that ESD discharge could induce latch-up in the device under test. This test is therefore more representative of a real-world I-O discharge where the equipment is operating normally with power applied. For maximum confidence, however, both tests should be performed on interface devices, thus ensuring maximum protection both during handling, and later, during field service.

A comparison of the test circuit values for the IEC1000-4-2 model versus the MIL-STD-883B Method 3015.7 Human Body Model is shown in Figure 7-86.

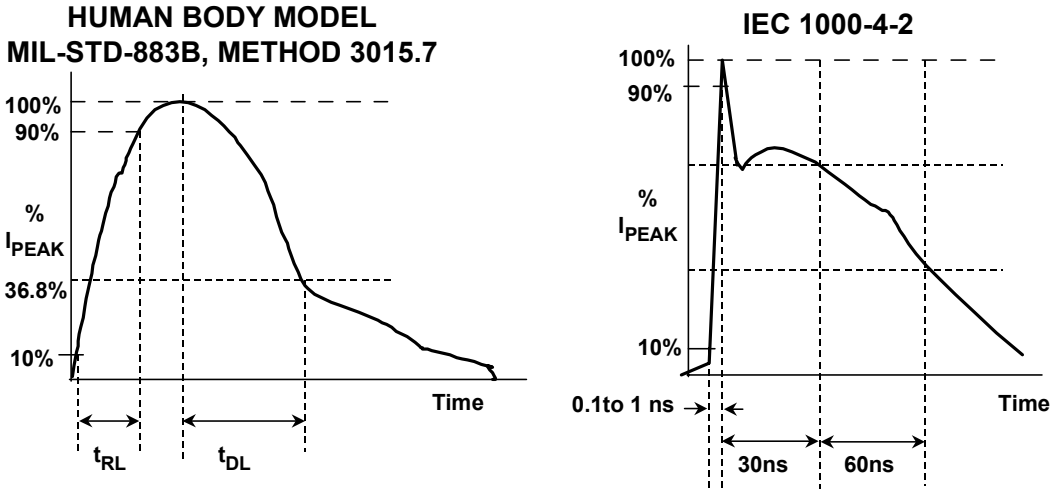


ESD TEST METHOD	R2	C1
Human Body Model MIL STD 883B Method 3015.7	1.5kΩ	100pF
IEC 1000-4-2	330Ω	150pF

NOTE: CONTACT DISCHARGE VOLTAGE SPEC FOR IEC 1000-4-2 IS ±8kV

Figure 7-86: *ESD test circuits and values*

The ESD waveforms for the MIL-STD-883B, METHOD 3015.7 and IEC 1000-4-2 tests are compared in Figure 7-87, left and right, respectively.



- Voltage : 8 kV
- Peak Current :
  - MIL-883B, Method 3015.7 HBM : 5 A
  - IEC 1000-4-2 : 25 A

Figure 7-87: *ESD test waveforms*

Suitable ESD-protection design measures are relatively easy to incorporate, and most of the over-voltage protection methods already discussed in this section will help. Additional protection can also be obtained. For RS-232 and RS-485 drivers and receivers, the ADMXXX-E series is supplied with guaranteed 15kV (HBM) ESD specifications.

For more general uses, the addition of TransZorbs at appropriate places in a system can provide protection against ESD (see References).

Figure 7-88 summarizes the major points about ESD prevention, from both an out-of-circuit as well as an in-circuit perspective.

- **Observe all Absolute Maximum Ratings on Data Sheet!**
- **Read ADI AN-397 (See Reference 16)**
- **Purchase ESD-Specified Digital Interface Devices**
  - **ADMXXX-E Series of RS-232 / RS-485 Drivers / Receivers (See Reference 18)**
- **Follow General Over-voltage Protection Recommendations**
  - **Add Series Resistance to Limit Currents**
  - **Add Zeners or Transient Voltage Suppressors (TVS) for Extra Protection (See Reference 19)**

Figure 7-88: *A summary of ESD points*

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11. MIL-STD-883 Method 3015, "Electrostatic Discharge Sensitivity Classification." Available from Standardization Document Order Desk, 700 Robbins Ave., Building #4, Section D, Philadelphia, PA, 19111-5094.

12. EIAJ ED-4701 Test Method C-111, "Electrostatic Discharges." Available from the Japan Electronics Bureau, 250 W 34th St., New York NY 10119, Attn.: Tomoko.

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14. ESD Association Draft Standard DS5.3 for "Electrostatic Discharge (ESD) Sensitivity Testing - Charged Device Model (CDM) Component Testing." Available from the ESD Association, Inc., 200 Liberty Plaza, Rome, NY 13440.

15. **ESD Prevention Manual**, Analog Devices, Inc.

16. Niall Lyne, "Electrically Induced Damage to Standard Linear Integrated Circuits: The Most Common Causes and the Associated Fixes to Prevent Reoccurrence," **Analog Devices AN397**.

17. Mike Bryne, "How to Reliably Protect CMOS Circuits Against Power Supply Overvoltaging," **Analog Devices AN311**.

18. Data sheet for **ADM3311E RS-232 Port Transceiver**, Analog Devices, Inc., http://www.analog.com

19. TransZorbs are available from General Semiconductor, Inc., 10 Melville Park Road, Melville, NY, 11747-3113, (631) 847-3000, http://www.gensemi.com/product/categories/tvs/tvs.htm

SECTION 7-5: THERMAL CONSIDERATIONS

Walt Jung

For reliability reasons, op amp systems handling appreciable power are increasingly called upon to observe *thermal management*. All semiconductors have some specified safe upper limit for junction temperature (T_J), usually on the order of 150°C (sometimes 175°C). Like maximum power supply voltages, maximum junction temperature is a worst case limitation which shouldn't be exceeded. In conservative designs, it won't be approached by less than an ample safety margin. Note that this is critical, since semiconductor lifetime is inversely related to operating junction temperature. Simply put, the cooler op amps are, the more they can approach their maximum life.

This limitation of power and temperature is basic, and is illustrated by a typical data sheet statement as in Figure 7-89. In this case it is for the AD8017AR, an 8-pin SOIC device.

> ***The maximum power that can be safely dissipated by the AD8017 is limited by the associated rise in junction temperature. The maximum safe junction temperature for plastic encapsulated device is determined by the glass transition temperature of the plastic, approximately +150°C. Temporarily exceeding this limit may cause a shift in parametric performance due to a change in the stresses exerted on the die by the package. Exceeding a junction temperature of +175°C for an extended period can result in device failure.***

Figure 7-89: *Maximum power dissipation data sheet statement for the AD8017AR, an ADI thermally enhanced SOIC packaged device*

Tied to these statements are certain conditions of operation, such as the power dissipated by the device, and the package mounting specifics to the printed circuit board (PCB). In the case of the AD8017AR, the part is rated for 1.3W of power at an ambient of 25°C. This assumes operation of the 8-lead SOIC package on a two-layer PCB with about 4 inches^2 (~2500 mm^2) of 2 oz. copper for heat sinking purposes. Predicting safe operation for the device under other conditions is covered below.

Thermal basics

The symbol θ is generally used to denote *thermal resistance*. Thermal resistance is in units of °C/watt (°C/W). Unless otherwise specified, it defines the resistance heat encounters transferring from a hot IC junction to the ambient air. It might also be expressed more specifically as θ_{JA}, for *thermal resistance, junction-to-ambient*. θ_{JC} and θ_{CA} are two additional θ forms used, and are further explained below.

In general, a device with a thermal resistance θ equal to 100°C/W will exhibit a temperature differential of 100°C for a power dissipation of 1W, as measured between two reference points. Note that this is a linear relationship, so 1W of dissipation in this part will produce a 100°C differential (and so on, for other powers). For the AD8017AR example, θ is about 95°C/W, so 1.3W of dissipation produces about a 124°C junction-to-ambient temperature differential. It is of course this rise in temperature that is used to predict the internal temperature, in order to judge the thermal reliability of a design. With

the ambient at 25°C, this allows an internal junction temperature of about 150°C. In practice most ambient temperatures are above 25°C, so less power can then be handled.

For any power dissipation P (in watts), one can calculate the effective temperature differential (ΔT) in °C as:

$$\Delta T = P \times \theta \qquad \text{Eq. 7-6}$$

where θ is the total applicable thermal resistance.

Figure 7-90 summarizes a number of basic thermal relationships.

- **θ = Thermal Resistance (°C/W)**
- **P = Total Device Power Dissipation (W)**
- **T = Temperature (°C)**
- **ΔT = Temperature Differential = P × θ**
- **θ_{JA} = Junction-Ambient Thermal Resistance**
- **θ_{JC} = Junction-Case Thermal Resistance**
- **θ_{CA} = Case-Ambient Thermal Resistance**
- **$\theta_{JA} = \theta_{JC} + \theta_{CA}$**
- **$T_J = T_A + (P \times \theta_{JA})$**
- ***Note: $T_{J(Max)}$ = 150°C (Sometimes 175°C)***

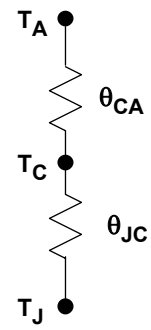

Figure 7-90: *Basic thermal relationships*

Note that series thermal resistances, such as the two shown at the right, model the total thermal resistance path a device may see. Therefore the total θ for calculation purposes is the sum, i.e., $\theta_{JA} = \theta_{JC}$ and θ_{CA}. Given the ambient temperature T_A, P, and θ, then T_J can be calculated. As the relationships signify, to maintain a low T_J, either θ or the power being dissipated (or both) must be kept low. A low ΔT is the key to extending semiconductor lifetimes, as it leads to lower maximum junction temperatures.

In ICs, one temperature reference point is always the device junction, taken to mean the hottest spot inside the chip operating within a given package. The other relevant reference point will be either T_C, the case of the device, or T_A, that of the surrounding air. This then leads in turn to the above mentioned individual thermal resistances, θ_{JC} and θ_{JA}.

Taking the most simple case first, θ_{JA} is the thermal resistance of a given device measured between its *junction* and the *ambient* air. This thermal resistance is most often used with small, relatively low power ICs such as op amps, which often dissipate 1W or less. Generally, θ_{JA} figures typical of op amps and other small devices are on the order of 90-100°C/W for a plastic 8 pin DIP package, as well as the better SOIC packages.

It should be clearly understood that these thermal resistances are *highly* package dependent, as different materials have different degrees of thermal conductivity. As a general rule of thumb, thermal resistance of conductors is analogous to electrical resistances, that is copper is the best, followed by aluminum, steel, and so on. Thus copper lead frame packages offer the highest performance, i.e., the lowest θ.

Heat sinking

By definition, a *heat sink* is an added low thermal resistance device attached to an IC to aid heat removal. A heat sink has additional thermal resistance of its own, θ_{CA}, rated in °C/W. However, most current op amp packages don't easily lend themselves to heat sink attachment (exceptions are older TO99 metal can types). Devices meant for heat sink attachment will often be noted by a θ_{JC} dramatically lower than the θ_{JA}. In this case θ will be composed of more than one component. Thermal impedances add, making a net calculation relatively simple. For example, to compute a net θ_{JA} given a relevant θ_{JC}, the thermal resistance of the heat sink, θ_{CA}, or *case* to *ambient* is added to the θ_{JC} as:

$$\theta_{JA} = \theta_{JC} + \theta_{CA} \qquad \text{Eq. 7-7}$$

and the result is the θ_{JA} for that specific circumstance.

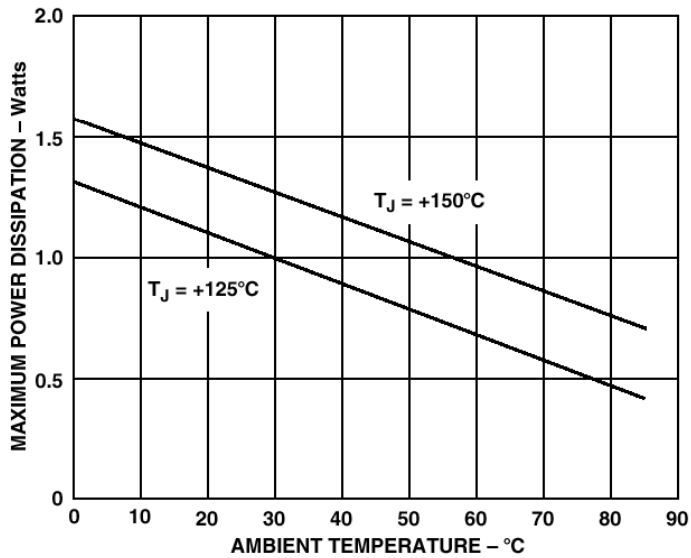

Figure 7-91: *Thermal rating curves for AD8017AR op amp*

More generally however, modern op amps *don't* use commercially available heat sinks. Instead, when significant power needs to be dissipated, such as ≥1W, low thermal resistance copper PCB traces are used as the heat sink. In such cases, the most useful form of manufacturer data for this heat sinking are the boundary conditions of a sample PCB layout, and the resulting θ_{JA} for those conditions. This is in fact the type of specific information supplied for the AD8017AR, as mentioned earlier. Applying this approach, example data illustrating thermal relationships for such conditions is shown by Figure 7-91. These data apply for an AD8017AR mounted to a heat sink with an area of about 4 square inches on a 2 layer, 2 ounce copper PCB.

These curves indicate the maximum power dissipation vs. temperature characteristic for the AD8017, for maximum junction temperatures of both 150°C and 125°C. Such curves are often referred to as *derating* curves, since allowable power decreases with ambient temperature.

With the AD8017AR, the proprietary ADI *Thermal Coastline* IC package is used, which allows additional power to be dissipated with no increase in the SO-8 package size. For a

$T_{J(max)}$ of 150°C, the upper curve shows the allowable power in this package, which is 1.3W at an ambient of 25°C. If a more conservative $T_{J(max)}$ of 125°C is used, the lower of the two curves applies.

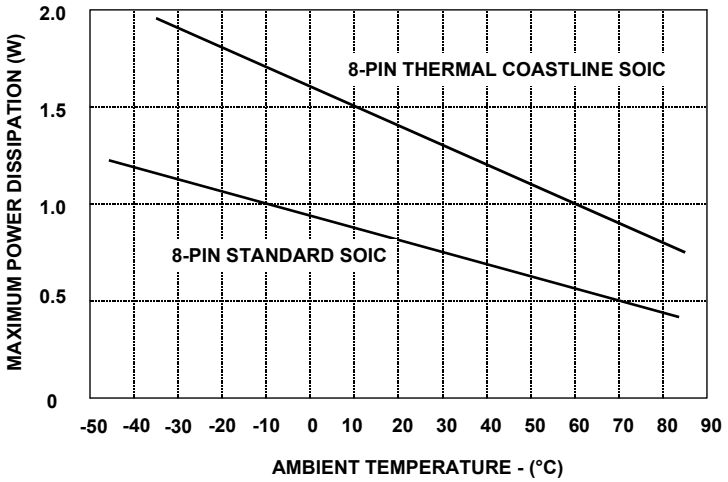

Figure 7-92: *Thermal rating curves for standard (lower) and ADI Thermal Coastline (upper) 8-pin SOIC packages*

A performance comparison for an 8-pin standard SOIC and the ADI Thermal Coastline version is shown in Figure 7-92. Note that the Thermal Coastline provides an allowable dissipation at 25°C of 1.3W, whereas a standard package allows only 0.8W. In the Thermal Coastline heat transferal is increased, accounting for the package's lower θ_{JA}.

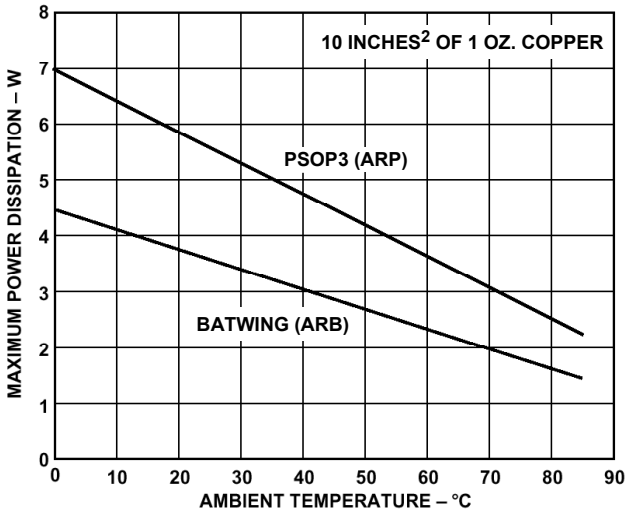

Figure 7-93: *Thermal characteristic curves for the AD8016 BATWING (lower) and PSOP3 (upper) packages, for $T_{J(max)}$ equal to 125°C*

Even higher power dissipation is possible, with the use of IC packages better able to transfer heat from chip to PCB. An example is the AD8016 device, available with two package options rated for 5.5 and 3.5W at 25°C, respectively, as shown in Figure 7-93.

Taking the higher rated power option, the AD8016ARP PSOP3 package, when used with a 10 inch^2 1 oz. heat sink plane, the combination is able to handle up to 3W of power at

an ambient of 70°C, as noted by the upper curve. This corresponds to a θ_{JA} of 18°C/W, which in this case applies for a maximum junction temperature of 125°C.

The reason the PSOP3 version of the AD8016 is so better able to handle power lies with the use of a large area copper slug. Internally, the IC die rest directly on this slug, with the bottom surface exposed as shown in Figure 7-94. The intent is that this surface be soldered directly to a copper plane of the PCB, thereby extending the heat sinking.

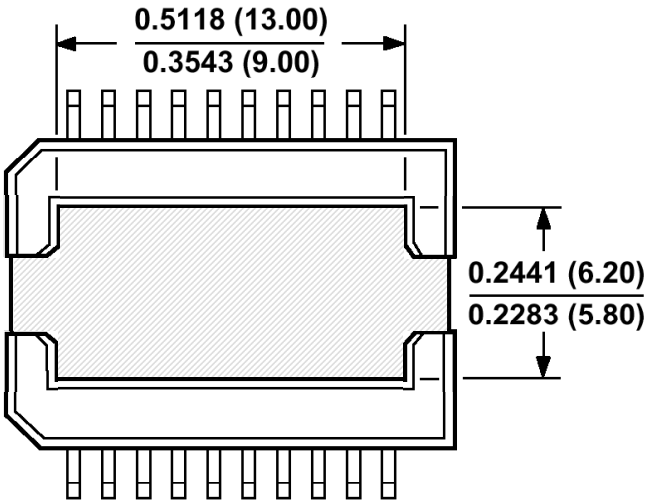

Figure 7-94: *Bottom view of AD8016 20-lead PSOP3 package showing copper slug for aid in heat transfer (central grayed area)*

Both of AD8016 package options are characterized for both still and moving air, but the thermal information given above applies *without* the use of directed airflow. Therefore, adding additional airflow lowers thermal resistance further (see Reference 2).

For reliable, low thermal resistance designs with op amps, several design *Do's and Don'ts* are listed below. Consider all of these points, as may be practical.

1) *Do use as large an area of copper as possible for a PCB heat sink, up to the point of diminishing returns.*

2) *In conjunction with 1), do use multiple (outside) PCB layers, connected together with multiple vias.*

3) *Do use as heavy copper as is practical (2 oz. or more preferred).*

4) *Do provide sufficient natural ventilation inlets and outlets within the system, to allow heat to freely move away from hot PCB surfaces.*

5) *Do orient power-dissipating PCB planes vertically, for convection-aided airflow across heat sink areas.*

6) *Do consider the use of external* power buffer *stages, for precision op amp applications.*

7) *Do consider the use of* forced air, *for situations where several watts must be dissipated in a confined space.*

8) *Don't use solder mask planes over heat dissipating traces.*

9) *Don't use excessive supply voltages on ICs delivering power.*

For the most part, these points are obvious. However, one that could use some elaboration is number 9. Whenever an application requires only modest *voltage* swings (such as for example standard video, 2Vp-p) a wide supply voltage range can often be used. But, as the data of Figure 7-95 indicates, operation of an op amp driver on higher supply voltages produces a large IC dissipation, even though the load power is constant.

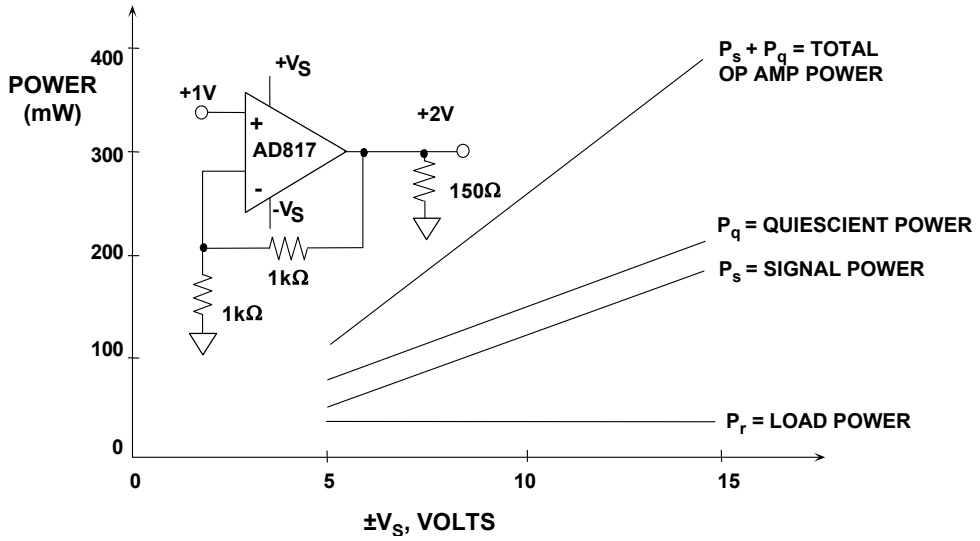

Figure 7-95: *Power dissipated in video op amp driver for various supply voltages with low voltage output swing*

In such cases, as long as the distortion performance of the application doesn't suffer, it can be advantageous to operate the IC on lower supplies, say ±5V, as opposed to ±15V. The above example data was calculated on a dc basis, which will generally tax the driver more in terms of power than a sine wave or a noise-like waveform, such as a DMT signal (see Reference 2). The general principles still hold for these ac waveforms, i.e., the op amp power dissipation is high when load current is high and the voltage low.

While there is ample opportunity for high power handling with the thermally enhanced packages described above for the AD8016 and AD8107, the increasingly popular smaller IC packages actually move in an opposite direction. Without question, it is true that today's smaller packages do noticeably sacrifice thermal performance. But, it must be understood that this is done in the interest of realizing a smaller size for the packaged op amp, and, ultimately, a much greater final PCB density for the overall system.

These points are illustrated by the thermal ratings for the AD8057 and AD8058 family of single and dual op amp devices, as is shown in Figure 7-96. The AD8057 and AD8058 op

amps are available in three different packages. These are the SOT-23-5, and the 8-pin μSOIC, along with standard SOIC.

As the data shows, as the package size becomes smaller and smaller, much less power is capable of being removed. Since the lead frame is the only heatsinking possible with such tiny packages, their thermal performance is thus reduced. The θ_{JA} for the packages mentioned is 240, 200, and 160°C/W, respectively. Note this is more of a *package* than *device* limitation. Other ICs with the same packages have similar characteristics.

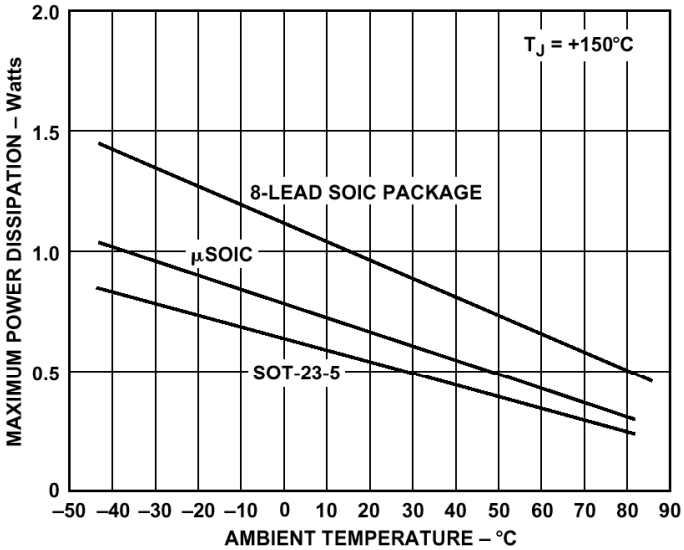

Figure 7-96: *Comparative thermal performance for several AD8057/58 op amp package options*

These discussions on the thermal application issues of op amps haven't dealt with the classic techniques of using clip-on (or bolt-on) type heat sinks. They also have not addressed the use of forced air cooling, generally considered only when tens of watts must be handled. These omissions are mainly because these approaches are seldom possible or practical with today's op amp packages.

The more general discussions within References 4-7 can be consulted for this and other supplementary information.

REFERENCES: THERMAL CONSIDERATIONS

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SECTION 7-6: EMI/RFI CONSIDERATIONS

James Bryant, Walt Jung, Walt Kester

Analog circuit performance is often affected adversely by high frequency signals from nearby electrical activity. And, equipment containing your analog circuitry may also adversely affect systems external to it. Reference 1 (page 4) describes this complementary transmission of undesirable high frequency signals from or into local equipment as per an IEC50 definition. These corresponding aspects of broad arena of *electromagnetic compatibility*, better known as EMC, are:

- *It describes the ability of electrical and electronic systems to operate without interfering with other systems…*
- *It also describes the ability of such systems to operate as intended within a specified electromagnetic environment.*

So, complete EMC assurance would indicate that the equipment under design should neither produce spurious signals, nor should it be vulnerable to out-of-band external signals (i.e., those outside its intended frequency range). It is the latter class of EMC problem to which analog equipment most often falls prey. And, it is the graceful handling of these spurious signals that are emphasized within this section.

The externally produced electrical activity may generate noise, and is referred to either as electromagnetic interference (EMI), or radio frequency interference (RFI). In this section, we will refer to EMI in terms of both electromagnetic and radio frequency interference. One of the more challenging tasks of the analog designer is the control of equipment against undesired operation due to EMI. It is important to note that in this context, *EMI and or RFI is almost always detrimental*. Once given entrance into your equipment, it can and will degrade its operation, quite often considerably.

This section is oriented heavily towards minimizing undesirable analog circuit operation due to the *receipt* of EMI/RFI. Misbehavior of this sort is also known as EMI or RFI *susceptibility*, indicating a tendency towards anomalous equipment behavior when exposed to EMI/RFI. There is of course a complementary EMC issue, namely with regard to spurious *emissions.* However, since analog circuits typically involve fewer of pulsed, high speed, high current signal edges that give rise to such spurious signals (compared to high speed logic, for example), this aspect of EMC isn't as heavily treated here. Nevertheless, the reader should bear in mind that it can be important, particularly if the analog circuitry is part of a mixed-signal environment along with high speed logic.

Since all of these various EMC design points can be critical, *the end-of-chapter references are strongly recommended for supplementary study*. Indeed, for a thorough, fully competent design with respect to EMI, RFI and EMC, the designer will need to become intimately acquainted with one or more of these references (see References 1- 6). As for the material following, it is best viewed as an introduction to this extremely broad but increasingly important topic.

EMI/RFI mechanisms

To understand and properly control EMI and RFI, it is helpful to first segregate it into manageable portions. Thus it is useful to remember that when EMI/RFI problems do occur, they can be fundamentally broken down into a *Source*, a *Path*, and a *Receiver*. As a systems designer, you have under your direct control the receiver part of this landscape, and perhaps some portion of the path. But seldom will the designer have control over the actual source.

EMI noise sources

There are countless ways in which undesired noise can couple into an analog circuit to ruin its accuracy. Some of the many examples of these noise sources are listed in Figure 7-97.

- **EMI/RFI noise sources can couple from *anywhere***
- **Some common sources of externally generated noise:**
  - **Radio and TV Broadcasts**
  - **Mobile Radio Communications**
  - **Cellular Telephones**
  - **Vehicular Ignition**
  - **Lightning**
  - **Utility Power Lines**
  - **Electric Motors**
  - **Computers**
  - **Garage Door Openers**
  - **Telemetry Equipment**

Figure 7-97: Some common EMI noise sources

Since little control is possible over these sources of EMI, the next best management tool one can exercise over them is to recognize and understand the possible paths by which they couple into the equipment under design.

EMI coupling paths

The EMI coupling paths are actually very few in terms of basic number. Three very general paths are by:

1. *Interference due to conduction (common-impedance)*
2. *Interference due to capacitive or inductive coupling (near-field interference)*
3. *Electromagnetic radiation (far-field interference)*

Noise Coupling Mechanisms

EMI energy may enter wherever there is an impedance mismatch or discontinuity in a system. In general this occurs at the interface where cables carrying sensitive analog signals are connected to PC boards, and through power supply leads. Improperly connected cables or poor supply filtering schemes are often perfect conduits for interference.

Conducted noise may also be encountered when two or more currents share a common path (impedance). This common path is often a high impedance "ground" connection. If two

circuits share this path, noise currents from one will produce noise voltages in the other. Steps may be taken to identify potential sources of this interference (see References 1 and 2, plus section 2 of this chapter).

Figure 7-98 shows some of the general ways noise can enter a circuit from external sources.

- **Impedance mismatches and discontinuities**
- **Common-mode impedance mismatches → Differential Signals**
- **Capacitively Coupled (Electric Field Interference)**
  - **dV/dt → Mutual Capacitance → Noise Current (Example: 1V/ns produces 1mA/pF)**
- **Inductively Coupled (Magnetic Field)**
  - **di/dt → Mutual Inductance → Noise Voltage (Example: 1mA/ns produces 1mV/nH)**

Figure 7-98: How EMI finds paths into equipment

There is a capacitance between any two conductors separated by a dielectric (air and vacuum are dielectrics, as well as all solid or liquid insulators). If there is a change of voltage on one conductor there will be change of charge on the other, and a *displacement current* will flow in the dielectric. Where either the capacitance or the dV/dT is high, noise is easily coupled. For example, a 1V/ns rate-of-change gives rise to displacement currents of 1 mA/pF.

If changing magnetic flux from current flowing in one circuit threads another circuit, it will induce an emf in the second circuit. Such *mutual inductance* can be a troublesome source of noise coupling from circuits with high values of dI/dT. As an example, a mutual inductance of 1nH and a changing current of 1A/ns will induce an emf of 1V.

Reducing Common-Impedance Noise

Steps to be taken to eliminate or reduce noise due to the conduction path sharing of impedances, or *common-impedance noise* are outlined in Figure 7-99.

- **Common-impedance noise**
  - **Decouple op amp power leads at LF and HF**
  - **Reduce common-impedance**
  - **Eliminate shared paths**
- **Techniques**
  - **Low impedance electrolytic (LF) and local low inductance (HF) bypasses**
  - **Use ground and power planes**
  - **Optimize system design**

Figure 7-99: *Some solutions to common-impedance noise*

These methods should be applied in conjunction with all of the related techniques discussed earlier within section 2 of this chapter.

Power supply rails feeding several circuits are good common-impedance examples. Real world power sources may exhibit low output impedance, or may they not— especially over frequency. Furthermore, PCB traces used to distribute power are both inductive and resistive,

and may also form a ground loop. The use of power and ground planes also reduces the power distribution impedance. These dedicated conductor layers in a PCB are continuous (ideally, that is) and as such, offer the lowest practical resistance and inductance.

In some applications where low-level signals encounter high levels of common-impedance noise it will not be possible to prevent interference and the system architecture may need to be changed. Possible changes include:

1. *Transmitting signals in differential form*
2. *Amplifying signals to higher levels for improved S/N*
3. *Converting signals into currents for transmission*
4. *Converting signals directly into digital form*

Noise Induced by Near-Field Interference

Crosstalk is the second most common form of interference. In the vicinity of the noise source, i.e., near-field, interference is not transmitted as an electromagnetic wave, and the term crosstalk may apply to either inductively or capacitively coupled signals.

Reducing Capacitance-Coupled Noise

Capacitively-coupled noise may be reduced by reducing the coupling capacity (by increasing conductor separation), but is most easily cured by shielding. A conductive and grounded shield (known as a *Faraday shield*) between the signal source and the affected node will eliminate this noise, by routing the displacement current directly to ground.

- **Reduce Level of High dV/dt Noise Sources**
- **Use Proper Grounding Schemes for Cable Shields**
- **Reduce Stray Capacitance**
  - **Equalize Input Lead Lengths**
  - **Keep Traces Short**
  - **Use Signal-Ground Signal-Routing Schemes**
- **Use Grounded Conductive Faraday Shields to Protect Against Electric Fields**

Figure 7-100: *Methods to reduce capacitance-coupled noise*

With the use of such shields, it is important to note that it is always *essential* that a Faraday shield be grounded. A floating or open-circuit shield almost invariably increases capacitively-coupled noise. For a brief review of this shielding, consult Section 2 of this chapter again, and see References 2 and 3 at the end of this section.

Methods to eliminate capacitance-coupled interference are summarized in Figure 7-100.

Reducing Magnetically-Coupled Noise

Methods to eliminate interference caused by magnetic fields are summarized in Figure 7-101.

- **Careful Routing of Wiring**
- **Use Conductive Screens for HF Magnetic Shields**
- **Use High Permeability Shields for LF Magnetic Fields (mu-Metal)**
- **Reduce Loop Area of Receiver**
  - **Twisted Pair Wiring**
  - **Physical Wire Placement**
  - **Orientation of Circuit to Interference**
- **Reduce Noise Sources**
  - **Twisted Pair Wiring**
  - **Driven Shields**

Figure 7-101: *Methods to reduce magnetically-coupled noise*

To illustrate the effect of magnetically-coupled noise, consider a circuit with a closed-loop area of A cm^2 operating in a magnetic field with an rms flux density value of B gauss. The noise voltage V_n induced in this circuit can be expressed by the following equation:

$$V_n = 2\,\pi\, f\, B\, A \cos\theta \times 10^{-8}\ V \qquad \text{Eq. 7-8}$$

In this equation, f represents the frequency of the magnetic field, and θ represents the angle of the magnetic field B to the circuit with loop area A. Magnetic field coupling can be reduced by reducing the circuit loop area, the magnetic field intensity, or the angle of incidence. Reducing circuit loop area requires arranging the circuit conductors closer together. Twisting the conductors together reduces the loop net area. This has the effect of canceling magnetic field pickup, because the sum of positive and negative incremental loop areas is ideally equal to zero. Reducing the magnetic field directly may be difficult. However, since magnetic field intensity is inversely proportional to the cube of the distance from the source, physically moving the affected circuit away from the magnetic field has a very great effect in reducing the induced noise voltage. Finally, if the circuit is placed perpendicular to the magnetic field, pickup is minimized. If the circuit's conductors are in parallel to the magnetic field the induced noise is maximized because the angle of incidence is zero.

There are also techniques that can be used to reduce the amount of magnetic-field interference, *at its source*. In the previous paragraph, the conductors of the receiver circuit were twisted together, to cancel the induced magnetic field along the wires. The same principle can be used on the source wiring. If the source of the magnetic field is large currents flowing through nearby conductors, these wires can be twisted together to reduce the net magnetic field.

Shields and cans are not nearly as effective against magnetic fields as against electric fields, but can be useful on occasion. At low frequencies magnetic shields using high-permeability material such a Mu-metal can provide modest attenuation of magnetic fields. At high frequencies simple conductive shields are quite effective provided that the thickness of the shield is greater than the skin depth of the conductor used (at the frequency involved). Note— copper skin depth is $6.6/\sqrt{f}$ cm, with f in Hz.

Passive Components: Your Arsenal Against EMI

Passive components, such as resistors, capacitors, and inductors, are powerful tools for reducing externally induced interference when used properly.

Simple RC networks make efficient and inexpensive one-pole, low-pass filters. Incoming noise is converted to heat and dissipated in the resistor. But note that a fixed resistor does produce thermal noise of its own. Also, when used in the input circuit of an op amp or in-amp, such resistor(s) can generate input-bias-current induced offset voltage. While matching the two resistors will minimize the dc offset, the noise will remain. Figure 7-102 summarizes some popular low-pass filters for minimizing EMI.

LP Filter Type	ADVANTAGE	DISADVANTAGE
RC Section	Simple Inexpensive	Resistor Thermal Noise I_B x R Drop → Offset Single-Pole Cutoff
LC Section (Bifilar)	Very Low Noise at LF Very Low IR Drop Inexpensive Two-Pole Cutoff	Medium Complexity Nonlinear Core Effects Possible
π Section (C-L-C)	Very Low Noise at LF Very Low IR Drop Pre-packaged Filters Multiple-Pole Cutoff	Most Complex Nonlinear Core Effects Possible Expensive

Figure 7-102: *Using passive components within filters to combat EMI*

In applications where signal and return conductors aren't well-coupled magnetically, a common-mode (CM) choke can be used to increase their mutual inductance. Note that these comments apply mostly to in-amps, which naturally receive a balanced input signal (whereas op amps are inherently unbalanced inputs— unless one constructs an in-amp with them). A CM choke can be simply constructed by winding several turns of the differential signal conductors together through a high-permeability (> 2000) ferrite bead. The magnetic properties of the ferrite allow differential-mode currents to pass unimpeded while suppressing CM currents.

Capacitors can also be used before and after the choke, to provide additional CM and differential-mode filtering, respectively. Such a CM choke is cheap and produces very low thermal noise and bias current-induced offsets, due to the wire's low DCR. However, there is a field around the core. A metallic shield surrounding the core may be necessary to prevent coupling with other circuits. Also, note that high-current levels should be avoided in the core as they may saturate the ferrite.

The third method for passive filtering takes the form of packaged π-networks (C-L-C). These packaged filters are completely self-contained and include feedthrough capacitors at the input and the output as well as a shield to prevent the inductor's magnetic field from radiating noise. These more expensive networks offer high levels of attenuation and wide operating frequency ranges, but the filters must be selected so that for the operating current levels involved the ferrite doesn't saturate.

Reducing System Susceptibility to EMI

The general examples discussed above and the techniques illustrated earlier in this section outline the procedures that can be used to reduce or eliminate EMI/RFI. Considered on a *system* basis, a summary of possible measures is given in Figure 7-103.

- **Always Assume That Interference Exists!**
- **Use Conducting Enclosures Against Electric and HF Magnetic Fields**
- **Use mu-Metal Enclosures Against LF Magnetic Fields**
- **Implement Cable Shields Effectively**
- **Use Feedthrough Capacitors and Packaged PI Filters**

Figure 7-103: *Reducing system EMI/RFI susceptibility*

Other examples of filtering techniques useful against EMI are illustrated later in this section, under "Reducing RFI rectification within op amp and in-amp circuits".

The section immediately below further details shielding principles.

A Review of Shielding Concepts

The concepts of shielding effectiveness presented next are background material. Interested readers should consult References 4-9 cited at the end of the section for more detailed information.

Applying the concepts of shielding effectively requires an understanding of the source of the interference, the environment surrounding the source, and the distance between the source and point of observation (the receiver). If the circuit is operating close to the source (in the *near*, or induction-field), then the field characteristics are determined by the source. If the circuit is remotely located (in the *far*, or radiation-field), then the field characteristics are determined by the transmission medium.

A circuit operates in a near-field if its distance from the source of the interference is less than the wavelength (λ) of the interference divided by 2π, or $\lambda/2\pi$. If the distance between the circuit and the source of the interference is larger than this quantity, then the circuit operates in the far field. For instance, the interference caused by a 1ns pulse edge has an upper bandwidth of approximately 350MHz. The wavelength of a 350MHz signal is approximately 32 inches (the speed of light is approximately 12"/ns). Dividing the wavelength by 2π yields a distance of approximately 5 inches, the boundary between near- and far-field. If a circuit is within 5 inches of a 350MHz interference source, then the circuit operates in the near-field of the interference. If the distance is greater than 5 inches, the circuit operates in the far-field of the interference.

Regardless of the type of interference, there is a characteristic impedance associated with it. The characteristic, or wave impedance of a field is determined by the ratio of its electric (or E-) field to its magnetic (or H-) field. In the far field, the ratio of the electric field to the magnetic field is the characteristic (wave impedance) of free space, given by $Z_O = 377\Omega$. In the near field, the wave-impedance is determined by the nature of the

interference and its distance from the source. If the interference source is high-current and low-voltage (for example, a loop antenna or a power-line transformer), the field is predominately magnetic and exhibits a wave impedance which is less than 377Ω. If the source is low-current and high-voltage (for example, a rod antenna or a high-speed digital switching circuit), then the field is predominately electric and exhibits a wave impedance which is greater than 377Ω.

Conductive enclosures can be used to shield sensitive circuits from the effects of these external fields. These materials present an *impedance mismatch* to the incident interference, because the impedance of the shield is lower than the wave impedance of the incident field. The effectiveness of the conductive shield depends on two things: First is the loss due to the *reflection* of the incident wave off the shielding material. Second is the loss due to the *absorption* of the transmitted wave *within* the shielding material. The amount of reflection loss depends upon the type of interference and its wave impedance. The amount of absorption loss, however, is independent of the type of interference. It is the same for near- and far-field radiation, as well as for electric or magnetic fields.

Reflection loss at the interface between two media depends on the difference in the characteristic impedances of the two media. For electric fields, reflection loss depends on the frequency of the interference and the shielding material. This loss can be expressed in dB, and is given by:

$$R_e(\mathrm{dB}) = 322 + 10\log_{10}\left[\frac{\sigma_r}{\mu_r f^3 {}_r^2}\right] \qquad \text{Eq. 7-9}$$

where σ_r = relative conductivity of the shielding material, in Siemens per meter;
μ_r = relative permeability of the shielding material, in Henries per meter;
f = frequency of the interference, and
r = distance from source of the interference, in meters

For magnetic fields, the loss depends also on the shielding material and the frequency of the interference. Reflection loss for magnetic fields is given by:

$$R_m(\mathrm{dB}) = 14.6 + 10\log_{10}\left[\frac{f r^2 \sigma_r}{\mu_r}\right] \qquad \text{Eq. 7-10}$$

and, for plane waves ($r > \lambda/2\pi$), the reflection loss is given by:

$$R_{pw}(\mathrm{dB}) = 168 + 10\log_{10}\left[\frac{\sigma_r}{\mu_r f}\right] \qquad \text{Eq. 7-11}$$

Absorption is the second loss mechanism in shielding materials. Wave attenuation due to absorption is given by:

$$A(\mathrm{dB}) = 3.34\ t\sqrt{\sigma_r \mu_r f} \qquad \text{Eq. 7-12}$$

where t = thickness of the shield material, in inches. This expression is valid for plane waves, electric and magnetic fields. Since the intensity of a transmitted field decreases exponentially relative to the thickness of the shielding material, the absorption loss in a shield one skin-depth (δ) thick is 9dB. Since absorption loss is proportional to thickness and inversely proportional to skin depth, increasing the thickness of the shielding material improves shielding effectiveness at high frequencies.

Reflection loss for plane waves in the far field decreases with increasing frequency because the shield impedance, Z_s, increases with frequency. Absorption loss, on the other hand, increases with frequency because skin depth decreases. For electric fields and plane waves, the primary shielding mechanism is reflection loss, and at high frequencies, the mechanism is absorption loss.

Thus for high-frequency interference signals, lightweight, easily worked high conductivity materials such as copper or aluminum can provide adequate shielding. At low frequencies however, both reflection and absorption loss to magnetic fields is low. It is thus very difficult to shield circuits from low-frequency magnetic fields. In these applications, high-permeability materials that exhibit low-reluctance provide the best protection. These low-reluctance materials provide a magnetic shunt path that diverts the magnetic field away from the protected circuit.

To summarize the characteristics of metallic materials commonly used for shielded purposes: Use high conductivity metals for HF interference, and high permeability metals for LF interference.

A properly shielded enclosure is very effective at preventing external interference from disrupting its contents as well as confining any internally-generated interference. However, in the real world, openings in the shield are often required to accommodate adjustment knobs, switches, connectors, or to provide ventilation. Unfortunately, these openings may compromise shielding effectiveness by providing paths for high-frequency interference to enter the instrument.

The longest dimension (not the total area) of an opening is used to evaluate the ability of external fields to enter the enclosure, because the openings behave as slot antennas. Equation Eq. 7-13 can be used to calculate the shielding effectiveness, or the susceptibility to EMI leakage or penetration, of an opening in an enclosure:

$$\text{Shielding Effectiveness}\left(\text{dB}\right) = 20\log_{10}\left(\frac{\lambda}{2\cdot L}\right) \qquad \text{Eq. 7-13}$$

where λ = wavelength of the interference and
L = maximum dimension of the opening

Maximum radiation of EMI through an opening occurs when the longest dimension of the opening is equal to one half-wavelength of the interference frequency (0dB shielding effectiveness). A rule-of-thumb is to keep the longest dimension less than 1/20 wavelength of the interference signal, as this provides 20dB shielding effectiveness.

Furthermore, a few small openings on each side of an enclosure is preferred over many openings on one side. This is because the openings on different sides radiate energy in different directions, and as a result, shielding effectiveness is not compromised. If openings and seams cannot be avoided, then conductive gaskets, screens, and paints alone or in combination should be used judiciously to limit the longest dimension of any opening to less than 1/20 wavelength. Any cables, wires, connectors, indicators, or control shafts penetrating the enclosure should have circumferential metallic shields physically bonded to the enclosure at the point of entry. In those applications where unshielded cables/wires are used, then filters are recommended at the shield entry point.

General Points on Cables and Shields

Although covered in detail elsewhere, it is worth noting that the improper use of cables and their shields can be a significant contributor to both radiated and conducted interference. Rather than developing an entire treatise on these issues, the interested reader should consult References 2, 3, 5, and 6 for background.

As shown in Figure 7-104, proper cable/enclosure shielding confines sensitive circuitry and signals *entirely within the shield*, with no compromise to shielding effectiveness.

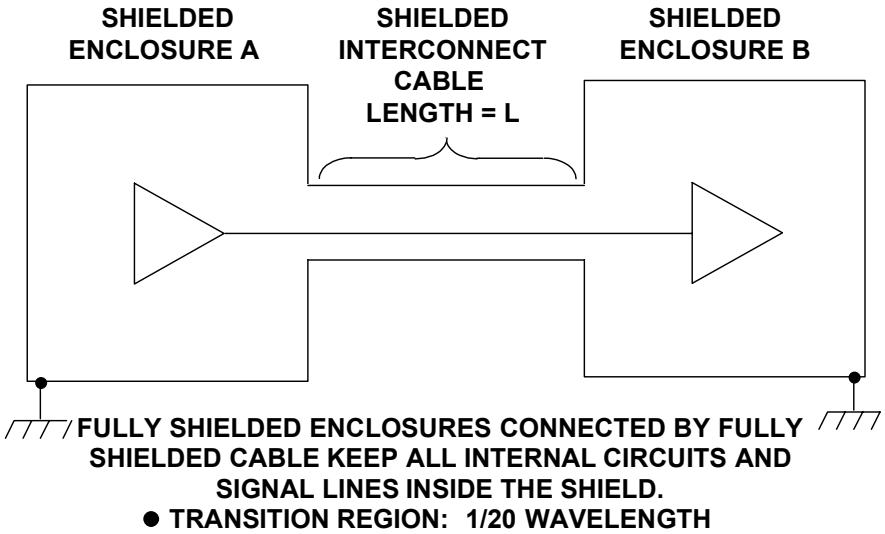


Figure 7-104: *Shielded interconnect cables are either electrically long or short, depending upon the operating frequency*

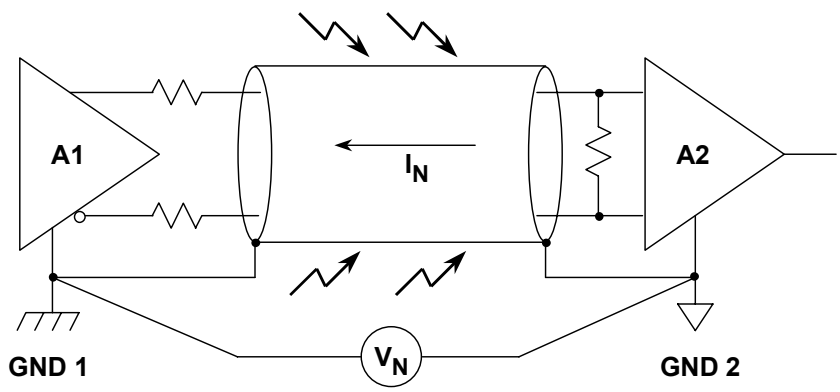
As can be noted by this diagram, the enclosures and the shield must be grounded properly, otherwise they can act as an antenna, thereby making the radiated and conducted interference problem worse (rather than better).

Depending on the type of interference (pickup/radiated, low/high frequency), proper cable shielding is implemented differently and is very dependent on the length of the cable. The first step is to determine whether the length of the cable is *electrically short* or *electrically long* at the frequency of concern. A cable is considered electrically short if the length of the cable is less than 1/20 wavelength of the highest frequency of the interference. Otherwise it is considered to be electrically long.

For example, at 50/60Hz, an electrically short cable is any cable length less than 150 miles, where the primary coupling mechanism for these low frequency electric fields is capacitive. As such, for any cable length less than 150 miles, the amplitude of the interference will be the same over the entire length of the cable.

In applications where the length of the cable is electrically long, or protection against high-frequency interference is required, then the preferred method is to connect the cable shield to low-impedance points, *at both ends*. As will be seen shortly, this can be a direct connection at the driving end, and a capacitive connection at the receiver. If left ungrounded, unterminated transmission lines effects can cause reflections and standing waves along the cable. At frequencies of 10MHz and above, circumferential (360°) shield bonds and metal connectors are required to main low-impedance connections to ground.

In summary, for protection against low-frequency (<1MHz), electric-field interference, grounding the shield at one end is acceptable. For high-frequency interference (>1MHz), the preferred method is grounding the shield at both ends, using 360° circumferential bonds between the shield and the connector, and maintaining metal-to-metal continuity between the connectors and the enclosure.



- **V_N Causes Current in Shield (Usually 50/60Hz)**
- **Differential Error Voltage is Produced at Input of A2 Unless:**
  - **A1 Output is Perfectly Balanced and**
  - **A2 Input is Perfectly Balanced and**
  - **Cable is Perfectly Balanced**

Figure 7-105: *Ground loops in shielded twisted pair cable can cause errors*

However in practice, there is a caveat involved with directly grounding the shield at both ends. When this is done, it creates a low frequency ground loop, shown in Figure 7-105.

Whenever two systems A1 and A2 are remote from each other, there is usually a difference in the ground potentials at each system, i.e., V_N. The frequency of this potential difference is generally the line frequency (50 or 60Hz) and multiples thereof. But, if the shield is directly grounded at both ends as shown, noise current I_N flows in the shield. In a perfectly balanced system, the common-mode rejection of the system is infinite, and this current flow produces no differential error at the receiver A2. However, perfect balance is never achieved in the driver, its impedance, the cable, or the receiver,

so a certain portion of the shield current will appear as a differential noise signal, at the input of A2. The following illustrate correct shield grounding for various examples.

As noted above, cable shields are subject to both low and high frequency interference. Good design practice requires that the shield be grounded at both ends if the cable is electrically long to the interference frequency, as is usually the case with RF interference.

Figure 7-106 (below) shows a remote passive RTD sensor connected to a bridge and conditioning circuit by a shielded cable. The proper grounding method is shown in the upper part of the figure, where the shield is grounded at the receiving end.

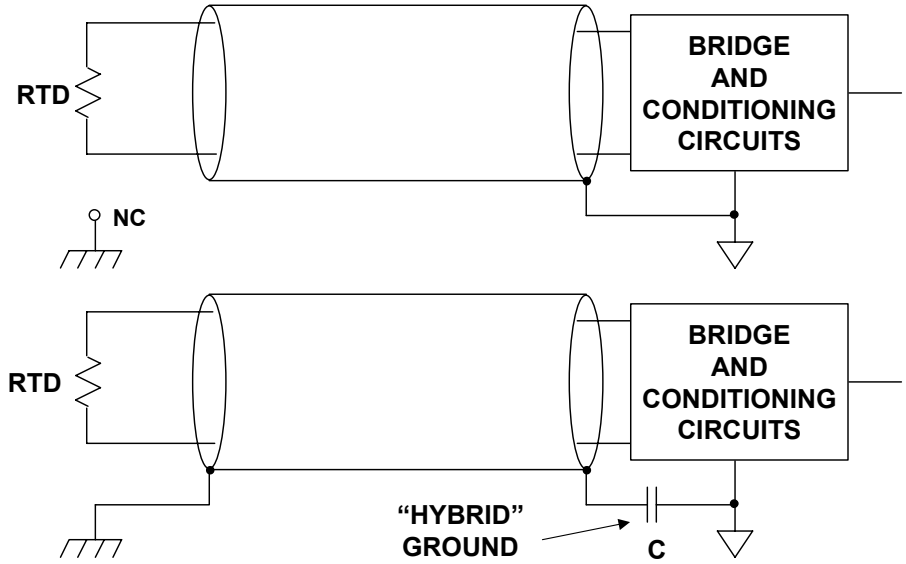


Figure 7-106: *Hybrid grounding of shielded cable with passive sensor*

However, safety considerations may require that the remote end of the shield also be grounded. If this is the case, the receiving end can be grounded with a low inductance ceramic capacitor (0.01µF to 0.1µF), still providing high frequency grounding. The capacitor acts as a ground to RF signals on the shield but blocks low frequency line current to flow in the shield. This technique is often referred to as a *hybrid ground*.

A case of an active remote sensor and/or other electronics is shown Figure 7-107 (opposite). In both of the two situations, a hybrid ground is also appropriate, either for the balanced (upper) or the single-ended (lower) driver case. In both instances the capacitor "C" breaks the low frequency ground loop, providing effective RF grounding of the shielded cable at the A2 receiving end at the right side of the diagram.

There are also some more subtle points that should be made with regard to the source termination resistances used, R_S. In both the balanced as well as the single-ended drive cases, the driving signal seen on the balanced line originates from a net impedance of R_S, which is split between the two twisted pair legs as twice $R_S/2$. In the upper case of a fully differential drive, this is straightforward, with an $R_S/2$ valued resistor connected in series with the complementary outputs from A1.

In the bottom case of the single-ended driver, note that there are still two $R_S/2$ resistors used, one in series with both legs. Here the grounded dummy return leg resistor provides an impedance-balanced ground connection drive to the differential line, aiding in overall system noise immunity. Note that this implementation is only useful for those applications with a balanced receiver at A2, as shown.

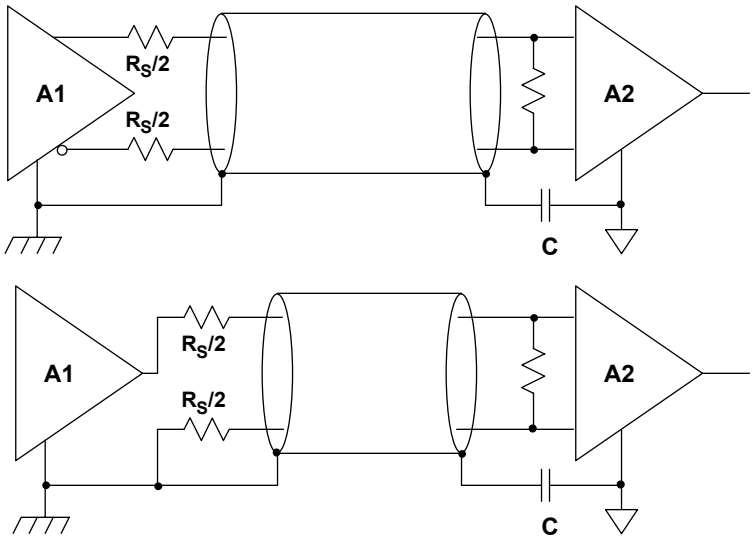


Figure 7-107: *Impedance-balanced drive of balanced shielded cable aids noise-immunity with either balanced or single-ended source signals*

Coaxial cables are different from shielded twisted pair cables in that the signal return current path is through the shield. For this reason, the ideal situation is to ground the shield at the driving end and allow the shield to float at the differential receiver (A2) as shown in the upper portion of Figure 7-108 (below). For this technique to work, however, the receiver must be a differential type with good high frequency CM rejection.

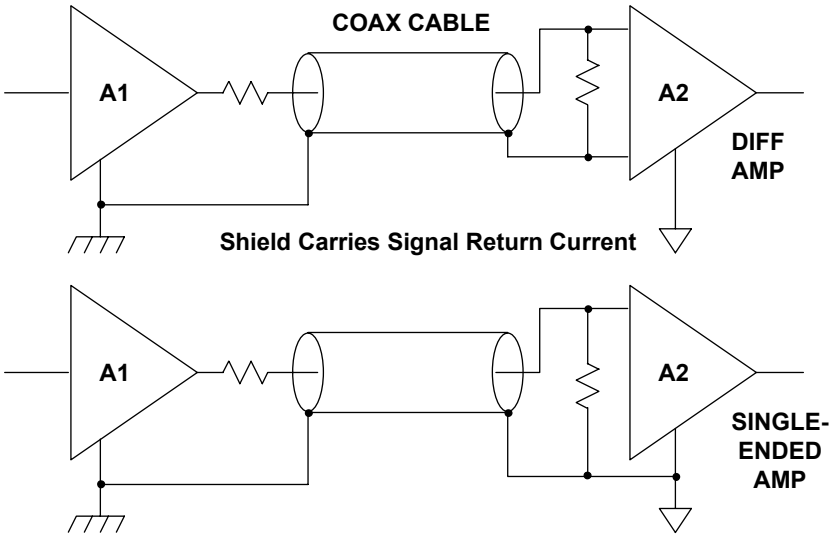


Figure 7-108: *Coaxial cables can use either balanced or single-ended receivers*

However, the receiver may be a single-ended type, such as typical of a standard single op amp type circuit. This is true for the bottom example of Figure 7-108, so there is no choice but to ground the coaxial cable shield at both ends for this case.

Input-stage RFI Rectification Sensitivity

A well-known but poorly understood phenomenon in analog integrated circuits is *RFI rectification*, specifically as it occurs in op amps and in-amps. While amplifying very small signals these devices can rectify large-amplitude, out-of-band HF signals, i.e., RFI. As a result, dc errors appear at the output in addition to the desired signal. The undesired HF signals can enter sensitive analog circuits by various means. Conductors leading into and out of the circuit provide a path for interference coupling into a circuit. These conductors pick up noise through capacitive, inductive, or radiation coupling, as discussed earlier. The spurious signals appear at the amplifier inputs, along with the desired signal. The spurious signals can be several tens of mV in amplitude however, which causes problems. Simply stated, it cannot be assumed that a sensitive, low-bandwidth dc amplifier will always reject out-of-band spurious signals. While this would be the case for a simple linear low pass filter, op amp and in-amp devices actually rectify high-level HF signals, leading to non-linearities and anomalous offsets. Methods of analysis for as well as the prevention of RFI rectification are discussed in this section.

Background: Op amp and In-Amp RFI Rectification Sensitivity Tests

Just about all in-amp and op amp input stages use emitter-coupled BJT or source-coupled FET differential pairs of some type. Depending on the device operating current, the interfering frequency and its relative amplitude, these differential pairs can behave as high-frequency detectors. As will be shown, the detection process produces spectral components at the harmonics of the interference, as well at dc! It is the detected dc component of the interference that shifts amplifier bias levels, leading to inaccuracies.

The effect of RFI rectification within op amps and in-amps can be evaluated with relatively simple test circuits, as described for the *RFI Rectification Test Configuration* (see page 1-38 of Reference 10). In these tests, an op amp or in-amp is configured for a gain of –100 (op amp), or 100 (in-amp), with dc output measured after a 100-Hz low-pass filter, preventing interference from other signals. A 100MHz, 20mV$_{p-p}$ signal is the test stimulus, chosen to be well above test device frequency limits. In operation, the test evaluates dc output shift observed under stimulus presence. While an ideal dc shift for this measurement would be zero, the actual dc shift of a given part indicates the relative RFI rectification sensitivity. Devices using both BJT and FET technologies can be tested by this method, as can devices operating at either low or high supply current levels.

In the original op amp test device set of Reference 10, some FET-input devices (OP80, OP42, OP249 and AD845) exhibited no observable shift in their output voltages, while several others showed shifts of less than 10µV referred to the input. Of the BJT-input op amps, the amount of shift decreased with increasing device supply current. Only two devices showed no observable output voltage shift (AD797 and AD827), while others showed shifts of less than 10µV referred to the input (OP200 and OP297). For other op amps, it is to be expected that similar patterns would be shown under such testing.

From these tests, some generalizations on RFI rectification can be made. First, device susceptibility appears to be inversely proportional to supply current; that is, devices biased at low quiescent supply currents exhibit greatest output voltage shift. Second, ICs

with FET-input stages appeared to be less susceptible to rectification than those with BJTs. Note that these points are independent of whether the device is an op amp or an in-amp. In practice this means that the lower power op amps *or* in-amps will tend to be more susceptible to RFI rectification effects. And, FET-input op amps (or in-amps) will tend to be *less* susceptible to RFI, especially those operating at higher currents.

Based on these data and from the fundamental differences between BJTs and FETs, we can summarize what we know. Bipolar transistor action is controlled by a forward-biased p-n junction (the base-emitter junction) whose I-V characteristic is exponential and quite nonlinear. FET behavior, on the other hand, is controlled by voltages applied to a reverse-biased p-n junction diode (the gate-source junction). The I-V characteristic of FETs is a square-law, and thus it is inherently more linear than that of BJTs.

For the case of the lower supply current devices, transistors in the circuit are biased well below their peak f_T collector currents. Although the ICs may be constructed on processes whose device f_Ts can reach hundreds of MHz, charge transit times increase, when transistors are operated at low current levels. The impedance levels used also make RFI rectification in these devices worse. In low-power op amps, impedances are on the order of hundreds to thousands of kΩs, whereas in moderate supply-current designs impedances might be no more than just a few kΩ. Combined, these factors tend to degrade a low-power device's RFI rectification sensitivity.

- ◆**BJT input devices *rectify readily***
  - **Forward-biased B-E junction**
  - **Exponential I-V Transfer Characteristic**
- ◆**FET input devices *less sensitive* to rectifying**
  - **Reversed-biased p-n junction**
  - **Square-law I-V Transfer Characteristic**
- ◆**Low I_{supply} devices versus High I_{supply} devices**
  - **Low I_{supply} ⇒ *Higher* rectification sensitivity**
  - **High I_{supply} ⇒ *Lower* rectification sensitivity**

Figure 7-109: *Some general observations on op amp and in-amp input stage RFI rectification sensitivity*

Figure 7-109 summarizes these general observations on RFI rectification sensitivity, and is applicable to both op amps and in-amps.

An Analytical Approach: BJT RFI Rectification

While lab experiments can demonstrate that BJT-input devices exhibit greater RFI rectification sensitivity than comparable devices with FET inputs, a more analytical approach can also be taken to explain this phenomenon.

RF circuit designers have long known that p-n junction diodes are efficient rectifiers because of their nonlinear I-V characteristics. A spectral analysis of a BJT transistor current output for a HF sinewave input reveals that, as the device is biased closer to its "knee," nonlinearity increases. This, in turn, makes its use as a detector more efficient.

This is especially true in low-power op amps, where input transistors are biased at very low collector currents.

A rectification analysis for the collector current of a BJT has been presented in Reference 10, and will not be repeated here except for the important conclusions. These results reveal that the original quadratic second-order term can be simplified into a frequency-dependent term, $\Delta i_c(AC)$, at twice the input frequency and a dc term, $\Delta i_c(DC)$. The latter component can be expressed as noted in Eq. 7-14, the final form for the rectified dc term:

$$\Delta i_C(DC) = \left(\frac{V_X}{V_T}\right)^2 \bullet \frac{I_C}{4} \qquad \text{Eq. 7-14}$$

This expression shows that the dc component of the second-order term is directly proportional to the *square* of the HF noise amplitude V_X, and, also, to I_C, the quiescent collector current of the transistor. To illustrate this point on rectification, note that the change in dc collector current of a bipolar transistor operating at an I_C of 1mA with a spurious $10mV_{peak}$ high-frequency signal impinging upon it will be about 38uA.

Reducing the amount of rectified collector current is a matter of reducing the quiescent current, or the magnitude of the interference. Since the op amp and in-amp input stages seldom provide adjustable quiescent collector currents, reducing the level of interfering noise V_X is by far the best (and almost always the only) solution. For example, reducing the amplitude of the interference by a factor of 2, down to $5mV_{peak}$ produces a net 4 to 1 reduction in the rectified collector current. Obviously, this illustrates the importance of keeping spurious HF signals away from RFI sensitive amplifier inputs.

An Analytical Approach: FET RFI Rectification

A rectification analysis for the drain current of a JFET has also been presented in Reference 10, and isn't repeated here. A similar approach was used for the rectification analysis of a FET's drain current as a function of a small voltage V_X, applied to its gate. The results of evaluating the second-order rectified term for the FET's drain current are summarized in Eq. 7-15. Like the BJT, an FET's second-order term has an ac and a dc component. The simplified expression for the dc term of the rectified drain current is given here, where the rectified dc drain current is directly proportional to the square of the amplitude of V_X, the spurious signal. However, Eq. 7-15 also reveals a very important difference between the *degree* of the rectification produced by FETs relative to BJTs.

$$\Delta i_D(DC) = \left(\frac{V_X}{V_P}\right)^2 \bullet \frac{I_{DSS}}{2} \qquad \text{Eq. 7-15}$$

Whereas in a BJT the change in collector current has a direct relationship to its quiescent collector current level, the change in a JFET's drain current is proportional to its drain current at zero gate-source voltage, I_{DSS}, and inversely proportional to the square of its channel pinch-off voltage, V_P — parameters that are geometry and process dependent. Typically, JFETs used in the input stages of in-amps and op amps are biased with their

quiescent current of ~0.5 • I_{DSS}. Therefore, the change in a JFET's drain current is independent of its quiescent drain current; hence, independent of the operating point.

A quantitative comparison of second-order rectified dc terms between BJTs and FETs is illustrated in Figure 7-110. In this example, a bipolar transistor with a unit emitter area of 576μm^2 is compared to a unit-area JFET designed for an I_{DSS} of 20μA and a pinch-off voltage of 2V. Each device is biased at 10μA and operated at T_A = 25°C.

The important result is that, under identical quiescent current levels, the change in collector current in bipolar transistors is about 1500 times greater than the change in a JFET's drain current. This explains why FET-input amplifiers behave with less sensitivity to large amplitude HF stimulus. As a result, they offer more RFI rectification immunity.

- **BJT:**
  Emitter area = 576μm^2
  I_C = 10μA
  V_T = 25.68mV @ 25°C

$$\Delta i_C = \left(\frac{V_X}{V_T}\right)^2 \bullet \frac{I_C}{4} = \frac{V_X^2}{264}$$

- **JFET:**
  I_{DSS} = 20μA (Z/L=1)
  V_P = 2V
  I_D = 10μA

$$\Delta i_D = \left(\frac{V_X}{V_P}\right)^2 \bullet \frac{I_{DSS}}{2} = \frac{V_X^2}{400\text{x}10^3}$$

- **Conclusion: *BJTs ~1500* more *sensitive than JFETs!***

Figure 7-110: *Relative sensitivity comparison - BJT versus JFET*

What all this boils down to is this: Since a user has virtually no access to the amplifier's internal circuitry, the prevention of IC circuit performance degradation due to RFI is left essentially to those means which are external to the ICs.

As the analysis above shows, regardless of the amplifier type, *RFI rectification is directly proportional to the square of the interfering signal's amplitude*. Therefore, to minimize RFI rectification in precision amplifiers, the level of interference must be reduced or eliminated, *prior to the stage*. The most direct way to reduce or eliminate the unwanted noise is by proper filtering.

This topic is covered in the section immediately following.

Reducing RFI rectification within op amp and in-amp circuits

EMI and RFI can seriously affect the dc performance of high accuracy analog circuits. Because of their relatively low bandwidth, precision op amps and in-amps simply won't accurately amplify RF signals in the MHz range. However, if these out-of-band signals are allowed to couple into a precision amplifier through either its input, output, or power supply pins, they can be internally rectified by various amplifier junctions, ultimately causing an undesirable dc offset at the output. The previous theoretical discussion of this phenomenon has shown its basic mechanisms. The logical next step is to show how proper filtering can minimize or eliminate these errors.

Elsewhere in this chapter we have discussed how proper supply decoupling minimizes RFI on IC power pins. Further discussion is required with respect to the amplifier inputs and outputs, *at the device level*. It is assumed at this point that system level EMI/RFI approaches have already been implemented, such as an RFI-tight enclosure, properly grounded shields, power rail filtering, etc. The steps following can be considered as circuit-level EMI/RFI prevention.

Op amp inputs

The best way to prevent input stage rectification is to use a low-pass filter located close to the op amp input as shown in Figure 7-111. In the case of the inverting op amp at the left, filter capacitor C is placed between equal-value resistors R1-R2. This results in a simple corner frequency expression, as shown in the figure. At very low frequencies or dc, the closed loop gain of the circuit is –R3/(R1+R2). Note that C cannot be connected directly to the inverting input of the op amp, since that would cause instability. The filter bandwidth can be chosen at least 100 times the signal bandwidth to minimize signal loss.

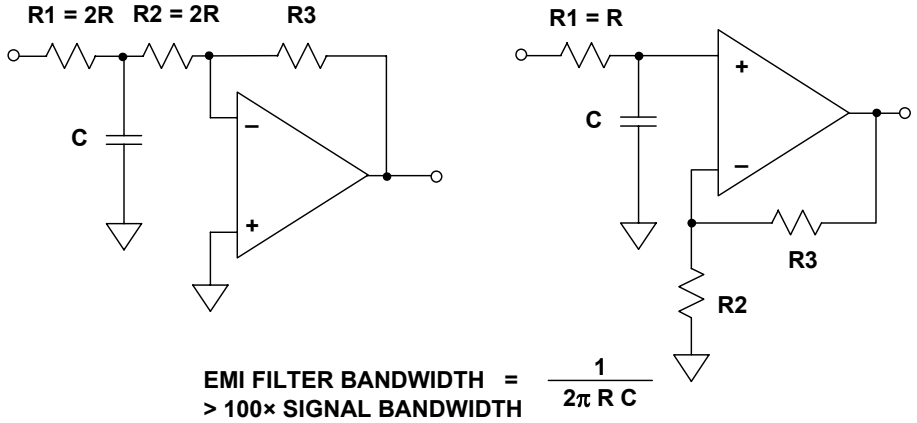


Figure 7-111: *Simple EMI/RFI noise filters for op amp circuits*

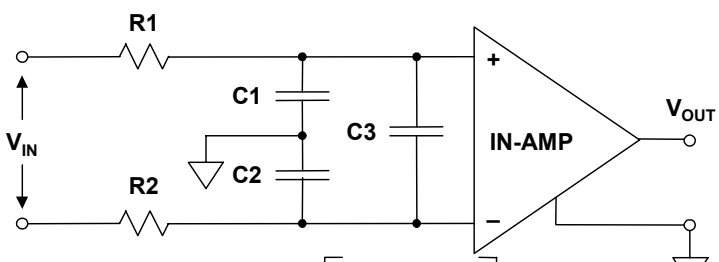
For the non-inverting case on the right, capacitor C can be connected directly to the op amp input as shown, and an input resistor with a value "R" yields the same corner frequency as the inverting case. In both cases low inductance chip-style capacitors should be used, such as NP0 ceramics. The capacitor should in any case be free of losses or voltage coefficient problems, which limits it to either the NP0 mentioned, or a film type.

It should be noted that a ferrite bead can be used instead of R1, however ferrite bead impedance is not well controlled and is generally no greater than 100Ω at 10MHz to 100MHz. This requires a large value capacitor to attenuate lower frequencies.

In-amp inputs

Precision in-amps are particularly sensitive to dc offset errors due to the presence of CM EMI/RFI. This is very much like the problem in op amps. And, as is true with op amps, the sensitivity to EMI/RFI is more acute with the lower power in-amp devices.

A general-purpose approach to proper filtering for device level application of in-amps is shown in Figure 7-112. In this circuit the in-amp could in practice be any one of a number of devices. The relatively complex balanced RC filter preceding the in-amp performs all of the high frequency filtering. The in-amp would be programmed for the gain required in the application, via its gain-set resistance (not shown).



$$\tau_{DIFF} = (R1 + R2)\left[\frac{C1 \cdot C2}{C1 + C2} + C3\right]$$

$$\tau_{CM} = R1 \cdot C1 = R2 \cdot C2$$

$$\tau_{DIFF} >> \tau_{CM}$$

R1•C1 = R2•C2
R1 = R2 SHOULD BE 1% RESISTORS
C1 = C2 SHOULD BE ≤ 5% CAPACITORS

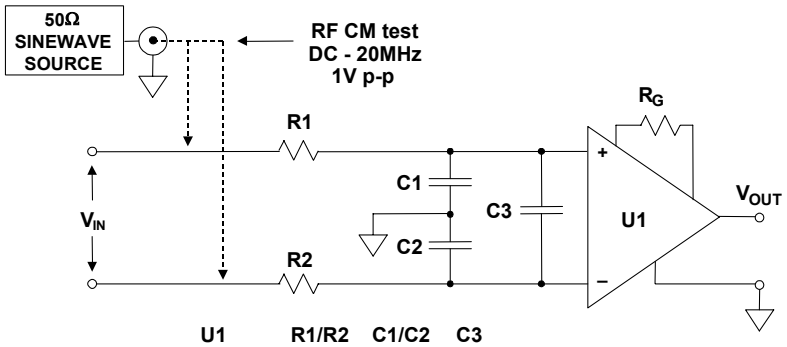
$$\text{DIFFERENTIAL FILTER BANDWIDTH} = \frac{1}{2\pi\,(R1 + R2)\left[\frac{C1 \cdot C2}{C1 + C2} + C3\right]}$$

Figure 7-112: *A general-purpose common-mode/differential-mode RC EMI/RFI filter for in-amps*

Within the filter, note that fully balanced filtering is provided for both CM (R1-C1 and R2-C2) as well as differential mode (DM) signals (R1+R2, and C3 || the series connection of C1-C2). If R1-R2 and C1-C2 aren't well matched, some of the input common-mode signal at V_{IN} will be converted to a differential mode signal at the in-amp inputs. For this reason, C1 and C2 should be matched to within at least 5% of each other. Also, R1 and R2 should be 1% metal film resistors, so as to aid this matching. It is assumed that the source resistances seen at the V_{IN} terminals are low with respect to R1-R2, and matched. In this type of filter, C3 should be chosen much larger than C1 or C2 (C3 ≥ C1, C2), in order to suppress spurious differential signals due to CM⇒DM conversion resulting from mismatch of the R1-C1 and R2-C2 time constants.

The overall filter bandwidth should be at least 100 times the input signal bandwidth. Physically, the filter components should be symmetrically mounted on a PC board with a large area ground plane and placed close to the in-amp inputs for optimum performance.

Figure 7-113 shows a family of these filters, as suited to a range of different in-amps. The RC components should be tailored to the different in-amp devices, as per the table. These filter components are selected for a reasonable balance of low EMI/RFI sensitivity and a low increase in noise (vis-à-vis that of the related in-amp, without the filter).



U1	R1/R2 1%	C1/C2 ≤5%	C3 10%
AD620/621/622	4.02k	1nF	47nF
AD623	10k	1nF	22nF
AD627	20k	1nF	22nF

Figure 7-113: *Flexible common-mode and differential-mode RC EMI/RFI filters are useful with the AD620 series, the AD623, AD627, and other in-amps*

To test the EMI/RFI sensitivity of the configuration, a 1Vp-p CM signal can be applied to the input resistors, as noted. With a typically used in-amp such as the AD620 working at a gain of 1000, the maximum RTI input offset voltage shift observed was 1.5µV over the 20MHz range. In the AD620 filter example, the differential bandwidth is about 400 Hz.

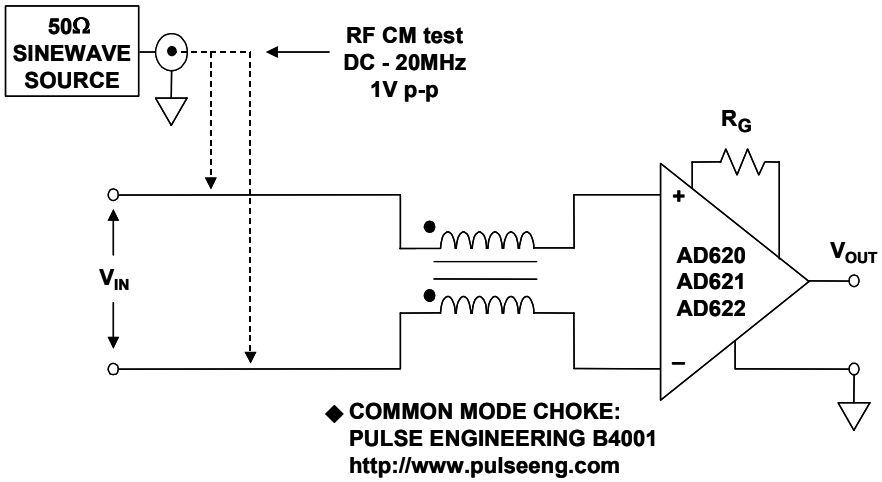


Figure 7-114: *For simplicity as well as lowest noise EMI/RFI filter operation, a common-mode choke is useful with the AD620 series in-amp devices*

Common-mode chokes offer a simple, one-component EMI/RFI protection alternative to the passive RC filters, as shown in Figure 7-114.

In addition to being a low component count approach, choke-based filters offer low noise, by dispensing with the resistances. Selecting the proper common-mode choke is critical, however. The choke used in the circuit of Figure 7-114 is a Pulse Engineering B4001. The maximum RTI offset shift measured from DC to 20MHz at G = 1000 was 4.5µV. Either an off-the-shelf choke such as the B4001 can be used for this filter, or, alternately one can be constructed. Since balance of the windings is important, bifilar wire is suggested. The core material must of course operate over the expected frequency band. Note that, unlike the Figure 7-113 family of RC filters, a choke-only filter offers no differential filtration. Differential mode filtering can be optionally added, with a second stage following the choke, by adding the R1-C3-R2 connections of Figure 7-112.

For further information on in-amp EMI/RFI filtering, see References 10, and 12 - 15.

Amplifier outputs and EMI/RFI

In addition to filtering the input and power pins, amplifier *outputs* also need to be protected from EMI/RFI, especially if they must drive long lengths of cable, which act as antennas. RF signals received on an output line can couple back into the amplifier input where it is rectified, and appears again on the output as an offset shift.

A resistor and/or ferrite bead, or both, in series with the output is the simplest and least expensive output filter, as shown in Figure 7-115 (upper circuit).

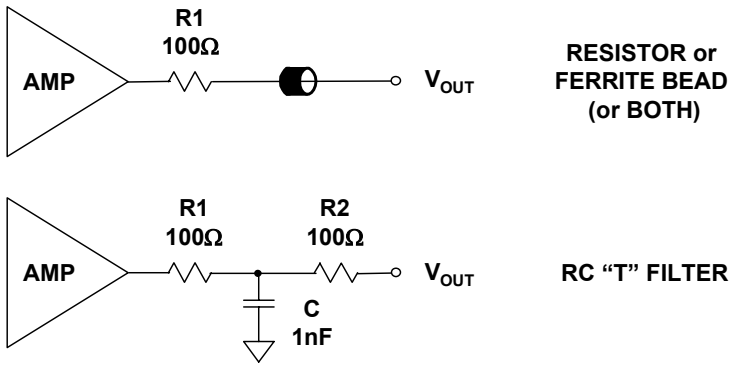


Figure 7-115: *Op amp and in-amp outputs should be protected against EMI/RFI, particularly if they drive long cables.*

Adding a resistor-capacitor-resistor "T" circuit as shown in Figure 7-115 (lower circuit) improves this filter with just slightly more complexity. The output resistor and capacitor divert most of the high frequency energy away from the amplifier, making this configuration useful even with low power active devices. Of course, the time constant of the filter parts must be chosen carefully, to minimize any degradation of the desired output signal. In this case the RC components are chosen for an approximate 3MHz signal bandwidth, suitable for instrumentation or other low bandwidth stages.

Printed Circuit Board Design for EMI/RFI Protection

This section summarizes general points on EMI/RFI with respect to the printed circuit board (PCB) layout. It complements earlier chapter discussions on general PCB design techniques.

When a PCB design has not been optimized in terms of EMI/RFI, system performance can be compromised. This is true not only for signal-path performance, but also for the system's susceptibility to EMI, plus the degree of EMI radiated by the system. Failure to implement sound PCB layout techniques will very likely lead to system/instrument EMC failures.

To summarize earlier points of this section, a real-world PCB layout may allow multiple paths through which high-frequency noise can couple/radiate into and/or out of the circuit. This is especially true for digital circuitry, operating at high *edge rates*. It is the rapid changes of logic state ($1 \Rightarrow 0$ or $0 \Rightarrow 1$), i.e., the edge rate which contains the HF energy which can easily radiate as EMI. While similar points are applicable to precision high-speed analog or mixed analog/digital circuits, logic devices are by far the worst potential EMI offenders. Identifying critical circuits and paths helps in designing the PCB for both low emissions and susceptibility to radiated and conducted external and internal noise sources.

Choose logic devices carefully!

Logic family speaking, a key point in minimizing system noise problems is to *choose devices no faster than actually required by the application*. Many designers assume that faster is always better— fast logic is better than slow, high bandwidth amplifiers better than low bandwidth ones, and fast DACs and ADCs are better, even if the speed isn't required by the system. Unfortunately, faster is *not* better, and actually may be worse for EMI concerns.

Many fast DACs and ADCs have digital inputs and outputs with edge rates in the 1ns/V region. Because of this wide bandwidth, the sampling clock and the digital inputs can respond to any form of high frequency noise, even glitches as narrow as 1 to 3ns. These high speed data converters and amplifiers are thus easy prey for the high frequency noise of microprocessors, digital signal processors, motors, switching regulators, hand-held radios, electric jackhammers, etc. With some of these high-speed devices, a small amount of input/output filtering may be required to desensitize the circuit from its EMI/RFI environment. A ferrite bead just before the local decoupling capacitor is very effective in filtering high frequency noise on supply lines. Of course, with circuits requiring bipolar supplies, this technique should be applied to both positive and negative supply lines.

To help reduce emissions generated by extremely fast moving digital signals at DAC inputs or ADC outputs, a small resistor or ferrite bead may be required at each digital input/output.

Design PCBs thoughtfully

Once the system's critical paths and circuits have been identified, the next step in implementing sound PCB layout is to partition the printed circuit board according to circuit function. This involves the appropriate use of power, ground, and signal planes. Good PCB layouts also isolate critical analog paths from sources of high interference (I/O lines and connectors, for example). High frequency circuits (analog and digital) should be separated from low frequency ones. Furthermore, automatic signal routing

CAD layout software should be used with extreme caution. Critical signal paths should be routed by hand, to avoid undesired coupling and/or emissions.

Properly designed multilayer PCBs can reduce EMI emissions and increase immunity to RF fields, by a factor of 10 or more, compared to double-sided boards. A multilayer board allows a complete layer to be used for the ground plane, whereas the ground plane side of a double-sided board is often disrupted with signal crossovers, etc. If the system has separate analog and digital ground and power planes, the analog ground plane should be underneath the analog power plane, and similarly, the digital ground plane should be underneath the digital power plane. There should be no overlap between analog and digital ground planes, nor analog and digital power planes.

Designing Controlled Impedances Traces on PCBs

A variety of trace geometries are possible with controlled impedance designs, and they may be either integral to or allied to the PCB pattern. In the discussions below, the basic patterns follow those of the IPC, as described in standard 2141 (see Reference 16).

Note that the figures below use the term "ground plane". It should be understood that this plane is in fact a large area, low impedance *reference* plane. In practice it may actually be either a ground plane or a power plane, both of which are assumed to be at zero ac potential.

The first of these is the simple wire-over-a-plane form of transmission line, also called a *wire microstrip*. A cross-sectional view is shown in Figure 7-116. This type of transmission line might be a signal wire used within a breadboard, for example. It is composed simply of a discrete insulated wire spaced a fixed distance over a ground plane. The dielectric would be either the insulation wall of the wire, or a combination of this insulation and air.

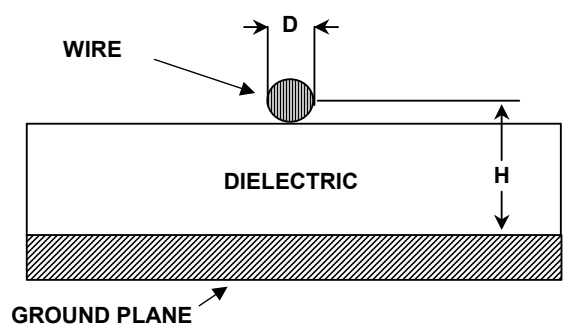


Figure 7-116: *A* wire microstrip *transmission line with defined impedance is formed by an insulated wire spaced from a ground plane*

The impedance of this line in ohms can be estimated with Eq. 7-16. Here D is the conductor diameter, H the wire spacing above the plane, and ε_r the dielectric constant.

$$Z_O(\Omega) = \frac{60}{\sqrt{\varepsilon_r}} \ln\left[\frac{4H}{D}\right] \qquad \text{Eq. 7-16}$$

For patterns integral to the PCB, there are a variety of geometric models from which to choose, single-ended and differential. These are covered in some detail within IPC standard 2141 (see Reference 16), but information on two popular examples is shown here.

Before beginning any PCB-based transmission line design, it should be understood that there are abundant equations, all claiming to cover such designs. In this context, "Which of these are accurate?" is an extremely pertinent question. The unfortunate answer is, *none are perfectly so!* All of the existing equations are approximations, and thus accurate to varying degrees, depending upon specifics. The best known and most widely quoted equations are those of Reference 16, but even these come with application caveats.

Reference 17 has evaluated the Reference 16 equations for various geometric patterns against test PCB samples, finding that predicted accuracy varies according to target impedance. Reference 18 also evaluates the Reference 16 equations, offering an alternative and even more complex set (see Reference 19). The equations quoted below are from Reference 16, and are offered here as a starting point for a design, subject to further analysis, testing and design verification. The bottom line is, study carefully, and take PCB trace impedance equations with a proper dose of salt.

Microstrip PCB transmission lines

For a simple two-sided PCB design where one side is a ground plane, a signal trace on the other side can be designed for controlled impedance. This geometry is known as a *surface microstrip,* or more simply, *microstrip*.

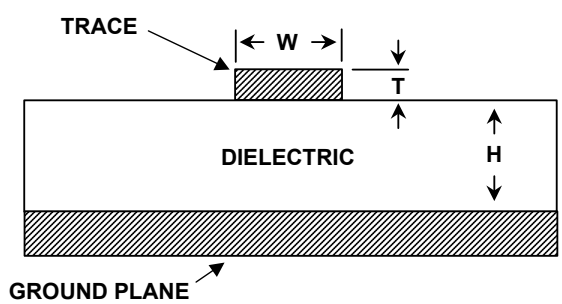


Figure 7-117: *A microstrip transmission line with defined impedance is formed by a PCB trace of appropriate geometry, spaced from a ground plane*

A cross-sectional view of a two-layer PCB illustrates this microstrip geometry as shown in Figure 7-117.

For a given PCB laminate and copper weight, note that all parameters will be predetermined except for W, the width of the signal trace. Eq. 7-17 can then be used to design a PCB trace to match the impedance required by the circuit. For the signal trace of width W and thickness T, separated by distance H from a ground (or power) plane by a PCB dielectric with dielectric constant ε_r, the characteristic impedance is:

$$Z_O(\Omega) = \frac{87}{\sqrt{\varepsilon_r + 1.41}} \ln\left[\frac{5.98H}{(0.8W + T)}\right] \qquad \text{Eq. 7-17}$$

Note that in these expressions, measurements are in common dimensions (mils).

These transmission lines will have not only a characteristic impedance, but also capacitance. This can be calculated in terms of pF/in as shown in Eq. 7-18.

$$C_O(\text{pF/in}) = \frac{0.67(\varepsilon_r + 1.41)}{\ln[5.98H/(0.8W + T)]} \qquad \text{Eq. 7-18}$$

As an example including these calculations, a 2-layer board might use 20-mil wide (W), 1 ounce (T=1.4) copper traces separated by 10-mil (H) FR-4 (ε_r =4.0) dielectric material. The resulting impedance for this microstrip would be about 50Ω. For other standard impedances, for example the 75Ω video standard, adjust "W" to about 8.3 mils.

Some Microstrip rules-of-thumb

This example touches an interesting and quite handy point. Reference 17 discusses a useful rule of thumb pertaining to microstrip PCB impedance. For a case of dielectric constant of 4.0 (FR-4), it turns out that when W/H is 2/1, the resulting impedance will be close to 50Ω (as in the first example, with W=20 mils).

Careful readers will note that Eq. 7-17 predicts Z_o to be about 46Ω, generally consistent with accuracy quoted in Reference 17 (>5%). The IPC microstrip equation is most accurate between 50 and 100Ω, but is substantially less so for lower (or higher) impedances. Reference 20 gives tabular results of various PCB industry impedance calculator tools.

The propagation delay of the microstrip line can also be calculated, as per Eq. 7-19. This is the one-way transit time for a microstrip signal trace. Interestingly, for a given geometry model, *the delay constant in ns/ft is a function only of the dielectric constant, and not the trace dimensions* (see Reference 21). Note that this is quite a convenient situation. It means that, with a given PCB laminate (and given ε_r), the propagation delay constant is fixed for various impedance lines.

$$t_{pd}(\text{ns/ft}) = 1.017\sqrt{0.475\varepsilon_r + 0.67} \qquad \text{Eq. 7-19}$$

This delay constant can also be expressed in terms of ps/in, a form which will be more practical for smaller PCBs. This is:

$$t_{pd}(\text{ps/in}) = 85\sqrt{0.475\varepsilon_r + 0.67} \qquad \text{Eq. 7-20}$$

Thus for an example PCB dielectric constant of 4.0, it can be noted that a microstrip's delay constant is about 1.63ns/ft, or 136ps/in. These two additional rules-of-thumb can be useful in designing the timing of signals across PCB trace runs.

Symmetric Stripline PCB transmission lines

A method of PCB design preferred from many viewpoints is a multi-layer PCB. This arrangement *embeds* the signal trace between a power and a ground plane, as shown in the cross-sectional view of Figure 7-118. The low-impedance ac-ground planes and the embedded signal trace form a *symmetric stripline* transmission line.

As can be noted from the figure, the return current path for a high frequency signal trace is located directly above and below the signal trace on the ground/power planes. The high frequency signal is thus contained entirely inside the PCB, minimizing emissions, and providing natural shielding against incoming spurious signals.

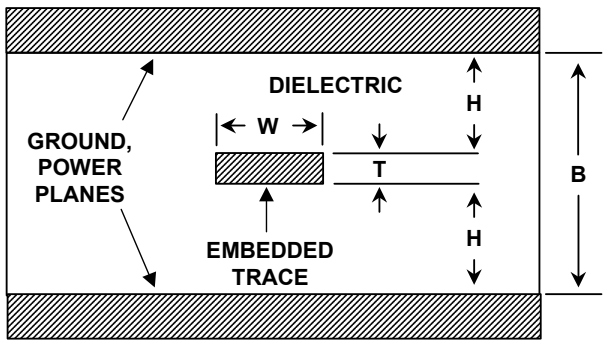


Figure 7-118: *A symmetric stripline transmission line with defined impedance is formed by a PCB trace of appropriate geometry embedded between equally spaced ground and/or power planes*

The characteristic impedance of this arrangement is again dependent upon geometry and the ε_r of the PCB dielectric. An expression for Z_O of the stripline transmission line is:

$$Z_O(\Omega) = \frac{60}{\sqrt{\varepsilon_r}} \ln\left[\frac{1.9(B)}{(0.8W + T)}\right] \qquad \text{Eq. 7-21}$$

Here, all dimensions are again in mils, and B is the spacing between the two planes. In this symmetric geometry, note that B is also equal to 2H + T. Reference 17 indicates that the accuracy of this Reference 16 equation is typically on the order of 6%.

Another handy rule-of-thumb for the symmetric stripline in an $\varepsilon_r = 4.0$ case is to make B a multiple of W, in the range of 2 to 2.2. This will result in an stripline impedance of about 50Ω. Of course this rule is based on a further approximation, by neglecting T. Nevertheless, it is still useful for ballpark estimates.

The symmetric stripline also has a characteristic capacitance, which can be calculated in terms of pF/in as shown in Eq. 7-22.

$$C_O(\text{pF/in}) = \frac{1.41(\varepsilon_r)}{\ln[3.81H/(0.8W + T)]} \qquad \text{Eq. 7-22}$$

The propagation delay of the symmetric stripline is shown in eq. 7-23.

$$t_{pd}(\text{ns/ft}) = 1.017\sqrt{\varepsilon_r} \qquad \text{Eq. 7-23}$$

or, in terms of ps:

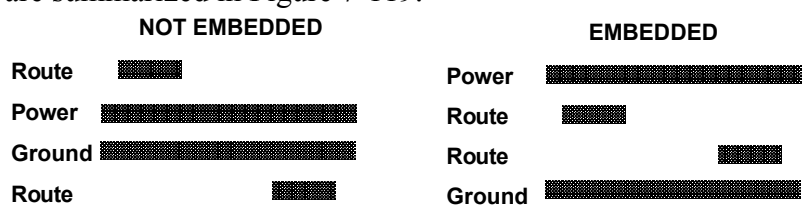
$$t_{pd}(\text{ps/in}) = 85\sqrt{\varepsilon_r} \qquad \text{Eq. 7-24}$$

For a PCB dielectric constant of 4.0, it can be noted that the symmetric stripline's delay constant is almost exactly 2ns/ft, or 170ps/in.

Some Pros and Cons of Embedding Traces

The above discussions allow the design of PCB traces of defined impedance, either on a surface layer or embedded between layers. There of course are many other considerations beyond these impedance issues.

Embedded signals do have one major and obvious disadvantage— the debugging of the hidden circuit traces is difficult to impossible. Some of the pros and cons of embedded signal traces are summarized in Figure 7-119.



- Advantages
  - Signal traces shielded and protected
  - Lower impedance, thus lower emissions and crosstalk
  - Significant improvement > 50MHz
- Disadvantages
  - Difficult prototyping and troubleshooting
  - Decoupling may be more difficult
  - Impedance may be too low for easy matching

Figure 7-119: *The pros and cons of not embedding vs. the embedding of signal traces in multi-layer PCB designs*

Multi-layer PCBs can be designed *without* the use of embedded traces, as is shown in the left-most cross-sectional example. This embedded case could be considered as a doubled two-layer PCB design (i.e., four copper layers overall). The routed traces at the top form a microstrip with the power plane, while the traces at the bottom form a microstrip with the ground plane. In this example, the signal traces of both outer layers are readily accessible for measurement and troubleshooting purposes. But, the arrangement does nothing to take advantage of the shielding properties of the planes.

This non embedded arrangement will have greater emissions and susceptibility to external signals, vis-a-vis the embedded case at the right, which uses the embedding, and does take full advantage of the planes. As in many other engineering efforts, the decision

of embedded vs. not-embedded for the PCB design becomes a tradeoff, in this case one of reduced emissions vs. ease of testing.

Transmission Line Termination Rule-of-Thumb

Much has been written about terminating PCB traces in their characteristic impedance, to avoid signal reflections. A good rule-of-thumb to determine when this is necessary is as follows: *Terminate the transmission line in its characteristic impedance when the one-way propagation delay of the PCB track is equal to or greater than one-half the applied signal rise/fall time (whichever edge is faster*). For example, a 2 inch microstrip line over an Er=4.0 dielectric would have a delay of ~270ps. Using the above rule strictly, termination would be appropriate whenever the signal rise time is < ~500ps. A more conservative rule is to use a 2 inch (PCB track length)/nanosecond (rise/fall time) rule. If the signal trace exceeds this trace-length/speed criterion, then termination should be used.

For example, PCB tracks for high-speed logic with rise/fall time of 5ns should be terminated in their characteristic impedance if the track length is equal to or greater than 10 inches (where measured length *includes* meanders).

In the analog domain, it is important to note that this same 2 inch/nanosecond rule of thumb should also be used with op amps and other circuits, to determine the need for transmission line techniques. For instance, if an amplifier must output a maximum frequency of f_{max}, then the equivalent risetime t_r is related to this f_{max}. This limiting risetime, t_r, can be calculated as:

$$t_r = 0.35/f_{max} \qquad \text{Eq. 7-25}$$

The maximum PCB track length is then calculated by multiplying t_r by 2 inch/nanosecond. For example, a maximum frequency of 100MHz corresponds to a risetime of 3.5ns, so a 7 inch or more track carrying this signal should be treated as a transmission line.

The best ways to keep sensitive analog circuits from being affected by fast logic are to physically separate the two by the PCB layout, and to use no faster logic family than is dictated by system requirements. In some cases, this may require the use of several logic families in a system. An alternative is to use series resistance or ferrite beads to slow down the logic transitions where highest speed isn't required.

A general method of doing this is to use a series R at a logic driver output, and a shunt C at a CMOS gate input. The series resistance and the net input capacitance of the gate form a lowpass filter. Typical CMOS input capacitance is 10pF. Locate the series resistor close to the driving gate, adding an additional small capacitance, as needed. The resistor minimizes transient switching currents, and may also eliminate the necessity for transmission line techniques. The value of the resistor should be chosen such that the rise and fall times at the receiving gate are fast enough to meet system requirement, but no faster. Also, make sure that the resistor is not so large that the logic levels at the receiver are out of specification because of the source and sink current which must flow through the resistor. Use of CMOS logic will simplify this, since the input currents are so low.

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Chip Center's "Signal Integrity" page, http://www.chipcenter.com/signalintegrity

Kimmel Gerke Associates website, http://www.emiguru.com

Henry Ott website, http://www.hottconsultants.com

IEEE EMC website, http://www.ewh.ieee.org/soc/emcs

Mark Montrose website, http://www.montrosecompliance.com/index.html

Tim Williams website, http://www.elmac.co.uk

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SECTION 7-7: SIMULATION, BREADBOARDING AND PROTOTYPING

Joe Buxton, Walt Kester, James Bryant, Walt Jung

In this final section of the chapter, the practical aspects of assembling hardware for op amp and other analog functions are brought to play. Various experimental techniques are useful towards verifying the integrity of a design. These include electronic *analog circuit simulation* programs, to be used with (but not to the exclusion of) the allied lab processes of *breadboarding* and *prototyping*.

Analog Circuit Simulation

In the past decade, circuit simulation has taken on an increasingly important role within analog circuit design. The most popular simulation tool for this is SPICE, which is available in multiple forms for various computer platforms (see References 1 and 2). However, to achieve meaningful simulation results, designers need accurate models of many system components. The most critical of these are realistic models for ICs, the active devices that drive modern designs. In the early 1990's, Analog Devices developed an advanced op amp SPICE model, which is in fact still in use today (see References 3 and 4). Within this innovative open amplifier architecture, gain and phase response can be fully modeled, enabling designers to accurately predict ac, dc, and transient performance behavior. This modeling methodology has also been extended to include other devices such as in-amps, voltage references, and analog multipliers.

- **Understand Realistic Simulation Goals**
- **Evaluate Available Models Accordingly**
- **Know the Capabilities for Each Competing Op Amp Model**
- **Following Simulation, *Breadboarding is Always Desirable and Necessary***

Figure 7-120: *Used wisely, simulation is a powerful design tool*

Figure 7-120 lists some major SPICE simulation objectives. The popularity of SPICE simulation has led to many op amp macromodel releases, which (ideally) software-mimic amplifier electrical performance. With numerous models available, several confusions are possible. There may be uncertainty as to what is/isn't modeled, plus a basic question of *model accuracy*. All of these points are important, in order to place confidence in simulation results. So, *verification* of a model is important, checking it by comparison to the actual device performance conditions, before trusting it for serious designs.

Of course, a successful first design step using an accurate op amp model by itself doesn't necessarily guarantee totally valid simulations. A simulation based on incomplete information has limited value. All parts of a target circuit should be modeled, including the surrounding passive components, various parasitic effects, and temperature changes. Then, the circuit needs to be verified in the lab, by breadboarding and prototyping. A breadboard circuit is a quickly executed mockup of a circuit design using a semi-permanent lab platform, i.e., one which is less than final physical form. It is intended to show real performance, but without the total physical environment. A good breadboard can often reveal behavior not predicted by SPICE, either because of an incomplete

model, external circuit parasitics, or numerous other reasons. However, by using SPICE along with intelligent breadboarding techniques, a circuit can be efficiently and quickly designed with reasonably good assurance of working properly on a prototype version, or even a final PCB. The following prototype phase is just one step removed from a final PCB, and may in fact be an actual test PCB, with nearly all design components incorporated, and with close to full performance.

The breadboard/prototype design steps are closely allied to simulation, usually following it in the overall design process. These are more fully discussed in subsequent sections.

Macromodel vs. Micromodel

The distinction between *macromodel* and *micromodel* is often unclear. A micromodel uses the actual *transistor level* and other SPICE models of an IC device, with all active and passive parts fully characterized according to the manufacturing process. In differentiating this type of model from a macromodel, some authors use the term *device level model* to describe the resulting overall op amp model (see Reference 5). Typically, a micromodel is used in the actual design process of an IC.

	METHODOLOGY	ADVANTAGES	DISADVANTAGES
MACROMODEL	Ideal Elements Model Device Behavior	Fast Simulation Time, Easily Modified	May Not Model All Characteristics
MICROMODEL	Fully Characterized Transistor Level Circuit	Most Complete Model	Slow Simulation, Convergence Difficulty, Non-Availability

Figure 7-121: *Differentiating the Macromodel and Micromodel*

A macromodel goes another route in emulating op amp performance. Taking into consideration final device performance, it uses ideal native SPICE elements to model observed behavior— as many as necessary. In developing a macromodel, a real device is measured in terms of lab and data sheet performance, and the macromodel is adjusted to match this behavior. Some aspects of performance may be sacrificed in doing this. Figure 7-121 compares the major pros and cons between macromodels and micromodels.

There are advantages and disadvantages to both approaches. A micromodel can give a complete and accurate model of op amp circuit behavior under almost all conditions. But, because of a large number of transistors and diodes with non-linear junctions, simulation time is very long. Of course, manufacturers are also reluctant to release such models, since they contain proprietary information. And, even though all transistors may be included, this isn't a guarantee of total accuracy, as the transistor models themselves don't cover all operational regions precisely. Furthermore, with a high node count, SPICE can have convergence difficulties, causing a failed simulation. This point would make a micromodel virtually useless for multiple amplifier active filters, for example.

On the other hand, a carefully developed macromodel can produce both accurate results and simulation time savings. In more advanced macromodels such as the ADSpice model

described below, transient and ac device performance can be closely replicated. Op amp non-linear behavior can also be included, such as output voltage and current swing limits.

However, because these macromodels are still simplifications of real devices, all non-linearities aren't modeled. For example, not all ADSpice models include common mode input voltage range, or noise (while more recent ones do). Typically, in model development parameters are optimized as may be critical to the intended application— for example, ac and transient response. Including every possible characteristic could lead to cumbersome macromodels that may even have convergence problems. Thus, ADSpice macromodels include those op amp behavior characteristics critical to intended performance for normal operating conditions, but not necessarily all non-linear behavior.

The ADSpice Op Amp Macromodels

The basic ADSpice model was developed as an op amp macromodeling advance, and as an improved design tool for more accurate application circuit simulations. Since being introduced in 1990, it has become a standard op amp macromodel topology, as evidenced by industry adoption of the frequency shaping concepts (see References 6 and 7).

Prior to about 1990, a dominant op amp model architecture was the Boyle model (see Reference 8). This macromodel, developed in the early 70's, cannot accurately model higher speed amplifiers. The primary reason for this is that it has limited frequency shaping ability— only two poles and no zeroes. In contrast, the ADSpice model topology has a flexible and open architecture, allowing virtually unlimited pole and zero frequency shaping stages to be cascaded. This key difference provides much more accurate ac and transient response, vis-à-vis the more simplistic Boyle model topology.

An ADSpice model is comprised of three main portions, described as follows. The first of these is a combined input and gain stage, which will include transistor models as appropriate to the device being modeled (NPN or PNP bipolar, JFET, MOSFET, etc.). Next are the synthetic pole and zero stages, which are comprised of ideal SPICE native elements. There may be only a few of these or there may be many, dependent on the complexity of the op amp's frequency response. Finally, there is an output stage, which couples the first two sections to the outside world.

Before describing these sections in detail, it is important to realize that many variations upon what is shown below do in fact exist. This is due to not just differences from one op amp model to another, but also to evolutionary topology developments in op amp hardware, which in turn has led to corresponding modeling changes. For example, modern op amps often include either rail-rail output or input stages, or both. Consequently more recent developments in the ADSpice models have addressed these issues, along with corresponding model developments.

Furthermore, although the Boyle model and the original ADSpice models were designed to support *voltage feedback* op amp topologies, subsequent additions have added *current feedback* amplifier topologies. In fact, Reference 9 describes an ADSpice current feedback macromodel which appeared just shortly after the voltage feedback model of Reference 3. These current feedback macromodels are discussed in more detail below.

Input and Gain/Pole stages

A basic ADSpice voltage feedback op amp macromodel input stage is shown in Figure 7-122. As noted, it uses what are (typically) the only transistors in the entire model, in this example the Q1-Q2 NPN pair, to the left on the diagram. These are needed to properly model an op amp's differential input stage characteristics. A basic tenet of this model topology is that this stage is designed for unity gain, by the proper choice of Q1-Q2 operating current and gain-setting resistors R3-R4 and R5-R6.

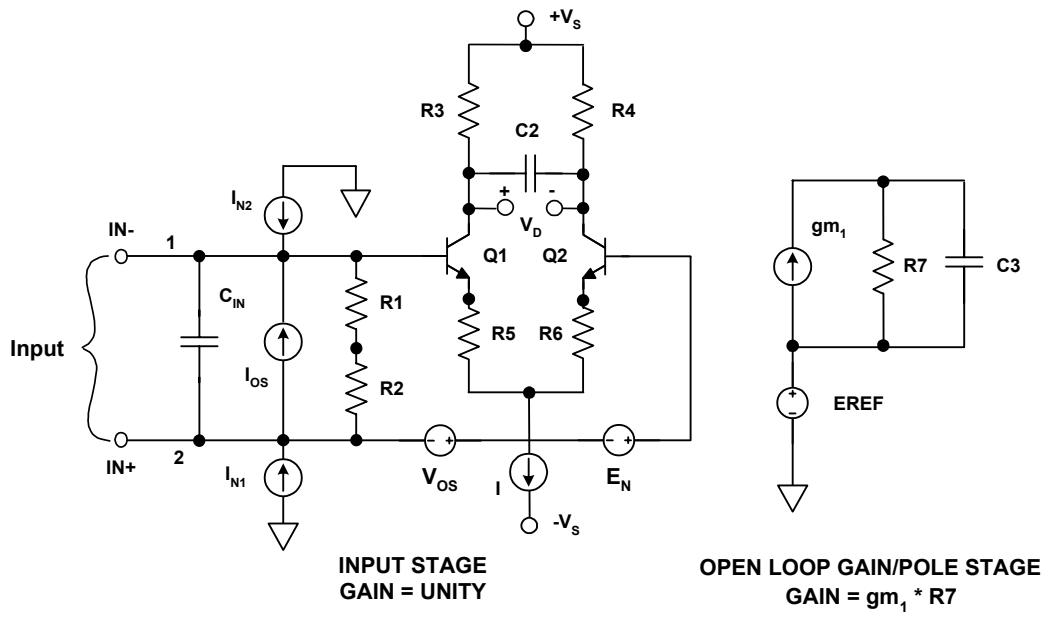


Figure 7-122: *Input and gain/pole stages of ADSpice macromodel*

Although this example uses NPN transistors, the input stage is easily modified to use PNP bipolars, JFET, or MOSFET devices. The rest of the input stage uses simple SPICE elements such as resistors, capacitors, and controlled sources.

The open-loop gain vs. frequency characteristics of the modeled op amp is provided by the gain stage, to the right in the diagram. Here controlled source gm_1 senses the differential collector voltage V_D from the input stage, converting this voltage to a proportional current. The gm_1 output current flows in load resistor R_7, producing a single ended voltage referenced to an internal voltage, EREF. Typically, this voltage is derived as a supply voltage midpoint, and is used throughout the model.

By simply making the gm_1-R_7 product equal to the specified gain of the op amp, this stage produces the entire open-loop gain of the macromodel. This design factor means that all other model stages operate at unity gain, a feature leading to significant flexibility in adding and deleting subsequent stages. This approach allows the quick synthesis of the complex ac characteristics typical of high performance, high speed op amps. In addition, this stage also provides the dominant pole of the amplifier's ac response. The open-loop pole frequency is set by selection of capacitor C3, as noted in the diagram.

Frequency Shaping Stages

Following the gain stage of the macromodel is a variable but unlimited number of pole and/or zero stages, which in combination provide frequency response shaping. Typical topologies for these stages are as shown in the Figure 7-123 diagram. The stages can be either a single pole or a single zero, or combined pole/zero or zero/pole stages. All such stages have a dc transfer gain of unity, and a given amplifier type can have all or just a few of these stages, as may be require to synthesize its response.

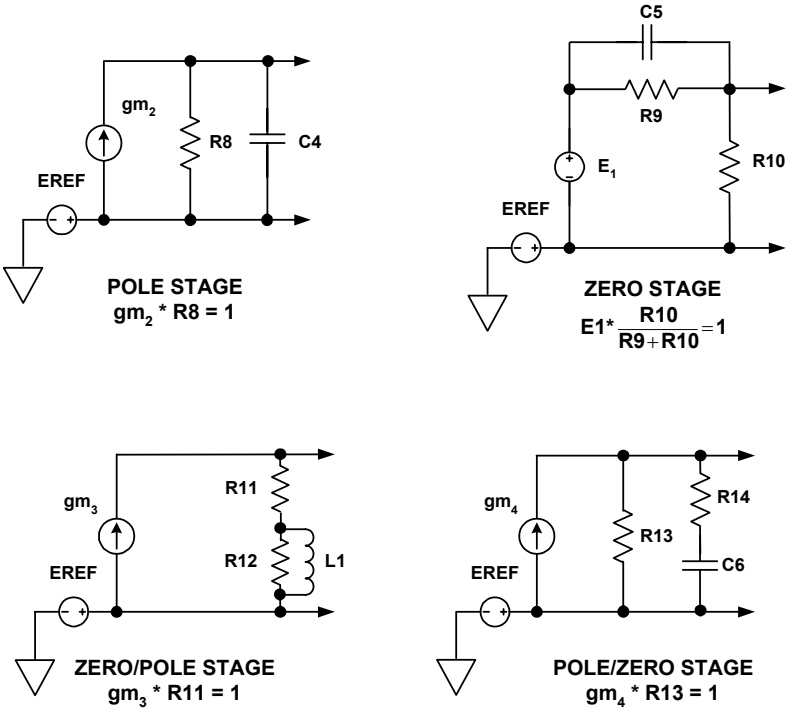


Figure 7-123: *The frequency shaping stages possible within the ADSpice model*

The pole or zero frequency is set by the combination of the resistor(s) and capacitor, or resistor(s) and inductor, as may be the case. Because an infinite number of values are possible in SPICE, choice of RC values is somewhat arbitrary, and a wide range work. Early ADSpice models used relatively high values, while later ones employ lower values to reduce noise (described in more detail later). In all instances, it is assumed that each stage provides zero loading to the driving stage. The stages shown reflect no particular op amp, but example principles can be found within the OP27 model (see Reference 10).

Because all of these frequency-shaping stages are dc-coupled and have unity gain, any number of them can be added or deleted, with no affect on the model's low frequency response. Most importantly, the high frequency gain and phase response can be precisely tailored to match a real amplifier's response. The benefits of this frequency-shaping flexibility are especially apparent in performance comparisons of the ADSpice model closed loop pulse response and stability analysis, versus that of a more simplistic model. This point is demonstrated by a later example.

Macromodel output stages

A general form of the output stage for the ADSpice model, shown in Figure 7-124, models a number of important op amp characteristics. The Thevenin equivalent resistance of R_{O1} and R_{O2} mimics the op amp's dc open loop output impedance, while inductor L_O models the rise in impedance at high frequencies. A unity gain characteristic for the stage is set by the g_7-R_{O1} and g_8-R_{O2} products.

Additionally, output load current is correctly reflected in the supply currents. This feature is a significant improvement over the Boyle model, because the power consumption of the loaded circuit can be analyzed accurately. Furthermore, circuits using the op amp supply currents as part of the signal path can also be correctly simulated. The output stage shown is not intended to reflect any particular op amp, but close similarity is found within the AD817 model (see Reference 11).

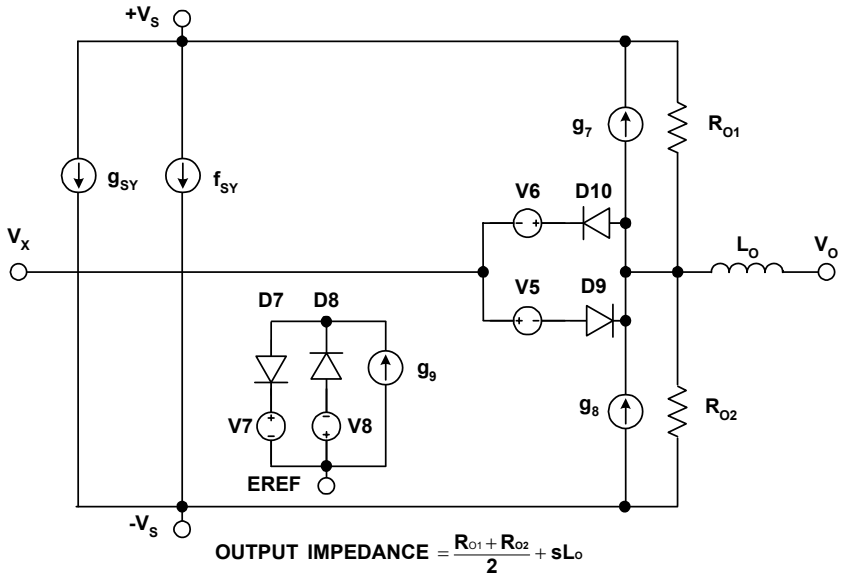


Figure 7-124: *General-purpose macromodel output stage*

With the recent advent of numerous rail-rail output stage op amps, a number of customized model topologies have been developed. This expands the ADSpice library to include rail-rail model behavior, matching op amp architectures using P and N MOSFET devices, as well as bipolar devices. Characteristically, a rail-rail output stage includes several key differentiating performance points. First and foremost is the ability to swing the op amp output to within a few mV of both supplies. A second point is the fact that such an output stage has a voltage gain greater than one, and a third is the relatively high output impedance (high as contrasted to traditional emitter follower outputs).

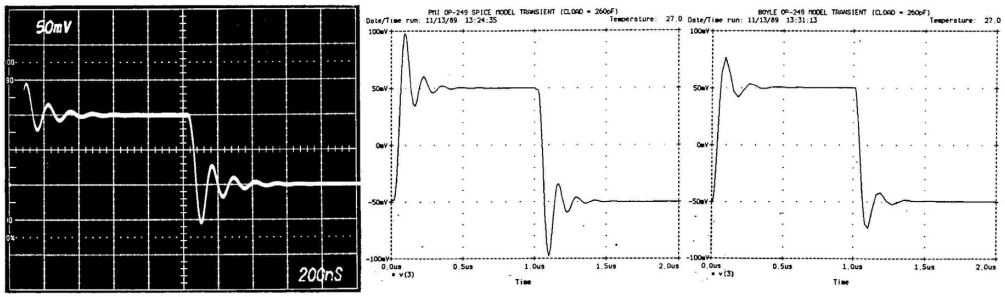
Examples of several modeling approaches to rail-rail output stages are found in the ADI SPICE macromodel library. Reference 12 employs CMOS devices to realize a rail-rail output, while Reference 13 uses bipolar devices to the same end. The macromodels of References 14 and 15 use synthesis techniques to model rail-rail outputs. References 16-18 utilize combinations of selected discrete device models and synthesis techniques, to realize rail-rail output operation for both op amp and in-amp devices.

In addition to rail-rail output operation, many modern op amps also feature rail-rail *input stages*. Such stages essentially duplicate, for example, an NPN-based differential stage with a complementary PNP stage, both stages operating in parallel. This allows the op amp to provide a CM range that includes both supply rails. This performance feature can also be accomplished within CMOS op amps, using both a P and N type MOS differential pairs. Model examples reflecting rail-rail input stages include References 13, 14, and 17.

Model transient response

The performance advantage of the multiple pole/zero stages is readily demonstrated in a transient pulse response test, as in Figure 7-125. This figure compares an actual OP249 op amp, the ADSpice model, and the Boyle model. It reveals the improved execution resulting from the unlimited number of poles and zeros in this model.

The difference is easily apparent from this transient analysis plot for a unity gain follower circuit. An OP249 amplifier was used, with the output connected to the inverting input, and a 260pF capacitive load.



VERTICAL SCALE: 50mV / div.
HORIZONTAL SCALE: 200ns / div.

LOAD = 260pF

Figure 7-125: *A pulse response comparison of an OP249 follower (left) model favors the ADSpice model in terms of fidelity (center), but not the Boyle (right)*

As can be noted, this results in ringing, as seen in the op amp response (left). Note that the ADSpice model accurately predicts the amount of overshoot and frequency of the damped ringing (center). In contrast, the Boyle model (right) predicts about half the overshoot and significantly less ringing.

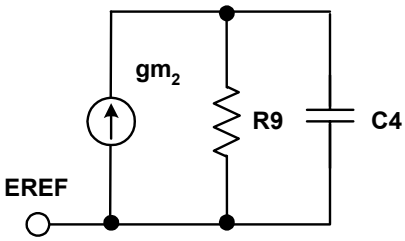
The Noise Model

An important enhancement to the ADSpice model is the ability to realistically model noise performance of an op amp. The capability to model a circuit's noise in SPICE can be appreciated by anyone who has tried to analyze noise by hand. A complete analysis is an involved and tedious task that involves adding all the individual noise contributions from all active devices and all resistors, and referring them to the input.

To aid this task, the ADSpice model was enhanced to include noise generators that accurately mimic the broadband and 1/f noise of an actual op amp. Conceptually, this involves first making an existing model noiseless, and then adding discrete noise generators, so as to emulate the target device. As noted earlier, all ADI models aren't

necessarily designed for this noise-accurate performance. Selected device models are designed for noise however, when their typical uses include low noise applications.

The first step is an exercise in scaling down the model internal impedances. For example, by reducing the resistances in the pole/zero stages from a base resistance of 1E6Ω to 1Ω, total noise is reduced dramatically, as figure 7-126 illustrates.



	CASE	
	"Noisy"	"Noiseless"
R9	$1x10^6\Omega$	1Ω
gm_2	$1x10^{-6}$	1.0
C4	$159x10^{-15}F$	$159x10^{-9}F$
Noise	129nV/√Hz	129pV/√Hz

Figure 7-126: *Towards achieving low noise operation, a first design step is the reduction of pole/zero cell impedances to low values*

For the "Noisy" column of the table, the noise from the pole stage shown with a large R9 resistor value is 129nV/$\sqrt{Hz}$. But when this resistor is scaled down by a factor of 10^6, to 1Ω , as in the "Noiseless" column, stage noise is 129pV/$\sqrt{Hz}$. Note also that transconductance and capacitance values are also scaled by the same factor, maintaining the same gain and pole frequency. To make the model's input stage noiseless, it is operated at a high current and with reduced load resistances, making noise contributions negligible. Extending these techniques to the entire model renders it essentially noiseless.

Once global noise reduction is achieved, independent noise sources are added, one for voltage noise and two for current noise. The basic noise source topology used is like Figure 7-127, and it can be set up to produce both voltage and current noise outputs.

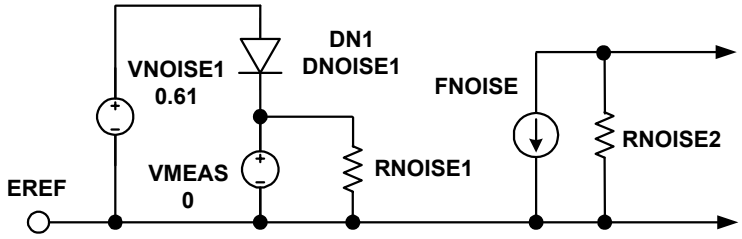


Figure 7-127: *A basic SPICE noise generator is formed with diodes, resistors, and controlled sources*

Note that, within SPICE, semiconductor models can generate 1/f (flicker) noise. The noise generators use diodes such as DN1 to produce this portion of the noise, modeling the 1/f noise of the op amp. By properly specifying diode model parameters and bias voltage VNOISE1, the 1/f noise is tailored to match the op amp. The noise current from DN1 passes through a zero voltage source. Here VMEAS is being used as a measurement device, combining the 1/f noise from DN1 and the broadband noise from RNOISE1.

RNOISE1 is selected for a value providing an appropriate broadband noise. The combined noise current in VMEAS is monitored by FNOISE, and appears as a voltage across RNOISE2. This voltage is then injected in series with one amplifier input via a

controlled voltage source, such as E_N of Figure 7-122 (see again). Either FNOISE or a controlled voltage source coefficient can be used for overall noise voltage scaling.

Current noise generation is similar to the above, except that the RNOISE2 voltage producing resistor isn't used, and two current-controlled sources drive the amplifier inputs. With all noise generators symmetrical about ground, dc errors aren't introduced.

Current Feedback Amplifier Models

As noted previously, a new model topology was developed for current feedback amplifiers, to accommodate their unique input stage structure (see Reference 9). The model uses a topology as shown in Figure 7-128 for the input and gain stages. The remaining model portions (not shown) contain multiple pole/zero stages and the output stage, and are essentially the same as voltage feedback amplifiers, described above.

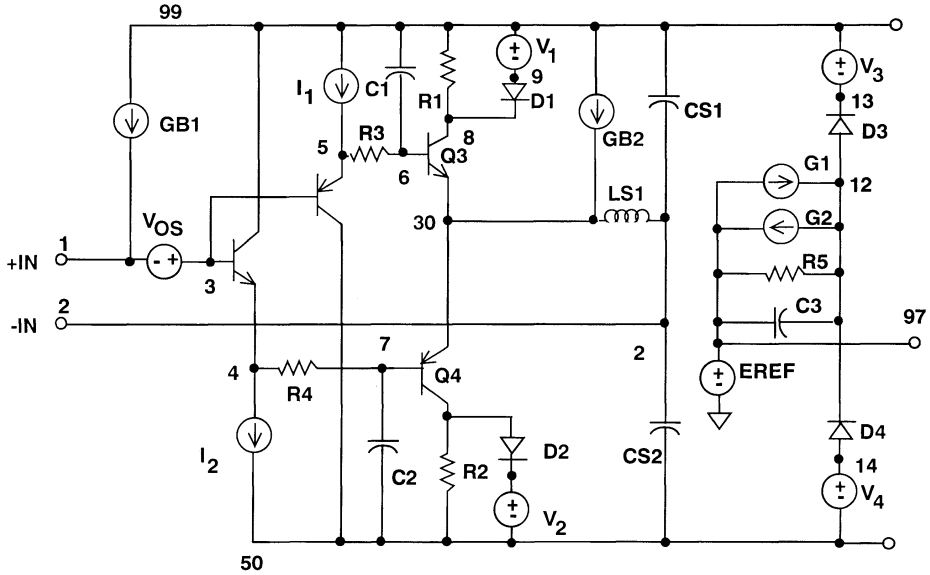


Figure 7-128: *Input and gain stages of current feedback op amp macromodel*

The four bipolar transistor input stage resembles actual current feedback amplifiers, with a high impedance non-inverting input (+IN) and a low impedance inverting input (-IN). In current feedback amplifiers, the maximum slew rate is very high, because dynamic slew current isn't limited to a differential pair tail current (as in voltage feedback op amps). In current feedback op amp designs, much larger amounts of error current can flow in the inverting input, as developed by the feedback network. Internally, this current flows in either Q3 or Q4, and charges compensation capacitor C3 via current mirrors.

The current mirrors of the ADSpice model are actually voltage controlled current sources in the gain stage, G1 and G2. They sense voltage drops across input stage resistors R1 and R2, and translating this into a C3 charging current. By making the value of G1 and G2 equal to the R1- R2 reciprocal, the slew currents will be identical. By clamping the R1-R2 voltage drops via D1-V1 and D2-V2, the maximum current is limited, which thus sets the highest slew rate. Open loop gain or transresistance of the model is set by R5, and the open loop pole frequency by C3-R5 (as described previously, Figure 7-122

again). The output from across R5-C3 (node 12) drives the model's succeeding frequency shaping stages, and EREF is again an internal reference voltage.

One of the unique properties of current feedback amplifiers is that bandwidth is a function of the feedback resistor and the internal compensation capacitor, C3. The lower the feedback resistor, the greater the bandwidth, until a practical lower limit is reached, i.e., the value at which the part oscillates. As the model includes a low impedance inverting input, it accurately mimics real part behavior as R_F is altered. Figure 7-129 compares the ADSpice model to the actual device for an AD811 video amplifier. As shown, the model accurately predicts the gain roll off at the much lower frequency for the 1kΩ feedback resistor as opposed to the 500Ω resistor.

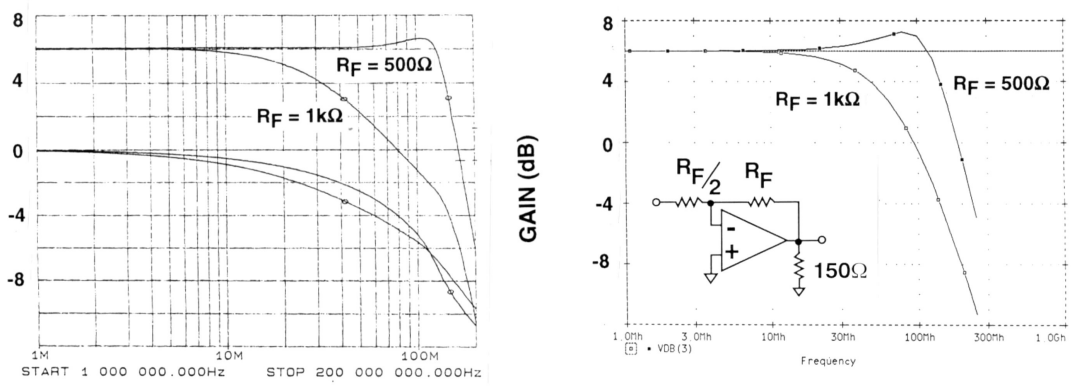


Figure 7-129: *Comparison of a real AD811 current feedback op amp (left) with macromodel (right) shows similar characteristics as feedback resistance is varied*

The current feedback amplifier input and gain stage is an enhancement to the ADSpice model that increases flexibility in modeling different op amp devices, and provides a net increase in design cycle speed.

Simulation Must Not Replace Breadboarding!

No matter how accurate your models are, or how much confidence you have with simulations, *SPICE analysis alone should never totally replace breadboarding*. As part of a layout and the actual devices existing within a real world PCB assembly, there are second and third order effects which can easily become relevant to performance. By and large, SPICE will never ever "know" of such things, unless you explicitly enter them into the SPICE netlist. However, this may be either difficult or outright impossible. You may not even be aware of some things before a PCB is built and tested within the final system— spurious signal coupling, the effects of crosstalk, the inevitable parasitic capacitance, inductance, and resistance— on and on goes the list. Let's face it, it is all but impossible to include all of these effects in a simulation. Even if generally aware of their existence, you simply won't have any data whatsoever on the magnitudes involved without actually building a PCB, and operating it under the intended conditions.

Furthermore, remember the fact that no macromodel includes all op amp characteristics. For example, exceeding the input voltage range can cause non-linear behavior in an op

amp, which is not necessarily included in its model. Because of such effects that a simulation might not predict, it is necessary to breadboard the circuit.

Even with models as comprehensive as those of the ADSpice library, external effects can easily cause a circuit to work improperly. As noted, PCB parasitics can significantly alter the frequency performance in high speed designs. Such parasitics are easily overlooked in a SPICE simulation, but a breadboard will reveal the problems.

Ultimately, simulation and breadboarding should be used together to maximize the design efficiency. Figure 7-130 summarizes these pro and con points of analog simulations.

- **Understand What's Real (Hardware), and What Isn't (SPICE)**
- **Use Breadboarding/Prototyping as Final Design Verification**
- **Be Aware of Non-Modeled Op Amp Characteristics**
- **Pay Attention to PCB Parasitics Impacting Circuit Behavior**

Figure 7-130: *Some analog simulation caveats*

Obviously, the designer needs to be wary of what SPICE can/cannot do, and the necessity of closely allying simulations with breadboarding and prototyping.

Simulation is a Tool to be Used *Wisely*

It must be remembered that while simulation is an extremely powerful tool, it must be used wisely to realize its full benefits. This includes knowing models well, understanding PCB and other parasitic effects, and anticipating the results. For example, consider a simple differential amplifier comprised of an op amp and four equal resistors, to be analyzed for common mode rejection ratio (CMRR) performance. At low frequencies, CMRR will be dominated by resistor mismatch, while at higher frequencies it is dominated by op amp CMRR performance. However, a SPICE simulation will only show this if the external resistors are realistically mismatched, and the op amp model used also properly treats not only dc CMRR, but also CMRR reduction at higher frequencies. If these critically important points are overlooked in the analysis, then an optimistic result will shows excellent CMRR performance over the entire circuit bandwidth. Unfortunately, this is simply wrong. Alternatively, substituting into the netlist resistors mismatched by their specified tolerances as well as an ADSpice model (which *does* have CMRR frequency effects modeled) the end results will be quite different. CMRR performance at low frequencies will be limited by resistor mismatch errors, and it will degrade at higher frequencies, as would a real op amp device with CMRR versus frequency effects.

Know the Models

Using various dc and ac tests, any op amp macromodel can be checked for accuracy and functional completeness. Specialized test simulations can also be devised for other op amp parameters important for a particular analysis. All this is critically important, as knowing a model's capabilities ahead of time can help prevent many headaches later.

Understand PCB Parasitics

Even if the model passes all preliminary tests, caution still should be exercised. As noted, PCB parasitics can have significant impact on a circuit's performance. This is especially true for high speed circuits. A few picofarads of capacitance on the input node can make the difference between a stable circuit and one that oscillates. Thus, these effects need to be carefully considered when simulating the circuit to achieve meaningful results.

To illustrate the impact of PCB parasitics, the simple voltage follower circuit of Figure 7-131 (left) was built twice. The first time this was on a carefully laid out PCB, and the second time on a component plug-in type of prototype board. An AD847 op amp is used because of its 50 MHz bandwidth, which makes the parasitic effects much more critical (smaller C values will have a greater effect on results).

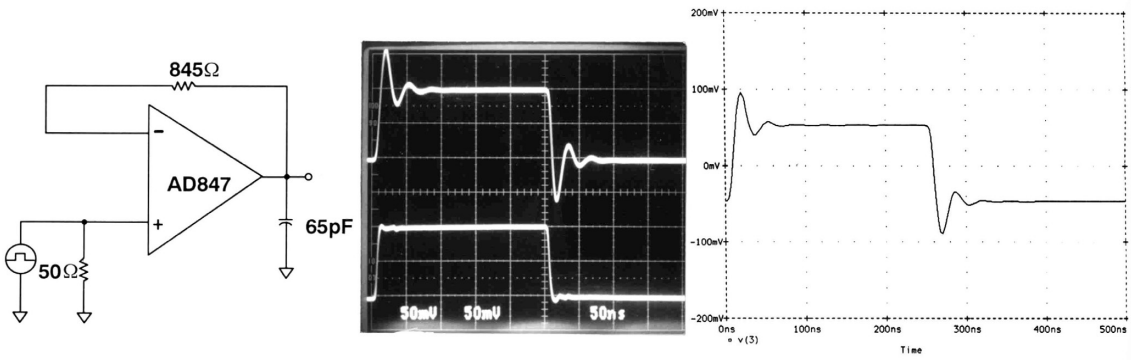


Figure 7-131: *With care and low parasitic effects in the PCB layout, results of lab testing (center) and simulation (right) can converge*

As the results above indicate, this circuit executed on a properly laid out PCB has a clean response with minor overshoot and ringing (center picture). The SPICE model results also closely agree with the real part, showing a corresponding simulation (right picture).

On the other hand, the same circuit built on the plug-in prototype board shows distinctly different results. In general it shows much worse performance, due to the relatively high nodal capacitances around the op amp inputs, which degrade the square wave response to severe ringing, much less than full capability of the part.

This is shown in Figure 7-132 (opposite) in the center and right pictures, respectively. The voltage follower circuit on the left shows the additional capacitances as inherent to the prototype board. With this test circuit and corresponding analysis, there was (initially) no agreement between the poor lab test, and the parallel SPICE test. However, when the relevant PCB parasitic capacitances are included in the SPICE file, then the simulation results do agree with the real circuit, as noted in the right picture.

This example illustrates several key points. One, PCB parasitics can easily make a high speed circuit behave much differently from a simplistic SPICE analysis. Secondly, when the SPICE netlist is adjusted to more reasonably reflect the parasitic elements of a PCB, then the simulation results do compare with the actual lab test. Finally, a point that should be obvious, a clean PCB layout with minimal parasitics is critically important to high

speed designs. To put this in a broader perspective, op amps of today are capable of operating to 1GHz or more!

Another interesting point is that the simulation can be used as a rough measure of the PCB layout design. If the simulation, without any parasitics, agrees with the PCB, then there is a reasonable assurance that PCB is well laid out.

Parasitic PCB elements are not the only area that may cause differences between the simulation and the breadboard. A circuit may exhibit non-linear behavior during power-on that will cause a device to lock-up. Or, a device may oscillate due to insufficient power supply decoupling or lead inductance. SPICE circuits need *no* bypassing, *but real world ones always do*! It is, practically speaking, impossible to anticipate all normal or abnormal operating conditions to which an amplifier might be subjected.

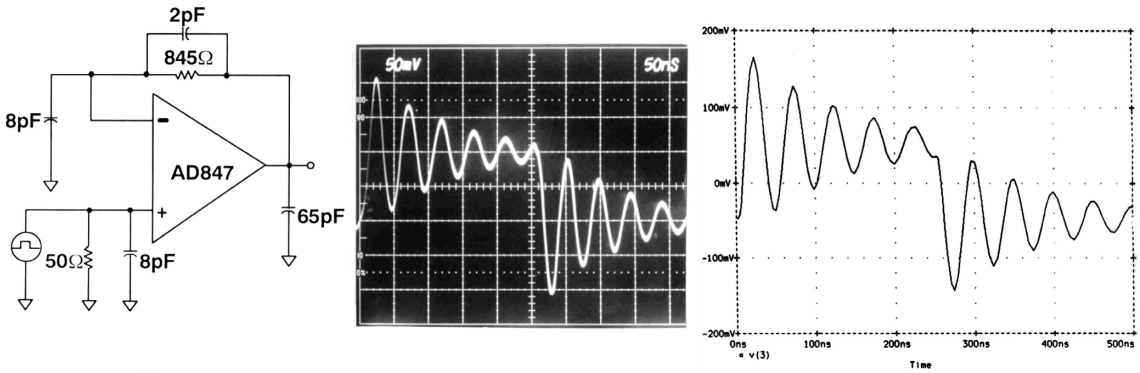


Figure 7-132: *Without low parasitics, lab testing results (center) and parallel simulation (right) still show convergence— with a poorly damped response*

Thus, it is always important that circuits be breadboarded and thoroughly checked in the lab. Careful forethought in these stages of design helps minimize any unknown problems from showing up when the final PCBs are manufactured.

Simulation Speeds the Design Cycle

Simulation is very effective in the initial design phase, to try out different ideas and circuit configurations. When a circuit topology has been decided upon and tested in SPICE, then a breadboard can be built. If the simulation was done carefully, the breadboard has good likelihood of working correctly without significant modifications.

When the simulation and the actual results correlate, then the circuit can be easily altered in SPICE to perform many different types of analysis. For example, it is much easier to try to optimize the circuit while working within in SPICE, as opposed to repeatedly modifying a breadboard. Quick substitutions of the op amps and components can be made in SPICE and the results immediately viewed.

Worst-case and sensitivity analyses are also done in SPICE much easier than on paper, and with multiple SPICE runs, the sensitivity to a certain parameter can be determined. Consider for example an analysis of a multi-stage active filter, for all possible combinations of component values. This is a nightmare if not impossible either by hand

or in the lab, but valid results for response extremes can be obtained relatively easily via a SPICE Monte Carlo option, providing greater design confidence.

Some general SPICE-related points are useful towards an overall healthy perspective on this, as shown in Figure 7-133.

- **Quickly Check Circuit Ideas**
- **Eases Circuit Optimization**
- **Allows Component Alteration for Worst Case and Sensitivity Analyses**
- **Allows Quick Comparison of Different Op Amps**

Figure 7-133: *Some useful points on using SPICE simulations*

While simulation cannot reasonably be allowed to replace breadboarding, the two can and should be used together, to increase the efficiency of a design cycle.

SPICE support

A variety of industry vendors offer SPICE analysis packages for various computer platforms, including the PC. The first of these and among the most popular is PSpice®, a commercial program which now includes allied packages for both schematic capture and PCB layout (see Reference 19). In addition, many vendors also offer low or no cost limited capability student versions of their SPICE programs.

Model support

The ADSpice model library is available in several different forms. Included within it are models of several IC device types, in addition to the op amps discussed above. These are for in-amps, analog multipliers, voltage references, analog switches, analog multiplexers, matched transistors, and buffers. Individual op amp models are available as listings on many data sheets. Electronic ASCII text files of the model library are found from either the ADI website (see References), the Analog Devices Literature Center via 1-800-ANALOGD (1-800-262-5643), or on the ADI support CD.

ACKNOWLEDGEMENTS:

There have been numerous model authors of SPICE macromodels for the ADI library. These include Derek Bowers, Eberhard Brunner, Joe Buxton, Vic Chang, Bob Day, Wes Freeman, Adolfo Garcia, Antonio Germano, John Hayes, John McDonald, Troy Murphy, Al Neves, Steve Reine, Bill Tolley, Tim Watkins, and James Wong.

Breadboard and Prototyping Techniques

A basic principle of a breadboard or a prototype structure is that it is a *temporary* one, designed to test the performance of an electronic circuit or system. By definition it must therefore be easy to modify, particularly so for a breadboard.

There are many commercial prototyping systems, but unfortunately for the analog designer, almost all of them are designed for prototyping *digital* systems. In such environments, noise immunities are hundreds of millivolts or more. Prototyping methods commonly used include non copper-clad Matrix board, Vectorboard, wire-wrap, and plug-in breadboard systems. Quite simply, these all are unsuitable for high performance or high frequency analog prototyping, because of their excessively high parasitic resistance, inductance, and capacitance levels. Even the use of standard IC sockets is inadvisable in many prototyping applications (more on this, below).

- **Always Use a Ground Plane for Precision or High Frequency Circuits**
- **Minimize Parasitic Resistance, Capacitance, and Inductance**
- **If Sockets Are Required, Use "Pin Sockets" ("Cage Jacks")**
- **Pay Equal Attention to Signal Routing, Component Placement, Grounding, and Decoupling in Both the Prototype and the Final Design**
- **Popular Prototyping Techniques:**
  - **Freehand "Deadbug" Using Point-to-point Wiring**
  - **"Solder-mount"**
  - **Milled PC Board From CAD Layout**
  - **Multilayer Boards: Double-sided With Additional Point-to-point Wiring**

Figure 7-134: *A summary of analog prototyping system key points*

Figure 7-134 summarizes a number of key points on selecting a useful analog breadboard and/or prototyping system, which are further discussed below.

One of the more important considerations in selecting a prototyping method is the requirement for a large-area ground plane. This is required for high frequency circuits as well as low speed precision circuits, especially when prototyping circuits involving ADCs or DACs. The differentiation between *high-speed* and *high-precision* mixed-signal circuits is difficult to make. For example, 16+ bit ADCs (and DACs) may operate on high speed clocks (>10MHz) with rise and fall times of less than a few nanoseconds, while the effective throughput rate of the converters may be less than 100kSPS. Successful prototyping of these circuits requires that equal (and thorough) attention be given to good high-speed and high-precision circuit techniques.

Deadbug prototyping

A simple technique for analog prototyping uses a solid copper-clad board as a ground plane (see References 20 and 21). In this method, the ground pins of the ICs are soldered directly to the plane, and the other components are wired together above it. This allows

HF decoupling paths to be very short indeed. All lead lengths should be as short as possible, and signal routing should separate high-level and low-level signals. Connection wires should be located close to the surface of the board to minimize the possibility of stray inductive coupling. In most cases, 18-gauge or larger insulated wire should be used. Parallel runs should not be "bundled" because of possible coupling. Ideally the layout (at least the relative placement of the components on the board) should be similar to the layout to be used on the final PCB. This approach is often referred to as *deadbug* prototyping, because the ICs are often mounted upside down with their leads up in the air (with the exception of the ground pins, which are bent over and soldered directly to the ground plane). The upside-down ICs look like deceased insects, hence the name.

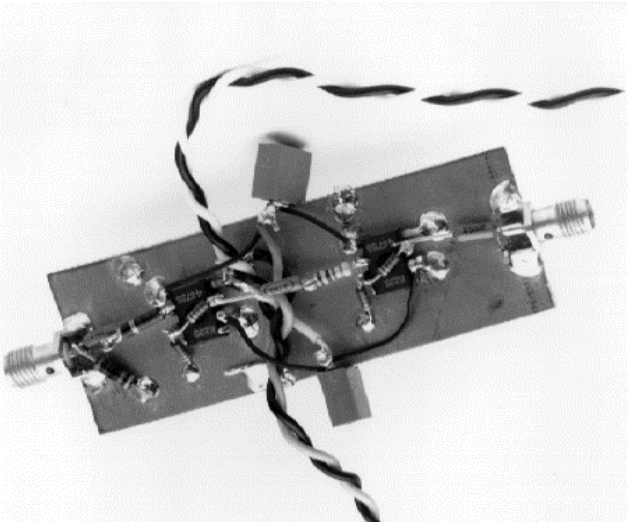


Figure 7-135: *A "deadbug" analog breadboard*

Figure 7-135 shows a hand-wired "deadbug" analog breadboard. This circuit uses two high speed op amps, and in fact gives excellent performance in spite of its lack of esthetic appeal. The IC op amps are mounted upside down on the copper board with the leads bent over. The signals are connected with short point-to-point wiring. The characteristic impedance of a wire over a ground plane is about 120Ω, although this may vary as much as ±40% depending on the distance from the plane. The decoupling capacitors are connected directly from the op amp power pins to the copper-clad ground plane. When working at frequencies of several hundred MHz, it is a good idea to use only one side of the board for ground. Many people drill holes in the board and connect the sides together by soldering short pieces of wire. If care isn't taken, this may result in unexpected ground loops between the two sides of the board, especially at RF frequencies.

Pieces of copper-clad board may be soldered at right angles to the main ground plane to provide screening, or circuitry may be constructed on both sides of the board (with through-hole connections) with the board itself providing screening. For this, the board will need corner standoffs to protect underside components from being crushed.

When the components of a breadboard of this type are wired point-to-point in the air (a type of construction strongly advocated by Bob Pease (see Reference 21) and sometimes known as "bird's nest" construction) there is always the risk of the circuitry being crushed and resulting short-circuits. Also, if the circuitry rises high above the ground plane, the screening effect of the ground plane is diminished, and interaction between different parts

of the circuit is more likely. Nevertheless, the technique is very practical and widely used because the circuit may easily be modified (this of course assumes the person doing the modifications is adept with soldering techniques).

Another prototype breadboard variation is shown in Figure 7-136. Here the single-sided copper-clad board has pre-drilled holes on 0.1" centers (see Reference 22). Power busses are used at the top and bottom of the board. The decoupling capacitors are used on the power pins of each IC. Because of the loss of copper area due to the pre-drilled holes, this technique does not provide as low a ground impedance as a completely covered copper-clad board of Figure 7-135, so be forewarned.

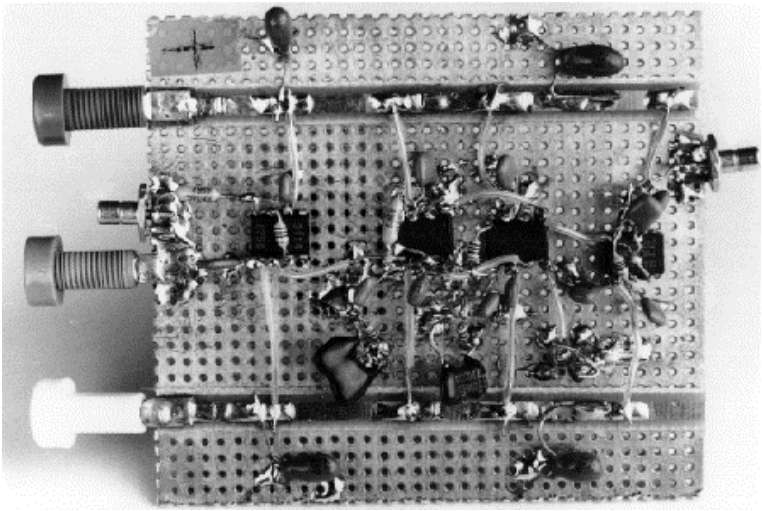


Figure 7-136: *"A deadbug" prototype using 0.1" pre-drilled single-sided, copper-clad printed board material*

In a variation of this technique, the ICs and other components are mounted on the non-copper-clad side of the board. The holes are used as vias, and the point-to-point wiring is done on the copper-clad side of the board. Note that the copper surrounding each hole used for a via must be drilled out, to prevent shorting. This approach requires that all IC pins be on 0.1" centers. For low frequency circuits, low profile sockets can be used, and the socket pins then will allow easy point-to-point wiring.

Solder-Mount Prototyping

There is a commercial breadboarding system which has most of the advantages of the above techniques (robust ground, screening, ease of circuit alteration, low capacitance and low inductance) and several additional advantages: it is rigid, components are close to the ground plane, and where necessary, node capacitances and line impedances can be calculated easily. This system is made by Wainwright Instruments and is available in Europe as "Mini-Mount" and in the USA (where the trademark "Mini-Mount" is the property of another company) as "Solder-Mount" (see References 23 and 24).

Solder-Mount consists of small pieces of PCB with etched patterns on one side and contact adhesive on the other. These pieces are stuck to the ground plane, and components are soldered to them. They are available in a wide variety of patterns,

including ready-made pads for IC packages of all sizes from 8-pin SOICs to 64-pin DILs, strips with solder pads at intervals (which intervals range from 0.040" to 0.25", the range includes strips with 0.1" pad spacing which may be used to mount DIL devices), strips with conductors of the correct width to form microstrip transmission lines (50Ω, 60Ω, 75Ω or 100Ω) when mounted on the ground plane, and a variety of pads for mounting various other components. Self-adhesive tinned copper strips and rectangles (LO-PADS) are also available as tie-points for connections. They have a relatively high capacitance to ground and therefore serve as low-inductance decoupling capacitors. They come in sheet form and may be cut with a knife or scissors.

The main advantage of Solder-Mount construction over "bird's nest" or "deadbug" is that the resulting circuit is far more rigid, and, if desired, may be made far smaller (the latest Solder-Mounts are for surface-mount devices and allow the construction of breadboards scarcely larger than the final PCB, although it is generally more convenient if the prototype is somewhat larger). Solder-Mount is sufficiently durable that it may be used for small quantity production as well as prototyping.

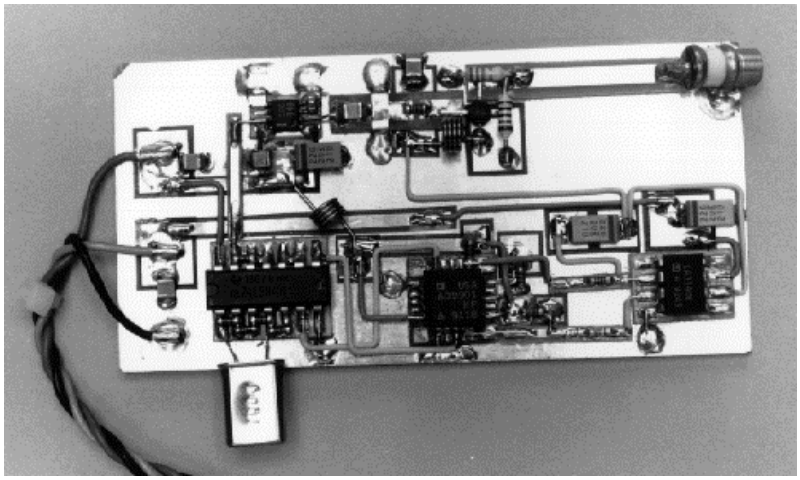


Figure 7-137: *A "Solder-Mount" constructed prototype board*

Figure 7-137 shows an example of a 2.5GHz phase-locked-loop prototype, built with Solder-Mount techniques. While this is a high speed circuit, the method is equally suitable for the construction of high resolution low frequency analog circuitry.

A particularly convenient feature of Solder-Mount at VHF is the relative ease with which transmission lines can be formed. As noted earlier, if a conductor runs over a ground plane, it forms a microstrip transmission line. The Solder-Mount components include strips which form microstrip lines when mounted on a ground plane (they are available with impedances of 50Ω, 60Ω, 75Ω, and 100Ω). These strips may be used as transmission lines for impedance matching, or alternately, more simply as power buses. Note that glass fiber/epoxy PCB is somewhat lossy at VHF/ UHF, but losses will probably be tolerable if microstrip runs are short.

Milled PCB Prototyping

Both "deadbug" and "Solder-Mount" prototypes become tedious for complex analog circuits, and larger circuits are better prototyped using more formal layout techniques.

There is a prototyping approach that is but one step removed from conventional PCB construction, described as follows. This is to actually lay out a double-sided board, using conventional CAD techniques. PC-based software layout packages offer ease of layout as well as schematic capture to verify connections (see References 25 and 26). Although most layout software has some degree of auto-routing capability, this feature is best left to digital designs. The analog traces and component placements should be done by hand, following the rules discussed elsewhere in this chapter. After the board layout is complete, the software verifies the connections per the schematic diagram net list.

Many designers find that they can make use of CAD techniques to lay out simple boards. The result is a pattern-generation tape (or Gerber file) which would normally be sent to a PCB manufacturing facility where the final board is made.

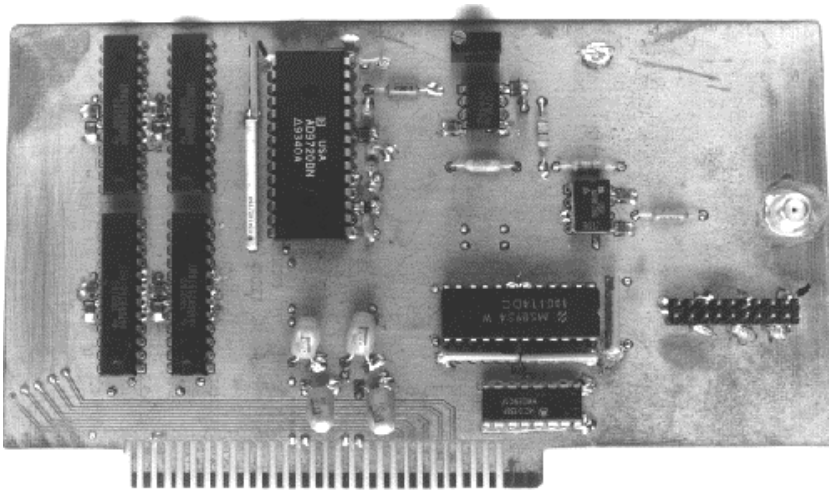


Figure 7-138: *A milled circuit construction prototype board (top view)*

Rather than use a PCB manufacturer, however, automatic drilling and milling machines are available which accept the PG tape directly (see References 27 and 28). An example of such a prototype circuit board is shown in Figure 7-138 (top view).

These systems produce either single or double-sided circuit boards directly, by drilling all holes and using a milling technique to remove conductive copper, thus creating the required insulation paths, and finally, the finished prototype circuit board. The result can be a board functionally quite similar to a final manufactured double-sided PCB.

However, it should be noted that a chief caveat of this method is that there is no "plated-through" hole capability. Because of this, any conductive "vias" required between the two layers of the board must be manually wired and soldered on both sides.

Minimum trace widths of 25 mils (1 mil = 0.001") and 12 mil spacing between traces are standard, although smaller trace widths can be achieved with care. The minimum spacing between lines is dictated by the size of the milling bit used, typically 10 to 12 mils.

A bottom-side view of this same milled prototype circuit board is shown in Figure 7-139. The accessible nature of the copper pattern allows access to the traces for modifications.

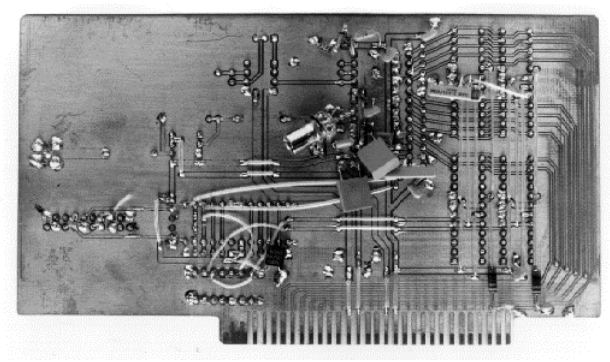


Figure 7-139: *A milled circuit construction prototype board (bottom view)*

Perhaps the greatest single advantage of the milled circuit type of prototype circuit board is that it approaches the format of the final PCB design most closely. By its very nature however, it is basically limited to only single or double-sided boards.

Beware of Sockets!

IC sockets can degrade the performance of high speed or high precision analog ICs. Although they make prototyping easier, even *low-profile* sockets often introduce enough parasitic capacitance and inductance to degrade the performance of a high speed circuit. If sockets must be used, a socket made of individual *pin sockets* (sometimes called *cage jacks*) mounted in the ground plane board may be acceptable, as in Figure 7-140.

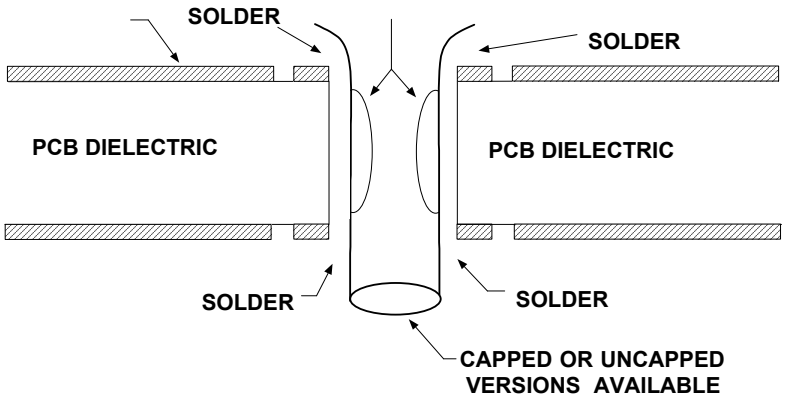


Figure 7-140: *When necessary, use* pin sockets *for minimal parasitic effects*

To use this technique, clear the copper (on both sides of the board) for about 0.5mm around each ungrounded pin socket, Then solder the grounded socket pins to ground, on both sides of the board.

Both capped and uncapped versions of these pin sockets are available (AMP part numbers 5-330808-3, and 5-330808-6, respectively). The pin sockets protrude through the board far enough to allow point-to-point wiring interconnections.

Because of the spring-loaded gold-plated contacts within the pin socket, there is good electrical and mechanical connection to the IC pins. Multiple insertions, however, may degrade the performance of the pin socket, so this factor should be kept in mind.

Note also that the uncapped versions allow the IC pins to extend out the bottom of the socket. This feature leads to an additional useful function. Once a prototype using the pin sockets is working and no further changes are to be made the IC pins can be soldered directly to the bottom of the socket. This establishes a rugged, permanent connection.

Some Additional Prototyping Points

The prototyping techniques discussed so far have been limited to single or double-sided PCBs. Multilayer PCBs do not easily lend themselves to standard prototyping techniques. If multilayer board prototyping is required, one side of a double-sided board can be used for ground and the other side for power and signals. Point-to-point wiring can be used for additional runs which would normally be placed on the additional layers provided by a multi-layer board. However, it is difficult to control the impedance of the point-to-point wiring runs, and the high frequency performance of a circuit prototyped in this manner may differ significantly from the final multilayer board.

Other difficulties in prototyping may occur with op amps or other linear devices having bandwidths greater than a few hundred megahertz. Small variations in parasitic capacitance (<1pF) between the prototype and the final board can cause subtle differences in bandwidth and settling time.

Sometimes, prototyping is done with DIP packages, when the final production package is an SOIC. *This is not recommended!* At high frequencies, small package-related parasitic differences can account for different performance, between prototype and final PCB. To minimize this effect, always prototype with the final packages.

Evaluation Boards

Most manufacturers of analog ICs provide *evaluation boards* usually at a nominal cost. These boards allow customers to evaluate ICs without constructing their own prototypes. Regardless of the product, the manufacturer has taken proper precautions regarding grounding, layout, and decoupling to ensure optimum device performance. Where applicable, the evaluation PCB artwork is usually made available free of charge, should a customer wish to copy the layout directly or make modifications to suit an application.

General Purpose Op Amp Evaluation Boards

Evaluation boards can be either dedicated to a particular IC, or they can also be general purpose. With op amps the most universal linear IC, it is logical that evaluation boards be developed for them, to aid easy applications. However, it is also important that a good quality evaluation board avoid the parasitic effects discussed above. An example is the general purpose dual amplifier evaluation board of in figure 7-141 (see Reference 29).

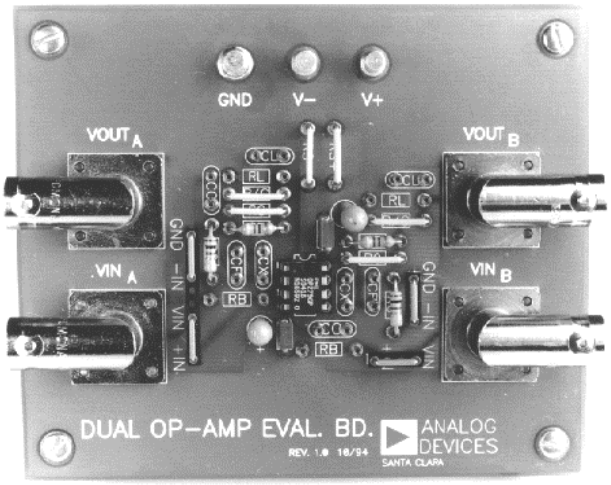


Figure 7-141: *A general purpose op amp evaluation board allows fast, easy configuration of low frequency op amp circuits*

This board uses pin sockets for any standard dual op amp pinout device, and a flexible set of component jumper locations allows it to be setup for inverting or non-inverting amplifiers. Various gains can be configured by choice of the component values, in either ac or dc-coupled configurations.

The card design provides signal coupling via BNC connectors at input and output. It also uses external lab power supplies, which are wired to the lug terminals at the top. The card does however contain local supply voltage decoupling and bypassing components.

These general purpose boards are intended for medium to high precision uses at frequencies below 10MHz, with moderate op amp input currents. For higher operating speeds, a dedicated, device-specific evaluation board is likely to be a better choice.

Dedicated Op Amp Evaluation Boards

In high speed/high precision ICs, special attention must be given to power supply decoupling. For example, fast slewing signals into relatively low impedance loads produce high speed transient currents at the power supply pins of an op amp. The transient currents produce corresponding voltages across any parasitic impedance that may exist in the power supply traces. These voltages, in turn, may couple to the amplifier output, because of the op amp's finite power supply rejection at high frequencies.

The AD8001 high speed current-feedback amplifier is a case in point, and a dedicated evaluation board is available for it. A bottom side view of this SOIC board is shown in Figure 7-142. A triple decoupling scheme was chosen, to ensure a low impedance ground path at all transient frequencies. Highest frequency transients are shunted to ground by dual 1000pF/0.01µF ceramic chip capacitors, located as close to the power supply pins as possible to minimize series inductance and resistance. With these surface mount components, there is minimum stray inductance and resistance in the ground plane path. Lower frequency transient currents are shunted by the larger 10µF tantalum capacitors.

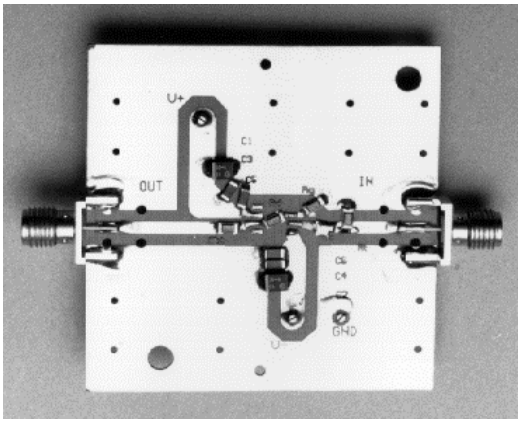


Figure 7-142: *A high speed op amp such as the AD8001 requires a dedicated evaluation board with suitable ground planes and decoupling (bottom view)*

The input and output signal traces of this board are 50Ω microstrip transmission lines, as can be noted towards the right and left. Gain-set resistors are chip-style film resistors, which have low parasitic inductance. These can be seen in the center of the photo, mounted at a slight diagonal.

Note also that there is considerable continuous ground plane area on both sides of the PCB. Plated-through holes connect the top and bottom side ground planes at several points, in order to maintain lowest possible impedance and best high frequency ground continuity.

Input and output connections to the card are provided via the SMA connectors as shown, which terminate the input/output signal transmission lines. The board's power connection from external lab supplies is made via solder terminals, which are seen at the ends of the broad supply line traces.

Some of these points are more easily seen in a topside view of the same card, which is shown in Figure 7-143. This AD8001 evaluation board is a non-inverting signal gain stage, optimized for lowest parasitic capacitance. The cutaway area around the SOIC outline of the AD8001 provides lowest stray capacitance, as can be noted in this view.

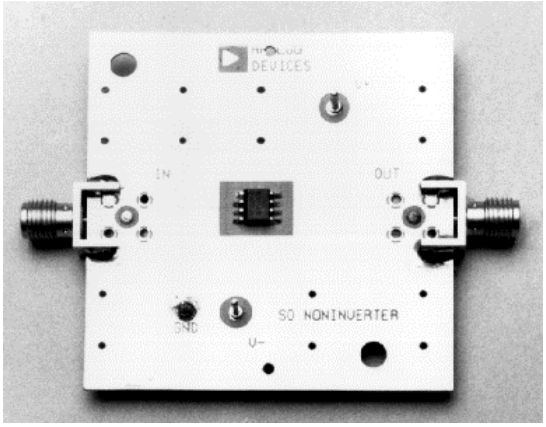


Figure 7-143: *The AD8001 evaluation board uses a large area ground plane as well as minimal parasitic capacitance (top view)*

In this view is also seen the virtually continuous ground plane and the multiple vias, connecting the top/bottom planes.

Summary

In summary, good analog designers utilize as many tools as possible to ensure that the final system design performs correctly. The first step is the intelligent use of IC op amp and other macromodels, where available, to simulate the circuit. The second step is the construction of a prototype board to further verify the design, and to validate the simulation. The final PCB layout should then be based on the prototype layout as much as possible, with careful attention to parasitic effects.

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