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CHAPTER 6: SIGNAL AMPLIFIERS

Walt Jung, Walt Kester

SECTION 6-1: AUDIO AMPLIFIERS

Walt Jung

Audio Preamplifiers

Audio signal preamplifiers (preamps) represent the low-level end of the dynamic range of practical audio circuits using modern IC devices. In general, amplifying stages with input signal levels of 10mV or less fall into the preamp category. This section discusses some basic types of audio preamps, which are:

■ *Microphone*— including preamps for dynamic, electret and phantom powered microphones, using transformer input circuits, operating from dual and single supplies.

■ *Phonograph*— including preamps for moving magnet and moving coil phono cartridges in various topologies, with detailed response analysis and discussion.

In general, when working signals drop to a level of ≈1mV, the input noise generated by the first system amplifying stage becomes critical for wide dynamic range and good signal-to-noise ratio. For example, if internally generated noise of an input stage is 1µV and the input signal voltage 1mV, the best signal-to-noise ratio possible is just 60dB.

In a given application, both the input voltage level and impedance of a source are usually fixed. Thus, for best signal-to-noise ratio, the input noise generated by the first amplifying stage must be minimized when operated from the intended source. This factor has definite implications to the preamp designer, as a "low noise" circuit for low impedances is quite different from one with low noise operating from a high impedance.

Successfully minimizing the input noise of an amplifier requires a full understanding of all the various factors which contribute to total noise. This includes the amplifier itself as well as the external circuit in which it is used, in fact *the total circuit environment must be considered*, both to minimize noise and maximize dynamic range and signal fidelity.

A further design complication is the fact that not only is a basic gain or signal scaling function to be accomplished, but *signal frequency response* may also need to be altered in a predictable manner. Microphone preamps are an example of wideband, flat frequency response, low noise amplifiers. In contrast to this, phonograph preamp circuits not only scale the signal, they also impart a specific frequency response characteristic to it. A major part of the design for the RIAA phono preamps of this section is a systematic analysis process, which can be used to predictably select components for optimum performance in frequency response terms. This leads to very precise functioning, and excellent correlation between a computer based design and measured lab operation.

Microphone Preamplifiers

The microphone preamplifier (mic preamp) is a basic low level audio amplification requirement. Mic preamps can assume a variety of forms, considering the wide range of possible signal levels, the microphone types, and their impedances. These factors influence the optimum circuit for a specific application. In this section mic preamps are discussed which work with both high and low impedance microphones, both with and without phantom power, and with transformer input stages.

Single-Ended, Single-Supply High-Impedance Mic Preamp

A very simple form of mic preamp is shown in Figure 6-1. This is a non-inverting stage with a single-ended input, most useful with high-impedance microphones such as dynamic and piezoelectric types. As shown it has adjustable gain of 20-40 dB via R_{GAIN}, and is useful with audio sources with 600Ω or greater source impedances.

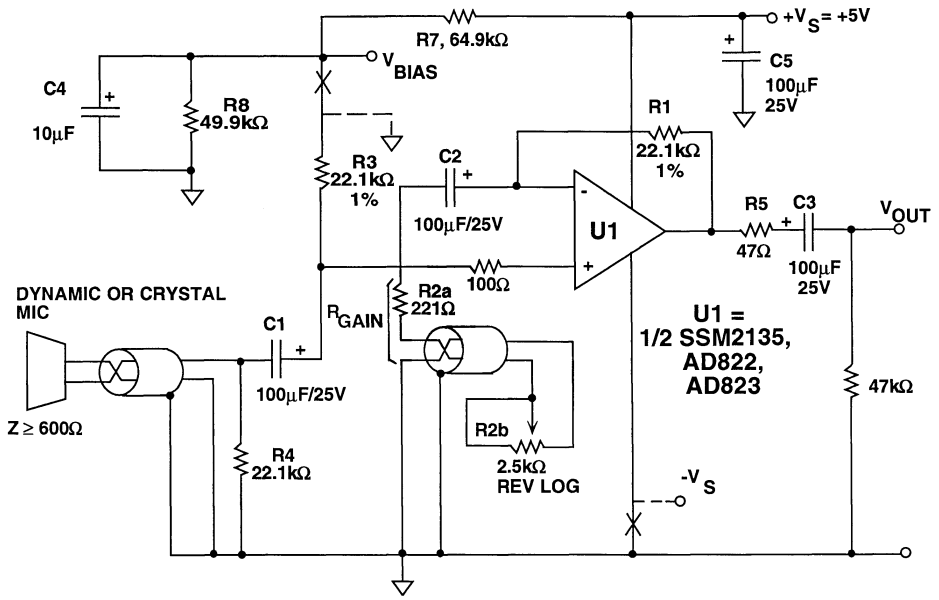

Figure 6-1: *A single-ended,single-supply mic preamp*

The U1 op amp can greatly affect the overall performance, both in general amplification terms but also in suitability for single supply operation (as shown here). In terms of noise performance, the U1 device should have a low input noise with ≥500Ω sources, with the external circuit values adjusted so that the source impedance (microphone) dominates the overall source resistance.

For very low noise on 5V supplies, very few devices are suitable. Among these the dual SSM2135 or the OP213, and AD822/AD823 stand out, and are recommended as first choices. For very low power, minimal quiescient current parts like the AD8541 can be considered. Many other low noise devices can also work well in this circuit for total supply voltages of 10V or more, for example the OP275, and OP270/470 types. The circuit is also easily adapted for dual supply use, as noted below.

In this circuit, gain-determining resistors R1||R2 (where R2a + R2b = R_{GAIN}) are scaled such that their total resistance is less than the expected source impedance, that is 1kΩ or less. This minimizes the contribution of the gain resistors to input noise, at high gain. As noted, gain of the circuit is adjusted in the feedback path via resistor R_{GAIN}. In a system sense, control of a microphone or other low level channel signal level is preferably done *after* it has undergone some gain, as the case here. R_{GAIN} can of course be a fixed value.

Because of the single supply operation, input/output coupling is via polar capacitors, namely C1, C2, and C3. C4 is a noise filter, and C5 a bypass. For lowest noise in the circuit, the amplifier biasing must also be *noiseless*, that is free from noise added directly or indirectly by the biasing (see Reference 1). Resistors with DC across them should have low excess noise (film types), or be AC-bypassed. Thus R1, R2, R3, R4, R7, and R8 are preferably metal films, with R7-R8 bypassed. A 2.2V bias provided from R7-R8 biases the output of U1 to near mid-supply. If higher supply voltage is used, R7-R8 can be adjusted for maximum output with a particular amplifier. For example, with low bias current, rail-rail output op amps, R7 and R8 should be high, equal values (≥100kΩ).

While the OP213 or SSM2135 for U1 is optimum when operating from lower impedance sources, FET input types such as the AD82x families (or a select CMOS part) is preferable for high impedance sources, such as crystal or ceramic mics. To adapt the circuit for this, R3 and R4 should be 1MΩ or more, and C1 a 0.1µF film capacitor.

Bandwidth using the OP213 or SSM2135 is about 30kHz at maximum gain, or about 20kHz for similar conditions with the AD822 (or AD820). Distortion and noise performance will reflect the U1 device and source impedance. With a shorted input, an SSM2135 measures output noise of about 110µVrms at a gain of 100, with a 1kHz THD+N of 0.022% at 1Vrms into a 2kΩ load. The AD820 measures about 200µVrms with 0.05% THD+N for similar conditions. For both, the figures improve at lower gains.

The circuit of Figure 6-1 is a good one if modest performance and simplicity are required, but requires attention to details. The input cable to the microphone must be shielded, and no longer than required. Similar comments apply to a cable for R_{GAIN} (if remote).

To adapt this circuit for dual supply use, R3 is returned to ground as noted, plus the bias network of R7, R8 and C4 is eliminated. U1 is operated on symmetric supplies (±5V, ±15V, etc.), with the $-V_S$ rail bypassed similar to $+V_S$. Coupling caps C1, C2 and C3 are retained, but must be polarized to matched the amplifier used (or non-polar types).

Although microphones with output impedances of less than 600Ω can be used with this circuit, the noise performance will not be optimum. Also, many of these typically require a balanced input interface. Subsequent circuits show methods of optimizing noise with low impedance, balanced output microphones, as suited for professional applications.

Electret Mic Preamp Interface

A popular mic type for speech recording and other non-critical applications is the electret type. This is a permanently polarized condenser mic, typically with a built in common-source FET amplifier. The amplified output signal is taken from the same single ended lead which supplies the microphone with DC power, typically from a 3-10V DC source.

Figure 6-2 illustrates a basic interface circuit which is useful in powering and scaling the output signal of an electret mic for further use. In this case the scaled output signal from this interface is fed into the LEFT and RIGHT inputs of a +5V supply powered CODEC, for digitization and processing. DC phantom power is fed to the mic capsules by the R_A-C_A-R_B decoupling network from the +5V supply, and the AC output signal is tapped off by C_{IN}-R2, and fed to U1. The R_B resistors will vary with different mics and supply voltages, and the values shown are typical. For a quiet mic supply voltage, a filtered/scaled V_R can be generated by the optional U2 connection shown.

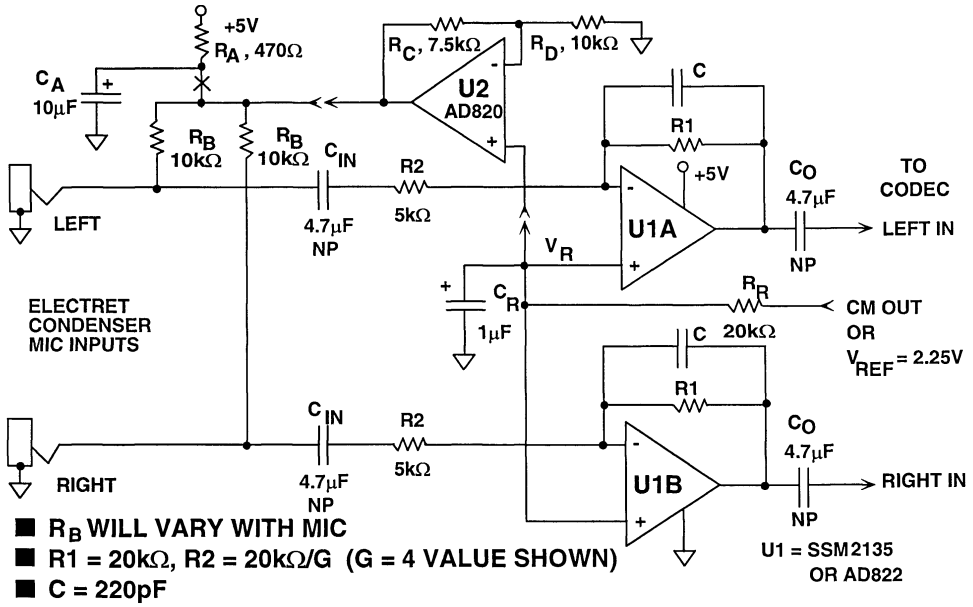

Figure 6-2: *An electret mic interface for 5V powered CODECs*

The U1 dual scaling amplifier is an SSM2135 or AD822, and is used to normalize the mic signal to either a 1Vrms line level or 100mVrms mic level typically required by CODEC inputs, and also to low pass filter it prior to digitization. With a wide variety of electret mics and operating parameters, some signal level scaling is often required.

The scaling gain is simply R1/R2, and R2 is selected to provide a gain "G", to yield 0.1Vrms at the mic inputs of the CODEC, with the rated output from the mic. The U1 stages are inverting, so G can be greater or less than unity, i.e., other than 4 as is shown here, to normalize any practical input signal to an optimum CODEC level. The amplifier's low pass corner frequency is set by the time constant R1-C, which results in a -3dB point of 36kHz. Bias for the U1 stages is provided from the CODEC, via the reference or CMOUT pins, typically a 2.25-2.5V reference voltage. The low frequency time constants C_{IN}-R_B/R2 and C_O-20kΩ are wideband to minimize LF phase shift. These (non-polar) capacitors can be reduced to 1µF or less, for narrowband uses.

Transformer-Coupled Low-Impedance Microphone Preamps

For any op amp, the best noise performance is attained when the characteristic *noise resistance* of the amplifier, R_n, is equal to the source resistance, R_s. Examples of microphone preamps that make use of this factor are discussed in this section. They utilize an input matching transformer to more closely optimize an amplifier to a source impedance which is unequal to the amplifier R_n. A basic circuit operating on this principle is shown in Figure 6-3. In order to select an optimum transformer turns ratio for a given source resistance (R_s), calculate the characteristic R_n of the op amp in use.

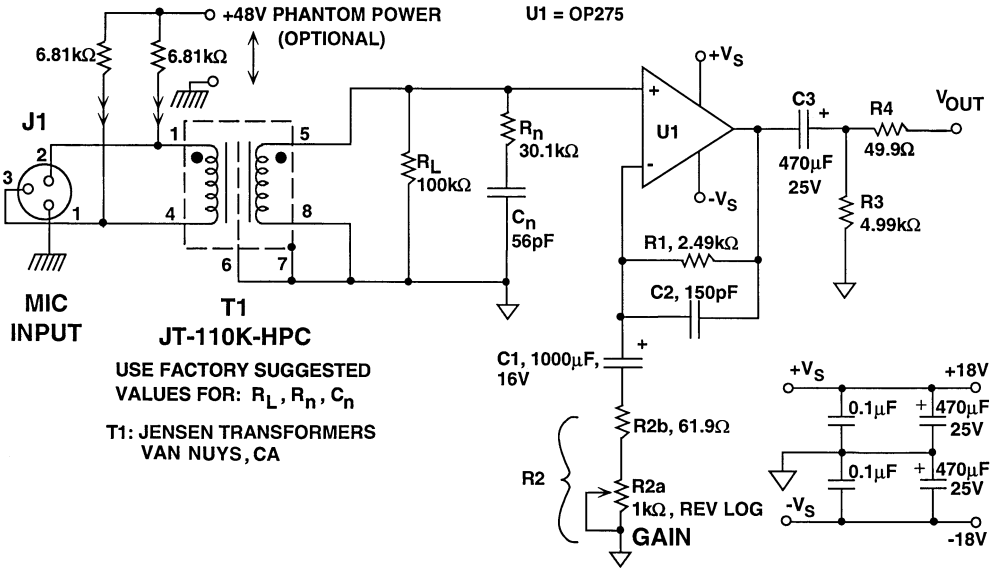

Figure 6-3: *Transformer input mic preamplifier with 28 to 50 dB gain*

R_n must first be calculated from the op amp's e_n and i_n data as:

$$R_n = \frac{e_n}{i_n} \qquad \text{Eq. 6-1}$$

where e_n is in V/√Hz and i_n is in A/√Hz. A turns ratio for T1 may be calculated as:

$$\frac{N_s}{N_p} = \sqrt{\frac{R_n}{R_s}} \qquad \text{Eq. 6-2}$$

where N_s/N_p is the transformer secondary/primary turns ratio. For the OP275 op amp, the values of e_n and i_n are 7nV/√Hz and 1.5 pA/√Hz, respectively; thus,

$$R_n = \frac{e_n}{i_n} = \frac{7 \times 10^{-9}}{1.5 \times 10^{-12}}$$

$$= 4.7\text{k}\Omega$$

Since both e_n and i_n vary with frequency, R_n will also vary with frequency. Therefore, a value calculated for R_n from the data sheet (such as above) is most accurate at the specified frequency. If the amplifier is to be optimized for a specific frequency, then the e_n and i_n values should be for that frequency. However audio amplifiers are wideband circuits, so latitude is due here. When available, a minimum noise-figure plot for the amplifier will allow graphical determination of the optimum source resistance for noise.

For this case, an optimum transformer turns ratio can be calculated to provide the optimum R_n to the op amp, working from a given R_s. For example, if R_s is 150Ω, then an optimum turns ratio for an OP275 (or other amplifier) with an R_n of 4.7kΩ will be:

$$\frac{N_s}{N_p} = \sqrt{\frac{R_n}{R_s}} = \sqrt{\frac{4.7 \times 10^3}{1.5 \times 10^2}}$$

$$\approx 5.6$$

Other examples matching these criteria would include OP27 family types.

Transformers are catalogued in fairly narrow and specific impedance ranges, so a unit with a rated secondary impedance in the range of 5kΩ to 10kΩ will be useful (the amplifier minimum noise impedance is reasonably broad). A suitable unit for this purpose is the Jensen JT-110K-HPC. Note that T1 must be adequately shielded and otherwise suitable for operation in low-level environments. The use of the matching transformer allows the circuit to achieve an equivalent input noise (referred to the transformer input) that is only a few decibels above the theoretical limit, or very close to the thermal noise of the source resistance. For example, the thermal noise of a 150Ω resistor in a 20kHz noise bandwidth at room temperature is 219nV. A real circuit has a higher input referred noise, due to the transformer plus op amp noise.

An additional advantage of the transformer lies in the *effective voltage gain* that it provides, due to the step up turns ratio. For a given circuit total numeric gain, G_{total}, this reduces the gain required from the op amp U1, $G_{(U1)}$, to:

$$G_{(U1)} = \frac{G_{total}}{N_s / N_p} \qquad \text{Eq. 6-3}$$

Thus, in the composite circuit of Figure 6-3 gain G_{total} is the product of the transformer step up, N_s/N_p, and (R1 + R2)/R1, which is $G_{(U1)}$. This has advantages of allowing more amplifier loop gain, thus greater bandwidth and accuracy, lower distortion, etc.

The transformer input example mic preamp stage of Figure 6-3 uses the JT-110K-HPC transformer for T1 with a primary/secondary ratio of about 1/8 (150Ω/10kΩ). The op amp section has a variable gain of about 3.3-41 times, which, in combination with the 17.8dB transformer gain, yields a composite gain of 28 to 50 dB (26 to 300 times). Transient response of the transformer plus U1 amplifier is excellent. U1 here is ½ an OP275, operating on ±18V power. Supplies should be well regulated and decoupled close

to U1, particularly with low impedance loads. *Care should be used to operate U1 below maximum voltage rating*. The OP275 is rated for maximum supplies of ±22V.

For best results, passive components should be high-quality, such as 1% metal film resistors, a reverse log taper film pot for R2a, and low ESR capacitors for C1 & C3. Microphone phantom powering (see References 2 and 3) can be used, simply by adding the ±0.1% matched 6.81kΩ resistors and a 48V DC source, as shown. Close matching of the DC feed resistors is recommended by the transformer manufacturer whenever phantom power is used, to optimize CMR and to minimize the transformer's primary DC current flow (see Reference 4). Note that use of phantom powering has little or no effect on the preamp, since the transformer decouples the CM DC variations at the primary. CMR in an input transformer such as the JT-110K-HPC is typically 85dB or more at 1kHz, and substantially better at lower frequencies.

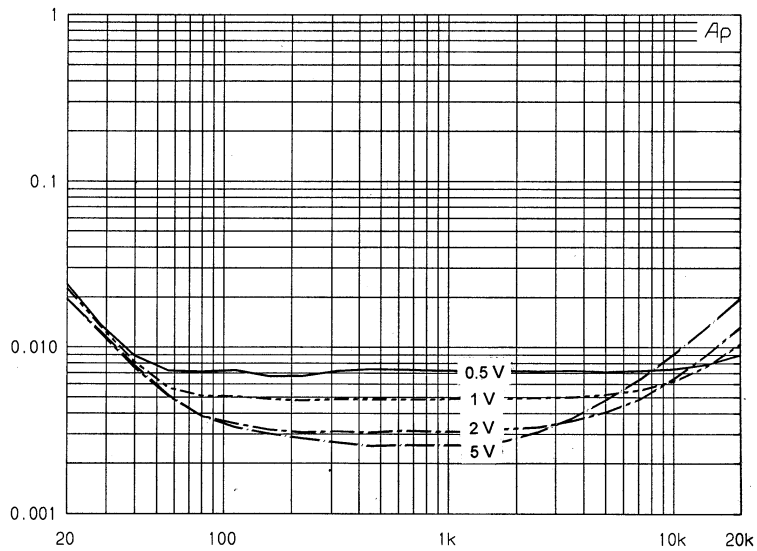

Figure 6-4: *Transformer coupled mic preamplifier THD+N (%) versus frequency (Hz) for 35dB gain, outputs of 0.5, 1, 2, and 5Vrms into 600Ω*

THD+N performance versus frequency of this OP275 mic preamp is shown in the family of curves in Figure 6-4. The test conditions are 35dB gain, and successive input sweeps resulting in outputs of 0.5, 1, 2, and 5Vrms into 600Ω. For these distortion tests as well as most of those following throughout these sections, THD+N frequency sweeps at various levels are used for sensitivity to slewing related distortions (see references 5-7), and output loaded tests are used for sensitivity to load related non-linearities.

For the OP275 data shown in Figure 6-4, there are three interest regions, a sub-100Hz region where distortion is largely transformer-related, a 100Hz-3kHz region where distortion is lowest, and a greater-than-3kHz region where it again rises. For most of the spectrum THD+N is ≤0.01% for medium outputs, and slightly higher at high frequencies.

The -3dB bandwidth of this circuit is about 100kHz, and is dominated by the JT-110K-HPC transformer and its termination network, assuming a 150Ω source impedance. Conversely, for higher or lower source impedances, the bandwidth will lower or rise in proportion, so application of this circuit should take this into account. For example, capacitor microphone capsules with emitter follower outputs appear as a ≈15Ω source.

Very Low Noise Transformer Coupled Mic Preamp

A high performance low noise mic preamp is shown in Figure 6-5, using a lower ratio transformer, the Jensen JT-16A. This transformer has a lower nominal step up ratio of about 2/1, and is optimized for use with lower noise resistance amplifiers such as the AD797. As can be noted from the figure, the general topology is similar to the previous transformer coupled preamp, but some details allow premium levels of performance.

This preamp has a selectable gain feature, using GAIN switch S1 to alter R2 of the feedback network. This varies U1's gain (and thus overall gain) over a range of 20-50dB, making the preamp suitable for a wide range of uses. With the R2 step values shown, gain is selectable in 5dB increments. This ranges from 50dB with R2 (total) = 15Ω, down to 20dB with R2 (total) = 588.5Ω. The transformer provides a fixed gain of about 5.6dB.

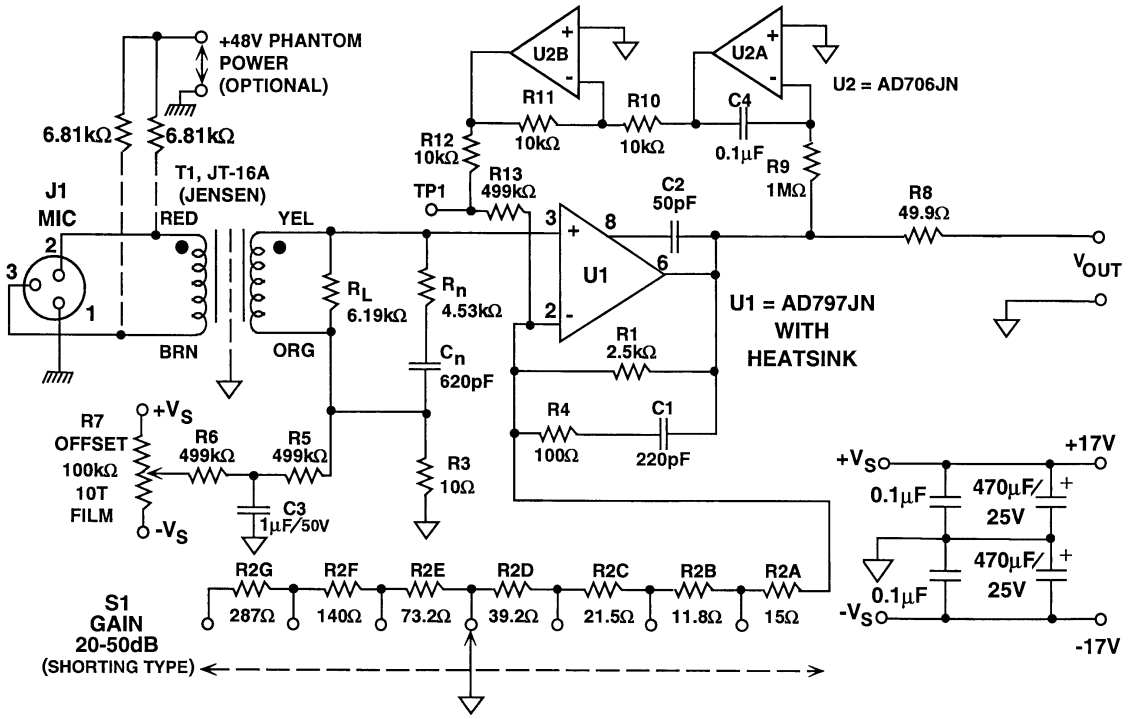

Figure 6-5: *Low noise transformer input 20 to 50 dB gain mic preamp*

Inasmuch as the AD797 has high precision as well as low distortion audio characteristics, this circuit can be DC coupled quite effectively. This has the worthwhile advantage of eliminating large electrolytic coupling caps in the gain network and in the output coupling between U1 and V_{OUT}. This is accomplished as follows:

The initial device offset of the AD797 is 80µV(max), a factor which allows a relatively simple trim by OFFSET trimmer R7 to null offset. R7 has a range of ±150µV at the AD797 input, with noise well decoupled by C3. With the preamp warmed up well, and working at a mid-range gain setting of 35dB, the offset can be trimmed out. This is best done with the servo temporarily defeated, by grounding test point TP1. Under this condition the V_{OUT} DC level is then trimmed to <1mV, via R7. This nulls out the residual offset of the AD797, and also ensures that the gain-range network sees minimal DC, which minimizes "pops" with gain changes. The offset shift thereafter with gain is only a

few mV, and is of little concern, since the servo circuit of U2A and U2B holds the longer term DC offset to 100µV or less, with little gain interaction. Note that for the gain-change scheme to work properly, S1 *must* be a shorting (make-before-break) type.

THD+N performance versus frequency of this mic preamp is shown in Figure 6-6, for conditions of 35dB gain, and successive input sweeps resulting in outputs of 0.5, 1, 2, and 5Vrms into 600Ω. From these data it is essentially clear that the only distortion in the circuit is due to the transformer, which is small and occurs only at the low frequencies. Above 100Hz, the apparent distortion is noise limited, to the highest frequencies.

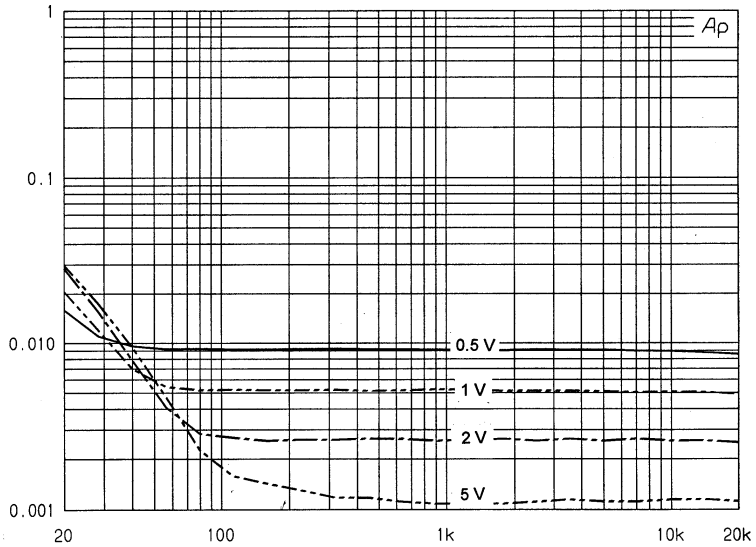

Figure 6-6: *Low noise transformer input mic preamp THD+N (%) versus frequency (Hz) for 35dB gain, outputs of 0.5, 1, 2, and 5Vrms into 600Ω*

The -3dB bandwidth of this circuit is just under 150kHz, and while this is essentially dominated by the JT-16A transformer and termination, bandwidth does reduce slightly at the highest gain (50dB). Like the previous transformer coupled circuit, this circuit also assumes a 150Ω source impedance, and similar application caveats apply.

The basic circuit as shown is single-ended with V_{OUT} taken from R8. However, a transformer can be simply added, as an option for driving balanced lines. When this is done, a nickel core type is suggested, for lowest distortion. One type suitable would be a Jensen JT-11-DM (or similar). It is coupled to the U1 output via a 10Ω resistor.

Just as shown the circuit is suited for local, higher impedance loads of 1kΩ and more. For very high levels of output drive or to drive long lines, a dedicated high current output driver should be used with U1, as generally described in the "Line Drivers" section. This can be most simply implemented by making U1 a composite amplifier, using a AD797 input section plus a follower-type output stage. A good choice for this would be a BUF04 IC, connected between pin 6 of the AD797 and the remaining circuitry. The buffer will isolate the U1 stage, allowing it to operate with highest linearity with difficult loads. Note also that ±17V supplies won't be necessary with the AD797 unless extreme voltage swings are required. More conventional (±15V) supplies will minimize the U1 heating.

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RIAA Phono Preamplifiers

An example of an audio range preamplifier application requiring equalized frequency response is the RIAA phono preamp. While LP record sales have faded with the establishment of new digital media, for completeness equipment is still designed to include phono playback stages. RIAA preamp stages, as amplifiers with predictable, non-flat frequency response, have more general application connotations. The design techniques within this section are specific to RIAA as an example, but they are also applicable to other frequency dependent amplitude designs in general. The techniques are also useful as a study tool, considering the various approaches advanced to optimize the function of high performance gain with predictable equalization (EQ). These last two points make these discussions useful in a much broader sense.

Some RIAA Basics

The RIAA equalization curve (see Reference 1) is shown in Figure 6-7, expressed as it is relative to DC. This curve indicates maximum gain below 50Hz (f1), with two high-frequency inflection points. Above f1, the gain rolls off at 6 dB/octave until a first high-frequency breakpoint is reached at 500Hz (f2). Gain then remains relatively constant until a second high-frequency breakpoint is reached at about 2.1kHz (f3), where it again rolls off at 6 dB/octave through the remainder of the audio region and above.

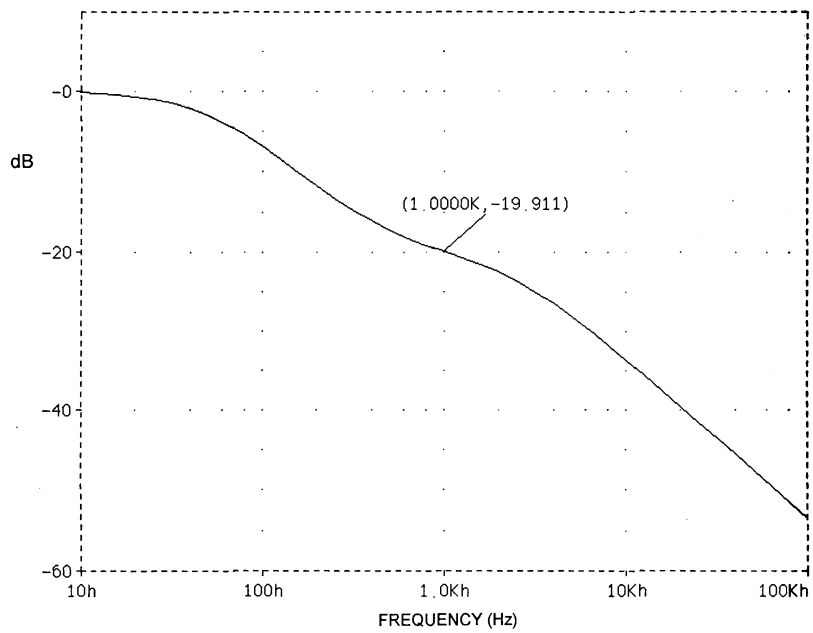

Figure 6-7: *Ideal RIAA de-emphasis (time constants of 3180, 318, 75μs)*

Use of a low frequency rolloff (f0, not shown) is at the option of the designer. Frequency response can be extended towards DC, or, alternately, rolled off at a low frequency below 50 Hz. When applied, this roll off is popularly called a "rumble" filter, as it reduces turntable/record related low-frequency disturbances, lessening low-frequency driver overload. This rolloff may or may not coincide with a fourth time constant (below).

However, gain at the frequencies f1, f2, and f3 describes the basic RIAA curve. In the standard, this is described in terms of three corresponding time constants, T1, T2, and T3, defined as 3180µs, 318µs, and 75µs, respectively (Reference 1, again). The T1-T3 are here described as they correspond to *ascending frequency*, the reverse of the terminology in Reference 1 (however the time constants themselves are identical). In some literature occasionally one may find the frequencies corresponding to T1, T2, and T3 referenced. These exact frequencies can be found simply by the basic relationship of:

$$f = 1/(2 \bullet \pi \bullet T) \qquad \text{Eq. 6-4}$$

So, for the three time constants specified, the frequencies are:

$$f1 = 1/(2 \bullet \pi \bullet T1) = 1/(2 \bullet \pi \bullet 3180E\text{-}6)$$

$$= 50Hz$$

$$f2 = 1/(2 \bullet \pi \bullet T2) = 1/(2 \bullet \pi \bullet 318E\text{-}6)$$

$$= 500Hz$$

$$f3 = 1/(2 \bullet \pi \bullet T3) = 1/(2 \bullet \pi \bullet 75E\text{-}6)$$

$$= 2122Hz$$

An IEC amendment to the basic RIAA response adds a fourth time constant of 7950µs, corresponding to an f0 of 20Hz when used (see Reference 2). Use of this rolloff has never been standardized in the US, and isn't treated in detail here.

The characteristic gain in dB for an RIAA preamp is generally specified relative to a 1kHz reference frequency. For convenience in evaluating the RIAA curve numerically, Figure 6-8 (opposite) is a complete 10-100kHz relative decibel table for the three basic RIAA time constants. From these data several key points can be observed: If the 1kHz gain is taken as the zero dB reference, frequencies below or above show higher or lower dB levels, respectively (Note 1, column 2). With a DC 0dB reference, it can be noted that the 1kHz gain is 19.91dB below the DC gain (Note 2, column 3).

Expressed in terms of a gain ratio, this means that in an ideal RIAA preamp the 1kHz gain is always 0.101 times the DC gain. The constant 0.101 is unique to all RIAA preamp designs following the above curve, therefore it can be designated as "K_{RIAA}", or:

$$K_{RIAA} = 0.101 \qquad \text{Eq. 6-5}$$

This constant logically shows up in the various gain expressions of the RIAA preamp designs following. In all examples discussed here (and virtually all RIAA preamps in general), the shape of the standard RIAA curve is fixed, so specifying gain for a given frequency (1kHz) also defines the gain for all other frequencies.

FREQ	VDB(6)(1)	VDB(5)(2)
1.000E+01	1.974E+01	-1.684E-01
1.259E+01	1.965E+01	-2.639E-01
1.585E+01	1.950E+01	-4.109E-01
1.995E+01	1.928E+01	-6.341E-01
2.512E+01	1.895E+01	-9.654E-01
3.162E+01	1.847E+01	-1.443E+00
3.981E+01	1.781E+01	-2.103E+00
5.012E+01	1.694E+01	-2.975E+00
6.310E+01	1.584E+01	-4.067E+00
7.943E+01	1.455E+01	-5.362E+00
1.000E+02	1.309E+01	-6.823E+00
1.259E+02	1.151E+01	-8.398E+00
1.585E+02	9.877E+00	-1.003E+01
1.995E+02	8.236E+00	-1.167E+01
2.512E+02	6.645E+00	-1.327E+01
3.162E+02	5.155E+00	-1.476E+01
3.981E+02	3.810E+00	-1.610E+01
5.012E+02	2.636E+00	-1.727E+01
6.310E+02	1.636E+00	-1.828E+01
7.943E+02	7.763E-01	-1.913E+01
1.000E+03	**8.338E-07**	**-1.991E+01**
1.259E+03	-7.682E-01	-2.068E+01
1.585E+03	-1.606E+00	-2.152E+01
1.995E+03	-2.578E+00	-2.249E+01
2.512E+03	-3.726E+00	-2.364E+01
3.162E+03	-5.062E+00	-2.497E+01
3.981E+03	-6.572E+00	-2.648E+01
5.012E+03	-8.227E+00	-2.814E+01
6.310E+03	-9.992E+00	-2.990E+01
7.943E+03	-1.184E+01	-3.175E+01
1.000E+04	-1.373E+01	-3.365E+01
1.259E+04	-1.567E+01	-3.558E+01
1.585E+04	-1.763E+01	-3.754E+01
1.995E+04	-1.960E+01	-3.951E+01
2.512E+04	-2.158E+01	-4.149E+01
3.162E+04	-2.357E+01	-4.348E+01
3.981E+04	-2.557E+01	-4.548E+01
5.012E+04	-2.756E+01	-4.747E+01
6.310E+04	-2.956E+01	-4.947E+01
7.943E+04	-3.156E+01	-5.147E+01
1.000E+05	-3.356E+01	-5.347E+01

Notes: **(1)** denotes 1kHz 0dB reference

(2) denotes DC 0dB reference

Figure 6-8: *Idealized RIAA frequency response referred to 1kHz and to DC*

It can also be noted from the RIAA curve of Figure 6-7 that the gain characteristic continues to fall at higher frequencies. This implies that an amplifier with unity-gain stability for 100% feedback is ultimately required, which can indeed be true, when a standard feedback configuration is used. There are many circuit approaches which can be used to accomplish RIAA phono-playback equalization, however all must satisfy the general frequency response characteristic of Figure 6-7.

Equalization Networks for RIAA Equalizers

Two equalization networks well suited in practice to RIAA phono reproduction are illustrated in Figure 6-9a and 6-9b, networks N1 and N2. Both networks with values as listed can yield with high accuracy the three standard RIAA time constants of 3180, 318, and 75µs as outlined by network theory (see References 3-6). For convenience, both theoretical values for the ideal individual time constants are shown at the left, as well as closest fit standard "no trim" values to the right. Designers can of course, parallel and/or series RC values as may be deemed appropriate, adhering to network theory.

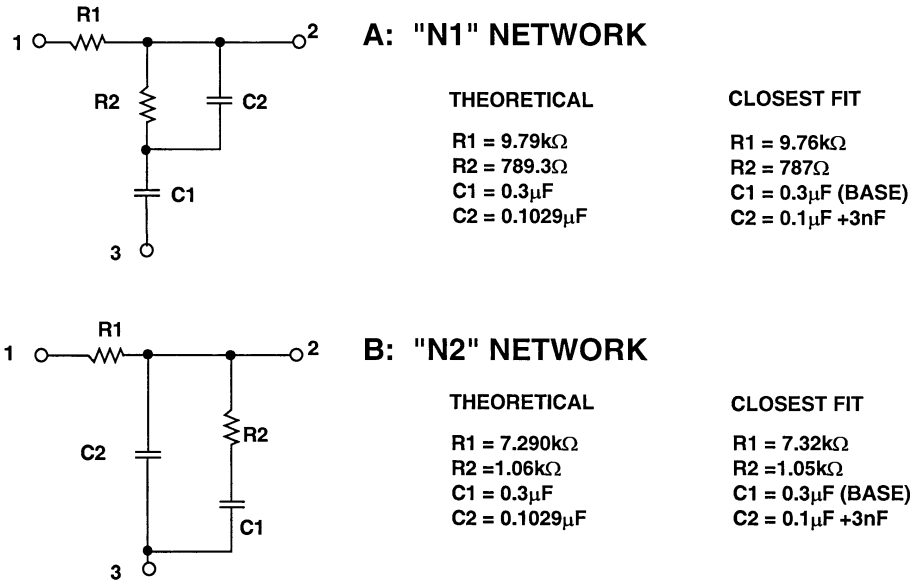

Figure 6-9: *Two RIAA EQ networks (T1=3180µs, T2=318µs, T3=75µs)*

There are of course an infinite set of possible RC combinations from which to choose network values, but practicality should rule any final selection. A theoretical starting point for a network value selection can begin with *any* component, but in practice the much smaller range of available capacitors suggests their selection first, then resistors, since they have a much broader span of (stock) values. Note that precision film resistors can in fact be obtained (on special order) in virtually *any* value, up to several megohms. The values listed here are those taken as standard from the E96 series.

Very high standards of EQ accuracy are possible, to tolerances of noticeably better than ±0.1dB (see for example data from Reference 8, also quoted in 6). In the design process, there are several distinct general aspects of EQ component selection which can impact the ultimate accuracy. These are worth placing in perspective before starting a design.

■ The *selection tolerance* of the component defines how far an ideal (zero manufacturing tolerance) component deviates from the theoretical value. A good design will seek to minimize this error by using either carefully selected standard values, or series and/or shunt combinations, so as to achieve selection tolerance of less than 1%, preferably zero.

■ The *manufacturing tolerance* of the component defines how far an otherwise ideal component deviates from its stated catalog value, such as ±1, ±2%, etc. This can

obviously be controlled by tighter specifications, but usually at some premium, particularly with capacitors of ±1% or less. Note that a "hidden" premium here can be long delivery times for certain values. Care should be taken to use standard stock values with capacitors— even to the extent that multiple standard values may be preferable (3 times 0.01µF for 0.03µF, as an example).

■ *Topology-related parasitics* must also be given attention, as they can also potentially wreck accuracy. Amplifier gain-bandwidth is one possible source of parasitic EQ error. However, a more likely error source is the parasitic zero associated with active feedback equalizers. If left uncompensated below 100kHz, this alone can be a serious error.

In any event, for high equalization accuracy to be "real", once a basic solid topology is selected, the designer must provide for the qualification of components used, by precise measurement and screening, or tight purchase tolerances. An alternative is iterative trimming against a reference standard such as that of Reference 9, but this isn't suited for production. An example is the data of Reference 8, derived with the network of Reference 9. If used, the utility of such a trim technique lies in the reduction of the equipment accuracy burden. While the comparator used needs to have high *resolution*, the accuracy is transferred to the network comparison standard used.

It should be understood that an appropriately selected high quality network will allow excellent accuracy, for example either N1 or N2 with the "closest fit" (single component) values of exact value yield a broadband error of about ±0.15dB. Accuracy about 3 times better than this is achieved with the use of N1 and the composite C2, as noted. The composite C2 is strongly suggested, as without it there is a selection error of about 3%.

It is also strongly recommended that only the highest quality components be employed for use in these networks, for obvious reasons. Regardless of the quality of the remainder of the circuit, it is surely true that the equalization accuracy and fidelity can be no better than the quality of those components used to define the transfer function. Thus only the best available components are used in the N1 (or N2) RC network, selected as follows:

■ *Capacitors*— should have close initial tolerance (1-2%), a low dissipation factor and low dielectric absorption, be non-inductive in construction, and have stably terminated low-loss leads. These criteria in general are best met by capacitors of the Teflon, polypropylene and polystyrene film families, with 1-2% polypropylene types being preferred as the most practical. Types to definitely avoid are the "high K" ceramics. In contrast, "low K" ceramic types, such as "NP0" or "COG" dielectrics, have excellent dissipation factors. See the passive component discussions of Chapter 7 on capacitors, as well as the component-specific references at the end of this section.

■ *Resistors*— should also be close tolerance (≤1%), have low non-linearity (low voltage coefficient), be temperature stable, with solid stable terminations and low-loss non-inductive leads. Types which meet these criteria best are the bulk metal foil types and selected thick films, or selected military grade RN55 or RN60 style metal film resistor types. See the passive component discussions of Chapter 7 on resistors, as well as the component-specific references at the end of this section.

It should be noted also that the specific component values suggested might not be totally optimum from a low impedance, low noise standpoint. But, practicalities will likely deter using appreciably lower ones. For example, one could reduce the input resistance of either network down to say 1kΩ, and thus lower the input referred noise contribution of the network. But, this in turn would necessitate greater drive capability from the amplifier stage, and raise the C values up to 1-3µF, where they are large, expensive, and most difficult to obtain. This may be justified for some uses, where performance is the guiding criterion rather than cost effectiveness, or the amplifiers used are sufficiently low in noise to justify such a step. Regardless of the absolute level of impedance used, in any case the components should be adequately shielded against noise pickup, with the outside foils of C1 or C2 connected either to common or a low impedance point.

These very same N1/N2 networks can suffice for both active and passive type equalization. Active (feedback) equalizers use the network simply by returning the input resistor R1 to common, that is jumpering points 1-3, and employing the network as a two-terminal impedance between points 1+3, and 2. Passive equalizers use the same network in a three-terminal mode, placed between two wideband gain blocks.

RIAA Equalizer Topologies

There are of course many different circuit topologies that can be used to realize an RIAA equalizer. Dependent upon the output level of the phono cartridge to be used, the 1kHz gain of the preamp can range from 30 to more than 50dB.

Magnetic phono cartridges in popular use consist of two basic types: moving magnet (MM) and moving coil (MC). The moving magnet types, which are the most familiar, are suitable for the first two circuits described. The moving coil cartridge types are higher performance devices; they are less commonplace but still highly popular.

Functionally, both types of magnetic cartridges perform similarly, and both must be equalized for flat response in accordance with the RIAA characteristic. A big difference in application, however, is the fact that moving magnet types have typical sensitivities of about 1mV of output for each cm/s of recorded velocity. In moving coil types, sensitivity on the order of 0.1mV is more common (for a similar velocity). In application then, a moving coil RIAA preamp must have more gain than one for moving magnets. Typically, 1kHz gains are 40-50 dB for moving coils, but only 30-40 dB for moving magnets.

Noise performance of a moving coil preamp can become a critical performance factor however, because of low-output voltage and low impedance involved— typically this is in the range of just 3-40Ω. The following circuit examples illustrate techniques that are useful to these requirements.

Actively Equalized RIAA Preamp Topologies

The most familiar RIAA topology is shown in general form in Figure 6-10, and is called an active feedback equalizer, as the network N used to accomplish the EQ is part of an active feedback path (see References 10, 11). In these and all of the following discussions it is assumed that the input from the pickup is appropriately terminated by R_t-C_t, which are selected for flat *cartridge* frequency response driving U1. The following discussions deal with the *amplification* frequency response, given this ideal input signal.

Assuming an adequately high gain amplifier for U1, the gain/frequency characteristics of this circuit are determined largely by the network. The gain of the stage is set by the values of the network N and R_3, and the U1 output is a low impedance, V_{OUT}. The 1kHz gain of this stage is defined by the RIAA curve and resistors R_1 and R_3, and is:

$$G = 0.101 \bullet [1 + (R_1/R_3)] \qquad \text{Eq. 6-6}$$

where 0.101 is the constant K_{RIAA}. R_1 is within N; R_4 and R_5 are discussed momentarily.

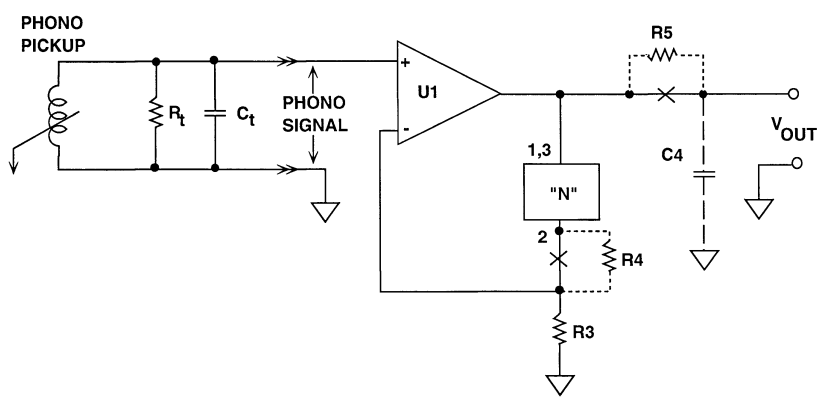

Figure 6-10: *Active feedback RIAA equalizer*

As noted previously, an ideal RIAA response continues to fall with increasing frequency, and can in fact be less than unity at some high frequency (Fig. 6-7, again). But, the basic U1 topology of Figure 6-10 can't achieve this, as the minimum gain seen at the output of U1 approaches unity at some (high) parasitic zero frequency, where the network equivalent series capacitive impedance of C_1 and C_2 is equal to R_3. At this zero frequency, the response from U1 simply levels off and ceases to track the RIAA curve.

However, in terms of practical consequence the error created by this zero may or may not be of significance, dependent upon where the zero falls (as determined by gain). If well above audibility (i.e., ≥ 100kHz), it will introduce a small equalization error at the upper end of the audio range. For example, if it falls at 100kHz, the 20kHz error is only about 0.3dB. Fortunately, this error is easily compensated by a simple low-pass filter after the amplifier, R_5-C_4. The filter time constant is set to match the zero T4, which is:

$$T4 = R_3 \bullet C_{EQUIV} \qquad \text{Eq. 6-7}$$

where R_3 is the value required for a specific gain in the design.

C_{EQUIV} is the series equivalent capacitance of network capacitors C_1 and C_2, or:

$$C_{EQUIV} = (C_1 \bullet C_2)/(C_1 + C_2) \qquad \text{Eq. 6-8}$$

Here the C_{EQUIV} is 7.6nF and R_3 200Ω, so T4 = 1.5µs The product of R5 and C4 are set equal to T4, so picking a R5 value solves for C4 as:

$$C4 = T4/R5 \qquad \text{Eq. 6-9}$$

The 1.5µs R_5-C_4 time constant is realized with R_5 = 499Ω and C4 = 3nF. This design step increases the output impedance, making it more load susceptible. This should be weighed against the added parts and loading. In general, R_5 should be low, i.e., ≤1kΩ.

In some designs, a resistor R_4 (dotted in Fig. 6-10) may be used with N (for example, for purposes of amplifier stability at a gain higher than unity). With R_4, T4 is calculated as:

$$T4 = (R_3 + R_4) \bullet C_{EQUIV} \qquad \text{Eq. 6-10}$$

The R_5-C_4 product is again chosen to be equal to this T4 (more on this below).

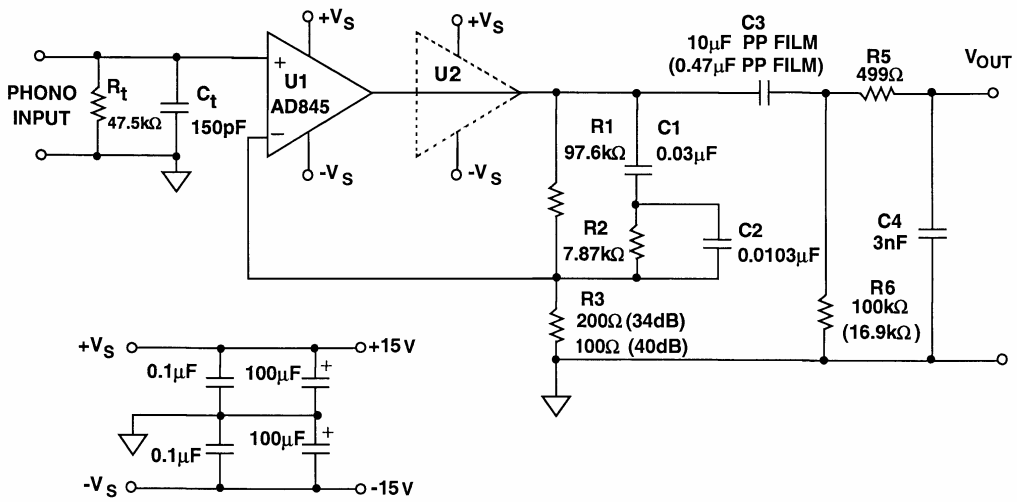

Figure 6-11: *A DC-coupled active feedback RIAA moving magnet preamp*

The next two schematics illustrate variations of the most popular approach to achieving a simple RIAA phono preamp, using active feedback, as just described. Figure 6-11 above is a high-performance, DC coupled version using precision 1% metal film resistors and 1 or 2% capacitors of polystyrene or polypropylene type. Amplifier U1 provides the gain, and equalization components R1-R2-C1-C2 form the RIAA network, providing accurate realization with standard component values. N1 is the network, with 1 and 3 common.

As mentioned, input RC components R_t-C_t terminate the moving magnet cartridge with recommended values (shown as typical). In terms of desired amplifier parameters for optimum performance, they are considerably demanding. For lowest noise from a cartridge's inductive source, the amplifier should have an input voltage noise density of 5nV/√Hz or less (favoring a bipolar), and an input current noise density of 1pA/√Hz or less (favoring a FET). In either case, the 1/F noise corner should be as low as possible.

For bipolar-input amplifiers, DC input-bias current can be a potential problem when direct coupling to the cartridge, so in this circuit only a very low input bias current type is suggested. If a bipolar input amplifier is used for U1, it should have an input current of <<100nA for minimum DC offset problems (assuming a typical phono cartridge of ≈1kΩ resistance). Examples are the OP27, OP270 families. FET-input amplifiers generally have negligible bias currents but also tend typically to have higher voltage noise. FET-input types useful for U1 are the AD845 and OP42, even though their voltage noise is not as low as the best of the bipolar devices mentioned. On the plus side, they both have a high output current and slew rate, for low distortion driving the feedback network load (approximately the R_3 value at high frequencies). Of the two, the OP42 has lower noise, the AD845 higher output current and slew rate.

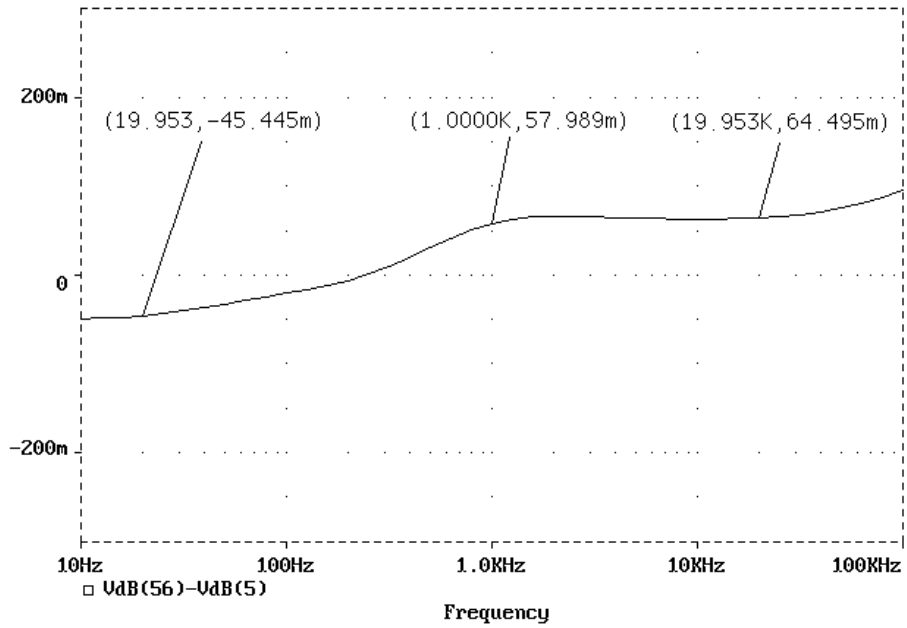

Figure 6-12: *Relative error (B) versus frequency for DC-coupled active feedback RIAA moving magnet preamp, gain of 34dB*

For high gain accuracy at high stage gains, the amplifier should have a high gain-bandwidth product; preferably >5MHz at audio frequencies. Because of the 100% feedback through the network at high frequencies, the U1 amplifier must be unity-gain-stable. To minimize noise from sources other than the amplifier, gain resistor R_3 is set to a relatively low value, which generates a low voltage noise in relation to the amplifier.

RIAA accuracy is quite good using the stock equalizer values. A PSpice simulation run is shown in Figure 6-12 above for the suggested gain of 34dB. In this expanded scale plot over the 20-20kHz range, the error relative to the 1kHz gain is less than ±0.1dB.

As can be noted from Fig. 6-12, the relative amplitude is expanded, to easily show response errors. A perfect response would be a straight line at 0dB, meaning that the circuit under test had exactly the same gain as an ideal RIAA amplifier of the same 1kHz gain. This high sensitivity in the simulation is done via the use of a feature in PSpice allowing the direct entry of Laplace statements (see Reference 10). With this evaluation

tool, the ideal transfer function of an RIAA equalizer can be readily generated. The key parameters are the three time constants described above, and the ideal DC gain.

The syntax to enable this mode of comparison is contained in the listing of Figure 6-13, which is the PSpice CIR file for the circuit of Fig. 6-11. The Laplace details are all contained within the dotted box, and need only the editing of one value, "ENORM", for gain normalization from one circuit to another (see boldface). In this case ENORM is set to 490.7, to match the ideal R1 and R3 values of Fig. 6-13. When the analysis is run, a difference display of the circuit-under-test and the ideal outputs (i.e., VdB(56)-VdB(5)) shows the relative response (Fig. 6-12, again). Vertical axis scaling is easily adjusted for sensitivity, and is ±300mB as displayed in Fig. 6-12.

```
RIAA34LP: 34 dB gain RIAA preamp with AD845
*
.OPT ACCT LIST NODE OPTS NOPAGE LIBRARY
.AC DEC 10 10 100KHZ
.LIB D:\PS\ADLIB\AD_RELL.LIB
.PRINT AC VDB(5) VDB(56)
.PROBE
VIN 1 0 AC 1E-3
VCC   52  0  +15V
VEE   53  0  -15V
* ---------- V(5) = idealized RIAA frequency response -----------------
*
* Uses Laplace feature of PSpice Analog Behavioral option
* for frequency response reference.
* ENORM = ideal U1 DC gain = 1+(R1/R3) Use ideal values for R1, R3
* T1 - T3 are time constants desired (in µs).
* Input = node 1, Laplace Output = node 5
.PARAM ENORM  = {490.7}
.PARAM T1 = {3180}      ; Reference RIAA constants, do not alter!
.PARAM T2 = {318}       ; Reference RIAA constants, do not alter!
.PARAM T3 = {75}        ; Reference RIAA constants, do not alter!
*
ERIAA 5 0 LAPLACE {ENORM*V(1)}={(1+(T2*1E-6)*S)/((1+(T1*1E-6)*S)*(1+(T3*1E-6)*S))}
RDUMMY5 5 0 1E9
*
* ---------------------------------------------------------------------
*
*    (+) (-) V+  V-  OUT
XU3   1  21  52  53  55 AD845
*  Active values         Theoretical values
R1 55  21  97.6K          ; 97.9k
R2 21  8   7.87K          ; 7.8931563k
C1 55  8   30NF           ; 30nF
C2 21  8   10.3NF         ; 10.2881nF
R3 21  0   200            ; 199.9148
C3 55  100 10E-6
R6 100 0   100K
R5 100 56  499
C4 56  0   3.0000E-9
.END
```

Figure 6-13: *An example PSpice circuit file which uses the Laplace feature for ideal RIAA response comparison*

The 1kHz gain of this circuit can be calculated from Eq. 6-6 above. For the values shown, the gain is just under 50 times (≈34dB). Higher gains are possible by decreasing R_3, but gains >40dB may show increasing equalization errors, dependent upon amplifier bandwidth. For example, R_3 can be 100Ω for a gain of about 100 times (≈40dB). Note that if R_3 is changed to 100Ω, C_4 should also be changed to 1.5nF, to satisfy Eq. 6-9.

Dependent upon the amplifier in use, this circuit is capable of very low distortion over its entire range, generally below 0.01% at levels up to 7Vrms, assuming ±15V supplies. Higher output with ±17V supplies is possible, but will require a heat sink for the AD845. U2 is an optional unity-gain buffer useful with some op amps, particularly at higher gains or with a low-Z network. But this isn't likely to be necessary with U1 an AD845.

For extended low-frequency response, C_3 and R_6 are the large values, with C_3 preferably a polypropylene film type. If applied, the alternate values form a simple 6dB per octave rumble filter with a 20Hz corner. As can be noted from the figure's simplicity, C_3 is the only DC blocking capacitor in the circuit. Since the DC circuit gain is on the order of 54dB, the amplifier used must be a low offset-voltage device, with an offset voltage that is insensitive to the source. Since these preamps are high-gain, low-level circuits (≥50dB of gain at 50/60Hz), supply voltages should be well regulated and noise-free, and reasonable care should be taken with the shielding and conductor routing in their layout.

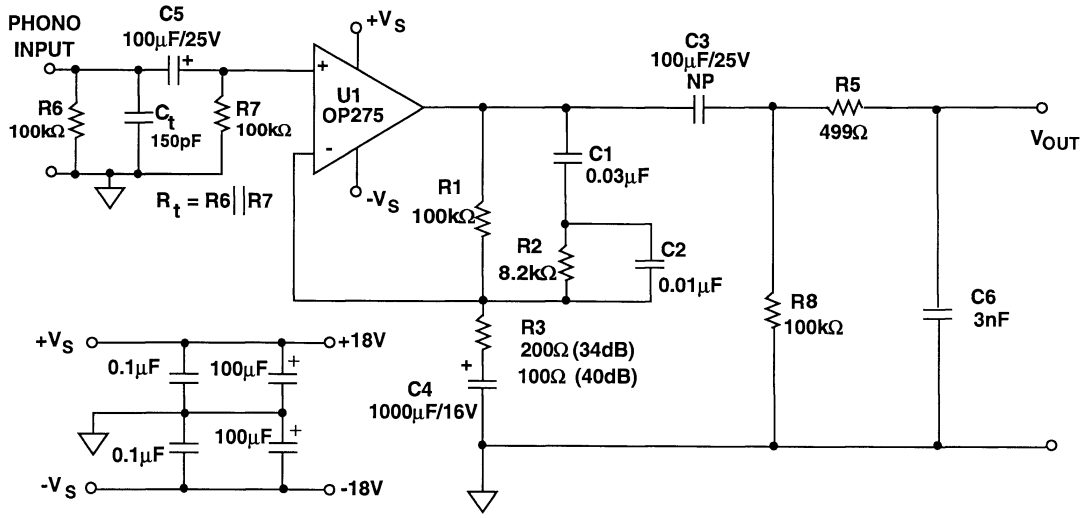

Figure 6-14: *An AC-coupled active feedback moving magnet RIAA preamp*

Alternately, an inexpensive AC-coupled form of this circuit can be built with higher bias current, low-noise bipolar op amps, for example the OP275, I_B = 350nA(max), which would tend to make direct coupling to a cartridge difficult. This form of the circuit is shown in Figure 6-14, and can be used with many unity gain stable bipolar op amps.

Here input AC coupling to U1 is added with C_5, and the cartridge termination resistance R_t is made up of the R_6-R_7 parallel equivalent. R_3 of the feedback network is AC-grounded via C_4, a large value electrolytic. These measures reduce the DC offset at the output of U1 to a few mV. Nearest 5% values are also used for the network components, making it easily reproducible and inexpensive. C_3 is a non-polar electrolytic type, and the R_3-C_4 time constant as shown provides a corner frequency of ≤1Hz at the 34dB gain.

Frequency response of this version (not shown) isn't quite as good as that of Figure 6-11, but is still within ±0.2dB over 20-20kHz (neglecting the effects of the low frequency rolloff). If a tighter frequency response is desired, the N1 network values can be adjusted. With a higher rated maximum supply voltage for the OP275, the power supplies of this version can be ±21V if desired, for outputs up to 10Vrms.

There is another, very useful variation on the actively equalized RIAA topology. This is one that operates at appreciably higher gain and with lower noise, making it suitable for operation with higher output moving coil (MC) cartridges. In this design example, shown below in Figure 6-15, the basic circuit is used is quite similar to that of Fig. 6-11. The lower R_t and C_t values shown are typical for moving coil cartridges. They are of course chosen per the manufacturer's recommendations (in particular the resistance).

To make it suitable for a high-output MC cartridge, a very low-noise FET op amp is used for U1, the AD745. The AD745 is stable at a minimum gain of five times, as opposed to the unity-gain stable op amps of the prior examples. This factor requires a modification to gain resistors R1-R3. This is the inclusion of an extra resistor, R4. With the ratio shown, R3 and R4 form a 5/1 voltage divider for the voltage seen at the bottom of network N (the R1-R2-C2 node). This satisfies U1's gain-of-five stability requirement.

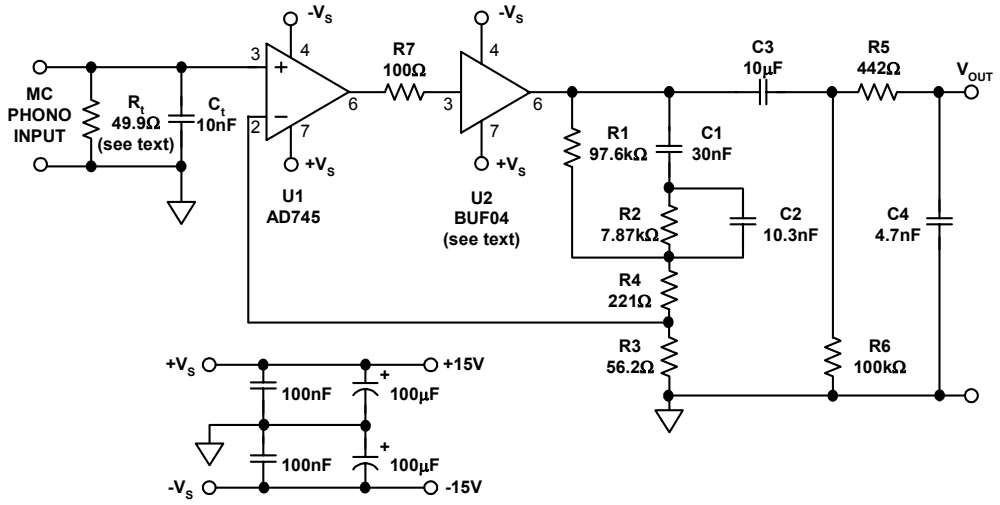

Figure 6-15: *A low noise DC-coupled active feedback RIAA moving coil preamp with 45dB of gain*

In this gain setup, R3 is still used for the gain adjustment, and R1-R2-C1-C2 still form the basic N1 RIAA network. With R4 used, Eq. 6-9 is used to calculate the T4 time constant. With C4 chosen as a standard value, R5 is then calculated. With these N1 network values and a 45dB 1kHz gain, R3 is 56.2Ω, which is still suitable as a low noise value operating with either an AD745 or an OP37 used for U1.

Some subtle points of circuit operation are worth noting. The DC gain of this circuit is close to 1800, which can result in saturation of U1 if offset isn't sufficiently low. Fortunately, the AD745 has a maximum offset of 1.5mV over temperature, making the output referred offset always less than 3V. While this may limit the maximum output swing some due to asymmetrical clipping, 5Vrms or more of swing should be available operating from ±15V supplies. Coupling capacitor C3 decouples the DC output offset at U2, so any negative consequences of DC-coupling the U1 gain path are minimal.

For minimal loading of U1 and maximum linearity at high gains, the unity-gain buffer amplifier U2 is used, a BUF04. The BUF04 is internally configured for unity-gain operation, and needs no additional components. Note that this buffer is optional, and is not absolutely required. Other buffer amplifiers are discussed later on in this chapter.

This Fig. 6-15 circuit was analyzed with PSpice using the Laplace comparison technique earlier described, and the results are displayed in Figure 6-16. As was true previously, the vertical scaling of this display is very sensitive; ±300mB (or ±0.3dB). Thus, placed in context, gain errors relative to 1kHz over 20-20kHz are extremely small, ≈0.1dB. Lab measurements of the circuit were also consistent with the simulation. Of course in terms of audible effects, errors of ±0.1dB or less aren't likely to be apparent.

Distortion/noise measurements of the circuit are essentially dominated by noise (as opposed to actual distortion) measuring ~0.01% THD+N or less, over output levels ranging from 0.5 to 5Vrms, from 20Hz-20kHz. Of course, as with any high gain circuit, layout and lead dress into the circuit are extremely critical to noise, and must be arranged for minimum susceptibility. Supply voltages must be low in noise, and well regulated.

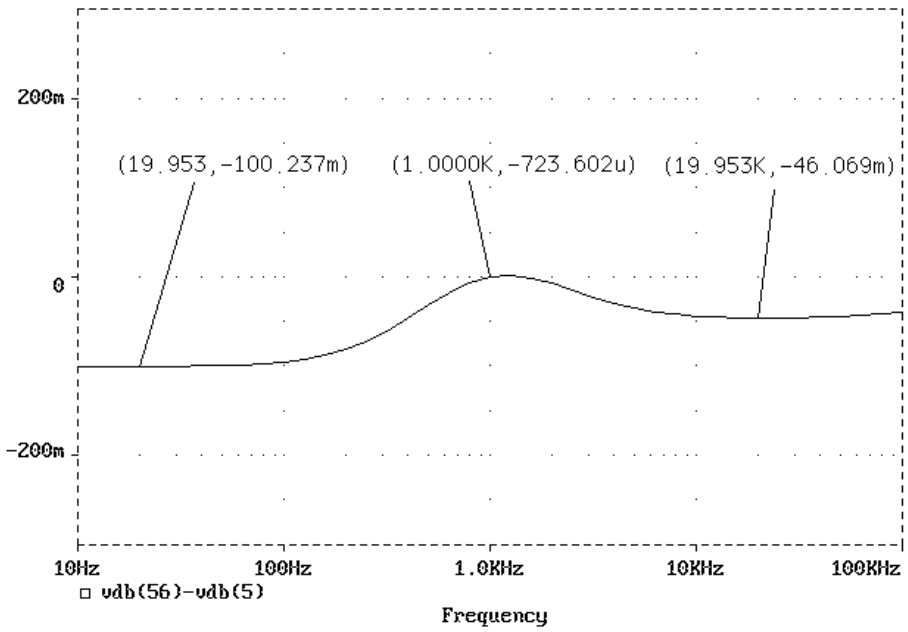

Figure 6-16: *Relative error (B) versus frequency for DC-coupled active feedback RIAA moving coil preamp, gain of 45dB (simulation)*

This exercise has illustrated both the basic design process of the active RIAA equalizer, as well as a convenient SPICE analysis method to optimize the design for best frequency response. It is not suggested that the exact network values shown of the examples are the only ones suitable. To the contrary, great many sets of values can be used with success comparable to that shown above.

This final active equalizer circuit example is the best of the bunch, and has a virtue of being easily adapted for other operating conditions; i.e., higher gain, other networks, etc. For example, note that even lower noise MC operation is possible, by using the ≤1nV/√Hz AD797 for U1, and scaling the N1 RC components further downward. This will have the desirable effect of making R3 lower than 50Ω, which minimizes the R1-R4 network's noise. Note that gains of 50dB or more are also possible, suitable for very low output moving coil cartridges (given suitable attention to worst case U1 offsets).

Passively Equalized RIAA Preamp Topologies

Another RIAA design approach is the so-called *passively equalized* preamp (see Reference 11). This topology consists of two high quality, wideband gain blocks, separated by a three terminal passive network, N (N can be either network N1 or N2). The gain blocks are assumed very wide in bandwidth, so in essence the preamp's entire frequency response is defined by the passive network, thus the name passively equalized.

A circuit topology useful for such RIAA phono applications is shown in Figure 6-17. This circuit consists of two high-quality wide bandwidth gain blocks, U1 and U2, as discussed above. Selection of these amplifiers and their operating conditions optimizes the preamp for gain, noise, and overload characteristics. The circuit can be set up for either MM or MC operation by simple value changes and op amp selection.

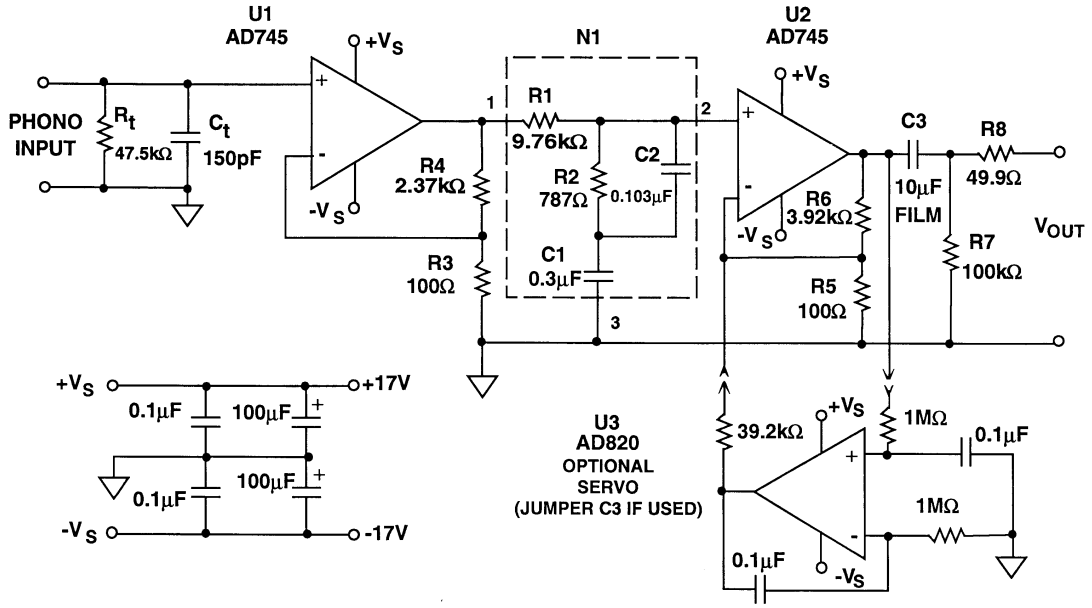

Figure 6-17: *A passively equalized RIAA preamp with 40dB gain*

The gain stages are set up for the required total gain, via R_4-R_3 and R_6-R_5. In general, the total 1kHz gain of this circuit G is:

$$G = 0.101 \bullet [1 + (R_4/R_3)] \bullet [1 + (R_6/R_5)] \qquad \text{Eq. 6-11}$$

The op amp gain blocks could be made identical for purposes of simplicity but are not necessarily so for the following reasons. A preamplifier topology such as this must be carefully optimized for signal-handling capability, both from an overload standpoint and from a low-noise viewpoint. Stage U1 is desirably chosen for a gain sufficiently high that the input-referred noise will be predominantly due to this stage and the cartridge, but yet not so high that it will readily clip at high-level high-frequency inputs. Amplifiers with a ≈10Vrms output capability allow U1 to accept ≈400 mVrms at high frequencies using ±18V supplies, while still operating with useful gain (about 25 times).

The gain of the two blocks are set by R_4-R_3 and R_6-R_5, as defined by Eq. 6-11. The gain values shown yield a 1kHz gain that is the product of the U1-U2 stage gains (24.7 times

40.2), times that of the interstage network N (0.101). This yields an overall 40dB 1kHz gain. Other gains are realized most simply by changes to R_5 or R_3.

As noted previously, a passively equalized preamplifier such as this must be carefully optimized both from an overload standpoint and from a low noise viewpoint. Stage U1 is desirably chosen for a gain sufficiently high that the input-referred noise will be predominantly due to this stage (and the cartridge, when connected), but yet not so high that it will readily clip at high-level high-frequency inputs. To aid this objective, maximum supply voltage and a high output capability amplifier should be used for U1.

Note that U1 operates at relatively high gain, but it needn't be unity gain stable. Decompensated low noise op amps such as the OP37 and the FET input AD745 will provide best signal/noise ratio here. For other FET-input types, the AD845 as well as the OP17 family types will also yield good performance, but with higher noise levels.

In general, the preceding factors dictate that gain distribution between U1 and U2 be LOW/HIGH from an overload standpoint, but HIGH/LOW from a noise standpoint. Practically, these conflicting requirements can be mitigated by choosing the highest allowable supply voltage for U1, as well as a low noise device. Because of nearly 40dB loss in the network N at 20 kHz, the output overload of the circuit will be noted at high frequencies first. With the gain distribution shown, the circuit allows a 3Vrms undistorted output to 20kHz with ±15V supplies, or more with higher supply voltages.

The equalization network N following U1 should use the lowest impedance values practical from the standpoint of low noise, as the noise output at pin 2 of the network is equivalent to the input referred noise of A2. The network of Fig. 6-17 uses the "N1" RC values of R_1-R_2-C_l-C_2 of Figure 6-9a. As noted, scaling can be applied to either network of Figure 6-9 for component selection, as long as the same ratios are maintained.

Noise in amplifier U2 is less critical than U1 at low frequencies, but is still not negligible. A low voltage noise device is very valuable to the U1 and U2 positions, as is a relatively low input current noise. If extremely low noise performance is sought, such as for a moving coil preamp, then the N1 values can be reduced further, and R3 be lowered for lower noise and additional gain. For example, a 45dB gain preamp could be realized by just dropping R3 to 56.2Ω, and using an OP37 for U1.

As mentioned before, a low bias current device is appropriate to U1 using bipolar amplifiers. With a 100nA or less bias current device, direct coupling to a moving magnet phono cartridge is practical. For example, the 80nA (maximum) bias current of the OP37 will induce only an additional 80-160µV input voltage offset at U1 for a typical 1-2kΩ cartridge resistance. For lower DC resistance MC cartridges, this will be much less of course. Similarly, the bias current induced offset voltage of U2, from the 10kΩ DC resistance of R_1 will also be low relative to the amplified offset of U1. As a result, the worst-case overall output DC offset using two AD745s can be held to under 2V for a 40dB gain, allowing a single C_3 coupling capacitor for DC blocking purposes.

Frequency response of this passively equalized preamp tends to be better than that of the active versions, because of less interaction with the amplifier(s) as compared to the active preamps. It can approach the inherent accuracy of the network components in the audio range, with potentially greater errors at higher frequencies.

Figure 6-18 illustrates this point, in a simulation of the Figure 6-17 circuit using the OP37 models. The midband error is on the order of ±0.02dB with the N1 network composite values. For practical purposes then, the frequency response errors of this circuit will be governed by the tolerances of the network components used within it.

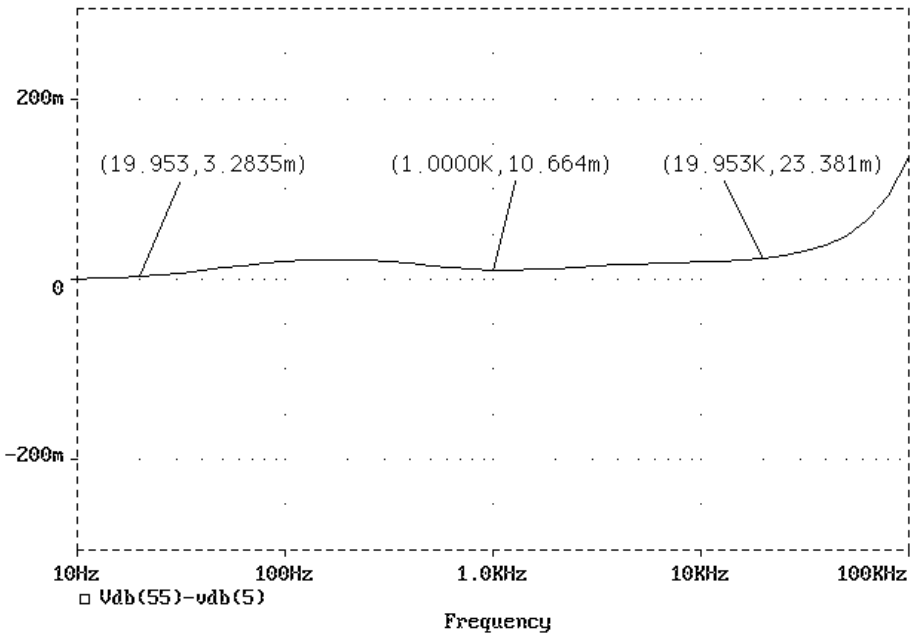

Figure 6-18: *Relative error (B) versus frequency for passively equalized RIAA preamp, gain of 40dB (simulation)*

This circuit also can be optionally adapted to servo control of the output offset. This is accomplished by deleting coupling capacitor C_3, substituting a jumper in its place, and using the noninverting servo integrator U3 around stage U2. This is shown as an option within Figure 6-17. A general-purpose noninverting servo can be used for U3, along with a low-offset op amp, such as the AD820, or the OP97.

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Audio Line Level Stages

Audio line level stages represent an intermediate level in dynamic range for practical audio circuits using modern IC devices. Line level amplifying stages generally work with single-ended or balanced input/output signal levels of 1-10V, and at medium levels of power. This section discusses some basic types of audio line stages which are:

■ *Line receivers*— including line receiver stages which accept single-ended or balanced line level signals with maximum noise immunity, and provide scaled outputs for further processing.

■ *Line amplifiers*— including amplifiers which scale a received signal in single-ended form and feature low distortion designs.

■ *Line drivers*— including single-ended and balanced drivers, which are capable of driving appreciable output levels in terms of voltage, swing, current levels, and/or difficult loads, such as capacitive lines.

Some general concepts of line driving and buffer amplifier design have been covered previously, with emphasis on video applications (see References 1-3). Some of the material in this section continues and expands on those themes with audio line-receiver and line-driver discussions in a wide variety of applications. Video applications for line driving and receiving is discussed in detail within section 6-2.

Audio transmission systems, unlike their video counterparts, do *not* use terminated transmission lines as a rule, so long transmission lines usually appear capacitive. Therefore, the concepts of capacitive load isolation are also important to audio drivers. In general, when building practical audio circuits of any type, "housekeeping" rules of layout and bypassing are strongly recommended, particularly so for audio buffer and line driver circuits. They are discussed in further detail in that section.

The function of sending/receiving audio signals between various system components has traditionally involved tradeoffs of one form or another. Fully differential or *balanced* transmission systems are best at rejecting low frequency and RF noise, so they are used for highest performance, and are discussed in some detail following.

A typical audio system block diagram using differential or balanced transmission is shown in Figure 6-19 (opposite). In concept, a balanced transmission system like this could use several input/output coupling schemes within the driver and receiver. Some major points distinguishing coupling method details are discussed briefly below, before addressing actual circuits.

Transformers (see References 4-7) have been a traditional audio line coupling element. They can be used at either input or output stage. They also have well known problems with noise pickup, frequency response, distortion, and operating level. While these problems are soluble to some degree, answers are usually costly. Nevertheless, transformers are unexcelled in notable areas.

The single most outstanding virtue of transformer operation lies in the ability to isolate while transmitting the signal, which shows up in two regards. The first of these is that transformers, which transmit an audio signal between the end terminals of an isolated winding, thus *galvanically isolate* driver and receiver stages. This is accomplished at common mode voltage (ground difference) levels up to the breakdown potential of the windings, allowing signals to be transmitted across very high ground potential differences (tens or hundreds of volts). This feature is one very difficult to achieve with solid state circuitry. Secondly, suitably designed transformers can have very high common mode rejection (CMR) over the audio range, ≥100dB in some cases, a factor basically intrinsic to their nature. Some transformer-isolated stages are described in this section.

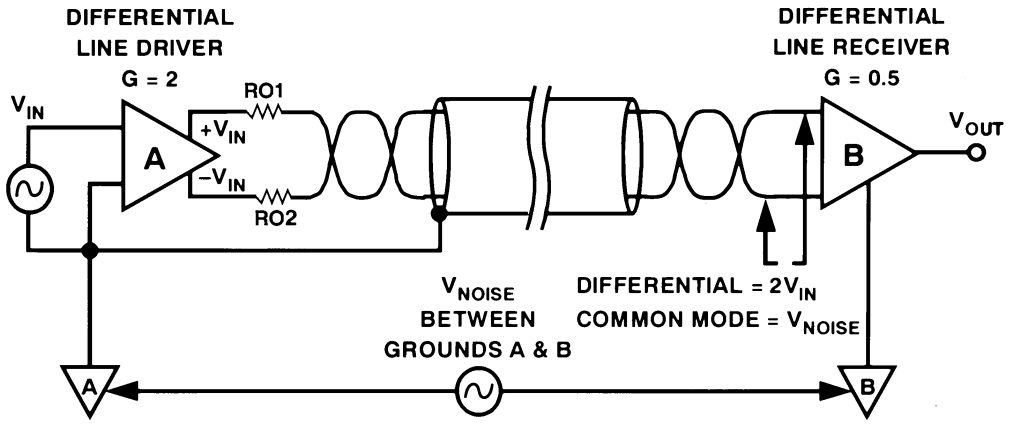

Figure 6-19: *An audio balanced transmission system*

In practice the general system of Figure 6-19 can use either transformer-based or active stage coupling to the line, at either end. The goal for either approach is to reproduce a final signal V_{OUT} equal to V_{IN}, while rejecting noise between grounds A and B by a factor of 80-100dB. Typically, a unity gain (overall) design uses a balanced line drive of $\pm V_{IN}$, followed by a receiver gain "G" of ½, which maximizes the receiver CM range.

A point worth noting that the ± voltage drive to the line need *not* be exactly balanced to reap the benefits of balanced transmission. In fact the drive can be asymmetrical to some degree, and the signal will still be received at V_{OUT} with correct amplitude, and with good noise rejection. What *does* need to be provided is two well-balanced line-driving impedances, R_{O1} and R_{O2}. Also, in conjunction with these balanced drive impedances, the associated (+) and (–) receiver input impedances should also be equal. The technical reasons for this will be apparent shortly.

Audio Line Receivers

A brief review of the topologies and application points of audio line receivers helps in understanding their evolution, and more importantly, how their audio performance differs with topological changes. Figure 6-20 is a diagram of a classic 4 resistor differential amplifier. This general circuit is also known as the most simple instrumentation amplifier form, even though its performance as an in-amp has severe limitations. Within audio applications, this and related circuits are called "line receivers" for the sake of brevity. Various in-amp type topologies have developmental histories dating from the late sixties up to and including today's modern in-amp ICs (see References 8-12 and Chapter 2).

In today's professional audio world, signals by and large get transmitted in balanced mode (Fig. 6-19, again). This fact is simply due to the much greater noise immunity of this method, vis-à-vis the more simple, but highly noise-susceptible single ended method.

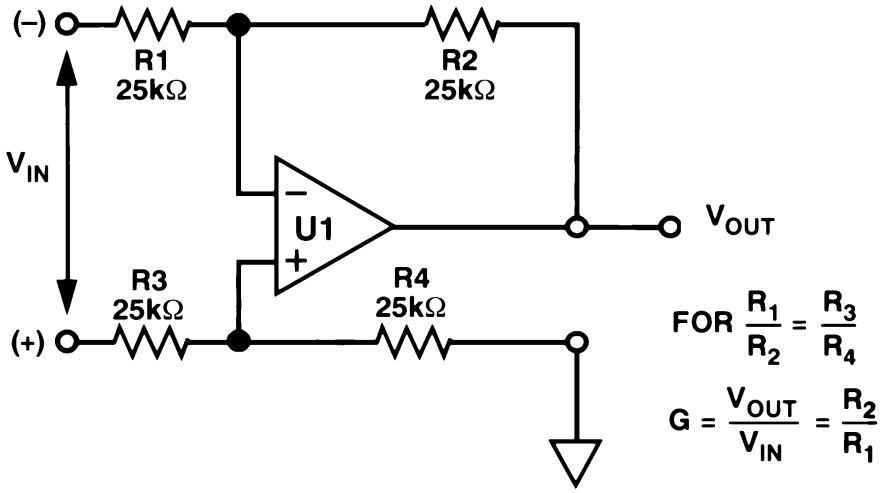

Figure 6-20: *A simple line receiver using a 4-resistor differential amplifier*

Yet, even within the professional audio world there is no real unanimity on signal driver and receiver circuits for use within balanced circuits— they take on many forms and have differing performance, and a wide variety of circuits find use. Before getting into actual receiver circuitry, it is helpful to take a brief look at some problems impacting circuit performance in terms of common mode (CM) noise susceptibility. This will illustrate how careful hardware choices lowers system cost/size, and maintains excellent performance. Conversely, simple receivers can also be used, for modest performance.

Source-Load Interactions Within Balanced Systems

Some recent attention has focused on the general problem of noise susceptibility in audio system interfacing (see references 13 and 14). The discussions below are concerned with how balanced system drivers and receivers interact fundamentally to produce undesired side effects of noise susceptibility. Suggestions for practical solutions are then offered.

In most simple form, a balanced audio transmission system consists of a differential output driver, an interconnecting cable, and a differential input receiver, such as shown in Fig. 6-19 (again). The driver produces nominally equal and out-of-phase output signals, with some characteristic (and matched) source impedances, R_{OUT1} and R_{OUT2}. As will be

seen, from a noise susceptibility standpoint, it is highly desirable that these two impedances be well balanced, i.e., matched. The driver is connected to the input end of a balanced transmission line, typically a shielded twisted pair. At the opposite end of this line, a differential input receiver receives the balanced signal, and (ideally) rejects the CM noise voltage V_{NOISE}.

The design of both the driver and the receiver has great influence upon how well the overall scheme works in transmitting a noise-free audio signal from driver to receiver. References 14 and 15 discuss different driver and receiver types, active and passive. These papers bring out the inherent degradation in noise sensitivity active receivers can trigger, if they do not have input characteristics which are an appropriate complement to the system driving impedances.

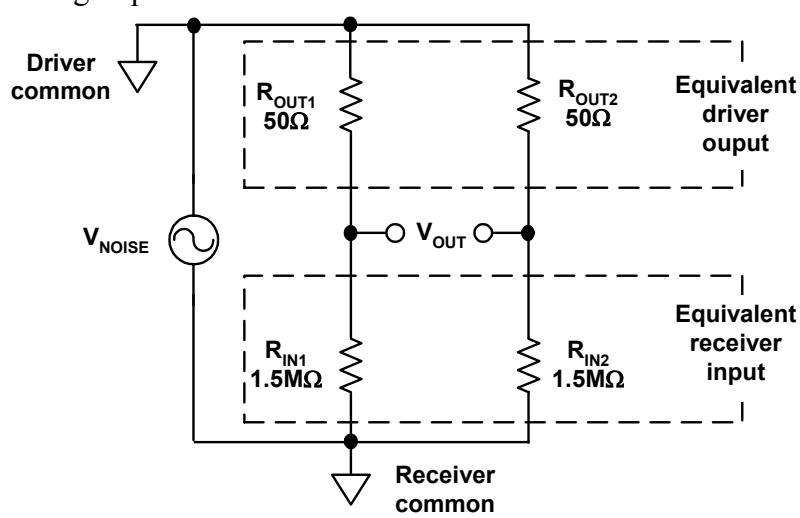

Figure 6-21: *A conceptual driver/receiver diagram of a balanced line audio system with key impedances and CM noise*

From a noise introduction point of view, the balanced transmission system we're talking about can be analyzed as a bridge circuit, as shown in Figure 6-21 above. Here the two source resistances R_{OUT1} and R_{OUT2} correspond to the output resistances of the differential driver voltage sources. Similarly, input resistances R_{IN1} and R_{IN2} correspond to the input resistances of the differential receiver. V_{OUT} represents the output of this bridge, which is due solely to the bridge mismatching and CM noise V_{NOISE}.

Such a bridge as Fig. 6-21, when *maximized* for output sensitivity, will produce a differential output V_{OUT} which is highest as a function of element unbalance when all four resistances are of the same order.

The following general expression illustrates the intrinsic common mode rejection (CMR) of this bridge as a function of the resistance values and their deviation, K_R:

$$CMR(dB) = 20 \bullet \log_{10} [(1+(R_{IN}/R_{OUT}))/K_R] \qquad \text{Eq. 6-12}$$

Some sample calculations with this relationship show that *CMR is a minimum* for a given change in K_R (the total resistor deviation expressed in fractional form) when $R_{IN} \approx R_{OUT}$. A CMR minimum is simply another way of saying that the bridge is most sensitive to the

excitation voltage V_{NOISE} when $R_{IN} \approx R_{OUT}$. To place this in perspective, a conventional instrumentation bridge operates thusly, with all four arms nominally equal. This yields the highest sensitivity to the applied voltage (see Chapter 4).

On the other hand, CMR is maximum and bridge sensitivity is *minimized,* when the upper and lower arm resistances differ widely. This improves substantially as R_{IN} becomes >> R_{OUT}. Or, within an audio system, as the driver R_{OUT} is by design made much less than the receiver R_{IN}. With the example values above, there is a 1/30,000 ratio between the R_{OUT}/R_{IN} upper/lower elements. This factor makes relatively high percentage changes in either the upper (or the lower) arm resistances a somewhat harmless phenomenon. In other words, small R_{OUT} or R_{IN} changes will then have little CMR effect upon the output.

For example, taking the Fig. 6-21 values and assuming a 10% change in R_{OUT}, will produce an output which is about 110dB down from the noise voltage V_{NOISE}. By contrast, if all the bridge values were to be equal, the same 10% deviation would produce an output only 26dB down! Note that there are two control point towards this. One can *lower* R_{OUT}, for a given R_{IN}, and increase CMR. Or, one can achieve the same effect by *increasing* R_{IN}, for a given R_{OUT}. This makes the point that *a high ratio between R_{IN} and R_{OUT}* aids in maintaining high CMR, as is shown by Figure 6-22.

R_{IN}/R_{OUT}	CMR(dB) for K_R = 0.1	CMR(dB) for K_R = 0.01
10	40.8	60.8
100	60.1	80.1
400	**72.1**	92.1
1k	**80**	100
10k	**100**	120
30k	**109.5**	129.5
100k	120	140

Figure 6-22: *High R_{IN}/R_{OUT} minimizes sensitivity to CM noise, bridge imbalance*

In a real transmission system, there will be inevitable noise potentials developed between the respective driver and receiver chassis common points, since they are located separately and are powered with different power sources. The resulting noise voltage can be predicted with the aid of Fig. 6-22. As a minimum, a good system should maintain an R_{IN}/R_{OUT} of at least 1000, with 10k or more a goal. Under such conditions, with a bridge unbalance of 10%, this will still allow a theoretical CMR of 80 to 100dB (see center column, with cited examples shown in boldface).

As noted, dependent upon the bridge impedance-related sensitivity, some fraction of the CM V_{NOISE} appears as V_{OUT}. The basic process of the conversion of the CM noise voltage into a differential voltage is called *mode conversion*. It is important to understand that mode conversion can only be prevented, not fixed after the fact. Once the noise voltage appears as a differential signal, no receiver can distinguish it from a valid signal.

Finally, it is important to realize that what has been discussed thus far addresses the most basic portion of this system and the impact on CMR. The line receiver circuitry itself obviously also has a big influence, as it determines R_{IN}. This is discussed next.

The Simple Line Receiver

The simple line receiver circuit of Figure 6-23 below uses four matched resistors and an op amp for gain. Such bridge-based difference amplifiers are *critically* dependent upon the resistor ratio matching for good performance, an enormously important point. The amplifier can also be critical, but most practical limitations of this topology arises from *un*-balancing of the R_1-R_4 bridge (for either/both AC and DC).

The circuit appears somewhat trivial, as the minimum ingredients are four matched film resistors and a good audio op amp. While this works functionally, how well it works in rejecting noise is another thing. C1 and C2 are optional, and can be used to trim HF CMR. Also optional is the use of an in-the-loop unity-gain buffer (more below).

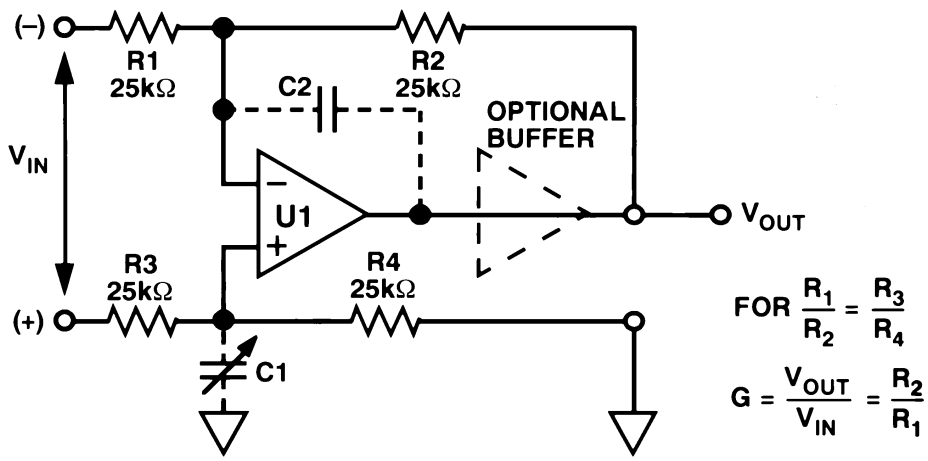

Figure 6-23: *A simple line receiver with optional HF trim and buffered output*

A main purpose of this circuit and all line receivers is to reject CM noise, as discussed above. But even with a high quality op amp for U1, noise rejection is only as good as the resistor matching. More precisely, the resistor *ratios* R_1/R_2 and R_3/R_4 must match extremely well to reject noise (the absolute values are relatively unimportant).

With care, picking four 1% resistors from a same-vendor, same-batch lot is a step which can yield ratio matching of, say, 0.1% total error, and will achieve a common mode rejection (CMR) of 66dB. Four 1% tolerance resistors with just one off by 1% will yield about 46dB CMR. In general, the worst case CMR of a circuit of this type is:

$$\text{CMR(dB)} = 20 \bullet \log_{10} [(1+(R_2/R_1))/4K_R] \qquad \text{Eq. 6-13}$$

where here "K_R" is the *individual resistor tolerance* in fractional form. This form of the expression is most useful for cases using 4 discrete resistors (see Reference 8). More likely, a single component network with a *net matching tolerance* of K_R would be used for this function, in which case the expression then becomes:

$$\text{CMR(dB)} = 20 \bullet \log_{10} [(1+(R_2/R_1))/K_R] \qquad \text{Eq. 6-14}$$

In either case, this assumes a significantly higher *amplifier* CMR, such as ≥100dB).

Eq. 6-13 shows that the worst case CMR due to tolerance build-up for 4 unselected 1% resistors to be much worse, 34dB in fact. Clearly for high and stable noise rejection, circuits such as these need four single-substrate resistors, made/trimmed simultaneously. Networks using thick-film and thin-film technology are available from companies such as Caddock and Vishay-Ohmtek, in ratio matches of 0.01% or better.

Some simulations may bring this point of critical matching home more clearly. Figure 6-24 shows the effect of various DC matching of a differential amplifier such as like Figure 6-23, with a single resistor mismatch in R_1 of 0.1% (top trace), 0.01% (middle trace) and perfect matching (bottom). Also, this display of CM error vs. frequency indicates a reactive imbalance for the perfect DC-balanced (bottom) case. This is due to an intentional capacitive mismatch in the circuit, representing stray capacitance imbalance.

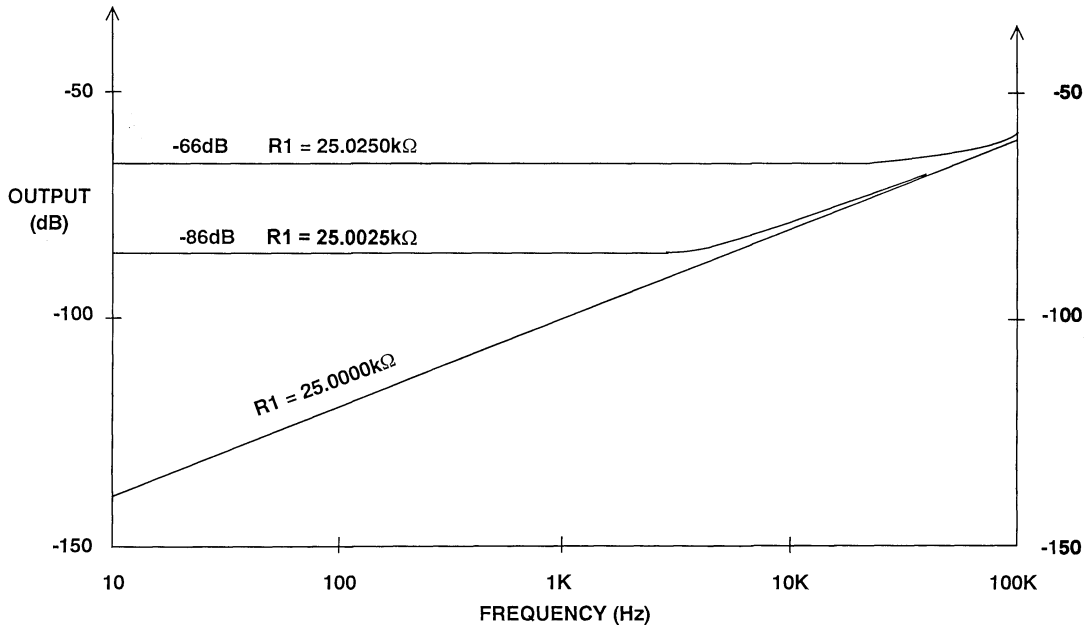

Figure 6-24: *Simple line receiver CM rejection vs. frequency for various R1 trims (simulation)*

The effect of AC matching on this differential amplifier using matched resistances, with C_2 matched to C_1 (10pF) results in essentially flat CM error vs. frequency (not shown). In contrast, a 10% capacitive mismatch results in a CM degradation as low as 10kHz. Clearly then, for wideband audio uses, the bridge ratio needs to be maintained for AC as well as DC, to achieve flat CMR versus frequency. Capacitances from the R_2/R_1 and R_4/R_3 nodes need to be balanced. In practice, this is best achieved with very low and/or balanced parasitic capacitances at C_1-C_2.

It is worthy of note that this circuit also has a highly desirable side property; that is, it *divides down* the input CM voltage. Thus it is inherently protected against overvoltage. In general, practical line receivers *require* some sort of input protection, for safe use in harsh environments, and to allow CM voltages to exceed the supply rails. The receiver gain-set resistors double in performing this function here. The working CM input range of Figure 6-23 is $(1+(R_3/R_4))\times V_{CM(U1)}$, and differential input resistance is R_1+R_3. Circuit gain isn't easily changed, because of the matched R_1-R_4 ratios.

Implementing the Simple Line Receiver Function

To offer a reasonably high impedance to the line, simple receivers such as these typically use input resistances of 25kΩ or more. When working from 50Ω sources, this allows a basic R_{IN}/R_{OUT} ratio of 500 (see previous discussion and Fig. 6-22, again). Given a well matched resistor network and low or balanced parasitic capacitances, suggested amplifiers for U1 are the AD711, AD744 (singles), and the AD712, AD746, OP249, OP275 (duals). With 10kΩ-25kΩ resistances, extremely low voltage noise in the amplifier isn't critical. High slew rate (SR) and output drive allows clean high frequency, high amplitude levels, and 600Ω load capability. If low impedance loads need to be driven, output current of a standard op amp can be boosted with an in-the-loop unity gain buffer, connected between U1 and the load/feedback point. Devices such as the BUF04 or a (follower-connected) AD811 can serve well here (discussed in the later sections).

From an DC and AC trim/balance perspective, the Figure 6-23 topology is most effective with resistors and amplifier made simultaneously in a single monolithic IC. The ADI SSM2141 and SSM2143 are such ICs, characterized as low distortion, high CMR audio line receivers with net gains of unity (SSM2141), and 0.5 (SSM2143). The SSM2141 has resistors as shown in Figure 6-23, while the SSM2143 uses 12kΩ/6kΩ resistors.

In applying circuits of the Figure 6-23 type (or other topologies which resistively load the source), a designer must bear in mind that all *external* resistances added to the four resistances can potentially degrade CMR, unless kept to proportional value increases. To place this in perspective, a 2.5Ω or 0.01% mismatch can easily occur with wiring, and if not balanced out, this mismatch will degrade the CMR of otherwise perfectly matched 25kΩ resistors to 86dB. These circuits are therefore best fed from balanced, low impedance drive sources, preferably 25Ω or less.

Other Issues with the Simple Line Receiver

An application point which becomes relevant for large high performance systems with multiple balanced pair lines is the issue of receiver *load balance*. Ideally, an audio line receiver should exhibit equal AC loading at the two inputs. With the simple line receiver of Figure 6-23 (and all similar circuits), this goal isn't met— i.e., the basic circuit does *not* present balanced loading to the two input lines. It is important to note at this point that this is not a function of the devices used to implement the circuit, it is more a function of the architecture itself.

When Figure 6-23 is driven from complementary sources V_{IN} and $-V_{IN}$, the simple line receiver exhibits a property of unbalanced input currents in the R_1 and R_3 legs, due generally to feedback action. For the like values of Figure 6-23, the current in R_1 is 3 times that in R_3. Thus the inputs load the two input lines differently, as noted.

In large systems with multiple balanced transmission line pairs, the current imbalance in the input lines is potentially serious, as associated fields will not cancel as they do for completely balanced loading. Thus there is potential for crosstalk impairment in such systems using the simple line receiver topology.

On the other hand, while not optimum from a large system and/or line balance viewpoint, the simple line receiver is nevertheless useful in more modest situations. With resistors R_1-R_3 relatively high (20k or more), it is adequate for small-scale or confined systems where I/O lines are relatively short, few in number, they are not cabled, and the source impedances are low. In such uses, devices like the SSM2141 and SSM2143 can serve well as efficient, single IC line receiver solutions.

Balanced Line Receivers

For highest performance uses, it is a key point that audio line receivers exhibit equal loading to the source at both inputs— i.e., they should be truly balanced. At least two topologies meet this criteria and are thus suited for professional use in balanced systems.

Balanced Feedback Differential Line Receiver

David Birt of the BBC has analyzed the simple line receiver topology and presented a modified and balanced form, as shown here in Figure 6-25 (see Reference 7). Here U1 uses an 4 resistor network identical to that of Figure 6-23, while a second feedback path from unity gain inverter U2 drives the previously grounded R_4 reference terminal. This has two basic effects overall; the input currents in the R_1-R_3 input legs become equal in magnitude, or balanced, and the gain of the stage is halved.

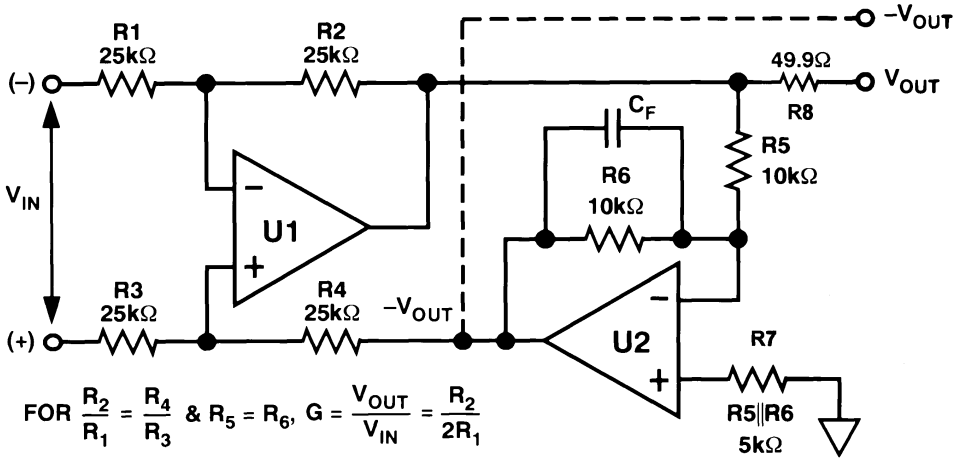

Figure 6-25: *Balanced line receiver using push-pull feedback*

Compared to Figure 6-23, and for like resistor ratios, the Figure 6-25 gain from V_{IN} to V_{OUT} is ½, or a gain of -6dB (0.5) as shown. However it also offers an optional complementary output from U2, $-V_{OUT}$. Like Figure 6-23, the gain of this circuit is not easily changed, as it also involves precise resistor ratios.

Because of the two feedback paths, this circuit holds the inputs of U1 at a null for differential input signals. However CM signals are still seen by U1, and the CM range of the circuit is $(1+(R_3/R_4))\times V_{CM(U1)}$. Differential input resistance is R_1+R_3. As can be noted from the figure, the circuit can be broken into a simple line receiver (left), plus an inverter (right). Existing line receivers like Figure 6-23 can be converted to a balanced topology by adding inverter U2. A performance example of this is discussed below.

Alternate Balanced Line Receivers

Other instrumentation amplifier types can achieve the goal of fully balanced input loading, but may not be desirable for other reasons. For example, there are standard in-amp circuits not shown here which use either 2 or 3 amplifiers and have properties of high input impedance, due to the use of non-inverting inputs (see References 8-11). The drawbacks of these topologies as audio line receivers lie in limited gain and CM range. Also, importantly, they require 4 resistors beyond those for gain, just for input overload protection. Since these resistors also influence gain and CMR, they must also be precision ratio matched types. As a net result, workable audio line receivers using these in-amps aren't really highly practical (8 or more matched resistors, plus 2 or 3 op amps).

An "All Inverting" Balanced Line Receiver

Figure 6-26 below is an elegantly attractive topology that seems well suited to audio line receiver use. Using all amplifiers as inverting stages, this circuit can be configured for very high CM voltage range and high input resistance. With the resistor ratios matched as shown, the CMR of this circuit can be better than the others for a given resistor match, since both amplifiers see no CM voltage. The CM range of this circuit is set as $(R_1/R_2)\times V_{OUT(MAX)U1}$. The differential input resistance is R_1+R_3.

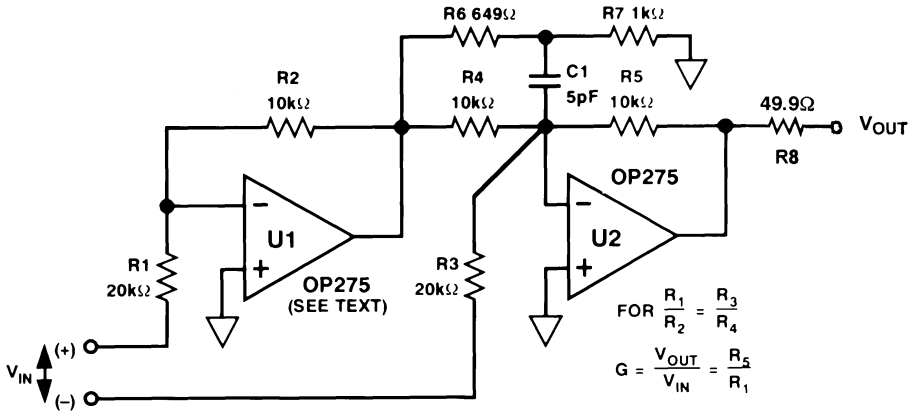

***Figure 6-26:** "All Inverting" balanced line receiver*

The circuit has the unusual and desirable property of single resistor gain adjustment via R_5, *without* any CMR interaction. Gain can also range from below to above unity, making it flexible in that regard. As shown it is driven with a balanced signal, but note that it can also be driven with single-ended sources at either the (+) or (–) terminal, with no gain interaction from the opposite input port, due to the use of inverting amplifiers. Multiple inputs can be summed, with additional ratio matched input resistor pairs (not shown). In this example gain is set at 0.5, consistent with general line receiver system requirements.

This circuit is also well known in basic form (see References 8-11). However, note that in this configuration, optional phase lead compensation is used to enhance high frequency CMR. A small capacitor shunting R_4 with a value chosen to compensate for the gain-bandwidth of U1 compensates for the lag through U1, and maximizes phase matching of the ± CM signals at U2. However, for op amps with gain bandwidths above a few MHz and practical resistor values, this can result in difficult-to-control small capacitor values.

The R_6-R_7-C_1 tee network reduces the effective value of C_1, by dividing the applied voltage. A nominal division ratio can be approximated by this expression:

$$K_C = 1/(2\pi\ BW_{(U1)}\ R_4C_1) \qquad \text{Eq. 6-15}$$

where K_C is the division ratio of R_6-R_7. For this example, with BW(U1) about 5MHz (the closed loop bandwidth of U1), K_C is about 0.6, making C_C effectively about 3pF. Circuit parasitics, loading effects and part variations make this inexact; however, once nominal compensation for a given layout and devices is achieved, a 30dB CMR improvement in 10kHz CMR is possible (vis-a-vis no phase compensation). This trim network isn't necessary to the circuit's basic function, but is nevertheless useful for audio applications.

Performance of balanced line receivers

The balanced line receiver configurations of Figure 6-25 and Figure 6-26 were tested for CM performance, with common conditions of G=0.5, Vs=±18V, and a 10Vrms input sweep, 20Hz-50kHz, filter bandwidth of 80kHz. The Figure 6-25 topology was implemented with an SSM2141for U1, with U2 an OP275 inverter, with C_F=68pF. Figure 6-26 was implemented with an OP275 and a resistor network matched to 0.005%, with the C_1 network trimmed as shown. These results are shown in Figure 6-27 below.

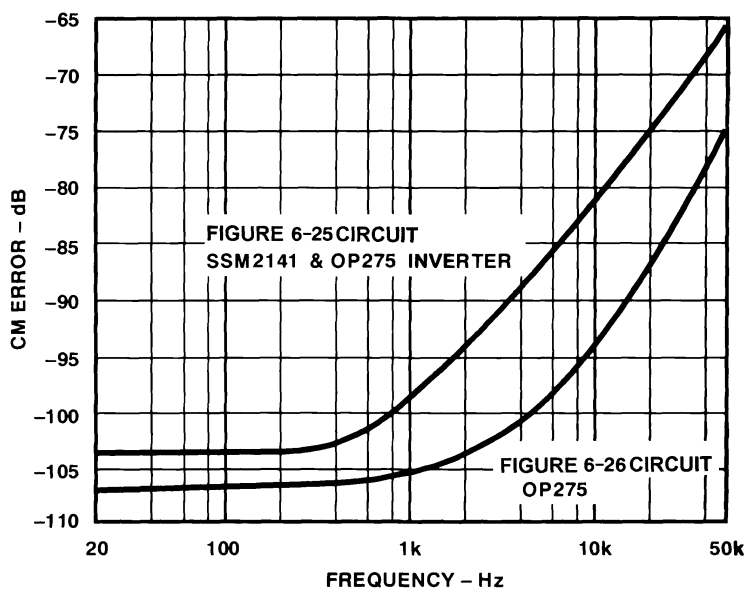

Figure 6-27: *Balanced line receivers CM error vs. frequency*

Both circuits show excellent results, with ≤1kHz CM errors of –100dB or lower. The Figure 6-26 topology offers better results at the higher frequencies, perhaps due to the trimming technique used (not applicable to the Figure 6-25 circuit). In the worst case, the CM errors are no poorer than –80dB at 10kHz, still very good for an untrimmed circuit.

THD+N data was taken on both circuits and, while dominated by the noise floor at many levels, there are some differences worth noting between the two. Figure 6-28 shows THD+N performance of the Figure 6-25 SSM2141/OP275 circuit for loading conditions of 100kΩ, successive input sweeps of 1, 2, 5 and 10Vrms, and ±18V supplies. The lower level sweeps are noise dominated, while the 5 and 10V sweeps show some distortion rise at high frequencies. Distortion of this circuit also rises with loading of 600Ω (not shown).

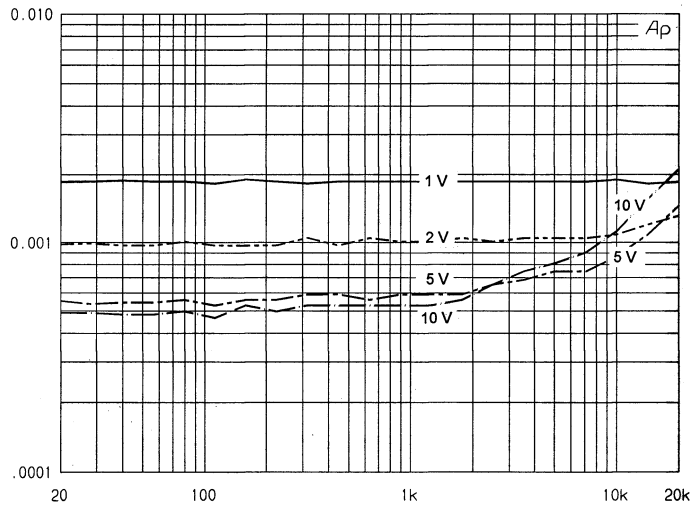

Figure 6-28: *Balanced line receiver of Fig. 6-25, THD+N vs. frequency*

The performance of the Figure 6-26 circuit for similar input drive and power supply conditions is shown in Figure 6-29, and for conditions of 600Ω loading. These data indicate less loading and frequency dependence, due primarily to the OP275's higher slew rate, and greater available output drive into 600Ω loads.

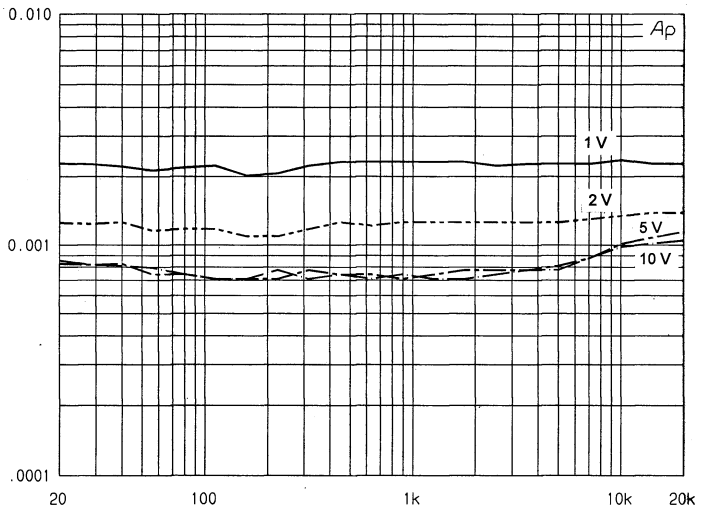

Figure 6-29: *Balanced line receiver of Fig. 6-26, THD+N vs. frequency*

In the all inverting circuit of Fig. 6-26, THD+N performance is much more limited by noise than actual distortion, over frequency. The circuit is a very flexible one, and it can be set up for a variety of other op amps and input resistances, as well as the already mentioned single-resistor gain change operation.

The line receivers covered just above offer good performance. However, with input resistances on the order of 25kΩ, they still can be subject to CM errors due to driver impedance mismatches. This is not an issue that can be dealt with cleanly, as the designer of a line receiver circuit doesn't necessarily have any pre-knowledge of the worst case driver impedance characteristics. So, to guarantee high CMR performance even in the instance of substantial driver impedance and/or mismatching, there are two possible solutions. One is to make the line receiver circuit input impedance as high as practical, which then allows good CM performance with impedance mismatches on the order of 10% (Fig. 6-22, again). Alternately, a line receiver can utilize a line transformer, which offers high CM rejection and galvanic isolation. Both approaches are discussed next.

A Buffered Input Balanced Line Receiver

The circuit of Figure 6-30 below represents an example of a classic 3 op amp instrumentation amplifier (in-amp) topology, dressed up and optimized for use as an audio line receiver (see Reference 16). The use of FET input stage buffers in amplifiers U1A and U1B allows megohm-level bias resistance to be used for R_{IN1} and R_{IN2}, which greatly de-sensitizes this receiver against loading of the source and CM errors. Optional resistor R_{IN3} terminates the line differentially. Protection resistors R_{P1} and R_{P2} allow over voltages at the two inputs, by limiting amplifier fault currents to safe levels. The input stage can use either dual or single amplifiers, with performance options described below.

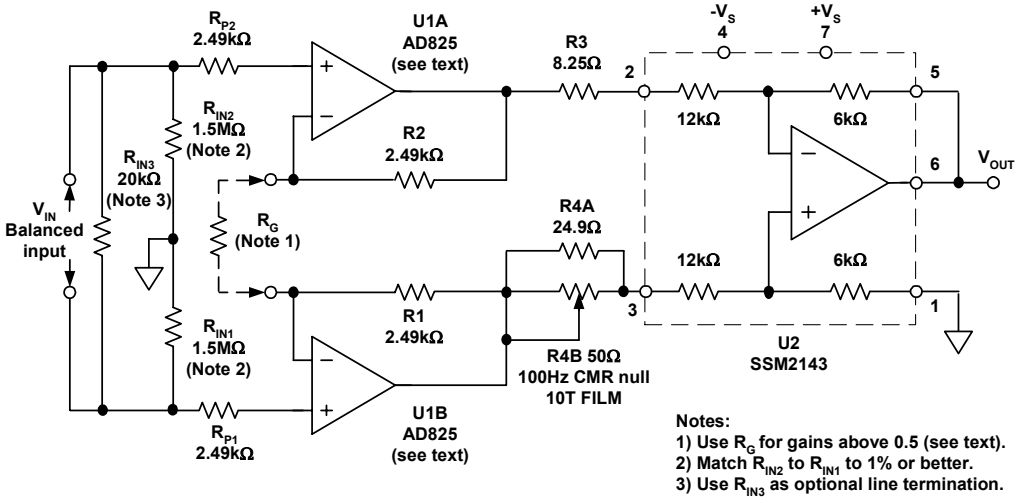

Figure 6-30: *A buffered input balanced line receiver*

Within the circuit, the *differential* gain of stage U1A, U1B (or G_1) is set by R_1-R_2-R_G, as:

$$G1 = 1 + [(2R_1)/R_G] \qquad \text{Eq. 6-16}$$

where $R_1 = R_2$, and R_G is used for high gains. Without R_G, the first stage gain is unity.

While the differential gain of U1 is as noted, the CM gain is unity, since the connection simply passes CM signals to the output. Thus both differential and CM forms of signal are presented to the inputs of stage U2. Note however, because differential and CM signals are scaled differently by U1, there can be a net potential gain in CMR. Practically,

it means that this overall configuration can achieve useful CMR figures higher than the intrinsic CMR of U2, whatever that figure may be.

The U2 stage, a pre-trimmed 4 resistor in amp, suppresses the CM component from U1A/U1B, while amplifying differential signals by a factor of 1/2. For an overall net gain G higher than 0.5 from this line receiver, the value of R_G is:

$$R_G = R_1/(G - 0.5) \qquad \text{Eq. 6-17}$$

For net overall gains of 1, 2 and 4 times, the required gain resistance R_G works out to be 4.99kΩ, 1.69kΩ, and 715Ω, respectively (using closest standard values).

Seasoned analog designers may wonder what's so new about this circuit, as it has been around for more than 30 years in solid state form (Reference 9, again). While true, some refinements here lend it worthwhile audio utility. First, as mentioned, FET input op amps for the U1 stages allow very low bias current, and load the inputs infinitesimally. Source loading will be essentially determined by the 1% resistances used for R_{IN1} and R_{IN2}.

While FET amplifiers are most useful here, a serious selection caveat is in order. The types used for U1A and U1B must *not* be general purpose types prone to sign-reversal, which could possibly come about with combined large signal and CM inputs (see Chapter 7 overvoltage discussions). All of the types tested for Fig. 6-30 have FET input stages, with CM ranges of at least ±10V on ±15V supplies. Note that any op amp can mis-behave if severely over-driven at the input (i.e., beyond the rails). Of the three types tested, the AD825 is the most robust for overload, while the AD845 is less robust, but offers best CM performance. Wideband operation is a virtue, allowing better high frequency performance before degradation sets in. Finally, an FET input structure is less susceptible to RF rectification problems, which can be critically important in an audio line receiver used within an RF environment (see Chapter 7 RFI discussions).

Selection of the U2 device also has a great bearing on CMR. Although there are a number of unity gain 4 resistor in-amps available for the U2 function, the choice here is for less than unity gain (in this case 0.5). To extract the highest possible CMR performance, the U2 network balance is externally trimmed by the R_3-R_4 resistances. R_{4B} can be either the film trimmer noted, or a selected fixed resistor. The values shown allow a trim range of more than ±0.05%, sufficient to trim any SSM2143 part to a null. In the performance data following, the SSM2143 used for U2 reflected such a trim, with a basic low frequency CMR of ~110dB for the stage.

Buffered Input Balanced Line Receiver Performance

To demonstrate these concepts, a number of measurements were made on the Fig. 6-30 circuit, using a number of single and dual IC op amps for the U1A and B positions, and an SSM2143 for U2. Although this basic 3 amplifier in amp structure can in principle offer potential gains in CM performance over the intrinsic CMR of U2, this phenomenon is less pronounced at relatively low overall gains as true here (i.e., gains of 1, 2 or 4 times). And, it is also dependent upon the specific U1 and U2 performance. Thus the CMR of both the U1 and U2 stage devices can effect the measured CM performance.

The test setup used employs an Audio Precision System 1 in a modified crosstalk test mode, where channel A drives the test circuit, which in turn has its output monitored by channel B. This allows a swept narrow band tracking analysis, over a dynamic range of 130dB or more at low frequencies, and a frequency range of 20 Hz to 200 kHz. In the results following, the CM error curves displayed are referenced to a 0dB calibrated output level from U2 of 1Vrms, with the circuit set for a gain of 0.5 (i.e., R_G open). The drive to the circuit was 2Vrms, and power supplies were ±13V.

Figure 6-31 below shows CM error results for paired (2) single samples of the AD825, the AD845, and the dual AD823. All devices have CM errors at or below a –90dB level below 3kHz, with low frequency errors of the AD845s well below –100 dB. The CM corner for all devices is enough to achieve –80dB or better 20kHz CM error.

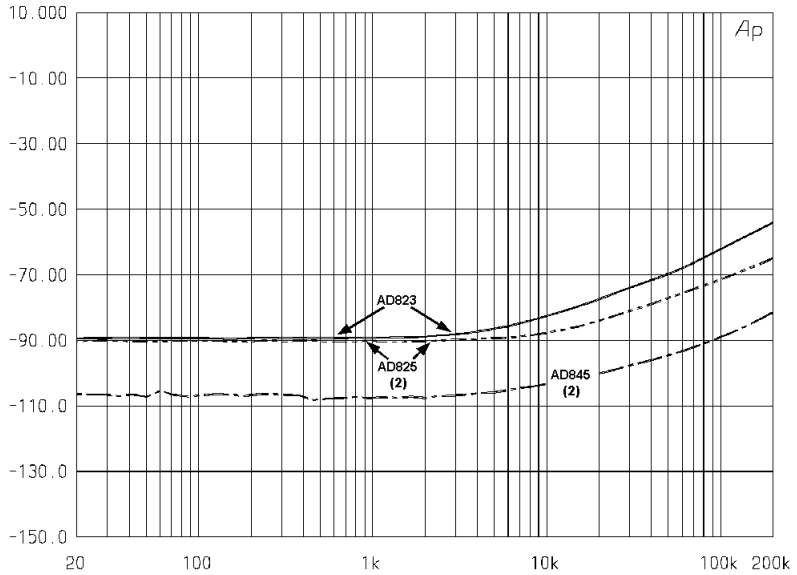

Figure 6-31: *CM error (dB) vs. frequency (Hz), for various U1A and U1B devices within the circuit of Fig. 6-30, gain = 0.5.*

While these results show generally what the various devices can do in this circuit, the data should not be taken as an absolute indication of future results. Sample-sample variations of a few dB will exist, and this should be taken into account. One point worth noting however is that devices with intrinsically high CMR input stages perform best. An example of this is the AD845, which uses cascode inputs for high CMR, and shows a CMR of 100dB or more to above 20kHz. It does however have less input dynamic range than the AD823 and AD825, because of the bias headroom required for the cascode stage

A criticism directed towards active line receiver circuits such as the SSM2141 and SSM2143 has been their high sensitivity to source resistance mismatches. However, as the discussions above have shown, the problem comes from the relative source/load impedances, and the degree by which these are mis-matched. One can specify a very well-controlled, high CMR receiver such as for example the SSM2141 or SSM2143, and have the as-used CMR degrade simply due to uncontrolled source impedance(s).

In the relatively uncontrolled environment of real world audio system interfacing, source resistance mismatches of a few ohms can be typical. This mismatch level is sufficient to ruin the CMR performance of a simple line receiver, if the receiver uses resistances on the order of 20k, and is fed from a source resistance of 50Ω or more. This can be readily illustrated by a sample calculation using the bridge circuit CMR relationship of Eq. 6-12, and plugging in R_{OUT} resistances of 50 and 55Ω (a 10% mis-match), using an R_{IN} resistance of 20kΩ. This degree of mis-match for 20kΩ loading conditions destroys CMR, as it degrades to 72dB with a 50Ω source mis-matched 10% (see Fig. 6-22, again).

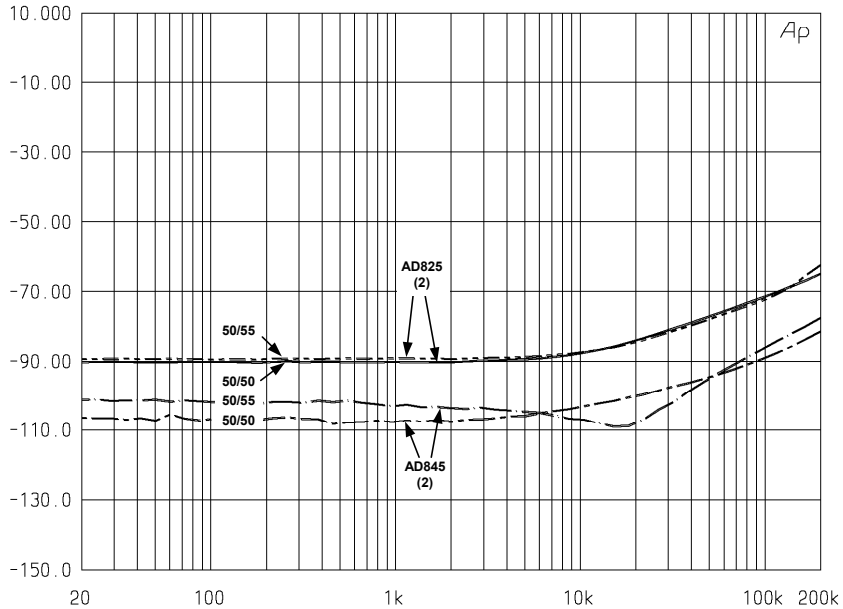

Figure 6-32: *CM error (dB) vs. frequency (Hz), for AD825 and AD845 pairs, nominally 50Ω source impedances matched/mis-matched 10%*

The buffered topology of Fig. 6-30 directly addresses this issue, as shown in the dual matched/mis-matched source resistance CM plots of Figure 6-32 above. In these tests, the Fig. 6-30 circuit is again exercised with the AD825 and AD845 op amp paired samples at an overall gain of 0.5, and R_{IN3} = 20kΩ. The circuit is fed from a source resistance of 50Ω, and is operated under both matched and mis-matched source resistance conditions. This allows the degradation with mis-matching to be clearly shown as separation between the 50/50 (matched) and 50/55 (mis-matched) paired curves for each device type.

In the AD825 pair curves, the CM degradation is less than 1dB, even for the test condition of the relatively high 10% source resistance mis-match. The AD845 device has better overall CMR than the AD825, which shows up as low frequency errors of better than –100dB with the matched impedances. While mis-matching degrades CMR by a few dB, it is still –100dB or below as high as 20kHz. The AD845 can be used for U1A and U1B in the Fig. 6-30 circuit for highest wideband CMR (do however be careful to note the device dynamic range limits). Considering its superior overload behavior, the AD825 is the best choice, and is thus recommended.

These tests make clear that higher R_{IN} aids in de-sensitizing system CMR degradation against source mismatching. The designer has the option of using even higher input resistance for R_{IN1} and R_{IN2}, to further reduce the source sensitivity.

Transformer-Input Line Receiver

The classic solution to the CM isolation of audio signals is the *line input* transformer (see References 4,5, again). This device, usually a 1:1 ratio unit, offers galvanic isolation and very high CM voltage breakdown ratings. It is a preferred (or only) solution where true galvanic isolation is a necessity. Transformers are also useful for high and consistent low to middle audio frequency CM performance, both from unit-unit, and also when high immunity to varying differential source resistance is sought. These features do come at some cost however. Quality transformers are pricey, at about 10-20 times a single IC's cost. They also occupy a relatively large package size vis-à-vis a solid state equivalent.

All of the various factors above are the designer's ultimate decision points, dependent upon the exact system requirements. When optimized for high performance, it is not likely that either a completely solid-state or a completely transformer based line receiver solution will be considered either simple, or low in cost. Performance comes with a price.

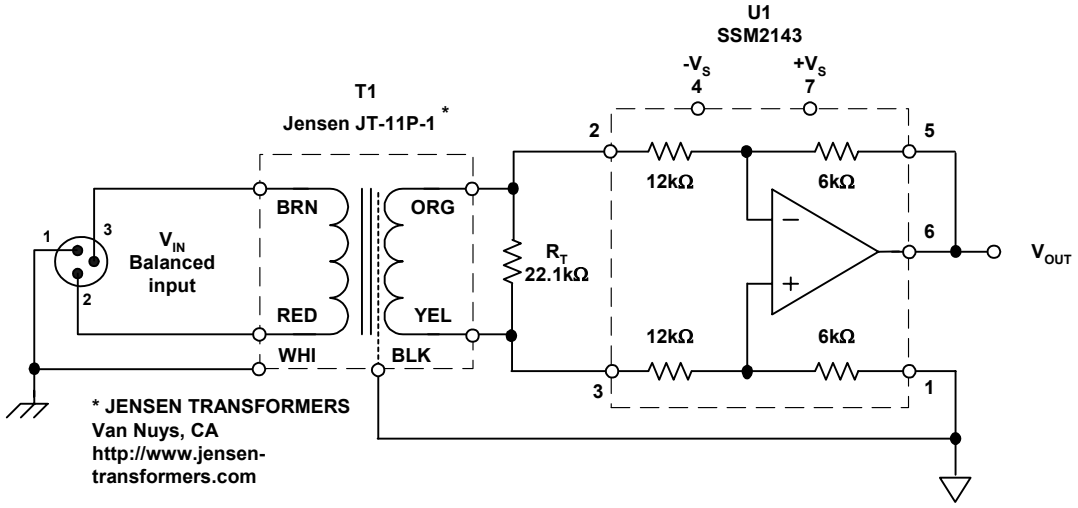

Figure 6-33: *A transformer-input line receiver circuit*

Interestingly, when a near-ultimate in low frequency CM rejection is required, or completely tweak-free operation is sought, a hybrid line receiver solution may be a good choice. An example of a line transformer buffered by a simple line receiver is shown in Figure 6-33 above. This circuit combines good features of the simple line receiver and the transformer, and offers outstanding performance with attractive simplicity.

The circuit has only three components; T1, the secondary termination resistor, and U1. It can be noted that this combination can operate the transformer in either a balanced mode (just as shown) or in an alternate single-ended mode (with U1-2 grounded). The choice of which mode is used does make a big CMR performance difference, as will be apparent.

The transformer secondary is terminated in a net 10kΩ resistance, which here is comprised of R_T and the 12kΩ input resistances of U1. If other forms of termination are used, or an alternate U1 part, R_T should be adjusted accordingly (see Reference 17). The net gain of the circuit is product of the loaded transformer primary/secondary voltage ratio, and the voltage gain of U1 (0.5). Inasmuch as T1 shows a voltage loss for such loaded conditions, the overall gain of the circuit is approximately 0.35 (or –9dB). If more

gain is desired, an alternate SSM2143 operational mode is possible. The 12kΩ/6kΩ input output resistors can be reversed, which will then allow it to operate at a gain of 2.

The CMR test results for the circuit of Fig. 6-33 are shown in Figure 6.34. Conditions for this test setup are similar to those of the buffered balanced line receiver test, described above. They are referenced to a 1V operating level at the output of U1.

Several important points should be apparent from these results. In the single-ended mode (upper curve), the basic data sheet performance of the JT-11P-1 transformer can be seen. This includes an approximate 60Hz CM error of –107dB. While this simply buffered operating mode does offers excellent low frequency CMR, it can also be noted that this also degrades with rising frequency. At 20kHz the single-ended mode error is just slightly more than –50dB— good, but not superlative. Any of the ICs tested for the Fig. 6-30 circuit better this performance, by about 30dB or more.

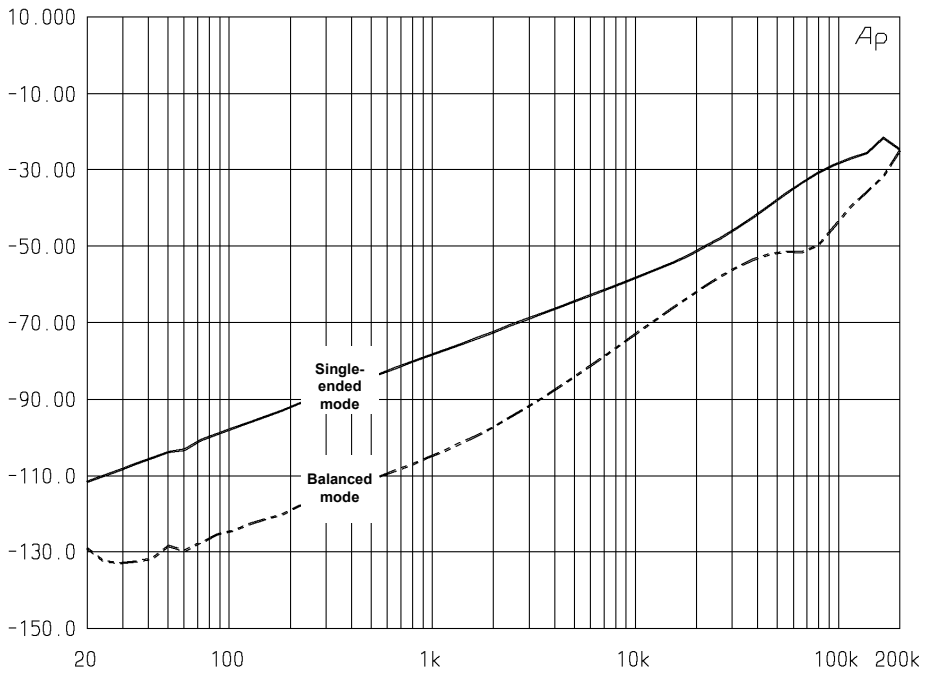

Figure 6-34: *CMR errors for Fig. 6-33 transformer-input line receiver circuit, operating in single-ended and balanced modes*

On the other hand, by simply letting the SSM2143 operate in a balanced mode, the lower curve CMR performance results. This is clearly a major improvement vis-à-vis the single-ended case, with the low frequency CM error reduced to –130 dB or better, approaching the noise floor of the instrumentation. The errors aren't quite as low at the higher frequencies, with a 20kHz CMR of ~60dB.

A point worth noting is the transformer-based line receiver cannot really compete with the buffered balanced receiver of Fig. 6-30 for high frequency CMR. This is because the transformer inter-winding capacitance acts as a high pass filter for CM noise. This has the effect of passing CM noise to the output at the higher frequencies. The degree of severity for this phenomenon will of course vary with the design of the specific transformer.

Nevertheless, it is readily apparent from the performance data that the preferred method of transformer operation is to operate it in a balanced secondary mode (i.e., as shown in Fig. 6-33), which does mitigate the CMR loss with frequency somewhat.

A Summary of Line Receivers

Both active and passive solutions for minimizing balanced transmission system CM noise have been explored, each with their own set of characteristics. Readers should take these data for the general trends they convey, not any absolute performance levels.

To summarize, the buffered balanced line receiver of Fig. 6-30 offers excellent broadband CMR with low differential source resistance sensitivity, and can be user customized in a variety of ways, including gain, CM input impedance, etc. The solid state line receiver approach here has virtues of the best high frequency CMR in absolute terms, as well as the better CMR vs. frequency flatness. While the example circuit shown works well, optimization for a production role may need some enhancement for worst case minimum CMR. This can be done via careful trim or selection of the U2 circuit, and/or selection of an optimum pair of singles for U1A and U1B. Input dynamic range of the circuit can be optimized by selection of the U1A-U1B pair types, and the supply voltages used. All types tested can be operated at supplies of up to ±18V (maximum), or as low as ±13V. The typically used ±15V supplies will provide both excellent performance and high input dynamic range.

The transformer-input approach to a line receiver offers good to superlative low frequency CMR, combined with "no tweak" operation. When the transformer used is combined with an in-amp for balanced mode secondary buffering, as in Fig. 6-33, further CMR reduction is possible over a range of low to middle frequencies. On the downside, there are negatives of cost, size, and eventual CMR degradation with frequency.

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Audio Buffers and Line Drivers

Audio line drivers and buffer amplifiers can take on a wide variety of forms. These include both single-ended and differential output drivers, as well as transformer isolated drivers. Within these general formats there are also many different performance options, and many of these are covered in this section. Note that a later section of this chapter also discusses buffers for a general context, as for video and instrumentation applications.

Many op amps useful as video drivers and/or buffers do well for audio drivers/buffers, because of the high current output stages necessary for good linearity over video bandwidths (see References 1-4). Some examples of video IC amplifiers that are audio-useful are the AD810, AD811 and AD812, AD815, AD817 and AD826, AD818, AD829, AD845, and AD847. Other types notable for either high or unusually linear output drives or other performance features useful towards audio are the AD797 and the OP275.

Some High Current Buffer Basics

As a preliminary to detailed application discussions, some basic circuit principles germane to high current buffers and drivers should be treated first. With output currents up to 100mA or more, "housekeeping" details of bypassing, grounding and wiring also become important, and must be considered to achieve high performance. These are briefly discussed here in the context of high current audio buffers, using the unity gain buffer circuit of Figure 6-35 below, as a point of departure.

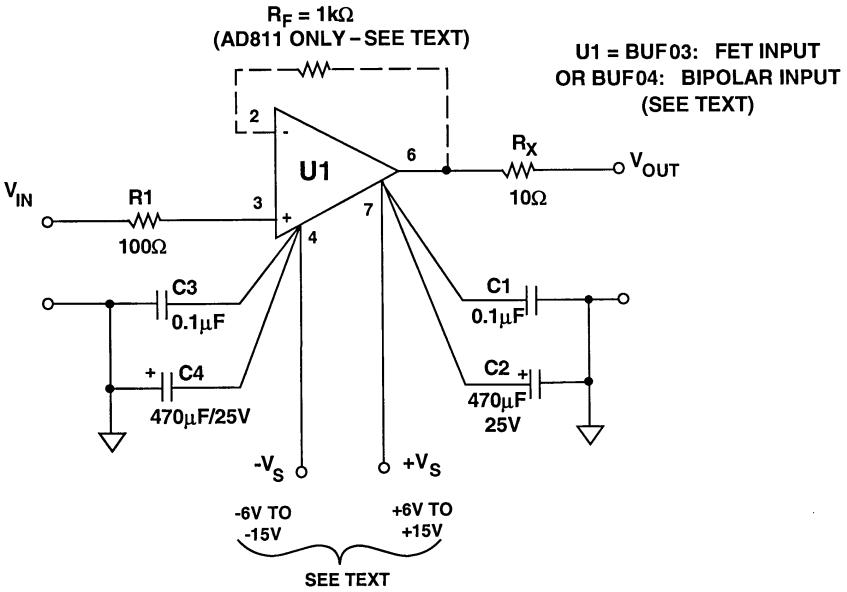


Figure 6-35: *A unity-gain, standalone buffer circuit*

First, despite which IC is used for U1, close attention should be given to making buffer stages free from parasitic effects, at both input, output, and supplies. Physical construction of buffer-drivers and other high current stages should be in accordance with high speed rules. A heavy copper ground plane is preferred, and circuit layout should be compact, with low capacitance high-Z nodes. Signal and ground runs should be laid out with signal coupling and load current flow in mind (see References 5-7 and Chapter 7).

In addition, the power supplies should be well bypassed close to the high current supply pins. In Figure 6-35 this is indicated by the Kelvin connections of C_1-C_4 to the U1 ±Vs pins. This should be used as standard practice for all high current stages, and is intended as a given for all the driver applications of this section.

As a minimum, local low inductance/low ESR RF bypass caps should used within 0.25" of the device supply pins, shown as C_1 and C_3. These are preferably 0.1µF stacked polyester film, or other low inductance capacitor type, preferably films. In addition, for high peak current loads, the high frequency bypasses are paralleled by local, short lead/large value, low ESR electrolytics such as C_2 and C_4, in a range of 470µF/25V and up. Note that capacitor ESR reduces in inverse proportion to electrical size and voltage rating, so larger size and/or voltage units help. These capacitors carry transient output currents, and should be aluminum electrolytic types rated for high frequency use, that is switching supply types. Such types tend to have a broad range of lowest high frequency minimum impedance and are thus less likely to cause power line resonance than are tantalum units.

DC power management and dissipation can also be important with buffer ICs. For example, the BUF03 and the AD811 ICs can dissipate fairly large power levels even with light loading, for supplies above ±12V. This is because the quiescent current of these devices is 15-18mA, relatively independent of operating voltage.

As a conservative general rule of reliability, any IC with a power dissipation above 300mW should not be used without a heat sink. For buffer or driver circuits using this power or more, use the lowest thermal resistance package possible, and add the appropriate heatsink (Thermalloy 2227 for the BUF03 or other TO-99 ICs, or Aavid #5801 for the BUF04, AD811 or other high dissipation 8 pin DIP ICs).

Output resistor R_X in this circuit should be 10 ohms or more, to isolate the buffer from capacitive loading (more on this, elsewhere in this chapter). For an extra safety margin against possible de-stabilization due to capacitive loads, make this resistor as high as feasible from a voltage loss point of view.

The input resistor R_1 is a "bullet-proof" safety item, and can serve two purposes. One is as a parasitic suppression device, which may be required for stability with some amplifiers (not absolutely essential for those here). A subtler feature of this resistance comes about when the buffer is operated within a feedback loop, and is driven from an op amp output. Internally, many buffer ICs have clamping diodes from input to output, and under overload conditions, these diodes act to clamp overdrive. With the inclusion of R_1, this prevents excess current drive into the buffer IC under this clamping condition.

Because of this stage's very high bandwidth, low phase shift, and low output impedance, fast buffers such as this can be used both "stand alone" just as shown, or as a more conventional "in loop" buffer as well, to minimize loading of a weaker, slower amplifier. The improvement raises the linear output up to ±100mA with the AD811 or the BUF04, while maximizing linearity, preserving gain, and lowering distortion.

Buffer THD+N Performance

Operating in a pure stand-alone mode, THD+N tests on several unity gain buffers are shown in Figure 6-36 below. These tests were for common conditions of 10Vrms output into a 600Ω load, operating from ±18V power supplies.

The BUF03, an open loop design, shows a distortion for these conditions of about 0.15%. The BUF04, a closed loop current feedback design buffer, shows a very low distortion of about 0.004%. The AD811 is also a current feedback amplifier, but it is externally configured as a unity gain follower, with R_F = 1kΩ. Note that *all current feedback ICs will require such a resistor*, but the value required may vary part to part. The AD811 shows an intermediate distortion level, under 0.01%.

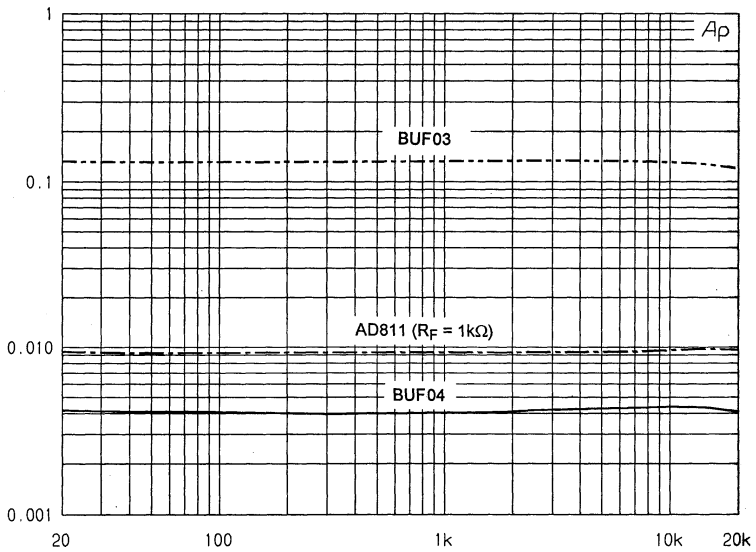


Figure 6-36: *THD+N (%) vs. frequency (Hz) for various buffer ICs, for $V_{OUT} = V_{IN}$ = 10Vrms, R_{LOAD} = 600Ω, V_S ±18V*

As a choice among these types, both the BUF04 and AD811 are capable of more than ±100mA of output, with input currents on the order of 1-2µA. The BUF03 has a lower output current (±70mA), but the advantage of a much lower input current (~200pA).

Dual Amplifier Buffers

In addition to standard operation of the various single op amps as unity-gain buffers, certain high output current *dual* op amp ICs also work exceedingly well as buffers. Using a dual IC to buffer a signal has the advantage of doubling the output drive while using basically the same package size, an obvious benefit. Two design steps allow this to be implemented successfully, The first is the selection of a basically linear single device that also is available as a dual. The second is to devise a method of combining the outputs of the two op amps in a linear fashion, without any side effects.

Among the suitable candidates for this task are the dual version of the AD817, the AD826, as well as the AD811 dual, the AD812. Figure 6-37 below shows a hookup that is useful towards increasing buffer output current to more than 100mA.

Ignoring Q1-Q2 for the moment, the circuit can be seen as a pair of unity-gain followers paralleled at the output, through small value resistors R_3 and R_4. These resistors provide balanced drive from the U1A and B sections, linearly combining the signals. With the use of the voltage feedback AD826 op amp, the circuit is quite simple, since R_1 and R_2 reduce to zero. If the AD812 current feedback device is used, these two resistors should be 1kΩ (shown dotted). The Q1-Q2 bi-directional clamp circuit is optional, and when used can provide protection against input overdrive, and/or adjustable current limiting via R_5.

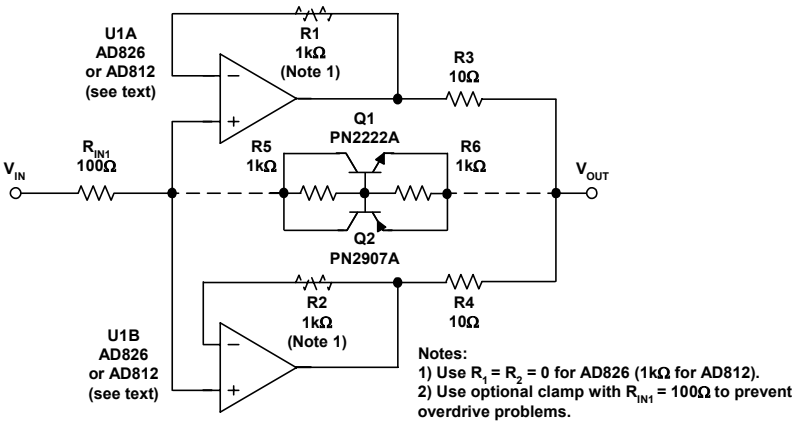


Figure 6-37: *Dual op amp buffer circuit raises output current to more than 100mA with low distortion*

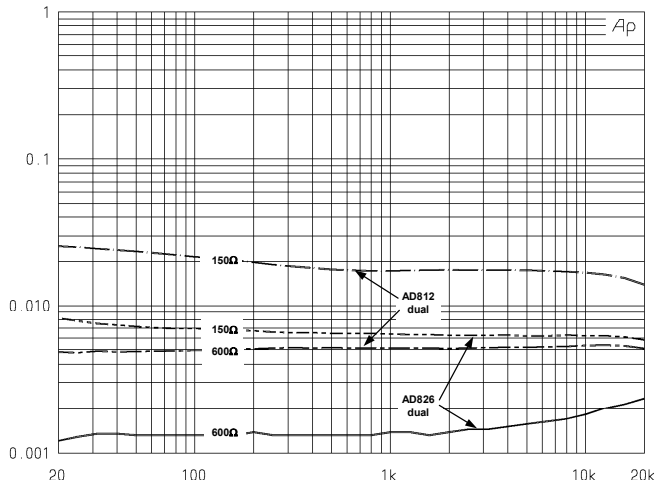


Figure 6-38: *THD+N (%) vs. frequency (Hz) for AD826 and AD812 dual buffer ICs, for $V_{OUT} = V_{IN} = 10Vrms$, $R_{LOAD} = 150/600\Omega$, $V_S \pm 18V$*

This circuit offers excellent performance, as shown in Figure 6-38 above. These THD+N plots show performance with loads of both 600 and 150Ω, at an output level of 10Vrms, from ±18V supplies (without clamping active). The AD826 offers the lowest distortion, due to the voltage feedback architecture, with less than 0.01% THD+N, even when driving 150Ω, which is an approximate 100mA combined peak output.

Capacitive Loading Issues

Audio driver output stages are typically operated as voltage sources feeding high impedance loads. When connected via long transmission lines between stages, the result is that the driver sees an unterminated line, which can appear highly capacitive. Audio driver stability with capacitive loading can be a difficult design issue, but for good reason— it isn't always an easy thing to achieve. If easy, it may be at the expense of performance or circuit complexity. Fortunately, some standard techniques exist for stabilizing op amp drivers with capacitive loads, and these can be implemented in a reasonably direct fashion. These are covered in detail within the next section of this chapter. The discussions immediately following emphasize driver linearity.

Op Amp Device/Topology Related Distortions

Single-ended audio drivers can be built using a linear, non-inverting gain stage as a starting point. Indeed such a circuit, given appropriate op amp choice and gain scaling, can well serve as a basic audio driver. Topologically, a non-inverting gain stage is preferable, since it loads the signal source less, and, it also adds no sign inversion. However, this configuration is subject to certain distortions, which should be understood in order to extract the best performance in an application. Distortion performance for a number of audio op amps in such a line driver circuit are now discussed, in this context.

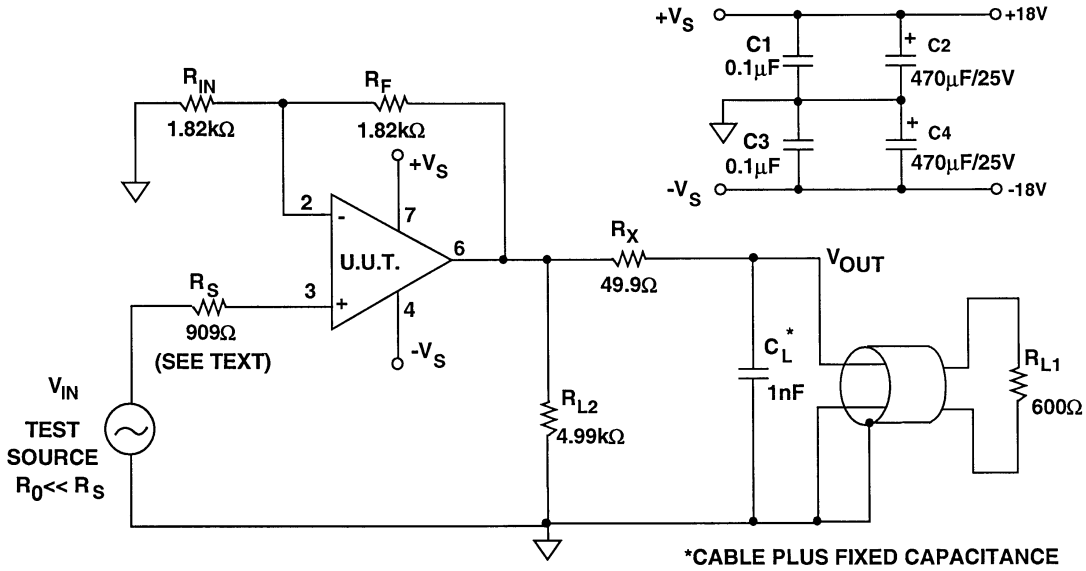


Figure 6-39: *Test circuit for audio line driver amplifiers*

The circuit of Figure 6-39 above is a test configuration that loads the U.U.T. op amp with 500Ω and 1nF. This is a reasonably stressful test load, which can differentiate the distortion of various devices with outputs of 7Vrms or more. A gain of 2 is used, which subjects the U.U.T to a relatively high input CM voltage, thus this configuration is sensitive to CM distortion in the amplifier. For the following tests of this section (except as noted to the contrary), V_S=±18V, and the analyzer bandwidth is 10Hz-80kHz.

Given amplifiers with sufficient load drive and output stage linearity in this circuit, there can still be non-linear effects due to the CM voltage. This distortion is due to the non-

linear C-V characteristic seen at the two amplifier inputs, and can be minimized by matching the two impedances seen at the respective (+) and (–) inputs (see Reference 8). When this done, the differential component of the error is minimized, and the distortion seen in V_{OUT} falls to a minimum.

This general point is illustrated by Figure 6-40, a family of plots for an OP275 op amp within the circuit of Figure 6-39. The OP275 use junction FET devices in the input stage, which have appreciable (non-linear) capacitance to the substrate. The test is done with various values of source resistance R_S. As noted, distortion is lowest when R_S is equal to the parallel equivalent of R_F and R_{IN}, or in this case, about 910Ω. For either higher or lower values of R_S, distortion rises. Appreciably higher source impedance (10kΩ) can cause the distortion to rise lower in frequency, making performance much worse overall.

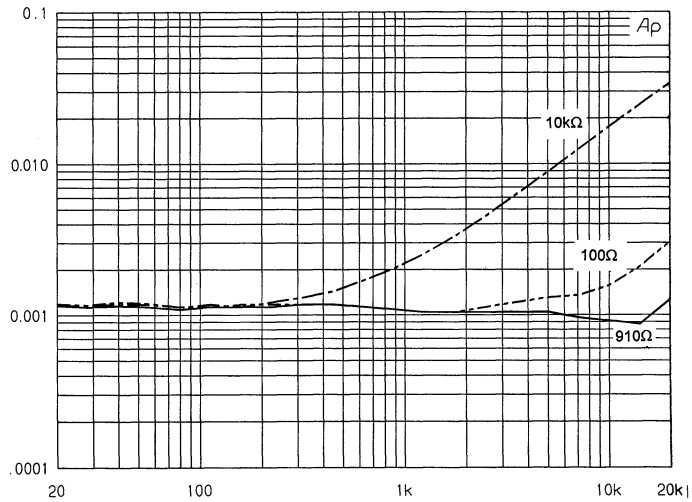


Figure 6-40: *Follower mode R_S sensitivity of OP275 bipolar/JFET input op amp-THD+N (%) vs. frequency (Hz), V_{OUT} = 7Vrms, R_L = 500Ω, V_S = ±18V*

It is therefore suggested that, whenever possible, amplifiers operated as voltage followers should have their source impedances balanced for lowest distortion. Note that the OP275 device is just one example, and its sensitivity to CM distortion effects is not at all unique in this regard.

While the balancing of the two source impedances is most helpful, *lowering the absolute value* can also minimize this distortion. With R_S low, this has the effect of moving the high frequency breakpoint of the distortion rise upwards in the spectrum, were it is less likely to be harmful. The best overall control of this distortion mechanism with an amplifier subject to it is the use of the lowest practical, balanced source impedances.

It is important to understand that virtually all IC op amps, *particularly those using JFET inputs*, as well as discrete JFET and bipolar transistors are subject to non-linear C-V effects, to some degree. In the tests of other amplifiers within the Figure 6-39 circuit, R_S was maintained at 910Ω, so as to minimize the effects of this distortion mechanism.

With high output, high slew rate linear amplifiers, the distortion generated for these test conditions can parallel that of the test equipment residual, as shown in Figure 6-41. Here the AD817, AD818 and AD845 amplifiers show THD+N which is essentially equal to the residual for these conditions, and appreciably below 0.001%.

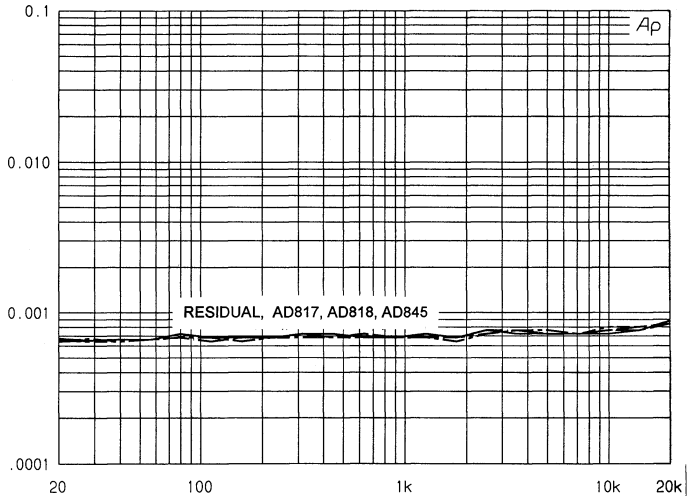


Figure 6-41: *A driver group, THD+N (%) vs. frequency (Hz), for V_{OUT} = 7Vrms, R_S = 909Ω, R_L = 500Ω, V_S = ±18V*

Amplifier types expressly designed for audio use also do well for these THD+N tests, as shown in Figure 6-42. The industry standard 5534 is near or just above the residual level, while the OP275 plot falls just above the 0.001% level and the 5532 is slightly higher.

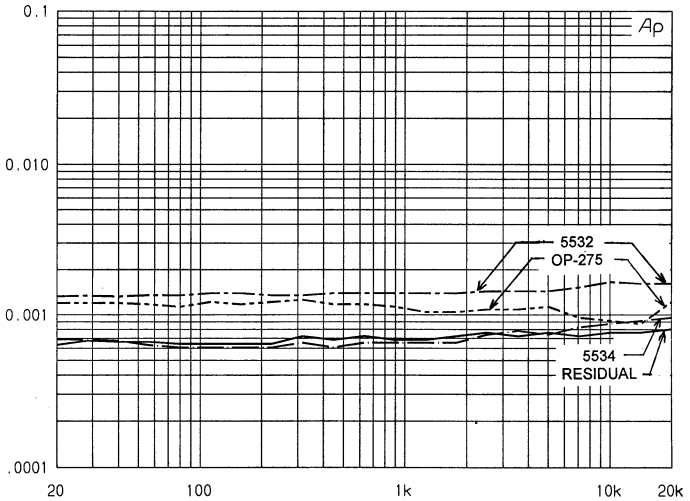


Figure 6-42: *B driver group, THD+N (%) vs. frequency (Hz), for V_{OUT} = 7Vrms, R_S = 909Ω, R_L = 500Ω, V_S = ±18V*

These tests reflect performance of a variety of single amplifiers, as exercised for matched-source test conditions, with medium output loading of 600Ω. Varying test conditions may change the absolute levels of performance. So also may different samples, or in the case of industry standard parts, alternate vendors.

The data of Figs. 6-41 and 6-42 reflect older (but available) op amp devices capable of very high performance in these tests. Several more recent devices also do well for this driver test. Figure 6-43 below shows performance of newer FET input op amps, the AD825, the AD8610 and the AD8065. The AD825 was tested under conditions identical to those of Fig. 6-41 and 6-42. The AD8610 and AD8065 were tested under similar conditions, but with ±13V power supplies, reflecting a lower maximum supply rating.

Interestingly, note that the latter two amplifiers still can accommodate more than a 7Vrms output swing, even with the reduced supplies. Under these conditions, the AD8065 distortion is near the test set residual and the AD8610 slightly higher at high frequencies. The AD825 has somewhat higher distortion, but this is almost frequency independent.

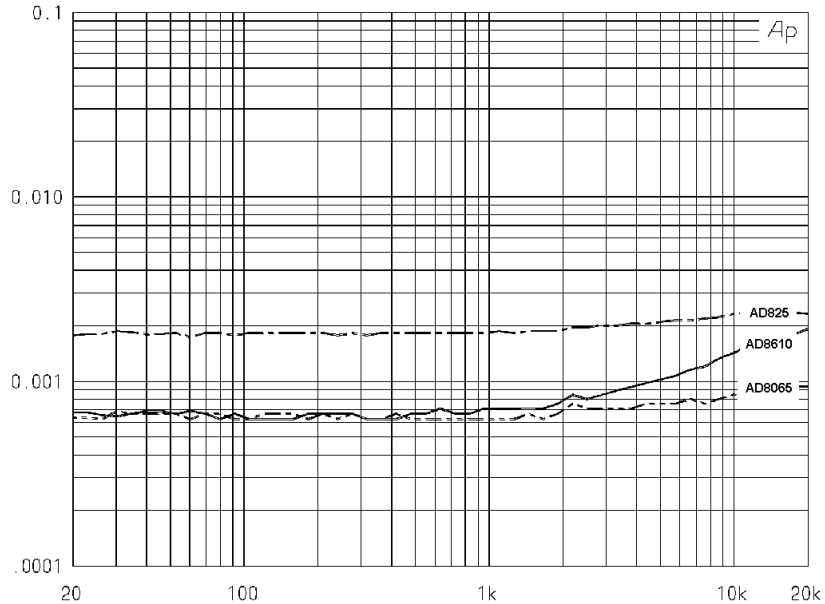


Figure 6-43: *C driver group, THD+N (%) vs. frequency (Hz), for V_{OUT} = 7Vrms, R_S = 909Ω, R_L = 500Ω, V_S = ±13V or ±18V*

Single-Ended Line Drivers

This section discusses a variety of line driver circuit examples that drive single-ended lines, optimized for different operating environments, supply voltages, and performance.

Consumer Equipment Line Driver

One common driver application is a line output stage for consumer preamps, CD and DVD players, etc. This is typically an economical audio stage with a nominal gain of 5 to 10 times, operating from supplies of ±10V to ±18V, usually with a rated output of 2-3Vrms, and a capability of driving loads of 10kΩ or more.

For simplicity of biasing and minimum output DC offset, AC coupling is used, and the circuit is typically fed from a volume control. For stereo operation, a dual channel device is typically sought for this type application, one which is also optimized for audio uses.

Such a stage is shown in Figure 6-44 below, and it uses an OP275 dual op amp as the gain element. In this circuit input and feedback resistors R_1 and R_3 are set equal, which makes the nominal DC bias at U1's output close to zero. The U1 bias current flowing in these resistors also serves to polarize coupling capacitors C_1 and C_2 positively, as noted. This bias is due to the sign of the OP275's PNP input stage bias currents, so reverse C_1-C_2 if an NPN input amplifier is used.

R_2 sets the gain of the stage in conjunction with R_1. The stage gain is nominally 5 times for the values shown. C_2 sets the low frequency rolloff along with R_2, which in this case is ≈0.3Hz. Although this frequency is quite low, it does allow some range of gain increase if desired, simply by lowering R_2. Output capacitor C_3 must be non-polarized, since the worst case DC at the output of U1 is ≤10mV (and can be bipolar). Typically it will be about ¼ this, so if a few mV can be tolerated, C_3 can be eliminated.

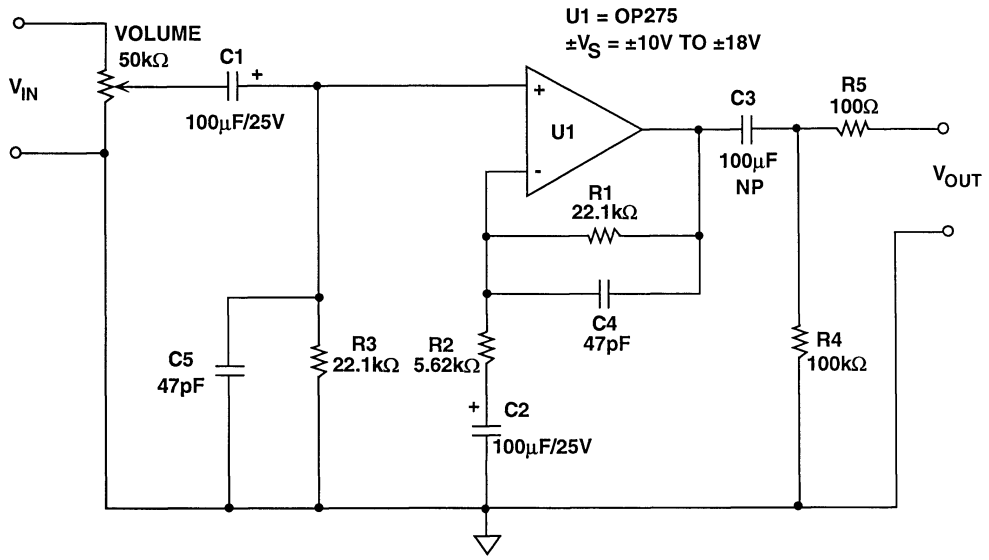


Figure 6-44: *Consumer equipment line driver stage*

THD+N performance of the stage (not shown) was measured for outputs of 1-3Vrms into a 10kΩ/600pF load, using ±18V supplies with an R_S of 1kΩ. At lower output levels performance is noise limited, measuring less than 0.002%. At the 3V output level a slight increase in high frequency distortion is noted. Although this application is an example where the amplifier ± source impedances cannot be matched (due to the variations of the volume control), nevertheless the performance is still quite good.

Noise is the limiting factor for lower level signals, so if lower noise is desired, R_2 can be reduced. The ultimate practical limit to noise is the volume control's finite output impedance. This causes higher noise at positions of high output resistance, interacting with the noise current from U1. For example if the effective R_S from the volume control is 10kΩ, a 1.2pA/√Hz noise current from U1 will produce an input referred 12nV/√Hz noise voltage, from this source alone. The Fig. 6-44 driver is a flexible one, and operates at supplies as low as ±10V with outputs up to 3Vrms, with slight distortion increases. With ±5V supplies up to 2Vrms is available, with higher distortion (but still ≤0.01%).

Paralleled Output Line Driver

Often a modest increase in output may be needed for a driver, but circumstances may not warrant the use of additional buffer devices. Figure 6-45 shows how a second section of a dual op amp can be used to provide additional load drive.

In this circuit using an OP275 dual op amp, the U1A section is a gain-of-five voltage amplifier, while the U1B section is a voltage follower, used simply to provide additional current to the load. Current sharing is determined by output summer resistors R_4 and R_5, and the parallel stage drives 600Ω loads with less distortion than a single OP275 section.

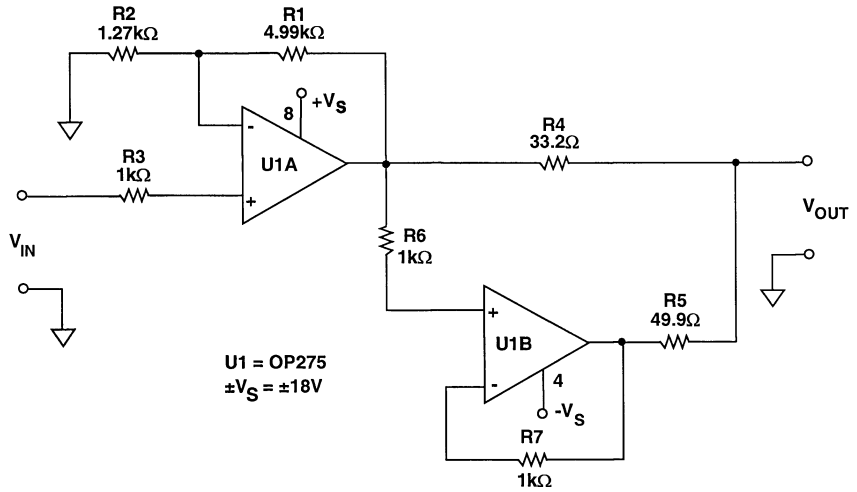


Figure 6-45: *Paralleled output dual op amp line driver*

THD+N performance data is shown in Figure 6-46 below, with the driver operating from ±18V supplies, and for output levels of 1, 2, 5, and 9Vrms into 600Ω.

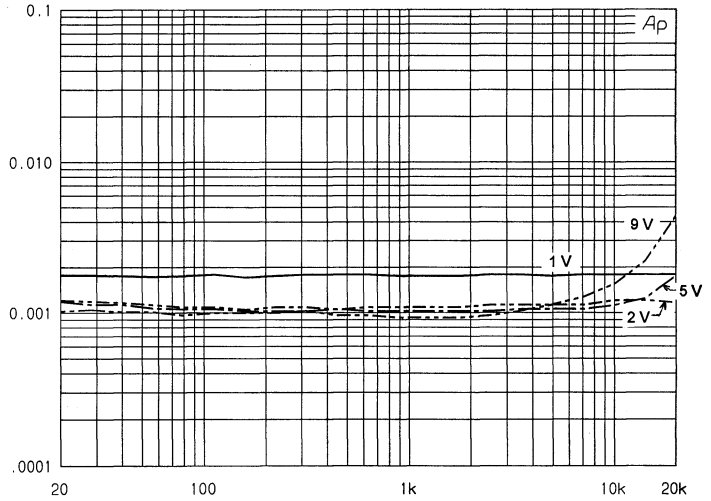


Figure 6-46: *Paralleled output dual op amp line driver, THD+N (%) vs. frequency (Hz), for V_{OUT} = 1, 2, 5, 9Vrms, R_L = 500Ω, V_S = ±18V*

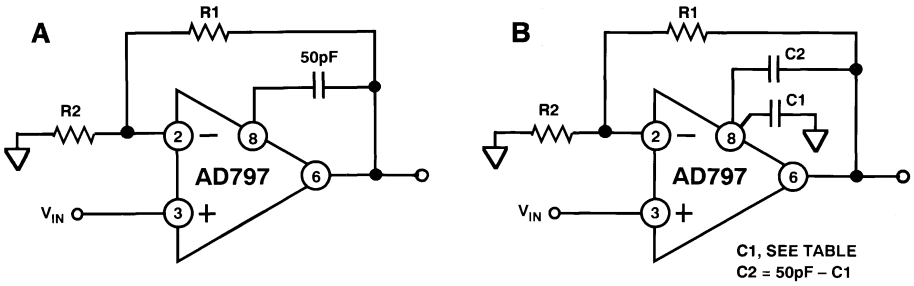
This general scheme can be used with any unity gain stable dual op amp, and also can be adapted for various gain levels, via R_1-R_2. For different devices and/or gains, the ratio of R_4 and R_5 may need adjustment, for lowest distortion into the load.

A Wide Dynamic Range Ultra Low Distortion Driver

Single ended line drivers are simple conceptually, but when pushed to performance limits in dynamic range and distortion, they challenge device choice. The AD797 answers this challenge with its input noise of ≤1nV/√Hz and a distortion canceling output stage. These features allow low and high extremes of dynamic range to be pushed simultaneously.

The AD797 uses a single voltage gain stage, comprised of a folded cascode input combined with a boot strapped current mirror load, allowing the high incremental impedance necessary for a 146dB gain. This buffered single-stage topology is a departure from past devices using multiple stages, with performance benefits in terms of bandwidth, phase margin, settling time, and input noise (see Reference 9).

For standard uses, the AD797 is employed like any 5 pin op amp, such as shown in Figure 6-47 below (neglecting the capacitors for the moment). From the A/B part of the table, relatively low values for resistors R_1-R_2 are recommended for lowest noise. Selecting these resistors should be done with care, since values ≥100Ω will degrade noise performance. Suggested values for gains of G = 10-1000 are noted. The AD797 can drive loads of up to 50mA, and is rated for distortion driving loads of 600Ω.



	A / B		A			B		
	R1	R2	C1	C2	3dB	C1	C2	3dB
	Ω	Ω	pF	pF	BW	pF	pF	BW
G=10	909	100	0	50	6 MHz	0	50	6 MHz
G=100	1k	10	0	50	1 MHz	15	33	1.5 MHz
G=1000	10k	10	0	50	110 kHz	33	15	450 kHz

Figure 6-47: *Recommended AD797 connections for distortion cancellation and/or bandwidth enhancement*

For amplifier applications requiring more top grade performance, optional capacitors C_1 and C_2 can be used. In the Fig. 6-47A configuration, superior performance is realized due to distortion cancellation with the use of a single extra capacitor, enabled simply by adding the 50pF unit as shown. This provides compensation for output stage distortion without effecting the forward gain path, effective over the range of gains noted.

An additional option with the AD797 is the use of *controlled decompensation*, available with the Fig. 6-47B option and the use of capacitors C_1, C_2. At gains of 100 or more, adding C_1 as in column B of the table enhances amplifier open loop bandwidth, allowing very high gain-bandwidths to be achieved— 150MHz at G=100, and 450MHz at G=1000. For high gain operation this extra gain-bandwidth can be very effective.

A family of distortion curves for various AD797 gain configurations driving 600Ω is shown in Figure 6-48 below. As noted, at low frequencies the data is limited by noise, while at high frequencies distortion is measurable, but still extremely low. The distortion for a gain of 10 times at 20kHz for example, is on the order of ≈0.0001%, implying a dynamic range of about 120dB re 3Vrms, or even more for higher level signals.

An additional point worth making at this point is one regarding the AD797's special distortion cancellation ability. Referring to Fig. 6-47A (again), it should be noted that the 50pF capacitor is connected between pins 8 and 6 of the AD797. Pin 6 is of course the output of the device for standard hookups. However, in special situations, even greater output current may be required, and a unity gain buffer amplifier can be added between pin 6 and the load. For example, one of the buffers of Fig. 6-36 or 6-37 could be used to extend output current to ≥100mA.

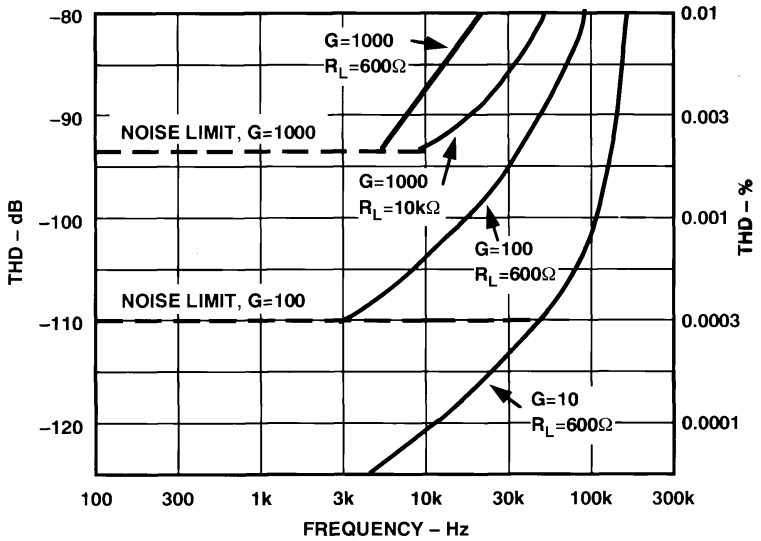


Figure 6-48: *THD vs. frequency at 3Vrms output for AD797 distortion cancellation and/or bandwidth enhancement circuit of Fig. 6-48*

The special point worth noting for this situation is that the 50pF distortion cancellation capacitor should then be connected between the AD797 pin 8 *and the output of the buffer* (not the AD797 pin 6). This step allows the distortion correction to be applied not just to the AD797 internal circuits, but also extends it to include the buffer.

A case in point where this would come to useful purpose lies with the AD797 mic preamp, discussed in some detail earlier in the chapter (Fig. 6-5, again). As mentioned therein, a BUF04 would work well as just such a buffered output option for the AD797 preamp. It would be connected as described above, with the 50pF distortion cancellation capacitor. Details of this are left as a reader exercise (but should even so be obvious).

Current Boosted Buffered Line Drivers

When load drive capability suitable for less than 600Ω in impedance is required, it is most likely outside the output current and/or linearity rating of even the best op amps. For such cases, a current boosted (buffered) driver stage can be used, allowing loads down to as low as 150Ω (or less) to be driven. Another example would a driver for long audio lines, i.e., lines more than several hundred feet in length.

Figure 6-49 below is a high quality current boosted driver example, using an AD845 at U1 as a gain stage and voltage driver, in concert with a unity voltage gain current booster stage, U2. The overall voltage gain is 5 times as shown, but this is easily modifiable via alternate values for R_1 and R_2. In any case, for lowest CM distortion effects, input resistor R_3 should be set equal to $R_1 \parallel R_2$ (this assumes a low impedance source for V_{IN}).

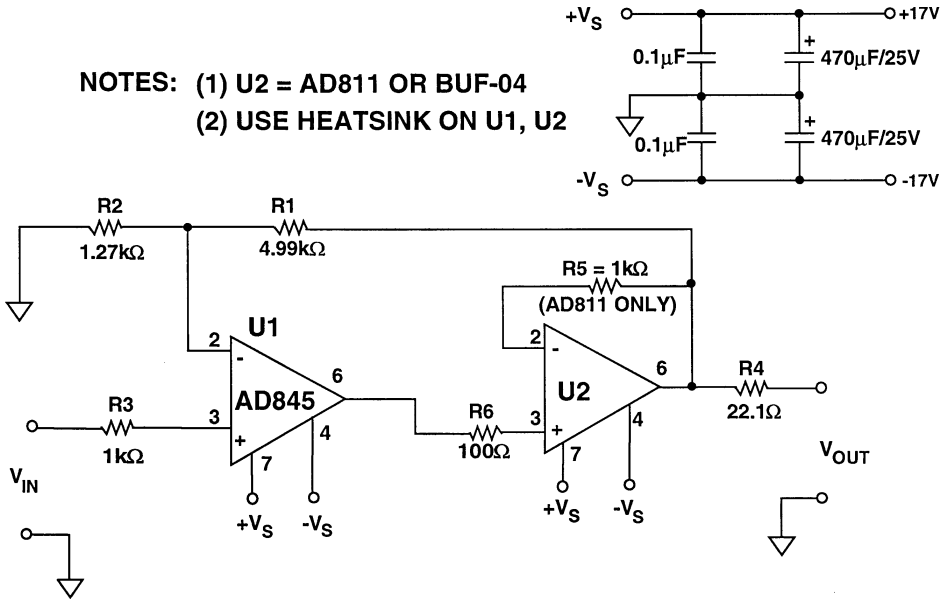


Figure 6-49: *Current boosted line driver*

The amplifier used for U2 can be either the AD811 op amp, or the BUF04 buffer for simplicity. If the AD811 or similar CFB op amp is used (AD812 etc.), it needs to be configured as a follower, with R_5 connected as shown. Since the BUF04 is internally connected as a follower, it doesn't need the R_5 external feedback resistor.

Because of the high internal dissipation of the AD845 and AD811, these devices *must* be used with a heat sink on supplies of ±17V. But, such high supplies are only justified for extreme outputs. Supplies of ±12V also work, and will eliminate need for a heat sink (with lower maximum outputs). In any case, power supplies should be well bypassed.

A special note is applicable here— Always *observe maximum device breakdown voltage ratings within applications. Production versions of this circuit should use supplies of ±17V or less, for 36V(max) rated parts. Similarly, 24V(max) rated parts should use supplies of ±12V or less. In all cases, use only enough supply voltage to achieve low distortion at the maximum required output swing.*

For loads of 150Ω, the output series isolation resistor R_4 is lowered to 22.1Ω to minimize power loss, and to allow levels of 7Vrms or more. The THD+N data for this circuit is shown in Figure 6-51 below, using an AD811 as the U2 buffer. The test conditions are input sweeps resulting in 1, 2, 4 and 8Vrms output, using ±18V power supplies.

For the AD811 operating as U2, the Figure 6-50 data below shows THD+N dominated by noise and residual distortion at nearly all levels and frequencies driving 150Ω, up to 8Vrms. At this level, a slight distortion rise is noted above 10kHz, yet it is still ≈0.001%. With the BUF04 as U2 (not shown) THD+N is comparable at lower output levels, but does show a distortion rise with 8Vrms output at high frequencies (yet still below 0.01%).

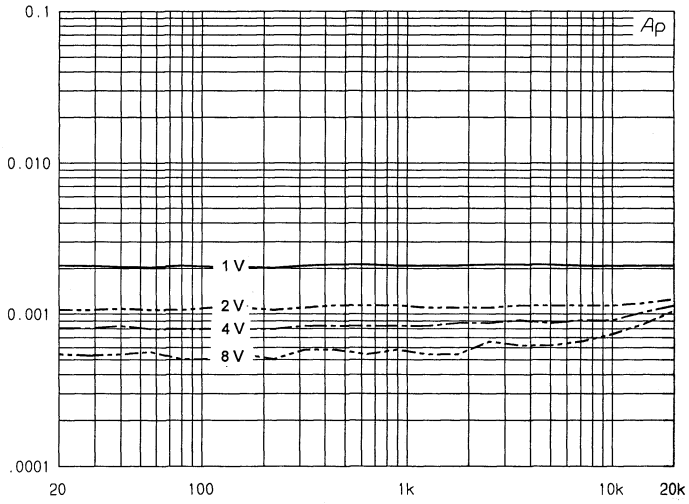


Figure 6-50: *Current boosted driver of Fig. 6-50 using AD811 as U2, THD+N (%) vs. frequency (Hz), for V_{OUT} = 1, 2, 4, 8Vrms, R_L = 150Ω, V_S = ±18V*

There is a power/performance tradeoff involved with the choice between the two mentioned U2 devices which should be understood. The BUF04 has a standby dissipation of about 200mW on ±15V, while the AD811 is more than double this dissipation, at 500mW. So while the AD811 does yield the lower distortion, it also should be operated more conservatively from a power standpoint. As noted above, only the minimum (±) supply voltage required to sustain a given output should be used with the circuit in general, and particularly with the AD811 employed at U2.

As for U1 in this circuit, other amplifiers can be used, but only with due caution against poor performance. Quite simply, it is difficult to improve upon the AD845's performance in this application. Three possible candidates would include the "Group C" op amps of Fig. 6-43, operating on suitable power supplies; ±17V or less for the AD825, and ±12V or less for the AD8610 and AD8065. Of these, the AD8065 would seem to hold the greatest promise, having shown the lowest wideband distortion in the Fig. 6-43 tests.

But, as considered within the buffered driver circuit of Fig. 6-50, the AD8065 will be operated in an even more linear fashion; that is it is operating essentially unloaded at the output. This is a key factor towards highest performance, as it moves the burden of linear load drive to the buffer stage. Further variations of this circuit technique will be reprised later, within other driver applications to be discussed.

Composite Current Boosted Drivers

Another useful current-boosted circuit technique combines the positive aspects of two different amplifiers into a single composite amp structure, producing a very high performance line driver (see References 10-13 for several variations of this basic circuit). With an FET input IC used as the input stage, DC offset change from source resistance variations of a typical volume control of ≈50kΩ is nil, allowing total direct coupling. As noted previously, with a high current, wide band booster output stage, line impedances down to 150Ω can be driven with excellent linearity.

This type of composite amplifier allows good features of two dissimilar ICs to be exploited; each optimized for the respective input and output tasks. Figure 6-51 shows a low distortion composite amplifier using two op amps ICs with such performance.

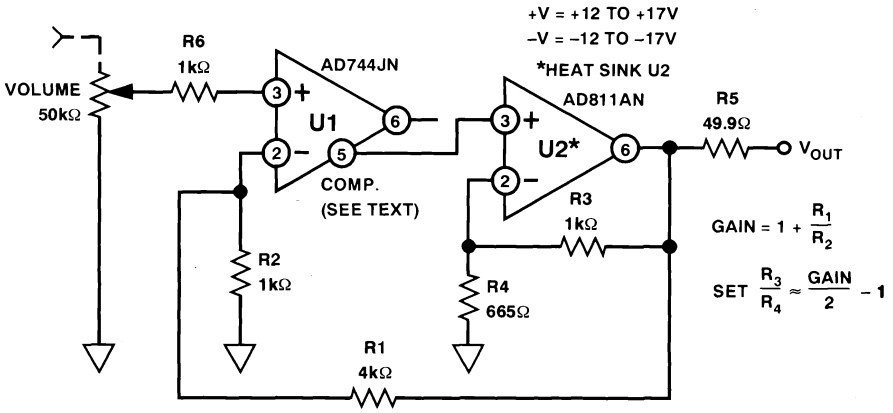


Figure 6-51: *Composite current boosted line driver one*

A factor here aiding performance is that the U1 AD744 stage operates unloaded, and also that the AD744's compensation pin (5) drives U2. This step (unique to the AD744) removes any possibilities of U1 class AB output stage distortion. Another key point is that the overall gain bandwidth and SR of U1 are boosted by a factor equal to the voltage gain of U2, an AD811 op amp, which itself operates at a voltage gain. These factors enhance this circuit by providing both high and linear load current capability, providing a composite equivalent of an FET input power op amp.

This design operates at an *overall* voltage gain set by R_1 and R_2 (just as a conventional non-inverting amplifier) which in this case is 5 times. Since the circuit also uses a local loop around stage U2, the R_3/R_4 ratio setting the U2 stage gain should be selected as noted. This complements the overall gain set by R_1 and R_2, and optimizes loop stability.

Also note that the U2's feedback resistor R_3 has a preferred minimum value for stability purposes (again, as is unique to CFB amplifier types). Here with the AD811, a 1kΩ value suffices, so this value is fixed. R_4 is then chosen for the required U2 stage gain. Further design details are contained in the original references (see References 2 and 10, again).

The composite amplifier performance for a typical audio load of 600Ω, THD+N at output levels of 1, 2, 4 and 8Vrms is shown in Figure 6-52 below, while operating from supplies of ±18V for this test. The apparent distortion is noise or residual limited at almost all levels, rising just slightly at the higher frequencies.

Lower impedance loads can also be driven with this circuit, down to 150Ω. Note that for operating supply voltages of more than ±12V, a clip on heat sink is recommended for U2, as previously discussed for the AD811. Practical versions of this circuit can readily use supplies of ±12V, and still operate very well.

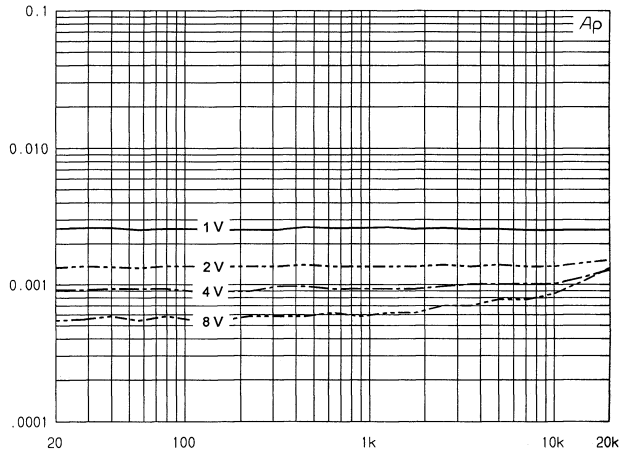


Figure 6-52: *Composite current boosted driver one of Fig. 6-51, THD+N (%) vs. frequency (Hz), for V_{OUT} = 1, 2, 4, 8Vrms, R_L = 600Ω, V_S = ±18V*

The circuit of Fig. 6-51 is a very flexible one, and it can also be adapted a variety of ways. Although the original version shown uses the AD744 compensation pin (5) to drive the output stage U2 device, conventional internally compensated op amps can also be used for U1, and still realize the many features of the architecture.

The ability to adapt the topology to differing devices in single and dual op amp formats allows such dual FET devices as the AD823 to be usefully employed in a stereo realization. Similarly, dual CFB op amps such as the AD812 can be used in the U2 output stage. Thus a complete stereo version of the circuit can be efficiently built, based on only two IC packages.

This topology's flexibility also opens up a diversity of other applications beyond the basic line driver. For example, using a power-packaged dual CFB op amp such as the AD815 for U2, allows very low impedance loads such as headphones to be driven, down to as low as 10Ω (see Reference 12, again).

The composite current boosted line driver two, shown in Figure 6-53 below, summarizes a number of the above mentioned options, and adds some other features as well.

Similarities within this circuit to the predecessor are resistances R_1-R_4, which perform similar functions to the previous version. Overall gain is again calculated via R_1-R_2, while output stage gain is set via R_3, R_4, etc.

Here, note that an additional pair of resistances, R_C and R_D, form a local feedback path around stage U1. This addition allows the effective open loop bandwidth of U1 as it operates within the overall loop to be increased. For the values shown, using an AD823 for U1, the open loop bandwidth is about 100kHz. This means that the open loop bandwidth of the entire circuit is greater than the audio bandwidth, which means phase errors within the passband will be minimized.

An optional small capacitance (C_F, 10-20pF) can be useful for stabilizing the U1 stage, particularly if it employs a wide bandwidth device such as the AD825. When C_F is used, a like capacitor C_{IN} can also be used, to preserve high frequency impedance matching.

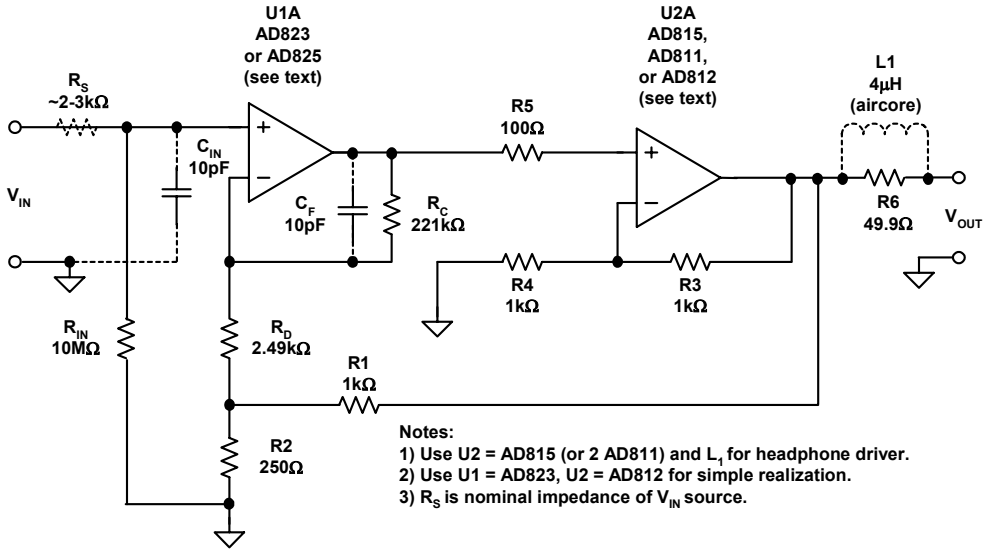


Figure 6-53: *Composite current boosted line driver two*

The primary input impedance balancing of the circuit is accomplished via resistance R_D, which has a dual role. External resistance R_S is the nominal output resistance of a volume control (typical for a 50kΩ audio taper control at listening level). R_D is chosen to match R_S, and R_C will be approximately 100 times the R_D value when using the AD823.

The necessity of inductor output L1 depends upon whether the circuit is to be used with low impedance loads. For headphones, the L1 choke is necessary to prevent excessive voltage loss from a simple R_6 connection. R_6 is used, in either a headphone or line driver case. If configured as a headphone driver, the circuit should use several square inches of PCB area around U2, to heat sink the AD815 device (see device data sheet). The AD811 and AD812 can also be used to drive higher impedance phones, such as 100Ω or more.

Because of the vast number of options with this circuit, no performance is presented here. However, some insight into headphone driver performance is contained in Reference 12.

Differential Line Drivers

Unlike differential line receivers, a standard circuit topology for differential line *drivers* isn't nearly so clear-cut. A variety of different circuit types for driving audio lines in a balanced mode are discussed in this section, with their contrasts in performance and complexity. The virtues of balanced audio line operation are many. The largest and most obvious advantage is the inherent rejection of inevitable system ground noises, between the driver and receiver equipment locations.

There are also more subtle advantages to balanced line operation. Differential drivers tend to inject less noise onto the power supply rails. Related to this, they also produce inherently less noise onto the ground system, since by definition the return path for a differential signal is not ground. This can be a significant advantage when high currents need to be driven into a long audio line, as it can reduce multiple channel crosstalk. The circuits that follow illustrate a variety of methods for differential line driving.

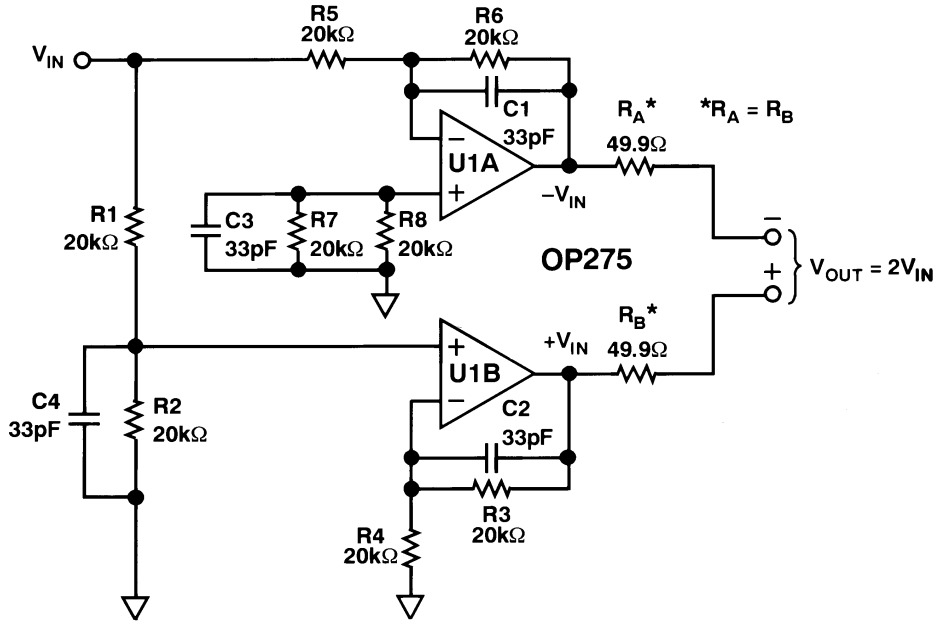


Figure 6-54: *An "inverter-follower" differential line driver*

"Inverter-Follower" Differential Line Driver

A straightforward approach to developing a differential drive signal of $2V_{IN}$ is to amplify in complementary fashion a single-ended input V_{IN}, with equal gain inverter and follower op amp stages. With op amp gains of ±1, this develops outputs $-V_{IN}$ and V_{IN} with respect to common, or $V_{OUT} = 2V_{IN}$ differentially. This "inverter/follower" driver is easily accomplished with a dual op amp such as the OP275, plus an 8x20k film resistor network (or discrete), as shown above, in Figure 6-54. Here U1A provides the gain of –1 channel, while U1B operates at a gain of +1. The differential output signal across the balanced output line is $2V_{IN}$, and the differential output impedance is equal to $R_A + R_B$, or 100Ω. The output resistors $R_A + R_B$ should be well matched, for reasons discussed earlier.

Use of like-value gain resistors around the U1 sections makes the respective channel noise gains match, and also makes their purchase easy. In addition, this forces the source

impedances seen by the op amp ± inputs to be matched. Capacitors C_1-C_2 provide a ultrasonic rolloff, and enhance stability into capacitive lines. Overall, this circuit is high in performance for its cost and simplicity. Note that if a resistor network is used for R_1-R_8, the entire circuit can be built with only 8 components.

THD+N performance of the Fig. 6-54 circuit operating on ±18V supplies is shown in Figure 6-55 below, for a series of successive sweeps resulting in output levels of 1, 2, 5 and 10Vrms across 600Ω. The distortion in most instances is about 0.001%, and somewhat higher at a 1V output level (noise limited at this level). Maximum output level is about 12Vrms into 600Ω before clipping (not shown).

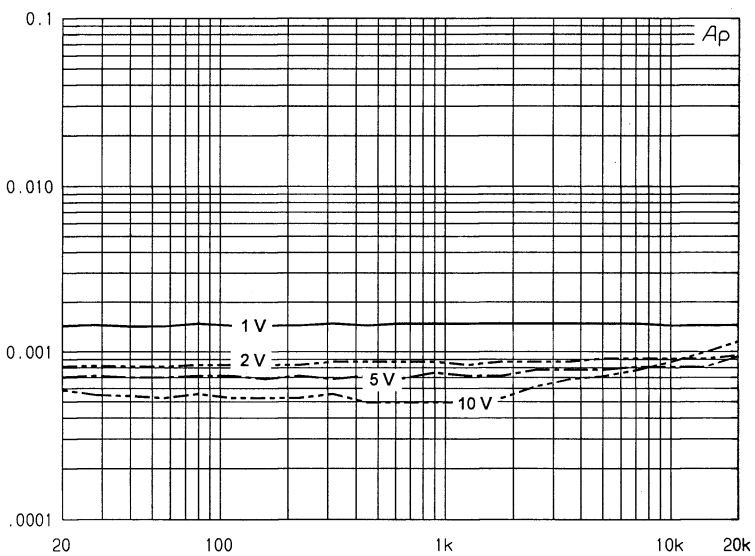


Figure 6-55: *Inverter-follower driver of Fig. 6-54, THD+N (%) vs. frequency (Hz), for V_{OUT} = 1, 2, 5, 10Vrms, R_L = 600Ω, V_S = ±18V*

In system terms, this type of differential line driver can potentially run into application problems, and should be used with some caveats in mind. In reality, this driver circuit uses two mirror-imaged, single-ended drivers, and they produce voltage output signals with respect to the source (V_{IN}) common point.

At the load end of a cable being driven, if the receiver used has a high impedance differential input (such as those discussed in the line receiver section) there is no real problem in application for this driver circuit. However, it should be noted that one side of the differential output from Figure 6-54 *cannot be grounded without side effect*. This is because the source drive V_{OUT} is *not* truly floating, as would be in the case of a transformer winding.

In this sense, the circuit is *pseudo differential*, and it shouldn't be used indiscriminately. Nevertheless, within small and defined systems, is still has the obvious advantage of simplicity, and, as noted, it can achieve high performance. Note also that with the matched source resistances R_A and R_B of 49.9Ω as shown, nothing will be damaged even if one output is shorted— other than a loss of half the signal! Finally, if balanced high impedance differential loading is used at the receiver, there will be no side effects.

Cross-Coupled Differential Line Driver

A more sophisticated form of differential line driver uses a pair of *cross-coupled* op amps with both positive and negative feedback paths. The general form of this type of circuit is a cross-coupled Howland circuit, after the classic resistor bridge based current pump. The cross-coupled form was described by Pontis in a solid-state transformer emulator for high performance instrumentation (see Reference 13).

Application-wise, this configuration provides maximum flexibility, allowing a differential output signal V_{OUT} to be maintained constant and independent of the load common connections. This means that either side can be shorted to common without loss of signal level, i.e., as can be done with a transformer.

Figure 6-56 below shows the SSM2142 balanced line driver IC in an application. The SSM2142 consists of two Howland circuits A2 and A3, cross-coupled as noted, plus an input buffer (A1). The trimmed multiple resistor array and trio of op amps shown is packaged in an 8 pin miniDIP IC with the pinout noted.

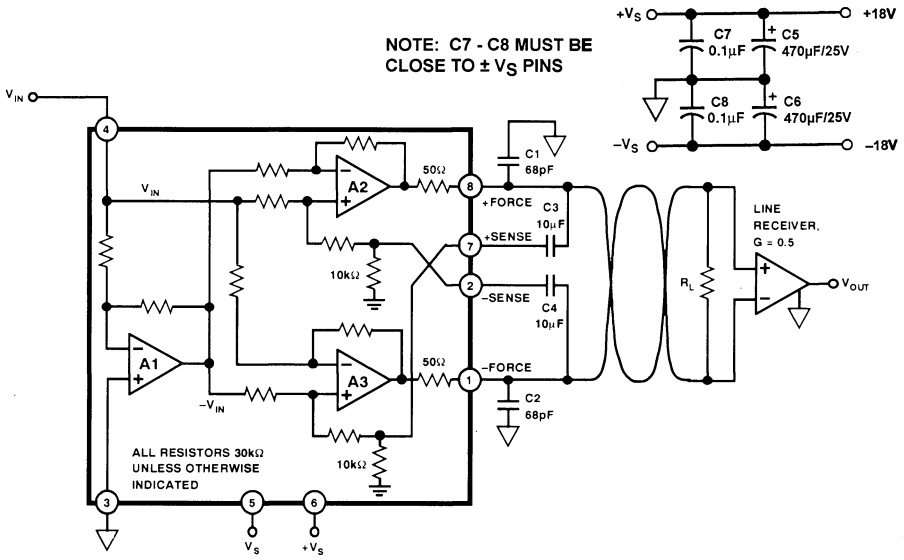


Figure 6-56: *SSM2142 cross-coupled differential line driver used within balanced driver/receiver system*

The SSM2142 line driver is designed for a single-ended to differential gain of 2 working into a 600Ω load. In the simplest use, it is strapped with the respective output FORCE/SENSE pins tied together (7-8, 1-2). Small film capacitors C_1-C_2 preload the IC for stability against varying cable lengths. To decouple line dc offsets, the optional capacitors C_3-C_4 are used as shown, and should be non-polar types, preferably films.

An additional "housekeeping" caveat with the SSM2142 involves the high frequency power supply bypassing. The 0.1µF low inductance bypass caps C_7 and C_8 must be within 0.25" of power supply pins 5 and 6, as noted in the figure. If this bypassing is compromised by long lead lengths, excessive THD will be evident.

In a system application, the SSM2142 is used with a complementary gain of 0.5 receiver, either an SSM2143, or one of the other line receivers discussed previously. The complete hookup of Fig. 6-56 comprises an entire single-ended to differential and back to single-ended transmission system, with noise isolation and a net end-to-end unity gain.

Figure 6-57 shows the THD+N performance of the SSM2142 driver portion of Fig. 6-56, for sweeps yielding output levels of 1, 2, 5 and 10Vrms across 600Ω. While performance is noise limited for the 1V output curve, distortion drops to ≤0.001% and near residual for most higher levels, rising only with higher frequencies and the 10V output curve.

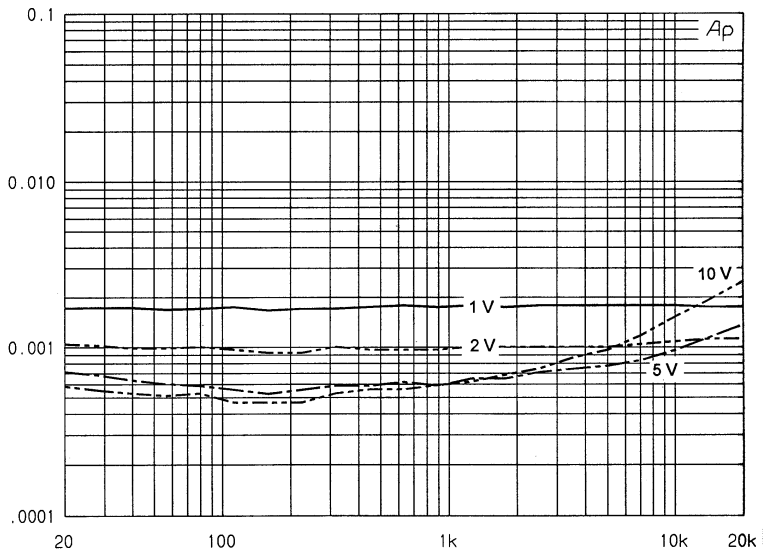


Figure 6-57: *SSM2142 driver portion of Fig. 6-56, THD+N (%) vs. frequency (Hz), for V_{OUT} = 1, 2, 5, 10Vrms, R_L = 600Ω, V_S = ±18V*

These two differential drivers are suited for 600Ω or higher loads, and, within those constraints, perform well.

As should be obvious, these drivers do *not* offer galvanic isolation, which means that in all applications there must be a DC current path between the grounds of the driver and the final receiver. In practice however this isn't necessarily a problem.

The following circuits illustrate differential drivers that do offer galvanic isolation, and can therefore be used with ground potential differences up to several hundred volts (or the actual voltage breakdown rating of the transformer in use).

Transformer Coupled Line Drivers

Transformers provide a unique method of signal coupling, which is one that allows completely isolated common potentials, i.e., *galvanic isolation*. As noted previously in the line receiver section, transformers are not without their technical and practical limitations, but their singular ability to galvanically isolate grounds maintains a place for them in difficult application areas (see References 15 and 16).

Basic Transformer Coupled Line Driver

The circuit of Figure 6-58 below uses some previously described concepts to form a basic low DC offset, high linearity driver using a high quality nickel core output transformer. U1 and U2 form a high current driver, similar to the Fig. 6-49 current boosted driver.

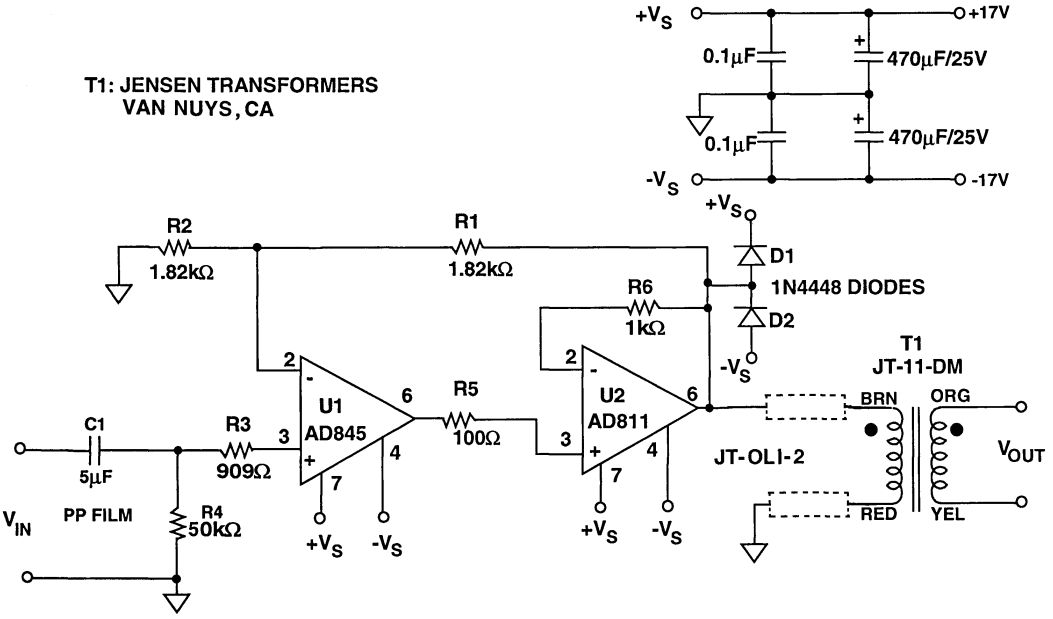


Figure 6-58: *A basic transformer coupled line driver*

In this circuit U1 is a low offset voltage FET input op amp, for the purpose of holding the DC offset seen at the primary of T1 to a minimum (±12.5mV maximum as shown, typically less). DC current flowing into the primary winding of a transformer should be minimized, for lowest distortion. C_1, a high quality film capacitor, decouples any DC offset present on V_{IN}, for similar reasons.

The U1-U2 device combination is capable of ±100mA or more of output, which aids greatly in the ability of this circuit to drive low impedances. The buffering of U2 is recommended for long lines, or for the absolute lowest distortion. Although T1 is shown with a 1:1 coupling ratio, other winding configurations are possible with transformer variations, that is step-up or step-down, allowing either 600Ω or 150Ω loads.

As can be noted, the T1 primary isn't driven directly, but is isolated by two series isolation devices, Jensen JT-OLI-2s. Each of these is an LR shunt combination of about 39Ω and 3.7µH. The net impedance offers a very low DCR, and an increasing impedance

above 1.5MHz for load isolation (see device data sheet and Reference 17). The use of two isolators as shown offers best output CMR rejection for the transformer, but one will also work (with less CMR performance), as will a single 10Ω resistor.

THD+N performance for this driver-transformer combination is shown in Figure 6-59 below, for supplies of ±18V and successive input sweeps, resulting in outputs of 1, 2, 4, and 8Vrms into 600Ω. These data were taken with a single series resistance of 10Ω driving T1 (which could be conservative compared to operation with two isolators).

As with the 2x and 5x basic drivers previously described, these data are essentially distortion free above 100Hz. At lower frequencies there is seen a level dependent, inverse-frequency dependent distortion. The measured distortion reaches a maximum at 20Hz with output levels of 8Vrms (≈20dBm), while at lower levels it is substantially less.

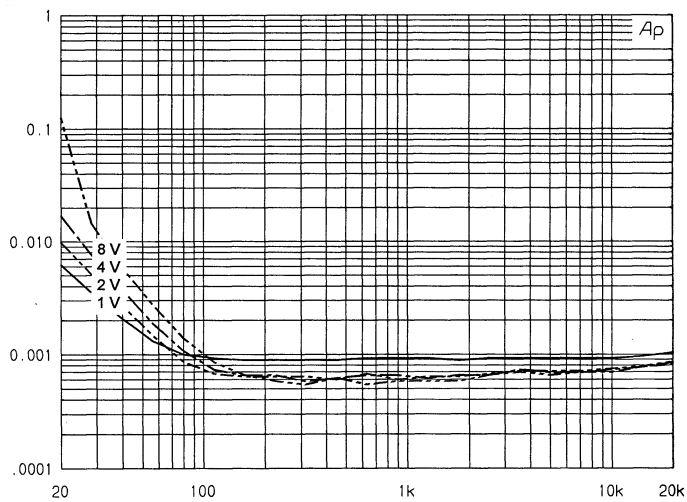


Figure 6-59: *Transformer driver of Fig. 6-58, THD+N (%) vs. frequency (Hz), for V_{OUT} = 1, 2, 4, 8Vrms, R_L = 600Ω, V_S = ±18V*

This distortion phenomenon is basic to audio transformers, to one degree or another. It is lessened (but not totally eliminated) in the higher quality transformer types, such as the nickel-core unit used in the Fig. 6-58 circuit.

In practice, there are some factors that tend to mitigate the seriousness of the low frequency distortion seen in the performance data of Fig. 6-59. First, rarely will maximum audio levels ever be seen at 20Hz. Thus suitably derated operation of T1 will strongly reduce the incidence of this distortion.

However, if the lowest distortion possible independent of level is desired, then some additional effort will need to be expended on making the transformer driver more sophisticated. This can take the form of actively applying feedback around the transformer, so as to lower its non-linearity to negligible levels. This is design approach is discussed with the next driver circuits.

Feedback Transformer Coupled Line Drivers

While non-premium core transformers are more economical than the nickel core types, as a tradeoff they do have much higher distortion. To further complicate the design issue, the distortion characteristics of most transformers varies with level and frequency in complex ways, rising more rapidly at higher levels and lower frequencies. This behavior is even less forgiving than that of the nickel core types, and complicates somewhat the application of audio transformers. While a nickel core transformer has distortion characteristics sufficiently low so as to allow their use without distortion correction (Fig. 6-58, again) the same simply isn't true for other core materials.

A family of distortion curves for another transformer type illustrates this behavior, shown in Figure 6-60 below. This series of plots is for a Lundahl LL1517 silicon iron C core unit, with successive output levels of 0.5, 1, 2 and 5Vrms into a 600Ω load. Individual device samples will vary, but the general pattern is typical of many audio transformers.

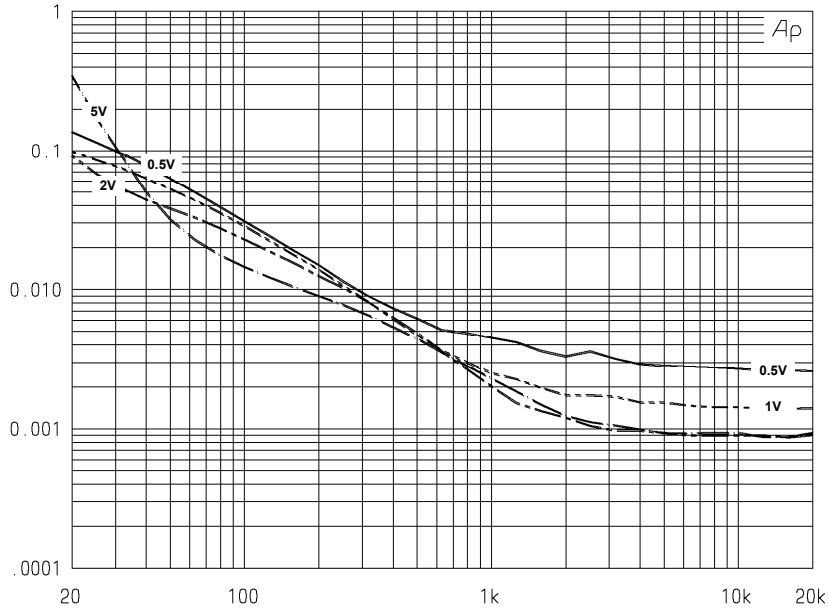


Figure 6-60: *Lundahl LL1517 transformer and driver (without feedback), THD+N (%) vs. frequency (Hz), for V_{OUT} = 0.5, 1, 2, 5Vrms, R_L = 600Ω*

Werner Baudisch (see Reference 18) developed a very effective driver technique for minimization of transformer distortion. The technique involves the use of a drive amplifier, connected to the transformer primary in a direct manner. The amplifier uses conventional negative feedback for gain stabilization. In addition, a primary sensing resistance develops a voltage sample proportional to primary current, and the voltage thus derived is also fed back to the amplifier. This second feedback path is positive feedback, so the arrangement is also known as a *mixed feedback* driver (see Reference 19).

This very useful technique of the mixed feedback driver can be used to advantage to integrate a line driver with the transformer primary within a feedback loop, which cancels the bulk of the objectionable distortion. In practice, with careful driver adjustment it is possible to reduce the distortion of the transformer plus driver almost to *that of the driver stage, operating without the transformer*. The beauty of the principle is that the inherent

floating transformer operation is not lost, and is still effectively applied in a highly linear mode. Due to the action of the mixed feedback, the transformer primary resistance is effectively cancelled, thus appreciably lowering the net secondary output impedance.

The circuit of Figure 6-61 below is a basic, single-ended mixed feedback driver using either a Lundahl LL1582 or LL2811 transformer as T1, and an AD845 or an OP275 as the amplifier. These transformers have two 1:1 primaries, as well as two 1:1 secondaries. As used, both primaries are connected in series, and the T1 net voltage transfer is unity.

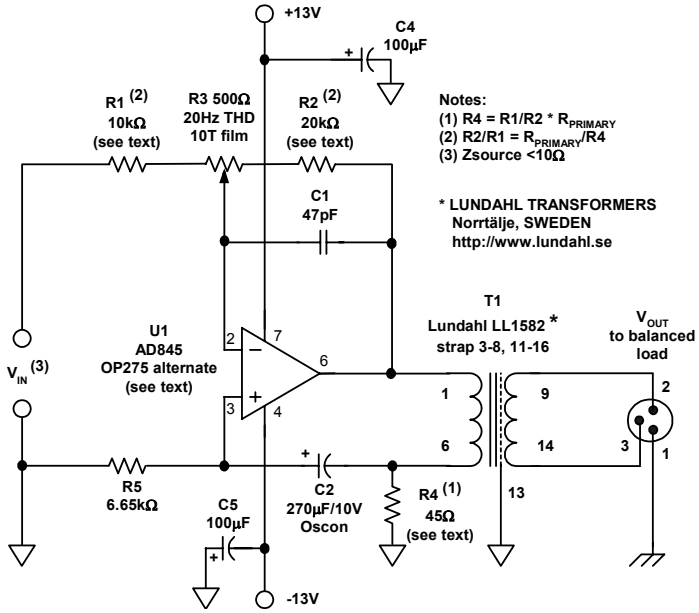


Figure 6-61: *A basic single-ended mixed feedback transformer driver*

To enable correct mixed feedback operation, two key ratios within the circuit must be set to match. One ratio is between the net T1 primary resistance, $R_{PRIMARY}$ and sample resistor R_4, and the other is R_2 and R_1. This relationship is:

$$R_{PRIMARY}/R_4 = R_2/R_1 \qquad \text{Eq. 6-18}$$

It is important to note that $R_{PRIMARY}$ is the total effective DC resistance of T1. As used here, two series 45Ω primaries are used, so $R_{PRIMARY}$ is 90Ω. Gain of the driver circuit is established as in a standard inverter, or the R_2-R_1 ratio. For a gain of 2x, R_2 is then simply 2 times R_1, i.e., 20kΩ and 10kΩ. R_4 may then be selected as:

$$R_4 = R_1/R_2 * R_{PRIMARY} \qquad \text{Eq. 6-19}$$

With the R_1/R_2 ratio of 0.5, this makes R_4 simply ½ $R_{PRIMARY}$, or in this case 45Ω.

Note the value of R_1 is critical, thus the V_{IN} source impedance must be low (<10Ω). This and other subtleties are effective performance keys. One is the sensitivity of the ratio match described by Eq. 6-18. Only when trimmed optimally will the lowest frequency THD be minimum. Thus a multi-turn film trimmer R_3 is used to trim out the various tolerances and the winding resistance of T1. Further, the positive feedback path is AC-coupled via C_2. This provision prevents DC latchup, should positive feedback override

the negative. However, a simple time constant of say, 8ms (corresponding to 20Hz) is *not sufficient* for lowest low frequency THD. To counteract this, the C_2-R_5 time constant is set quite long (≈1.8 seconds), which enable lowest possible 20Hz THD. With the suggested AD845 for U1, distortion is lowest, as it is also with an Oscon capacitor for C_2. A larger value ordinary aluminum electrolytic can also be used for C_2, with a penalty of somewhat high distortion. Alternately, an OP275 can also be used for U1 (see below).

With the AD845 FET input op amp used for U1, the maximum DC at the T1 primary is essentially the amplifier Vos times the stage's 3x noise gain, or ≤7.5mV. Since the AD845 can also dissipate ≈250mW, the lowest possible supplies help keep the offset change with temperature as low as possible.

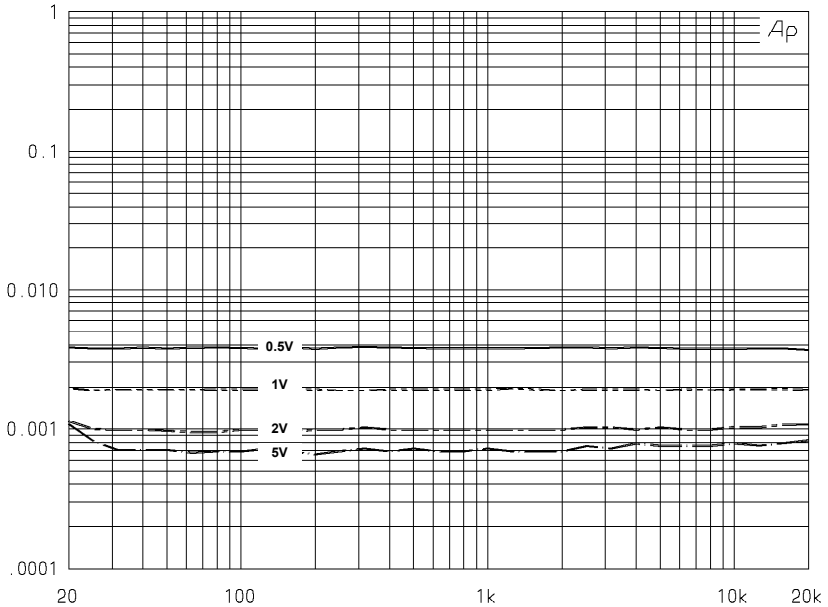


Figure 6-62: *Fig. 6-61 driver with Lundahl LL2811 transformer and AD845, THD+N (%) vs. frequency (Hz), for V_{OUT} = 0.5, 1, 2, 5Vrms, R_L = 600Ω*

Lab THD+N measurements of Fig. 6-61 were made using an LL2811, a transformer like the LL1582, but without a Faraday shield. The two transformers are very similar, but the LL1582 is recommended for single-ended drive circuits. The performance of this feedback driver is shown in Figure 6-62 above, for successive output levels of 0.5, 1, 2, and 5Vrms into a 600Ω load. Comparison of these data with Fig. 6-60 bears out the utility of the distortion reduction; it is decreased by orders of magnitude. More importantly, the level dependence with decreasing frequency is essentially eliminated.

These data do in fact represent almost an ideal THD+N pattern; the distortion level is flat with frequency, and it decreases with increasing output level. An extremely slight increase in THD+N can just be discerned at 20Hz in the 5V curve. The alternate OP275 for U1 also works well, but does have slightly higher distortion (not shown).

Although directly comparable data is not presented for it, it is worth noting that the LL1517 transformer can also be used with the Fig. 6-61 circuit, with R_4 = 9.2Ω, and the two primaries connected in series. However, some additional data on a circuit quite similar to Fig. 6-61 does reveal a potential limitation for this type of driver.

Figure 6-63 below shows a set of high level THD+N curves for a mixed feedback driver using an AD8610 op amp for U1, and the LL1517 transformer. Three THD+N sweeps are made, with the lowest THD+N curve representing the best possible null. The other two curves show increased THD+N at low frequencies, for conditions of R_2/R_1 ratio mismatches of 1 and 5%, respectively. This demonstrates how critical a proper null is towards achieving the lowest possible distortion at the low end of the audio band.

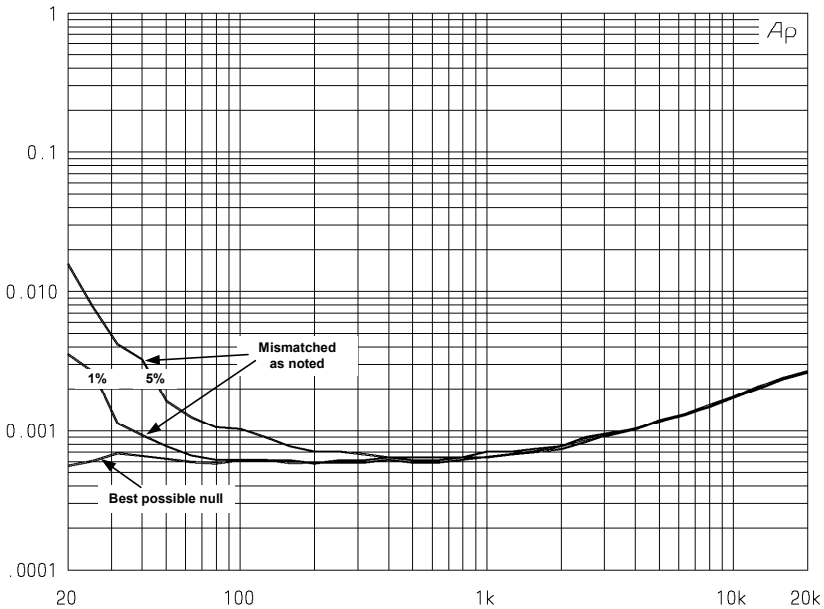


Figure 6-63: *Lundahl LL1517 transformer with mixed feedback AD8610 driver, THD+N (%) vs. frequency (Hz) for various null accuracies*

It is possible to tweak the ratio via R_3 for an excellent 20Hz high level null at room temperature, and this is recommended to get the most from one of these circuits. But, it must also be remembered that the TC of the T1 copper windings is about 0.39%/°C. So, only a 10°C ambient temperature change would be sufficient to degrade the best null by nearly 5%. The resulting performance would then roughly represent the upper curve of Fig. 6-63— still quite good, but just not quite as good as possible in absolute terms.

For the best and most consistent performance, wide temperature range applications of this type of circuit should therefore employ some means of temperature compensation for the copper winding(s) of T1. One means of achieving this would be to employ a thermally sensitive device to track the copper TC of T1. The net goal should be to hold the $R_{PRIMARY}/R_4$ ratio constant over temperature. It should also be noted that for this approach to work, it is assumed that the R_2/R_1 ratio is temperature independent. This is possible with the use of close tolerance, low TC metal film resistors, i.e., 50ppm/°C or better (or the use of a low tracking TC network).

It should also be noted that the *output balance* of an audio transformer is a very important factor when designing audio line drivers. Poor transformer balance can lead to mode conversion of CM signals on the output line (see Reference 20). The result is that a spurious differential mode signal can be created due to poor balance. A transformer can attain good balance (i.e., 60dB or better) by the use of sophisticated winding techniques, or the use of a Faraday shield, as is true in the case of the LL1582 and the LL1517.

Transformer drivers can of course also be operated in a balanced drive fashion. This has the advantage of doubling the available drive voltage for given supply voltages, plus lowering the distortion produced. Mixed feedback principles can be extended to a balanced arrangement, which lowers the distortion in the same manner as for the single-ended circuit just described. An example circuit is shown in Figure 6-64, below.

In Fig. 6-64, a U1-U2 low distortion op amp pair drive an LL1517 transformer. U1 is an inverting gain circuit as defined by gain resistors R_1-R_2, which drives the top of T1. Placed in series with the T1 primary, R_3 acts as a current sampling resistor, and develops a correction voltage to drive the second inverter, U2, through R_4.

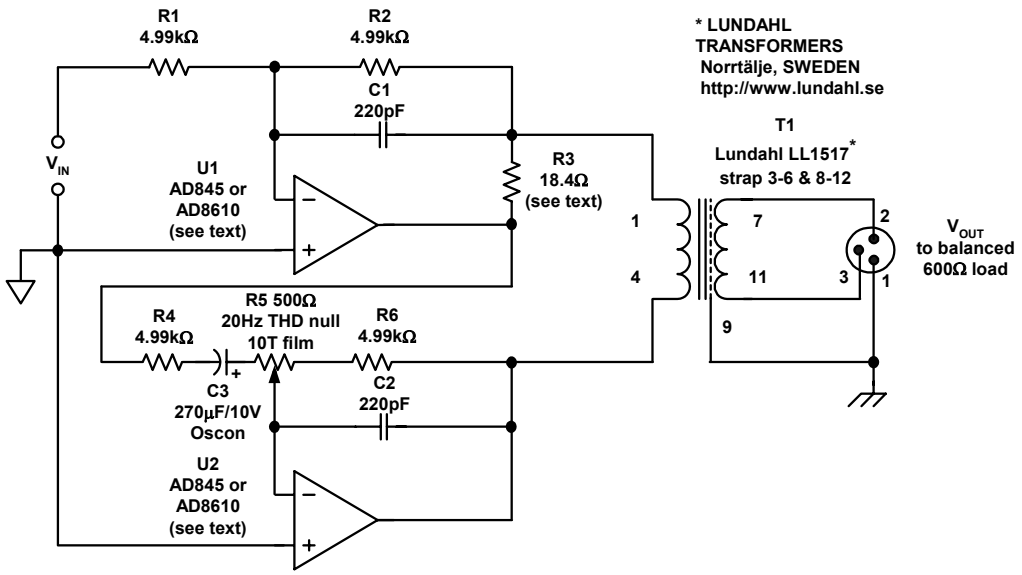


Figure 6-64: *A balanced transformer driver circuit that applies mixed feedback principles of distortion minimization*

This scheme is adapted from the mixed feedback balanced driver circuit of Arne Offenberg (see Reference 21). There are however two main differences in this version. One is operation of the U1 stage as an inverter, which eliminates any CM distortion effects in U1, and the second being the ability to easily set the overall driver gain via R_1-R_2. Within this circuit, it should be noted that the resistances R_1-R_2 do *not* affect the distortion null (as they do in the simpler circuit of Fig. 6-61).

The distortion null in this form of the circuit occurs when the ratios $R_3/R_{PRIMARY}$ and R_4/R_6 match. For simplicity, the second inverter gain is set to unity, so R_3 is selected as:

$$R_3 = R_4 / R_6 * R_{PRIMARY} \qquad \text{Eq. 6-20}$$

For the R_4-R_6 values shown, R_3 then is simply equal to $R_{PRIMARY}$, or 18.4Ω when used with the LL1517 transformer with series connected primaries.

As with any of these driver circuits, the exact op amp selection has a great bearing on final performance. Within a circuit using two amplifiers, dual devices are obviously attractive. The distortion testing below discusses amplifier options.

THD+N performance data for the balanced transformer driver of Fig. 6-64 is shown in Figure 6-65 below, using an LL1517 transformer with successive output levels of 0.5, 1, 2, and 5Vrms into a 600Ω load. For these tests, the supply voltages were ±13V, and the U1-U2 op amp test devices were pairs of either the AD8610 or the AD845 (note— two AD8610 singles are comparable to a single AD8620 dual).

An interesting thing about these plots are the fact that the THD+N is both low and essentially unchanged with frequency, which is again, near ideal. Low frequency nulling of the distortion is almost as critical in this circuit as in the previous, and a slight upturn in THD+N can be seen at 20Hz, for the highest level (5V).

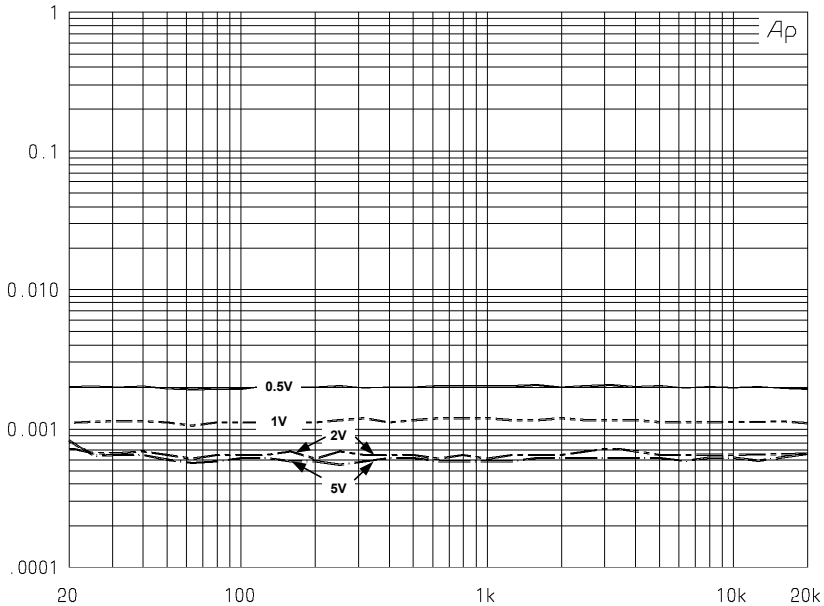


Figure 6-65: *Fig. 6-64 balanced driver with Lundahl LL1517 transformer and two AD8610s, THD+N (%) vs. frequency (Hz), for V_{OUT} = 0.5, 1, 2, 5Vrms, R_L = 600Ω*

For the AD8610 devices shown by these data, the wideband THD+N was slightly lower than a comparable test with the AD845 pair (the latter not shown). Both amplifier sets show essentially flat THD+N vs. frequency characteristics.

Because of the balanced drive nature of this circuit, the realization offers lower distortion than the simpler single-ended version of Fig. 6-61, plus a buffering of the distortion null sensitivity against the input source impedance and gain adjustment. It can thus be considered a more robust method of transformer distortion minimization. For these reasons, the balanced form of driver is recommended for professional or other high performance requirements. Note however that similar caveats do apply with regard to stabilizing the distortion null against temperature.

This driver can be used with the LL1517 and many other transformers, with of course an appropriate choice of R_3. Note that the performance data above reflects use of the op amps operating unbuffered. For very low impedance loads and/or long lines, a pair of the previously described unity gain buffers should be considered, and both the U1 and U2 stages operated with output buffering. This will allow the retention of THD+N performance as is shown in Fig. 6-65 above, but in the face of more difficult loads.

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ACKNOWLEDGEMENTS:

Portions of this section were adapted from Walt Jung, "Audio Preamplifiers, Line Drivers, and Line Receivers," within Chapter 8 of Walt Kester, **System Application Guide**, Analog Devices, Inc., 1993, ISBN 0-916550-13-3, pp. 8-1 to 8-100.

During the preparation of this material the author received much appreciated helpful comments and other inputs from Per Lundahl of Lundahl Transformers, and from Arne Offenberg of Norway.

SECTION 6-2: BUFFER AMPLIFIERS AND DRIVING CAPACITIVE LOADS

Walt Jung, Walt Kester

Buffer Amplifiers

In the early days of high speed circuits, simple emitter followers were often used as high speed buffers. The term *buffer* was generally accepted to mean a unity-gain, open-loop amplifier. With the availability of matching PNP transistors, a simple emitter follower can be improved, as shown below in Figure 6-66A. This complementary circuit offers first-order cancellation of DC offset voltage, and can achieve bandwidths greater than 100MHz. Typical offset voltages without trimming are usually less than 50mV, even with unmatched discrete transistors. The HOS-100 hybrid amplifier from Analog Devices represented an early implementation of this circuit. This device was a popular building block in early high speed ADCs, DACs, sample-and-holds, and multiplexers.

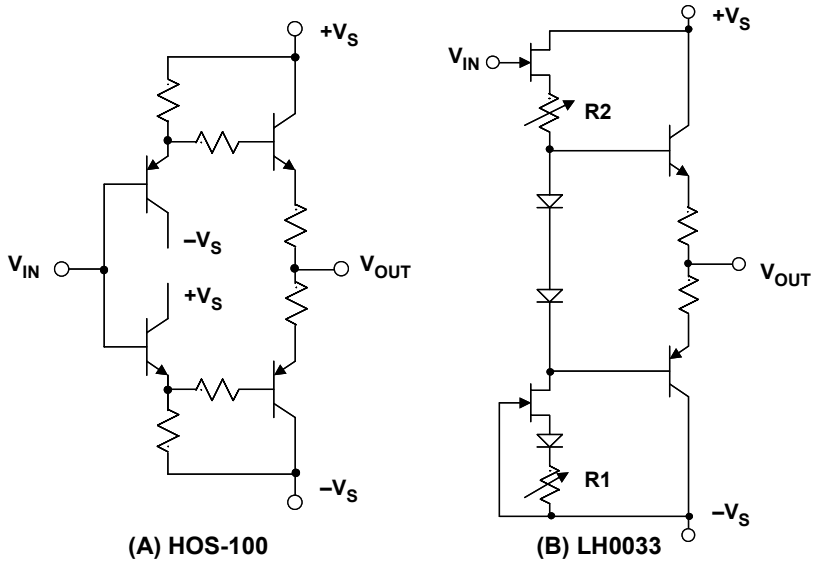


Figure 6-66: *Early open-loop hybrid buffer amplifiers: (A) HOS-100 bipolar, (B) LH0033 FET input*

If high input impedance is required, a dual FET can be used as an input stage ahead of a complementary emitter follower, as shown in Figure 6-66B. This form of the buffer circuit was implemented by both National Semiconductor Corporation as the LH0033, and by Analog Devices as the ADLH0033.

In the realizations of these hybrid devices, thick film resistors were laser trimmed to minimize input offset voltage. For example, in the Fig. 6-66(B) circuit, R1 is first trimmed to set the bias current in the dual matched FET pair, which is from the 2N5911 series of parts. R2 is then trimmed to minimize the buffer input-to-output offset voltage.

Circuits such as these achieved bandwidths of about 100MHz at fairly respectable levels of harmonic distortion, typically better than –60dBc. However, they suffered from DC and AC nonlinearities when driving loads less than 500Ω.

One of the first totally monolithic implementations of these functions was the Precision Monolithics, Inc. BUF03 shown below in Figure 6-67 (see Reference 1). PMI is now a division of Analog Devices. This open-loop IC buffer achieved a bandwidth of about 50MHz for a 2V peak-to-peak signal.

The BUF03 circuit is interesting because it demonstrates techniques that eliminated the requirement for the slow, bandwidth-limited vertical PNP transistors associated with most IC processes available at the time of the design (approximately 1979).

Within the circuit, input transistor J1 is a FET source follower that is biased by an identical FET J2, thereby making the gate-to-source voltage of J1 nominally zero. The output of J1 is applied to emitter follower Q1, and diodes Q5 and Q6 compensate for the combined base-emitter drops of Q1 and Q7/Q9.

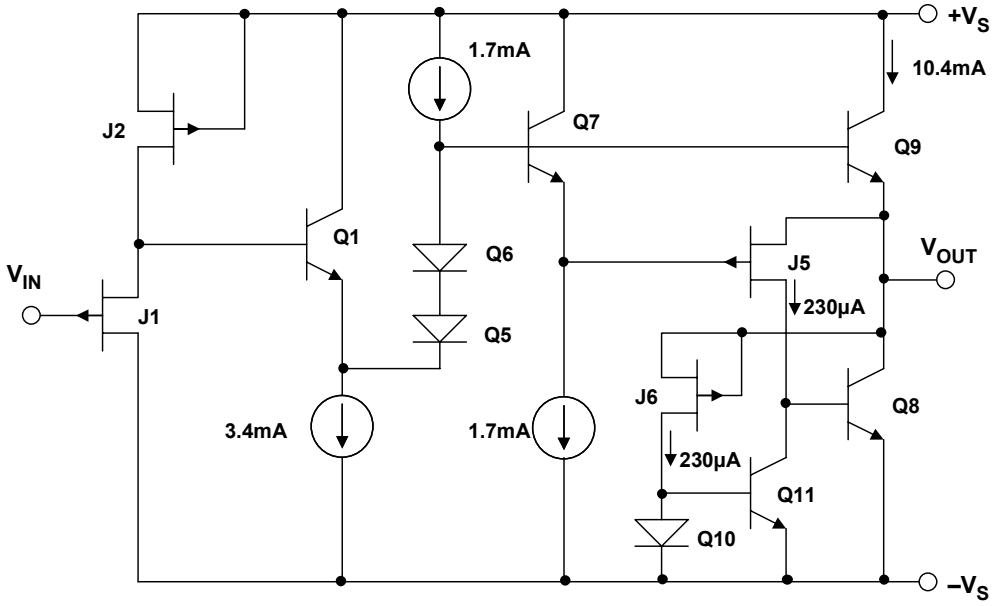


Figure 6-67: *BUF03 monolithic open-loop buffer 1979 vintage*

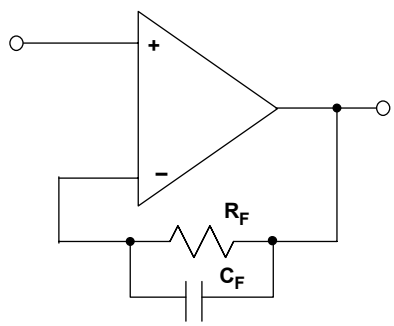
The current through Q7 is held at a constant 1.7mA, therefore its V_{BE} is constant. Transistors Q7 and Q9 are scaled such that the current in Q9 is six times that of Q7 for equal V_{BE} drops. If the load current changes, and Q9 is required to source more or less current, its V_{BE} attempts to increase or decrease. This change is applied between the gate and source of J5, which then reduces/increases current in the base of Q8 to maintain the current in Q9 at six times that of Q7. The localized feedback works for load currents up to ±10mA. The current in Q9 is therefore held constant at 10.4mA (independent of load) because its V_{BE} drop does not change with either output voltage or load current.

With a 1kΩ load, and an output voltage of +10V, transistor Q8 must sink 0.2mA, and Q9 supplies 10mA to the load, 0.2mA to J5, and 0.2mA to J6. For an output of –10V, Q8

must sink 20.2mA so that the net current delivered to the load is −10mA. In addition to achieving a bandwidth of approximately 50MHz (2V peak-to-peak output), on-chip zener-zap trimming was used to achieve a DC offset of typically less than 6mV.

One of the problems with all the open-loop buffers discussed thus far is that although high bandwidths can be achieved, the devices discussed don't take advantage of negative feedback. Distortion and DC performance suffer considerably when open-loop buffers are loaded with typical video impedance levels of 50, 75, or 100Ω. The solution is to use a properly compensated wide bandwidth op amp in a unity-gain follower configuration. In the early days of monolithic op amps, process limitations prevented this, so the open-loop approach provided a popular interim solution.

Today, however, practically all unity-gain-stable voltage or current feedback op amps can be used in a simple follower configuration. Usually, however, the general-purpose op amps are compensated to operate over a wide range of gains and feedback conditions. Therefore, bandwidth suffers somewhat at low gains, especially in the unity-gain non-inverting mode, and additional external compensation is usually required.



AD9620	AD9630	BUF04
Voltage Feedback	Voltage Feedback	Current Feedback
G = 1	G = 1	G = 1
BW = 650MHz	BW = 750MHz	BW = 110MHz
V_S = ±5V	V_S = ±5V	V_S = ±5 to ±15V
1990		1994

Figure 6-68: *Early closed-loop unity-gain monolithic buffers*

A practical solution is to compensate the op amp for the desired closed-loop gain, while including the gain setting resistors on-chip, as shown in Figure 6-68 above. Note that this form of op amp, internally configured as a buffer, may typically have no feedback pin. Also, putting the resistors and compensation on-chip also serves to reduce parasitics.

There are a number of op amps optimized in this manner. Roy Gosser's AD9620 (see Reference 2) was probably the earliest monolithic implementation. The AD9620 was a 1990 product release, and achieved a bandwidth of 600MHz using ±5V supplies. It was optimized for unity gain, and used the voltage feedback architecture. A newer design based on similar techniques is the AD9630, which achieves a 750MHz bandwidth.

The BUF04 unity gain buffer (see Reference 3) was released in 1994 and achieves a bandwidth of 120MHz. This device was optimized for large signals and operates on

supplies from ±5V to ±15V. Because of the wide supply range, the BUF04 is useful not only as a standalone unit-gain buffer, but also within a feedback loop with a standard op amp, to boost output (see discussions within "Audio Amplifiers" portion of this chapter).

Closed-loop buffers with a gain of two find wide applications as transmission line drivers, as shown below in Figure 6-69. The internally configured fixed gain of the amplifier compensates for the loss incurred by the source and load termination. Impedances of 50, 75, and 100Ω are popular cable impedances. The AD8074/AD8075 500MHz triple buffers are optimized for gains of 1 and 2, respectively. The dual AD8079A/AD8079B 260MHz buffer is optimized for gains of 2 and 2.2, respectively.

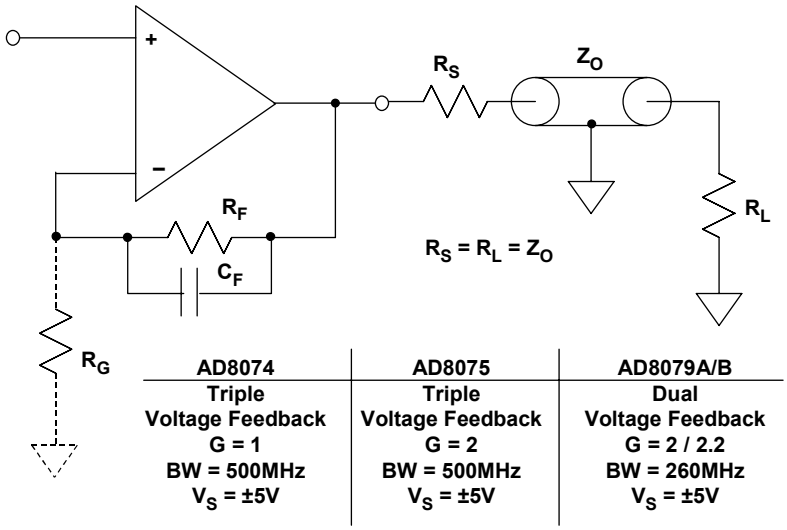


Figure 6-69: *Fixed-gain video transmission line drivers*

The buffer amplifiers discussed above are all dedicated to either unity or some higher fixed gain setting. As wide bandwidth fixed gain blocks they are simply applied, without the need for additional gain configuration components. They will of course (as with any high-speed amplifier) require supply bypassing components, as well as appropriate layout.

Buffers can also be implemented with almost any unity-gain-stable voltage or current feedback op amp. Examples that come to mind for voltage feedback devices are the single AD817 (or the dual counterpart AD826), or for current feedback devices the AD811, AD8001, AD8015, along with their dual-device cousins (as is applicable). In addition, there are op amps with feature rail-rail outputs as well as operation at low supply voltages— the AD8031/32 and AD8041/42 are examples.

In implementing a high-speed unity-gain buffer with a voltage feedback op amp, there will typically be no resistor required in the feedback loop, which considerably simplifies the circuit. Note that this isn't a 100% hard-and-fast rule however, so always check the device data sheet to be sure. A unity-gain buffer with a current feedback op amp will *always* require a feedback resistor, typically in the range of 500-1000Ω. So, be sure to use a value appropriate to not only the basic part, but also the specific power supplies in use.

Driving Capacitive Loads

From either a system or signal fidelity point of view, transmission line coupling between stages is best, and is described in some detail in the next section. However, complete transmission line system design may not always be possible or practical. In addition, various other parasitic issues need careful consideration in high performance designs. One such problem parasitic is amplifier *load capacitance*, which potentially comes into play for all wide bandwidth situations that do not use transmission line signal coupling.

A general design rule for wideband linear drivers is that capacitive loading (cap loading) effects should *always* be considered. This is because PC board capacitance can build up quickly, especially for wide and long signal runs over ground planes insulated by a thin, higher K dielectric. For example, a 0.025" PC trace using a G-10 dielectric of 0.03" over a ground plane will run about 22pF/foot (see References 4 and 5). Even relatively small load capacitance (i.e., <100pF) can be troublesome, since while not causing outright oscillation, it can still stretch amplifier settling time to greater than desirable levels for a given accuracy.

The effects of cap loading on high speed amplifier outputs are not simply detrimental, they are actually an anathema to high quality signals. However, before-the-fact designer knowledge still allows high circuit performance by employing various tricks of the trade to combat the capacitive loading. If it is not driven via a transmission line, remote signal circuitry should be checked for capacitive loading very carefully, and characterized as best possible. Drivers which face poorly defined load capacitance should be bulletproofed accordingly with an appropriate design technique from the options list below.

Short of a true matched transmission line system, a number of ways exist to drive a load that is capacitive in nature, while still maintaining amplifier stability.

Custom capacitive load (cap load) compensation includes two possible options, namely a); overcompensation, and b); an intentionally forced-high loop noise gain allowing crossover in a stable region. Both of these steps can be effective in special situations, as they reduce the amplifier's effective closed loop bandwidth, so as to restore stability in the presence of cap loading.

Overcompensation of the amplifier, when possible, reduces amplifier bandwidth so that the additional load capacitance no longer represents a danger to phase margin. As a practical matter however, amplifier compensation nodes to allow this are available on very few of the newer high speed amplifiers.

Nevertheless, there are still useful examples, and one is the AD829, compensated by a single capacitor to AC-common, at pin 5. A more recent and analogous part is the AD8021, which is compensated similarly. In general, almost any amplifier using external compensation can always be over compensated to reduce bandwidth. This will restore stability against cap loads, by lowering the amplifier’s unity gain frequency.

Forcing a high noise gain is shown in Figure 6-70 below, where the left side capacitively loaded amplifier with a noise gain of unity is unstable, due to a 1/β - open loop rolloff intersection on the Bode diagram in a –12dB/octave rolloff region. For such a case, introducing higher noise gain can restore often stability, so that the critical intersection occurs in a stable –6dB/octave region, as depicted at the right diagram and Bode plot.

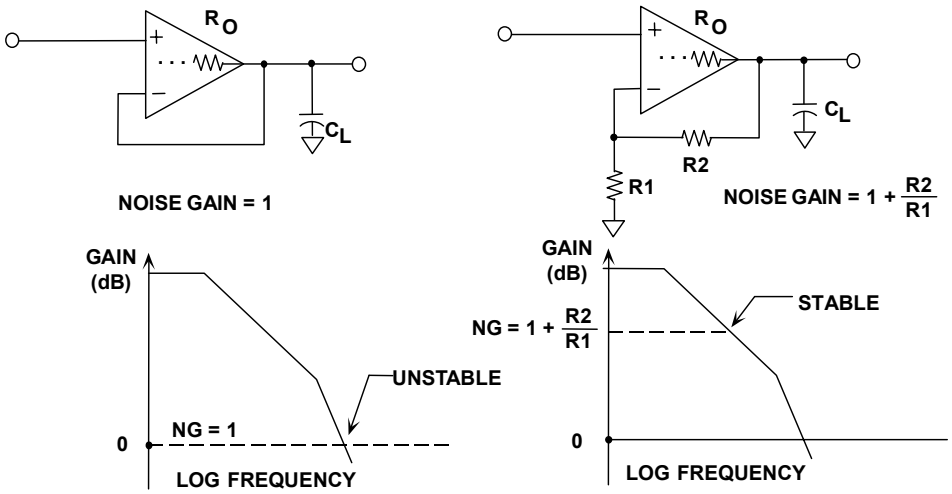


Figure 6-70: *Effect of capacitive loading on op amp stability*

To enable a higher noise gain (which does not necessarily need to be the same as the stage's *signal gain*), use is made of resistive or RC pads at the amplifier input, as in Figure 6-71 below. This trick is broader in scope than overcompensation, and has the advantage of not requiring access to any internal amplifier nodes. This generally allows use with any amplifier setup, even voltage followers (left) or inverters (right). An extra resistor R_D, is added which works against R_F to force the noise gain of the stage to a level appreciably higher than the signal gain (unity for both cases here).

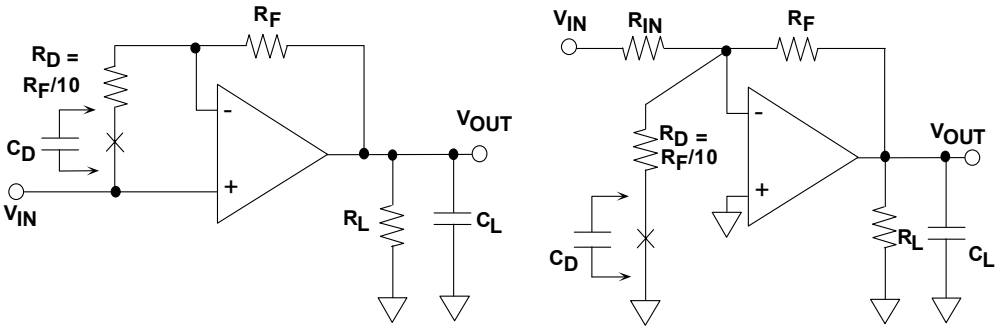


Figure 6-71: *Raising noise gain (DC or AC) for follower (A) or inverter (B) stability*

Assuming C_L is a value that produces a parasitic pole slightly above or near the amplifier's natural crossover, this loading combination would lead to oscillation due to the excessive phase lag. However with R_D connected, the forced higher amplifier noise gain produces a new 1/β and open loop rolloff intersection, purposely set about a decade lower in frequency. This is low enough that the extra phase lag from C_L near the amplifier's natural unity-gain crossover is no longer a problem, and stability is restored.

A drawback to this trick is that both the DC offset and input noise of the amplifier are raised by the value of the noise gain, when R_D is DC-connected. But, when C_D is used in series with R_D, the offset voltage of the amplifier is not raised, and the gained-up AC noise components are confined to a frequency region above $1/(2\pi \cdot R_D \cdot C_D)$. A further caution is that this technique can be somewhat tricky when separating these operating DC and AC regions, and should be applied carefully with regard to settling time (see Reference 6). Note that these simplified examples are generic, and in practice the absolute component values should be matched to a specific amplifier.

"Passive" cap load compensation, shown in Figure 6-72 below, is the most simple (and most popular) isolation technique available. It uses a simple "out-of-the-loop" series resistor R_X to isolate the cap load, and can be used with any amplifier, current or voltage feedback, FET or bipolar input.

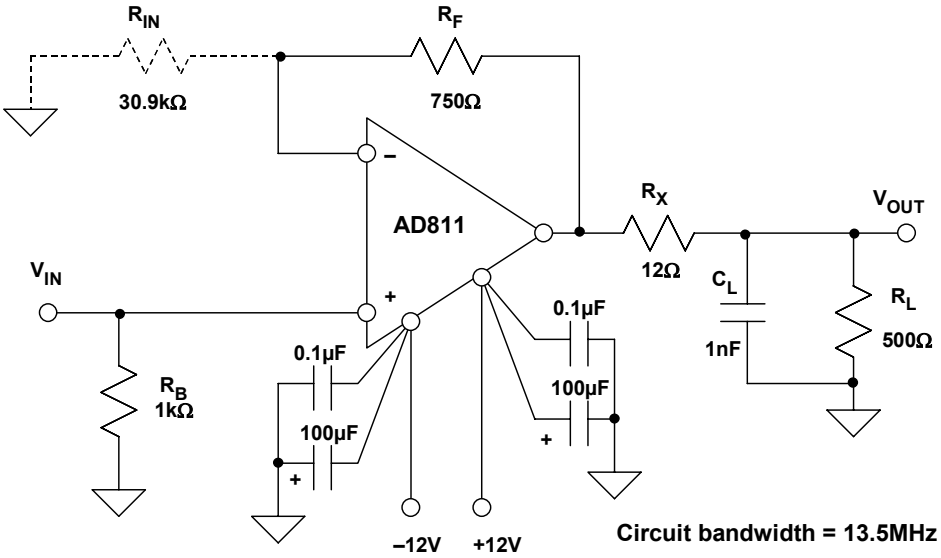


Figure 6-72: *Open-loop series resistance isolates capacitive load*

As noted, since this technique applies to just about any amplifier, this is a major reason why it is so useful. It is shown here with a current feedback amplifier suitable for high current line driving, the AD811, and it consists of just the simple (passive) series isolation resistor, R_X. This resistor's minimum value for stability will vary from device to device, so the amplifier data sheet should be consulted for other ICs. Generally, information will be provided as to the amount of load capacitance tolerated, and a suggested minimum resistor value for stability purposes.

Drawbacks of this approach are the loss of bandwidth as R_X works against C_L, the loss of voltage swing, a possible lower slew rate limit due to I_{MAX} and C_L, and a gain error due to the R_X-R_L division. The gain error can be optionally compensated with R_{IN}, which is ratioed to R_F as R_L is to R_X. In this example, a ±100mA output from the op amp into C_L can slew V_{OUT} at a rate of 100V/µs, far below the intrinsic AD811 slew rate of 2500V/µs. Although the drawbacks are serious, this form of cap load compensation is nevertheless useful because of its simplicity. If the amplifier isn't otherwise protected, then an R_X resistor of 50-100Ω should be used with virtually any amplifier facing capacitive loading. Although a non-inverting amplifier is shown, the technique applies equally to inverters.

With very high speed amplifiers, or in applications where lowest settling time is critical, even small values of load capacitance can be disruptive to frequency response, but are nevertheless sometimes inescapable. One case in point is an amplifier used for driving ADC inputs. Since high speed ADC inputs quite often look capacitive in nature, this presents an oil/water type problem. In such cases the amplifier *must* be stable driving the capacitance, but it must also preserve its best bandwidth and settling time characteristics. To address this cap load case, R_S and C_L data for a specified settling time is appropriate.

Some applications, in particular those that require driving the relatively high impedance of an ADC, do not have a convenient back termination resistor to dampen the effects of capacitive loading. At high frequencies, an amplifier's output impedance is rising with frequency and acts like an inductance, which in combination with C_L causes peaking or even worse, oscillation. When the bandwidth of an amplifier is an appreciable percentage of device F_t, the situation is complicated by the fact that the loading effects are reflected back into its internal stages. In spite of this, the basic behavior of most very wide bandwidth amplifiers such as the AD8001 is very similar.

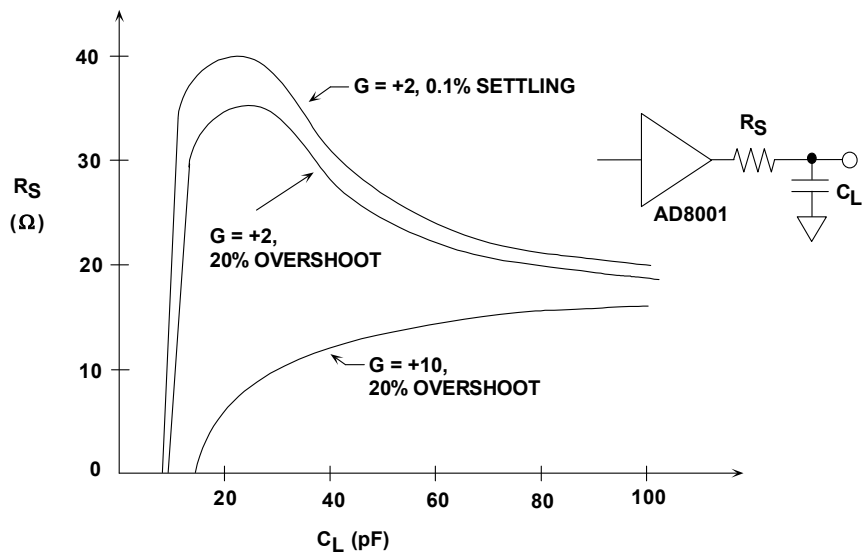


Figure 6-73: *AD8001 R_S required for various C_L values*

In general, a small damping resistor (R_S) placed in series with C_L will help restore the desired response (see Figure 6-73 above). The best choice for this resistor's value will depend upon the criterion used in determining the desired response. Traditionally, simply stability or an acceptable amount of peaking has been used, but a more strict measure such as 0.1% (or even 0.01%) settling will yield different values. For a given amplifier, a family of R_S-C_L curves exists, such as those of Fig. 6-73. These data will aid in selecting R_S for a given application.

The basic shape of this curve can be easily explained. When C_L is very small, no resistor is necessary. When C_L increases to some threshold value an R_S becomes necessary. Since the frequency at which the damping is required is related to the $R_S \bullet C_L$ time constant, the R_S needed will initially increase rapidly from zero, and then will decrease as C_L is increased further. A relatively strict requirement, such as for 0.1%, settling will generally require a larger R_S for a given C_L, giving a curve falling higher (in terms of R_S) than that

for a less stringent requirement, such as 20% overshoot. For the common gain configuration of +2, these two curves are plotted in the figure for 0.1% settling (upper-most curve) and 20% overshoot (middle curve). It is also worth mentioning that higher closed loop gains lessen the problem dramatically, and will require less R_S for the same performance. The third (lower-most) curve illustrates this, demonstrating a closed loop gain of 10 R_S requirement for 20% overshoot for the AD8001 amplifier. This can be related to the earlier discussion associated with Figure 6-70.

The recommended values for R_S will optimize response, but it is important to note that generally C_L will degrade the maximum bandwidth and settling time performance which is achievable. In the limit, a large $R_S \bullet C_L$ time constant will dominate the response. In any given application, the value for R_S should be taken as a starting point in an optimization process which accounts for board parasitics and other secondary effects.

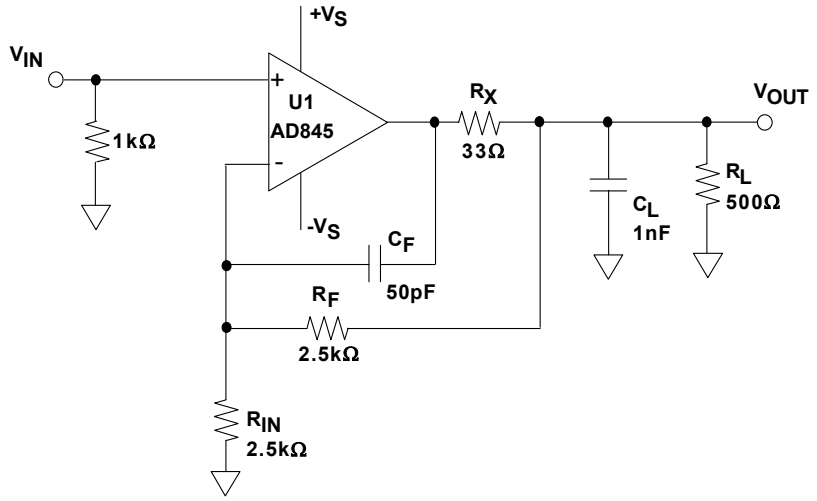


Figure 6-74: *Active "in-the-loop" capacitive load compensation corrects for DC and LF gain errors*

Active or "in-the-loop" cap load compensation can also be used as shown above in Figure 6-74, and this scheme modifies the passive configuration, providing feedback correction for the DC and low frequency gain error associated with R_X. In contrast to the passive form, active compensation can only be used with voltage feedback amplifiers, because current feedback amplifiers do not allow the integrating connection of C_F.

This circuit returns the DC feedback from the output side of isolation resistor R_X, thus correcting for errors. AC feedback is returned via C_F, which bypasses R_X/R_F at high frequencies. With an appropriate value of C_F (which varies with C_L, for fixed resistances) this stage can be adjusted for a well damped transient response (see References 6 and 7). There is still a bandwidth reduction, a headroom loss, and also (usually) a slew rate reduction, but the DC errors can be very low. A drawback is the need to tune C_F to C_L, as even if this is done well initially, any change to C_L will alter the response away from flat. The circuit as shown is useful for voltage feedback amplifiers only, because capacitor C_F provides integration around U1. It also can be implemented in inverting fashion, by driving the bottom end of R_{IN}, while grounding the op amp (+) input.

Internal cap load compensation involves the use of an amplifier that has topological provisions for the effects of external cap loading. To the user, this is the most transparent of the various techniques, as it works for any feedback situation, for any value of load capacitance. Drawbacks are that it produces higher distortion than does an otherwise similar amplifier without the network, and the compensation against cap loading is somewhat signal level dependent.

The internal cap load compensated amplifier sounds at first like the best of all possible worlds, since the user need do nothing at all to set it up. Figure 6-75 below is a simplified diagram of an AD817 amplifier with internal cap load compensation. The cap load compensation is the C_F-resistor network, which is highlighted by the dotted area within the unity gain output stage of the amplifier. It is important to note at this point that *this RC network only makes its presence felt for certain load conditions*.

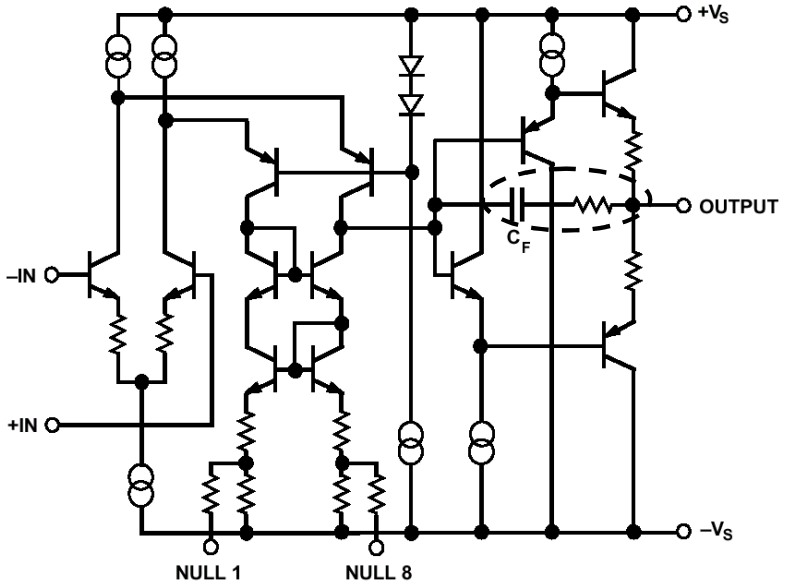


Figure 6-75: *AD817 simplified schematic illustrates internal compensation for driving capacitive loads*

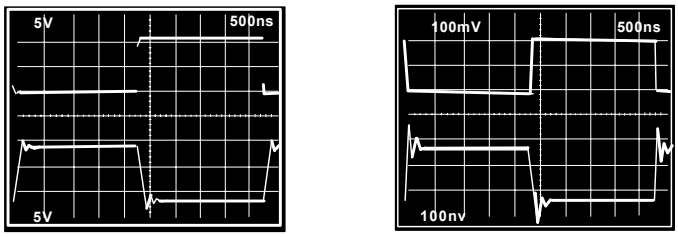
Under normal (non-capacitive or light resistive) loading, there is limited input/output voltage error across the output stage, so the C_F network then sees a relatively small voltage drop, and has little or no effect on the AD817's high impedance compensation node. However when a capacitor (or other heavy) load is present, the high currents in the output stage produce a voltage difference across the C_F network, which effectively adds capacitance to the compensation node. With this relatively heavy loading, a net larger compensation capacitance results, and reduces the amplifier speed in a manner that is adaptive to the external capacitance, C_L. *As a point of reference, note that it requires 6.3mA peak current to support a 2Vp-p swing across a 100pF load at 10MHz.*

Since this mechanism is resident in the amplifier output stage and it affects the overall compensation characteristics dynamically, it acts independent of the specific external feedback hookup, as well as the external capacitor's size. In other words, it can be transparent to the user in the sense that no specific design conditions need be set to make

it work (other than selecting the right IC). Some amplifiers using internal cap load compensation are the AD817, the AD847, and their dual equivalents, AD826 and AD827.

There are, however, some caveats also associated with this internal compensation scheme. As with the passive compensation techniques, bandwidth decreases as the device slows down to prevent oscillation with higher load currents. Also, this adaptive compensation network has its greatest effect when enough output current flows to produce significant voltage drop across the C_F network. Conversely, at small signal levels, the effect of the network on speed is less, so greater ringing may actually be possible for some circuits, with lower-level outputs.

Vertical Scale: 5V/div **Vertical Scale: 100mV/div**



Horizontal Scale: 500ns/div

Figure 6-76: *Response of internal cap load compensated amplifier varies with signal level*

The dynamic nature of this internal cap load compensation is illustrated in Figure 6-76, which shows an AD817 unity gain inverter being exercised at both high (left) and low (right) output levels, with common conditions of $V_S = \pm 15V$, $R_L = 1k\Omega$, $C_L = 1nF$, and using 1kΩ input/feedback resistors. In both photos the input signal is on the top trace and the output signal is on the bottom trace, and the time scale is fixed.

In the 10Vp-p output left photo, the output has slowed down appreciably to accommodate the capacitive load, but settling is still relatively clean, with a small percentage of overshoot. For this high level case, the bandwidth reduction due to C_L is most effective. In the right photo, the 200mVp-p output shows greater overshoot and ringing, for the lower level signal. The point is that the performance of the cap load compensated amplifier is signal dependent, but is always stable with any cap load.

Finally, because the circuit is based on a nonlinear principle, the internal network affects distortion performance and load drive ability, and these factors influence amplifier performance in video applications. Though the network's presence does not by any means make devices like the AD817 or AD847 unusable for video, it does not permit the very lowest levels of distortion and differential gain and phase which are achievable with amplifiers without this network, but otherwise comparable.

While the individual techniques for countering cap loading outlined above have various specific tradeoffs as noted, all of the techniques have a common drawback of reducing speed (both bandwidth and slew rate). If these parameters cannot be sacrificed, then a

matched transmission line system is the solution, and is discussed in more detail later, in the "Video Amplifiers" portion of this chapter.

As for choosing among the cap load compensation schemes, it would seem on the surface that amplifiers using the internal form offer the best possible solution to the problem— just pick the right amplifier and simply forget about it. And indeed, that would seem the "panacea" solution for all cap load situations— if you use the "right" amplifier you never need to think about cap loading again. Could there be more to it?

Yes! The "gotcha" of internal cap load compensation is subtle, and lies in the fact that the dynamic adaptive nature of the compensation mechanism actually can produce higher levels of distortion, vis-à-vis an otherwise similar amplifier, *without* the C_F -resistor network. Like the old saying about no free lunches, if you care about attaining top-notch levels of high frequency AC performance, you should give the issue of whether to use an internally compensated cap load amplifier more serious thought than simply picking a trendy device. For example, the AD818, which is a gain-of-two stable video op amp, offers excellent performance in terms of video gain and phase measurements. It is simply a gain-of-two stable AD817 op amp, but without the internal cap load compensation network. For similar video stage driver applications, the AD817 will not perform as well as the more suitable AD818.

On the other hand, if you have no requirements for the lowest levels of distortion, then such an amplifier as the AD817 could be a very good choice. Such amplifiers are certainly easier to use, and are relatively forgiving about output loading issues.

REFERENCES: BUFFERS AND DRIVING CAP LOADS

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7. Walt Jung, "Op Amps in Line-Driver and Receiver Circuits, Part 1," **Analog Dialogue**, Vol. 26-2, 1992.

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NOTES:

SECTION 6-3: VIDEO AMPLIFIERS

Walt Kester

Video Signals and Specifications

Before discussing some video applications for op amps, we will review some basics regarding video signals and specifications. The standard video format is the specification of how the video signal looks from an electrical point of view. Light strikes the surface of an image sensing device within the camera, producing a voltage level corresponding to the amount of light hitting a particular spatial region of the surface. This information is then placed into the standard format and sequenced out of the camera. Along with the actual light and color information, synchronization pulses are added to the signal to allow the receiving device— a television monitor, for instance— to identify where the sequence is in the frame data.

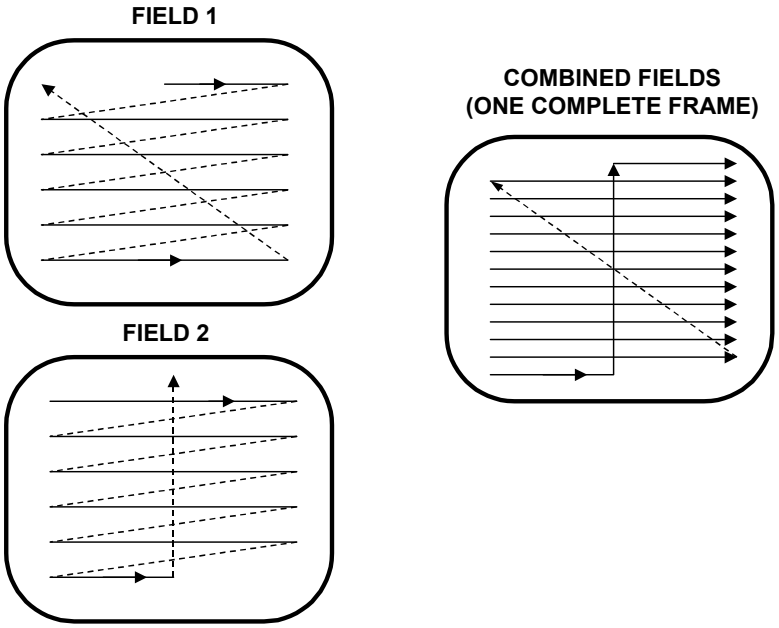


Figure 6-77: *Standard broadcast television interlace format*

A standard video format image is read out on a line-by-line basis from left to right, top to bottom. A technique called *interlacing* refers to the reading of all even numbered lines, top to bottom, followed by all odd lines as shown in Figure 6-77 above.

The television picture *frame* is thus divided into even and odd *fields*. Interlacing is used to produce an apparent update of the entire frame in half the time that a full update actually occurs. This results in a television image with less apparent flicker. Typical broadcast television frame update rates are 30 and 25Hz, depending upon the line frequency. It should be noted that interlacing is not always required in graphics display systems where the refresh rate is usually greater (typically 60Hz).

The original black and white, or *monochrome*, television specification in the USA is the EIA RS-170 specification that prescribes all timing and voltage level requirements for standard commercial broadcast video signals. The standard American specification for color signals, NTSC, modifies RS-170 to work with color signals by adding color information to the signal which otherwise contains only brightness information.

A video signal comprises a series of analog television lines. Each line is separated from the next by a synchronization pulse called the *horizontal sync*. The fields of the picture are separated by a longer synchronization pulse, called the *vertical sync*. In the case of a monitor receiving the signal, its electron beam scans the face of the display tube with the brightness of the beam controlled by the amplitude of the video signal. A single line of an NTSC color video signal is shown in Figure 6-78, below.

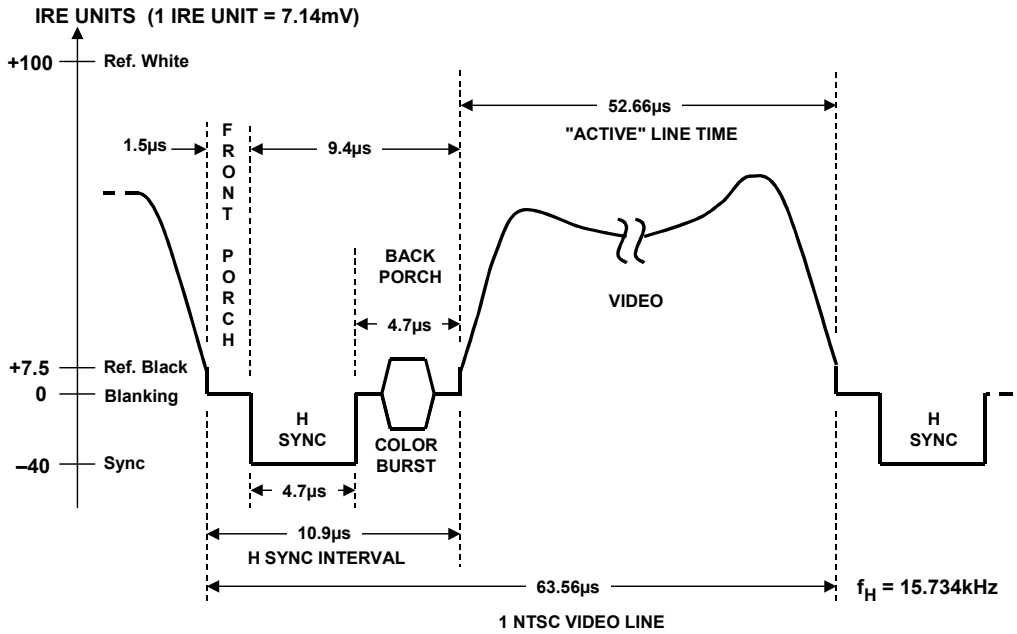


Figure 6-78: *NTSC composite color video line*

Whenever a horizontal sync pulse is detected, the beam is reset to the left side of the screen and moved down to the next line position. A vertical sync pulse, indicated by a horizontal sync pulse of longer duration, resets the beam to the top left point of the screen to a line centered between the first two lines of the previous scan. This allows the current field to be displayed between the previous one.

A simplified block diagram of the NTSC color processing system is shown in Figure 6-79, below. The three color signals (RGB: red, green, and blue) from the color camera are combined in a *matrix* unit to produce what is called the *luminance* signal (Y) and two color difference signals (I and Q). These *components* are further combined to produce what is called the *composite* color signal.

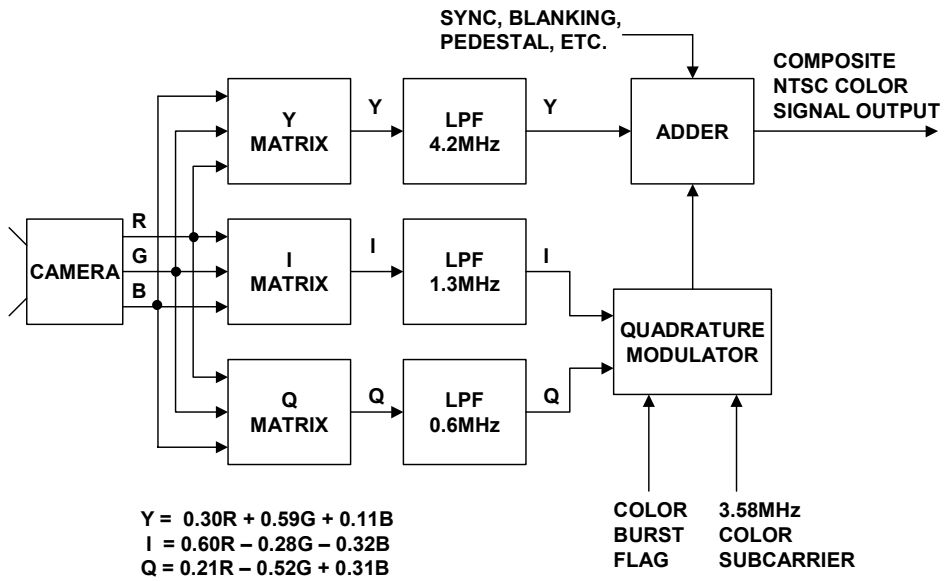


Figure 6-79: *Generating the composite NTSC color signal*

In the NTSC system (used in the U.S. and Japan), the color subcarrier frequency is 3.58MHz. The PAL system (used in the U.K. and Germany) and SECAM system (used in France) use a 4.43MHz color subcarrier.

	NTSC	PAL
Horizontal Lines	525	625
Color Subcarrier Frequency	3.58MHz	4.43MHz
Frame Frequency	30Hz	25Hz
Field Frequency	60Hz	50Hz
Horizontal Sync Frequency	15.734kHz	15.625kHz

Figure 6-80: *NTSC and PAL signal characteristics*

In terms of their key frequency differences, a comparison between the NTSC system and the PAL system are given in Figure 6-80, above.

Differential Gain And Phase Specifications

The color (or *chrominance*) information in the composite video signal is contained in the amplitude and phase of the subcarrier. The *intensity* or *saturation* of the color is determined by the amplitude of the subcarrier signal, and the precise color displayed (i.e. red, green, blue, and combinations) is determined by the phase of the subcarrier signal with respect to the phase of the color burst. The chrominance signal modulates the luminance signal which determines the relative blackness or whiteness of the color. To preserve color fidelity, it is important that the amplitude and phase of a constant-amplitude and phase color subcarrier remain constant across the range of black to white.

Any variation of the *amplitude* of the color subcarrier from black to white levels is called *differential gain* (expressed in %), and any variation in phase with respect to the color subcarrier is called *differential phase* (expressed in degrees). Degradations of up several percent of differential gain and several of degrees differential phase are acceptable for home viewing purposes, but individual components in the video signal path (amplifiers, switches, etc.) must meet much tighter specifications. This is because the signal must pass through many circuits from the camera to the home. As a result, individual professional video systems therefore have stringent requirements for differential gain and phase, usually limiting changes to less than 0.1% and 0.1°.

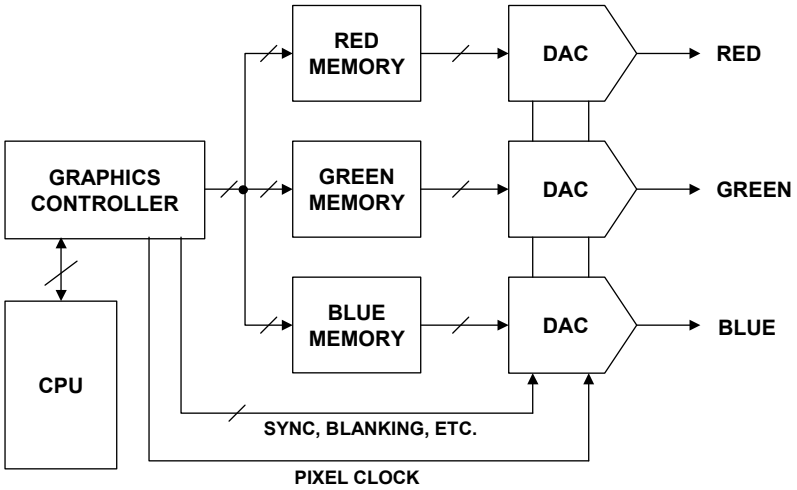


Figure 6-81: *Simplified graphics control system for generating RGB signals*

These system specifications mandate even more stringent standards for individual components, with the differential gain and differential phase requirements for op amps approaching 0.01% and 0.01°.

Video Formats in Graphics Display Systems

There are several system architectures which may be used to build a graphics display system. The most general approach is illustrated in Figure 6-81, above. It consists of a host microprocessor, a graphics controller, three color memory banks or frame buffer, one for each of the primary colors red, green, and blue, (only one for monochrome systems). The microprocessor provides the image information to the graphics controller. This

information typically includes position and color information. The graphics controller is responsible for interpreting this information and adding the required output signals such as sync, blanking, and memory management signals.

Unlike broadcast video, the horizontal and vertical resolution as well as the refresh rate in a graphics display system can vary widely depending upon the desired performance. The resolution in such a system is defined in terms of *pixels*: the number of horizontal lines (expressed as pixels) and the number of pixels in each line. For instance, a 640 × 480 monitor has 480 horizontal lines, and each horizontal line is divided into 640 pixels. So a single frame would contain 307,200 pixels. In a color system, each pixel requires RGB intensity data. This data is generally stored as 8 or 10-bit words in the memory.

The memory holds the intensity information for each pixel. The DACs use the words in the memory and information from the memory controller to write the pixel information to the monitor. Special video DACs called "RAMDACs" greatly simplify the storage of the pixel data by using color lookup tables. These DACs also have inputs to facilitate the generation of the sync and blanking signals.

RESOLUTION	PIXEL RATE
640 × 480	25MHz
800 × 600	38MHz
1024 × 768	65MHz
1280 × 1024	105MHz
1500 × 1500	180MHz
2048 × 2048	330MHz

Pixel Rate ≈ Vertical Resolution × Horizontal Resolution × Refresh Rate × 1.3

Figure 6-82: *Typical graphics resolution and pixel rates for 60Hz non-interlaced refresh rate*

Figure 6-82 above shows some typical resolutions and pixel rates for common display systems, assuming a 60Hz, non-interlaced refresh rate. Standard computer graphics monitors, like television monitors, use a display technique known as *raster scan*. This technique writes information to the screen line by line, left to right, top to bottom, as has been previously discussed. The monitor must receive a great deal of information to display a complete picture. Not only must the intensity information for each pixel be present in the signal but information must be provided to determine when a new line needs to start (HSYNC) and when a new picture frame should start (VSYNC). The computer industry has generally standardized on formats defined in EIA video standard RS-343A. Unlike broadcast video, the refresh rate can also vary, and interlacing may or may not be utilized. The pixel clock frequency gives a good idea of the settling time and bandwidth requirements for any analog component, such as the DAC, which is placed in the path of the RGB signals. The pixel clock frequency can be estimated by finding the product of the horizontal resolution times the vertical resolution times the refresh rate. An additional 30% should be added, called the retrace factor, to allow for overhead.

Bandwidth Considerations in Video Applications

The bandwidth of an op amp used in a video application must be sufficient so that the video signal is not attenuated or shifted in phase significantly. This generally implies that the bandwidth of the op amp be much greater than that of the maximum video frequency. It is not uncommon to require that amplifiers in the signal path in video equipment such as switchers or special effects generators have 0.1dB bandwidths of 50MHz or greater. High definition television requires even higher 0.1dB bandwidth. Circuit parasitics as well as the load impedance can significantly affect the 0.1dB bandwidth at high frequencies. This implies careful attention to layout, decoupling, and grounding as well as the use of transmission line techniques at the op amp output. It is common to use source and load terminations with high quality 75Ω coaxial cable so that the load presented to the op amp output appears as a 150Ω resistive load. Maintaining accurate control of 0.1dB bandwidth is almost impossible with reactive loads.

Achieving the highest 0.1dB bandwidth flatness is therefore important in many video applications. Voltage feedback op amps can be optimized for maximum 0.1dB bandwidth provided the closed-loop gain and load conditions are known. In video applications, closed-loop gains of +1 and +2 are the most common with a 100Ω or 150Ω output load, representing the impedance of 50Ω or 75Ω source and load terminated cables.

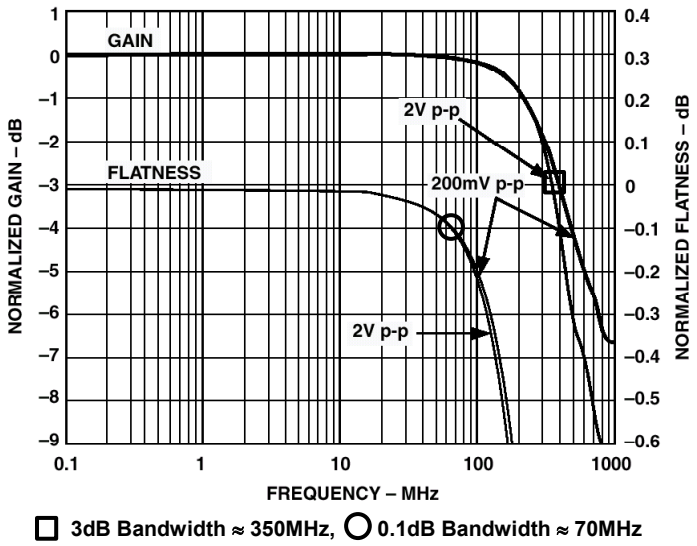


Figure 6-83: *AD8075 triple video buffer gain and gain flatness, G = +2, R_L = 150Ω*

As an example, the AD8074 (G = +1) and AD8075 (G = +2) are triple video buffers optimized for driving source and load terminated 75Ω cables. These devices use a voltage feedback architecture and have on-chip gain-setting resistors. Figure 6-83 above shows the frequency response of the AD8075 buffer on two vertical scales: 1dB/division and 0.1dB/division. The plots labeled "GAIN" show a 3dB bandwidth of 350MHz (□), and the plots labeled "FLATNESS" show a 0.1dB bandwidth of 70MHz (○). Note that the small-signal (200mVp-p) and large-signal (2Vp-p) bandwidths are approximately equal.

Voltage feedback op amps are optimized for bandwidth flatness by adjusting both the compensation capacitor which sets the dominant pole as well as the external feedback network. However, because of the critical relationship between the feedback resistor and the bandwidth of a current feedback op amp, optimum bandwidth flatness is highly dependent on the feedback resistor value, the resistor parasitics, as well as the op amp package and PCB parasitics. Figure 6-84 below shows the bandwidth flatness (0.1dB/division) plotted versus the feedback resistance for the AD8001 in a non-inverting gain of 2. The 100Ω load resistor represents a source and load terminated 50Ω cable. These plots were made using the AD8001 evaluation board with surface mount resistors.

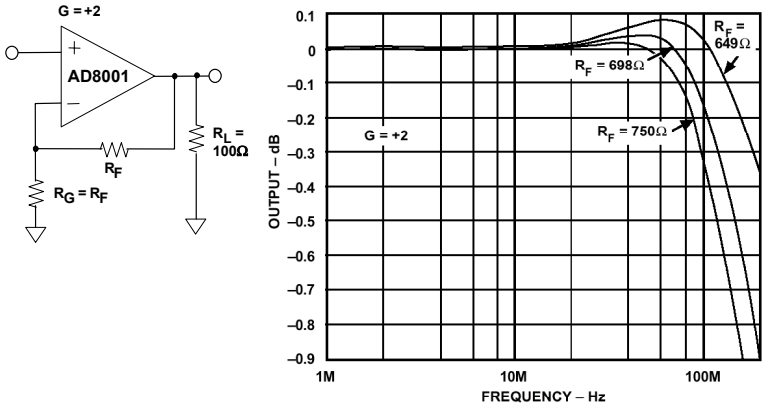
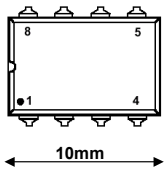


Figure 6-84: *AD8001 current feedback op amp bandwidth flatness versus feedback resistor value*

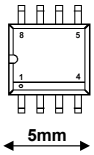
It is recommended that once the optimum resistor values have been determined, 1% tolerance values should be used. In addition, resistors of different construction have different associated parasitic capacitance and inductance. Surface mount resistors are an optimum choice, thus leaded components aren't recommended for high frequency use.

AD8001AN (DIP)



GAIN	–1	+1	+1
R_F	649Ω	1050Ω	750Ω
R_G	649Ω	-	750Ω
0.1dB Flatness	105MHz	70MHz	105MHz

AD8001AR (SOIC)



GAIN	–1	+1	+1
R_F	604Ω	953Ω	681Ω
R_G	604Ω	-	681Ω
0.1dB Flatness	130MHz	100MHz	120MHz

Figure 6-85: *Optimum values of R_F and R_G for AD8001 DIP and SOIC packages for maximum 0.1dB bandwidth*

Slightly different resistor values may be required to achieve optimum performance of the AD8001 in the DIP versus the SOIC packages (see Figure 6-85 above). The SOIC package exhibits slightly lower parasitic capacitance and inductance than the DIP. The

data shows the optimum feedback (R_G) and feedforward (R_F) resistors for highest 0.1dB bandwidth for the AD8001 in the DIP and the SOIC packages. As you might suspect, the SOIC package can be optimized for higher 0.1dB bandwidth because of lower parasitics.

As has been discussed, the current feedback op amp is relatively insensitive to capacitance on the inverting input when it is used in the inverting mode (as in an I/V application). This is because the low inverting input impedance is in parallel with the external capacitance and tends to minimize its effect. In the non-inverting mode, however, even a few picofarads of stray inverting input capacitance may cause peaking and instability. Figure 6-86 shows the effects of adding summing junction capacitance to the inverting input of the AD8004 (SOIC package) for G = +2. Note that only 1pF of added inverting input capacitance (C_J) causes a significant increase in bandwidth and an increase in peaking. For G = –2, however, 5pF of additional inverting input capacitance causes only a small increase in bandwidth and no significant increase in peaking.

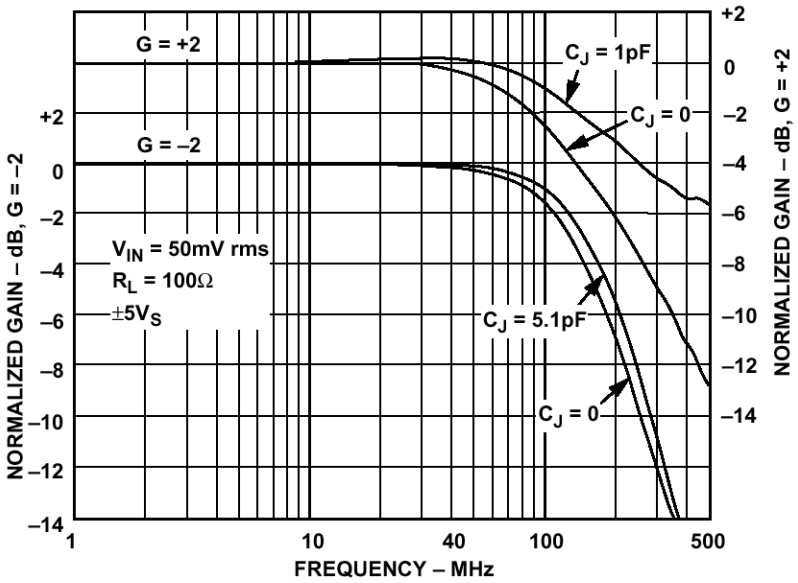


Figure 6-86: *AD8004 current feedback op amp sensitivity to inverting input capacitance for G = +2, G = –2*

It should be noted that high-speed voltage feedback op amps are sensitive to stray inverting input capacitance when used in either the inverting or non-inverting mode, because both positive and negative inputs are high impedance.

Video Signal Transmission

High quality video signals are best transmitted over terminated coaxial cable having a controlled characteristic impedance. The characteristic impedance is given by the equation $Zo = \sqrt{(L/C)}$ where L is the distributed inductance per foot, and C is the distributed capacitance per foot. Popular values are 50, 75, and 93 or 100Ω.

If a length of coaxial cable is properly terminated, it presents a *resistive* load to the driver. If left unterminated, however, it may present a predominately capacitive load to the driver depending on the output frequency. If the length of an unterminated cable is much less than the wavelength of the output frequency of the driver, then the load appears approximately as a lumped capacitance. For instance, at the audio frequency of 20kHz (wavelength ≈ 50,000 feet, or 9.5miles), a 5 foot length of unterminated 50Ω coaxial cable would appear as a lumped capacitance of approximately 150pF (the distributed capacitance of coaxial cable is about 30pF/ft).

- **All interconnections are really transmission lines which have a characteristic impedance (even if not controlled).**
- **The characteristic impedance is equal to $\sqrt{(L/C)}$, where L and C are the distributed inductance and capacitance.**
- **Correctly terminated transmission lines have impedances equal to their characteristic impedance.**
- **Unterminated transmission lines behave approximately as lumped capacitance if the wavelength of the output frequency is much greater than the length of the cable.**
  - **Example: At 20kHz (wavelength = 9.5 miles), 5 feet of unterminated 50Ω cable (30pF/ft) appears like a 150pF load**
  - **Example: At 100MHz, (wavelength = 10 feet), 5 feet of 50Ω must be properly terminated to prevent reflections and standing waves.**

Figure 6-87: *Driving cables*

At 100MHz (wavelength ≈ 10 feet), however, the unterminated coax must be treated as a transmission line in order to calculate the standing wave pattern and the voltage at the unterminated cable output. Figure 6-87 above summarizes transmission line behavior for different frequencies.

Because of skin effect and wire resistance, coaxial cable exhibits a loss that is a function of frequency. This varies considerably between cable types. For instance at 100MHz the attenuation RG188A/U is 8dB/100ft, RG58/U is 5.5dB/100ft, and RG59/U 3.6dB/100ft (see Reference 4). Skin effect also affects the pulse response of long coaxial cables. The response to a fast pulse will rise sharply for the first 50% of the output swing, then taper off during the remaining portion of the edge. Calculations show that the 10 to 90% waveform risetime is 30 times greater than the 0 to 50% risetime when the cable is skin effect limited (Reference 4, again).

Transmission Line Driver Lab

It is useful to examine the fidelity of a pulse signal, for conditions of proper/improper transmission line source/load terminations. Some lab experiments were set up to do this.

To illustrate the behavior of a high speed op amp driving a coaxial cable, consider the circuit of Figure 6-88 below. Here the AD8001 drives 5 feet of 50Ω coaxial cable, which is load-end terminated in the characteristic impedance of 50Ω. No termination is used at the amplifier (driving) end. The pulse response is also shown in the figure.

The output of the cable was measured by connecting it directly to the 50Ω input of a 500MHz Tektronix 644A digitizing oscilloscope. The 50Ω resistor termination is actually the input of the scope. However, this 50Ω load is not a perfect line termination, it is lower at high frequencies (due to the scope shunt input capacitance of about 10pF).

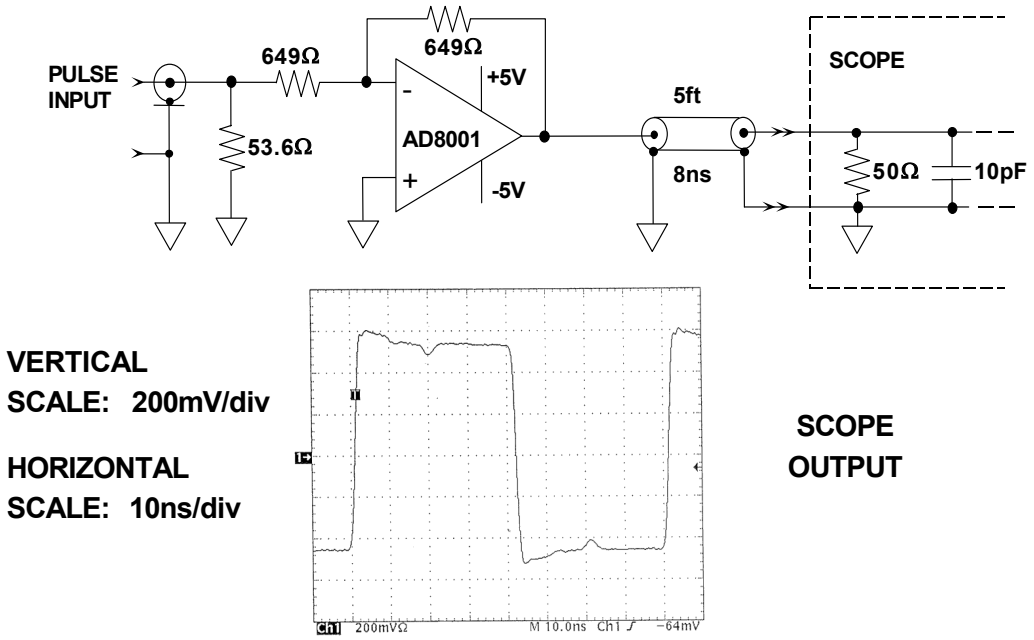


Figure 6-88: *Pulse response of AD8001 driving 5 feet of load-only terminated 50Ω coaxial cable*

As a consequence some of the positive going pulse edge is reflected out of phase to the source. When this reflection reaches the op amp, it sees the op amp closed-loop output impedance, which, at 100MHz, is approximately 100Ω (higher than line impedance).

Upon arriving at the op amp output, the negative-going reflection from the load is then re-reflected back towards the load, without undergoing another phase reversal. This then accounts for the negative going "blip" seen on the upper plateau of the waveform, which occurs approximately 16ns after the leading edge. This time difference is equal to the round-trip delay of the cable (2•5ft•1.6 ns/ft=16ns). An additional point worth noting is that, in the frequency domain (which is not shown by these tests) the cable mismatch will also cause a loss of bandwidth flatness at the load.

Figure 6-89 below shows a second case, the results of driving the same coaxial cable, but now used with both a 50Ω source-end as well as the 50Ω load-end termination at the scope. It should be noted that this case is the preferred way to drive a transmission line, because a portion of the reflection from the load impedance mismatch is absorbed by the amplifier's source termination resistor of 50Ω. A disadvantage is that there is a gain loss of 6dB, because of the 2/1 voltage division which occurs between the equal value source and load terminations, i.e., 50Ω/50Ω.

However, a major positive attribute of this configuration, with the line impedance matched source and load terminations in conjunction with a low-loss cable, is that *the best bandwidth flatness is ensured*, especially at lower operating frequencies. In addition to this, the amplifier is operated with a near optimum load condition, i.e., into a resistive load. The load in this case is 50Ω plus 50Ω, or 100Ω. In general, it will be twice the impedance of the transmission line in use, i.e., 150Ω for a 75Ω line, etc.

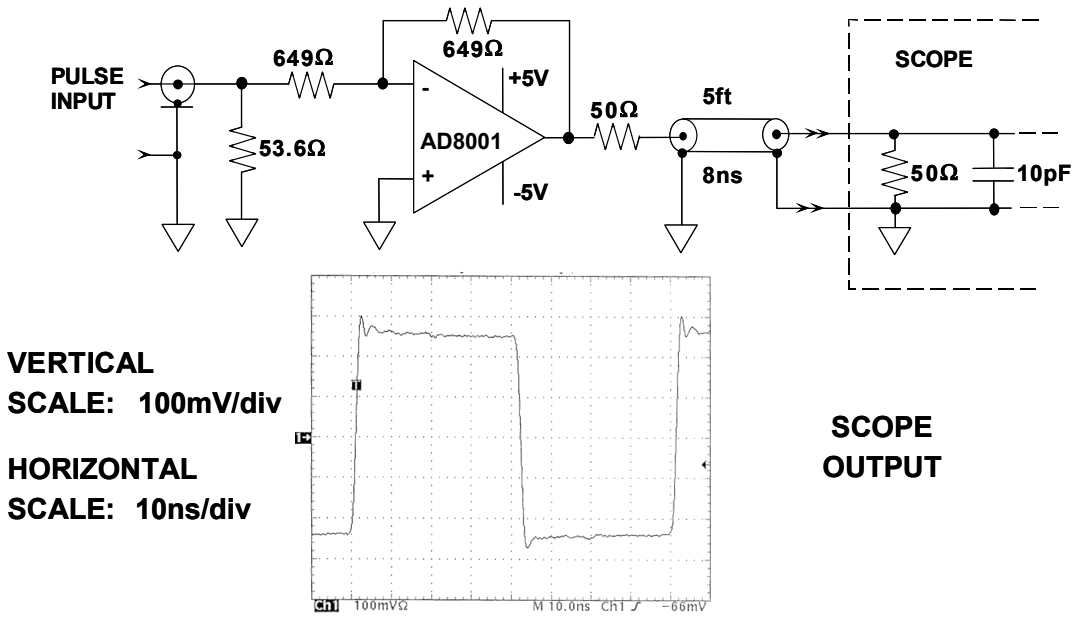


Figure 6-89: *Pulse response of AD8001 driving 5 feet of source and load terminated 50Ω coaxial cable*

In practice, the gain loss associated with the 2/1 source/load impedance is easily made up, simply by operating the line driver stage at a gain of 2x. Typically, video driver stages are non-inverting to preserve the waveform sign, and operate at a fixed and precise gain of 2 times. Thus they will inherently provide a net signal transfer gain of unity, as measured from input to the final end-of-line load termination (this neglects any associated transmission line losses, and assumes precise resistor ratios for the gain resistors). Another very practical point is that the same driver can be used for a wide variety of transmission lines, simply by changing the value of the source termination resistor.

Source-end (only) terminations can also be used as shown in Figure 6-90 below, where the op amp is now source terminated by the 50Ω resistor which drives the cable. At the load end, the scope is set for 1MΩ input impedance, which represents an approximate open circuit. The initial leading edge of the pulse at the op amp output sees a 100Ω load (the 50Ω source resistor in series with the 50Ω coax impedance. When the pulse reaches the load, a large portion is reflected in phase, because of the high load impedance, resulting in a full-amplitude pulse at the load. When the reflection reaches the source-end of the cable, it sees the 50Ω source resistance in series with the op amp closed loop output impedance (approximately 100Ω at the frequency represented by the 2ns risetime pulse edge). The re-reflected portion remains in phase, and then appears at the scope input as the positive going "blip", approximately 16ns after the leading edge.

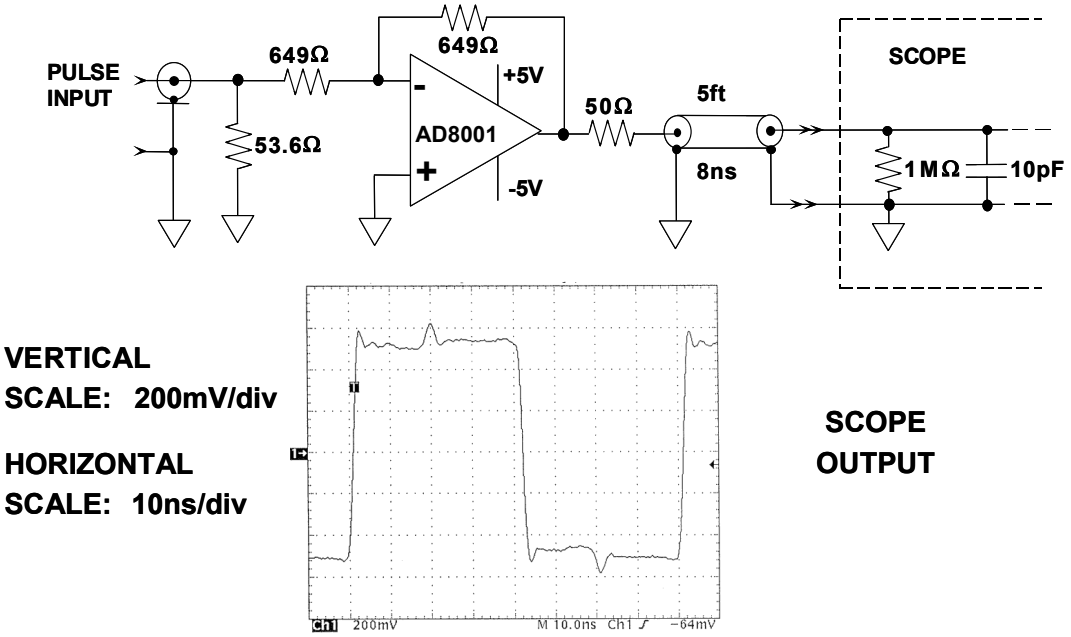


Figure 6-90: *Pulse response of AD8001 driving 5 feet of source-only terminated 50Ω coaxial cable*

From these experiments, one can easily see that the preferred method for minimum reflections (and therefore maximum bandwidth flatness) is to use both source and load terminations and try to minimize any reactance associated with the load. The experiments represent a worst-case condition, where the frequencies contained in the fast edges are greater than 100MHz. (using the rule-of-thumb that bandwidth = 0.35/risetime).

At less demanding video frequencies, either load-only, or source-only terminations may give acceptable results, but the op amp data sheet should always be consulted to determine the op amp's closed-loop output impedance at the maximum frequency of interest; i.e., is it less than the line impedance. A major disadvantage of the source-only termination is that it requires a truly high impedance load (high resistance and minimal parasitic capacitance) for minimum absorption of energy. It also places a burden on the driving amplifier, to maintain the low output impedance at high frequencies.

Now, for a truly worst case, let us replace the 5 feet of coaxial cable with an uncontrolled-impedance cable (one that is largely capacitive with little inductance). Also, let's use a capacitance of 150pF to simulate the cable (corresponding to the total capacitance of 5 feet of coaxial cable, whose distributed capacitance is about 30pF/foot). Figure 6-91 below shows the output of the AD8001 op amp, driving a lumped 160pF capacitance (including the scope input capacitance of 10pF).

Overshoot and severe ringing on the pulse waveform is noted, due to the capacitive loading. This example illustrates the need to use good quality controlled-impedance coaxial cable in the transmission of high frequency signals, even over short distances. Failure to adhere to controlled-impedance lines for signal distribution can result in severe loss of pulse waveform fidelity, and loss of bandwidth flatness in the frequency domain.

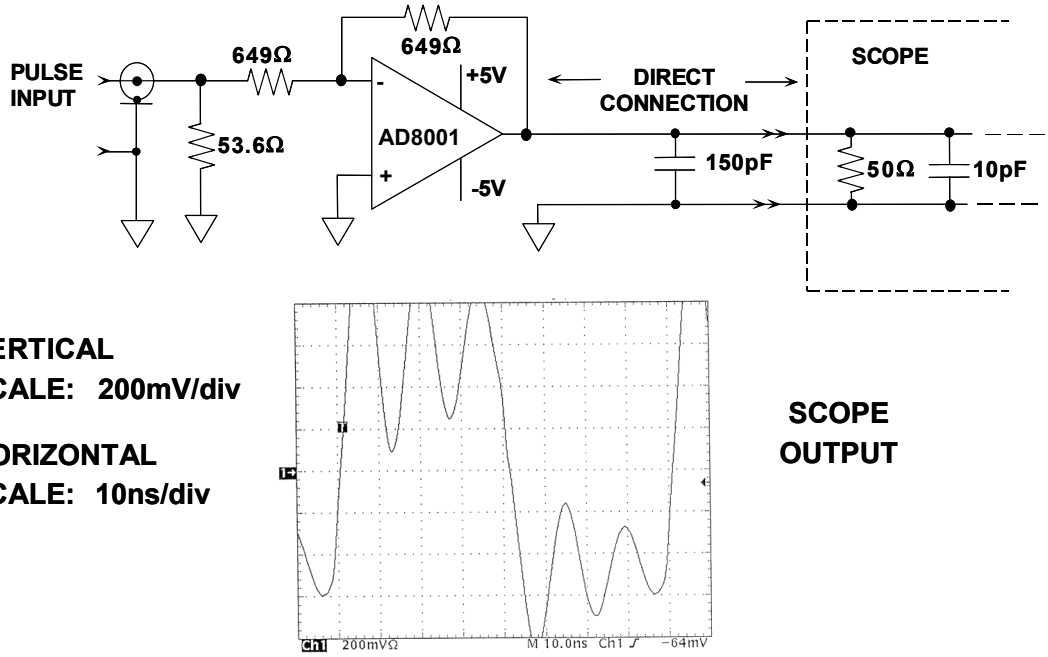


Figure 6-91: *Pulse response of AD8001 driving 160pF || 50Ω load*

To summarize, transmission line driver circuits should use proper line terminations for best response. The ideal method of line termination is matching line-impedance-value resistances at both source and load end (Fig. 6-89, again). The associated 6dB gain loss is easily made up in the amplifier. Next best is a source-only termination (Fig. 6-90, again), with due care towards maintaining a high impedance at the load end, and a low drive impedance amplifier. This type of termination provides near-full amplitude level at the load end, making the gain of the driver less critical. Load-only termination can also be used (Fig. 6-88, again), but may be more critical of load end parasitic effects and the amplifier performance. It also provides near-full amplitude level at the load end.

Direct drive of uncontrolled load impedances, especially lumped capacitive lines, should be avoided wherever signal fidelity is important (Fig. 6-91, again).

Video Line Drivers

The AD8047 and AD8048 voltage feedback op amps have been optimized to offer outstanding performance as video line drivers. They utilize the "quad core" g_m stage as previously described for high slew rate and low distortion (see Chapter 1). The AD8048 (optimized for G = +2) has a differential gain of 0.01% and a differential phase of 0.02°, making it well suited for HDTV applications.

In the configuration using the AD8048 shown in Figure 6-92 below, the 0.1dB bandwidth is 50MHz for ±5V supplies, slew rate is 1000V/µs, and 0.1% settling time is 13ns. The total quiescent current is 6mA (±5V), and quiescent power dissipation 60mW. Performance of this circuit will be optimum with the gain-of-two stable AD8048 op amp, as its parameters have been optimized for this gain. Alternately, if a gain-of-one stable op amp is desired, the AD8047 can be used.

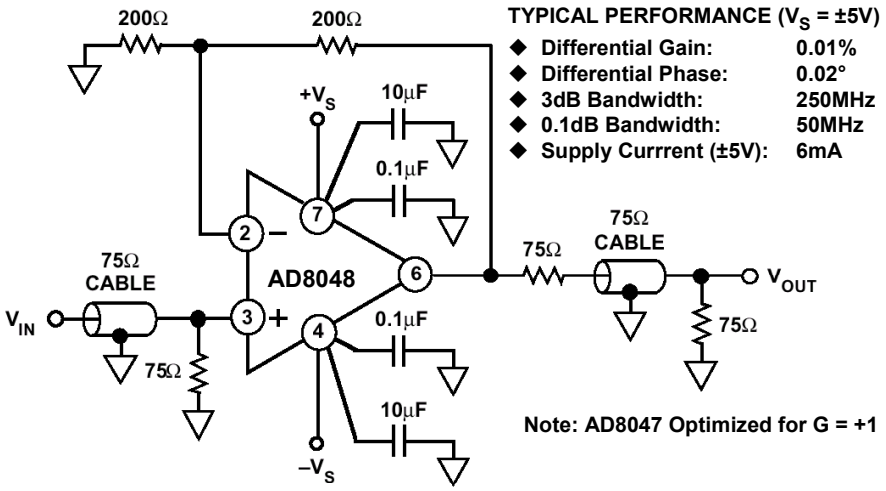


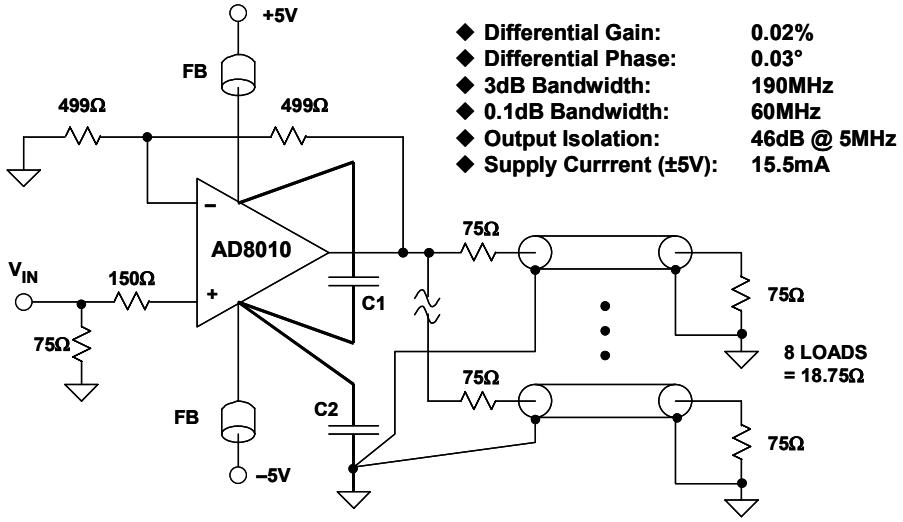
Figure 6-92: *High performance video line driver using the AD8048*

Note that a very wide variety of both voltage feedback and current feedback devices can be used similarly as a gain-of-two line driver (although the required feedback resistances may vary by device). Examples would be the AD818/828, AD8055/56, AD8057/58, and AD8061/62/63 families of voltage feedback op amps, and the AD811/12/13, AD8001/02, AD8012 families as a partial list. There are differences among all of these devices for applicable supply ranges, single-supply compatibility, etc., so consult device data sheets.

It is often desirable to drive more than one coaxial cable, which represents a DC load of 150Ω to a driver. The typical maximum video signal level is 1V into 75Ω, which represents 2V at the output of the driver, and a current of 13.3mA. Thus a 50mA output current video op amp such as the AD8047 or AD8048 would theoretically be capable of driving three source and load-terminated 75Ω loads. But, there are other important subtle considerations for this application. Differential gain and phase may be degraded for high output currents. Also, the op amp closed-loop output impedance affects crosstalk between the driven output channels. So it is often better to select a video driver fully specified for the required fan-out and load, especially if the fan-out is greater than two.

Video Distribution Amplifier

The AD8010 op amp is optimized for driving multiple video loads in parallel. Video performance of 0.02% differential gain and 0.03% differential phase is maintained, while driving eight 75Ω source and load-terminated video lines. The AD8010 uses the current feedback architecture and has a 0.1dB bandwidth of 60MHz with eight video loads. Typical supply current (neglecting load current) is 15.5mA on ±5V supplies. A typical connection diagram is shown below in Figure 6-93. The AD8010 is offered in three packages: an 8-lead DIP (θ_{JA} = 90ºC/W), 16-lead wide body SOIC (θ_{JA} = 73ºC/W), and a low thermal resistance, 8-lead SOIC (θ_{JA} = 122ºC/W).



FB = FERRITE BEAD (Amidon, Inc, #43101, http://www.amidoncorp.com)
C1 = C2 = 47µF/16V Tantalum + 10µF/10V Tantalum + 0.1µF Ceramic Chip

Figure 6-93: *The AD8010 video distribution amplifier*

The power supply decoupling scheme used for the AD8010 requires special attention. The conventional technique of bypassing each power supply pin individually to ground can have an adverse effect on the differential phase error of the circuit. This is because there is an internal compensation capacitor in the AD8010 that is referenced to the negative supply. The recommended technique shown in Figure 6-93 is to connect three parallel bypass capacitors from the positive supply to the negative supply, and then to bypass the negative supply to ground with a similar set, as shown. For high frequency decoupling, 0.1µF ceramic surface mount capacitors are recommended. The high currents that can flow through the power supply pins require additional large tantalum electrolytic decoupling capacitors. As shown, a 47µF/16V tantalum in parallel with a 10µF/10V tantalum capacitor is desirable. The grounded side of the C2 capacitors bypassing the negative supply should be brought to a single-point output return ground. In addition to the bypass capacitors described above, ferrite beads such as those noted should be placed in series with both positive and negative supplies for further decoupling.

Another important consideration for driving multiple cables is high frequency isolation between the outputs. Due largely to its low output impedance, the AD8010 achieves better than 46dB output-to-output isolation at 5MHz, while driving 75Ω source and load-terminated cables.

Differential Line Drivers/Receivers

There are a number of applications for differential signal drivers and receivers. Among these are analog-digital-converter (ADC) input buffers, where differential operation can provide lower levels of second order distortion for certain converters. Other uses include high frequency bridge excitation, and drivers for balanced transmission twisted pair lines such as in ADSL and HDSL.

The transmission of high quality signals across noisy interfaces (either between individual PC boards or between racks) has always been a challenge to designers. Differential techniques using high common-mode-rejection-ratio (CMRR) instrumentation amplifiers largely solves the problem at low frequencies. Examples of this have already been discussed, under the "Audio Amplifiers" portion of this chapter.

At audio frequencies, transformers, or products such as the SSM2142 balanced line driver and SSM2141/SSM2143 line receivers offer outstanding CMRRs and the ability to transmit low-level signals in the presence of large amounts of noise, as noted. At high frequencies, small bifilar-wound toroid transformers are effective.

In contrast to this, the problem of signal transmission at video frequencies is a more complex one. Transformers suitable for video coupling aren’t very effective, because the baseband video signal has low-frequency components down to a few tens of Hz, and an upper bandwidth limit that can be in the tens (hundreds) of MHz. This make a workable video transformer an item extremely difficult to make.

Another point is that video signals are generally processed in single-ended form, and therefore don't adapt easily to balanced transmission line techniques. Related to this, shielded twin-conductor coaxial cable with good bandwidth is usually somewhat bulky and expensive, and has not found great acceptance.

As a result of these factors, designing high bandwidth, low distortion differential video drivers and receivers with high CMRR at high frequencies is an extremely difficult task.

Nevertheless, even in the face of all of the above problems, there are various differential techniques available right now that offer distinct advantages over single-ended methods. Some of these techniques make use of discrete components, while others utilize state-of-the-art video differential amplifiers.

Approaches To Video Differential Driving/Receiving

Two solutions to differential transmission and reception are shown in Figure 6-94 below. One is the ideal case (top), where a balanced differential driver drives a balanced twin-conductor coaxial cable, which then drives a terminated differential line receiver. However, as discussed, this circuit is difficult to implement fully at video frequencies.

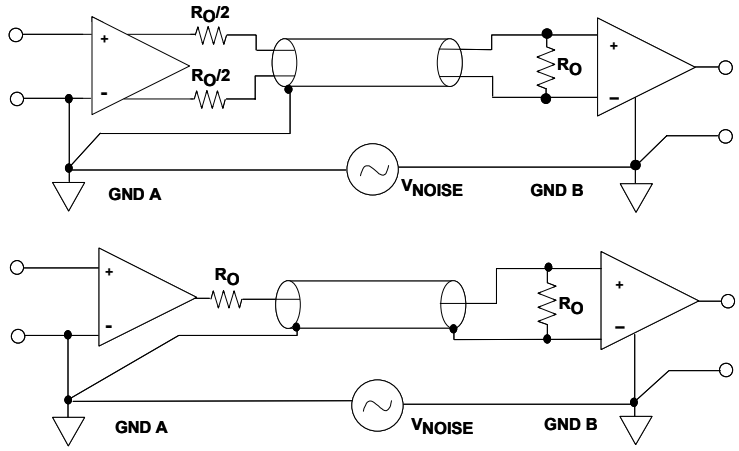


Figure 6-94: *Two approaches to differential line driving and receiving*

A second, most often used approach uses a single-ended driver driving a source-terminated coaxial cable (bottom), with the cable shield grounded at the transmitter. At the receiver, the coaxial cable is terminated in its characteristic impedance, but the shield is left floating in order to prevent a ground loop between the two systems. Common mode ground noise is rejected by the CMRR of the differential line receiver.

Inverter-Follower Differential Driver

The circuit of Figure 6-95 below is a useful differential driver for high speed 10-12 bit ADCs, differential video lines, and other balanced loads at 1-4Vrms output levels.

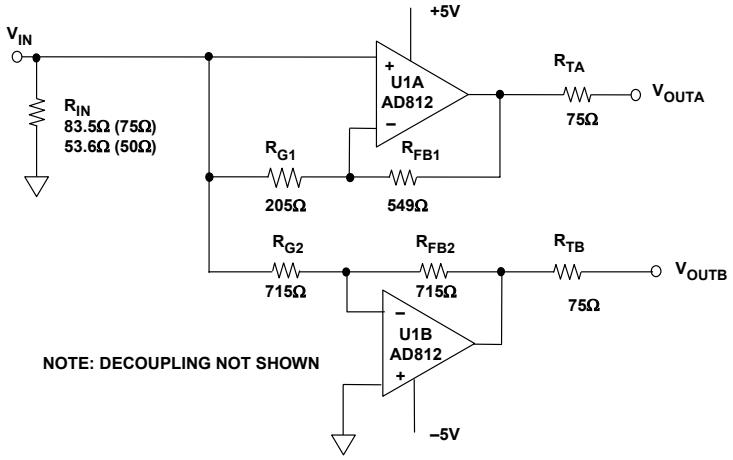


Figure 6-95: *Differential driver using an inverter and a follower*

It is shown operating from ±5V supplies, but it can also be adapted to supplies in the range of ±5 to ±15V. When operated directly from ±5V as here, it minimizes potential for

destructive ADC overdrive when higher supply voltage buffers drive a ±5V powered ADC, in addition to also minimizing driver power.

In many of these differential drivers the performance criteria is often high. In addition to low output distortion, the two signals should maintain gain and phase flatness. In this topology, two sections of an AD812 dual current feedback amplifier are used for the channel A and B buffers. This provides inherently better open-loop bandwidth matching than using two singles, where bandwidth varies between different manufacturing lots. The two buffers here operate with precise gains of ±1, as defined by their respective feedback and input resistances. Channel B buffer U1B is conventional, and uses a matched pair of 715Ω resistors— an optimum value for the AD812 on ±5V supplies.

In channel A, non-inverting buffer U1A has an inherent signal gain of 1, by virtue of the bootstrapped feedback network R_{FB1} and R_{G1} (see Reference 5). It also has a higher noise gain, for phase matching. Normally a current feedback amplifier operating as a simple unity gain follower would use one (optimum) resistor R_{FB1}, and no gain resistor at all. Here, with input resistor R_{G1} added, a U1A noise gain like that of U1B results. Due to the bootstrap connection of R_{FB1}-R_{G1}, the signal gain is maintained at unity. Given the matched open loop bandwidths of U1A and U1B, similar noise gains in the A-B channels provide closely matched output bandwidths between the driver sides, a distinction which greatly impacts overall matching performance.

In setting up a design for the driver, the effects of resistor gain errors should be considered for R_{G2}-R_{FB2}. Here a worst case 2% mis-match will result in less than 0.2dB gain error between channels A and B. This error can be improved simply by specifying tighter resistor ratio matching, avoiding trimming.

If desired, phase match can be trimmed via R_{G1}, so that the phase of channel A matches that of B. This can be done by using a pair of closely matched (0.1% or better) resistors to sum the A and B channels, as R_{G1} is adjusted for the best null conditions at the sum node. The A-B gain and phase matching is quite effective in this driver; the test results of the circuit as shown 0.04dB and 0.1° between the A and B output signals at 10MHz, when operated into dual 150Ω loads. The 3dB bandwidth of the driver is about 60MHz.

Net input impedance of the circuit is set to a standard line termination value such as 75Ω (or 50Ω), by choosing R_{IN} so that the desired value results when paralleled with R_{G2}. In this example, an R_{IN} value of 83.5Ω provides a standard input impedance of 75Ω when paralleled with 715Ω. For the circuit just as shown, dual voltage feedback amplifier types with sufficiently high speed and low distortion can also be used. This allows greater freedom with regard to resistor values using such devices as the AD826 and AD828.

Gain of the circuit can be changed if desired, but this isn't totally straightforward. An easy step to satisfy diverse gain requirements is to simply use a triple amplifier such as the AD813 or AD8013, with the third channel as a variable gain input buffer. Note that if an amplifier is used with specifications substantially different than the AD812, some adjustment of resistor values may be necessary.

Cross-Coupled Differential Driver

Another differential driver approach uses cross-coupled feedback to get very high CMR and complementary outputs at the same time. In Figure 6-96 below, AD8002 dual current feedback amplifier sections are used as cross-coupled inverters, the outputs are forced equal and opposite, assuring zero output common mode voltage (see Reference 6).

The gain cell that results, U1A and U1B plus cross-coupling resistances R_X, is fundamentally a differential input/output topology. But, it behaves as a voltage feedback amplifier with regard to the feedback port at the U1A (+) node. The V_{IN} to V_{OUT} gain is:

$$G = \frac{V_{OUT}}{V_{IN}} = \frac{2R2}{R1} \qquad \text{Eq. 6-21}$$

where V_{OUT} is the differential output, equal to $V_{OUTA}–V_{OUTB}$.

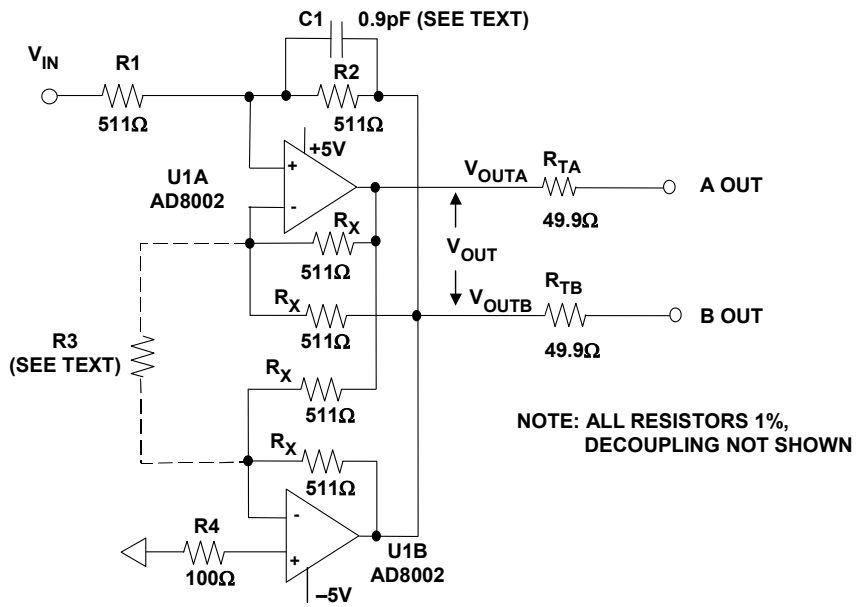


Figure 6-96: *Cross-coupled differential driver provides balanced outputs and 250MHz bandwidth*

The relationship of Eq. 6-21 may not be obvious, so it can be derived as follows:

Using the conventional inverting op amp gain equation, the input voltage V_{IN} develops an output voltage V_{OUTB} given by:

$$V_{OUTB} = -V_{IN}\frac{R2}{R1}. \qquad \text{Eq. 6-22}$$

Also, $V_{OUTA} = –V_{OUTB}$, because V_{OUTA} is inverted by U1B.

However, $V_{OUT} = V_{OUTA}–V_{OUTB} = –2V_{OUTB}$.

Therefore,

$$V_{OUT} = -2\left(-V_{IN}\frac{R2}{R1}\right) = 2V_{IN}\frac{R2}{R1}, \qquad \text{Eq. 6-23}$$

and

$$\frac{V_{OUT}}{V_{IN}} = \frac{2R2}{R1}. \qquad \text{Eq. 6-24}$$

This circuit has some unique benefits. First, the differential voltage gain is set by a single resistor ratio, so there is no necessity for side-side resistor matching with gain changes, as is the case for conventional differential amplifiers (see line receivers, below). Second, because the (overall) circuit emulates a voltage feedback amplifier, these gain resistances are not as restrictive as in the case of a conventional current feedback amplifier. Thus, they are not highly critical as to value as long as the equivalent resistance seen by U1A is reasonably low (≤1kΩ in this case).

A third and important advantage is that cell bandwidth can be optimized to a desired gain by a single optional resistor, R3, as follows. If for instance, a gain of 20 is desired (R2/R1=10), the bandwidth would otherwise be reduced by roughly this amount, since without R3, the cell operates with a constant gain-bandwidth product (voltage feedback mode). With R3 present however, advantage can be taken of the AD8002 current feedback amplifier characteristics. Additional internal gain is added by the connection of R3, which, given the appropriate value, effectively raises gain-bandwidth to a level so as to restore the bandwidth which would otherwise be lost by the higher closed loop gain.

In the circuit as shown, no R3 is necessary at the low working gain of 2, since the 511Ω R_X resistors are already optimized for maximum bandwidth. Note that these four matched R_X resistances are somewhat critical, and will change in absolute value with the use of another current feedback amplifier. At higher gain closed loop gains, R3 can be chosen to optimize the working transconductance in the input stages of U1A and U1B, as follows:

$$R3 \cong \frac{Rx}{(R2/R1) - 1}. \qquad \text{Eq. 6-25}$$

As in any high speed inverting feedback amplifier, a small high-Q chip type feedback capacitance, C1, may be needed to optimize flatness of frequency response. In this example, a 0.9pF value was found optimum for minimizing peaking. In general, provision should be made on the PC layout for an NPO chip capacitor in the range of 0.5-2pF. This capacitor is then value selected at board characterization for optimum frequency response.

Performance for the circuit of Fig. 6-96 was examined with a dual trace, 1-500MHz swept frequency response plot, as is shown in Figure 6-97 below. The test output levels were 0dBm into matched 50Ω loads, through back termination resistances R_{TA} and R_{TB}, as measured at V_{OUTA} and V_{OUTB}.

In this plot the vertical scale is 2dB/div, and it shows the 3dB bandwidth of the driver measuring about 250MHz, with peaking about 0.1dB. The four R_X resistors along with R_{TA} and R_{TB} control low frequency amplitude matching, which was within 0.1dB in the lab tests, using 511Ω 1% resistor types. For tightest amplitude matching, these resistor ratios can be more closely controlled.

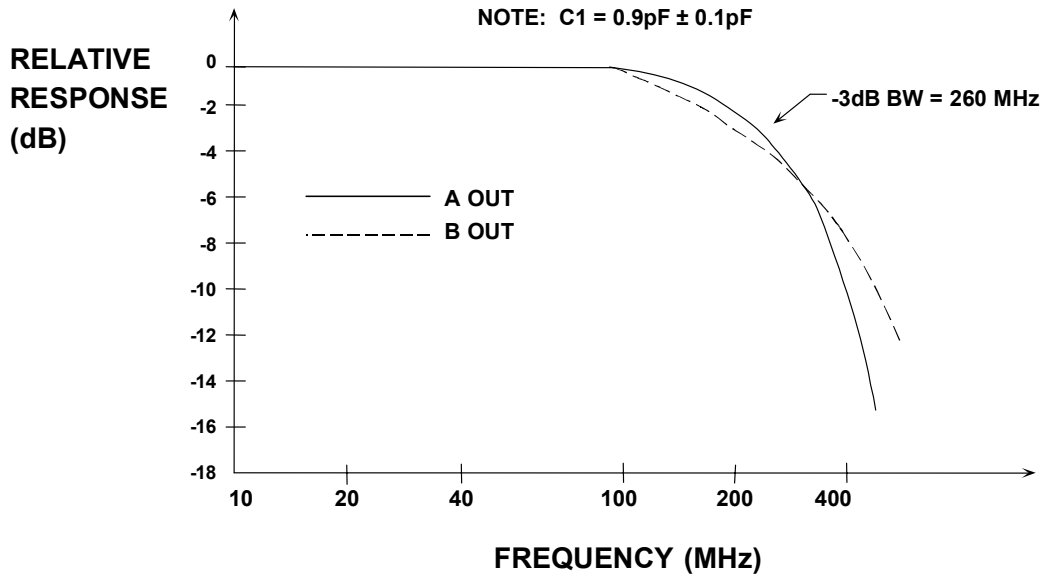


Figure 6-97: *Frequency response of AD8002 cross-coupled driver*

Due to the very high gain-bandwidths involved with the AD8002, the construction of this circuit should only be undertaken by following RF rules. This includes the use of a heavy ground plane, and the use chip bypass capacitors of zero lead length at the ±5V supply pins. For lowest parasitic effect and low inductance, chip style resistors are also recommended for this circuit (see Reference 7). The optimization of C1 has already been noted, above. While a chip style NP0 is good in general for C1, a small film trimmer may also be useful, as it will allow optimizing peaking on an individual circuit basis.

Although this circuit example illustrates wideband a video driver, it should be noted that lower bandwidth applications could also find this push-pull topology useful. An audio frequency application could for example use an AD812 for U1A and U1B, or pair of AD811s. Operating on ±15V, these with allow a high level of balanced, linear output.

Fully Integrated Differential Drivers

A block diagram of the new AD813X family of fully differential amplifiers optimized for differential driving is shown in Figure 6-98. Figure 6-98A shows the details of the internal circuit, and Figure 6-98B shows the equivalent circuit. The gain is set by the external R_F and R_G resistors, and the common-mode voltage is set by the voltage on the V_{OCM} pin. The internal common-mode feedback forces the V_{OUT+} and V_{OUT-} outputs to be balanced, i.e., the signals at the two outputs are always equal in amplitude but 180° out of phase per the equation:

$$V_{OCM} = (V_{OUT+} + V_{OUT-}) / 2 \ . \qquad \text{Eq. 6-26}$$

The circuit can be used with either a differential or a single-ended input, and the voltage gain is equal to the ratio of R_F to R_G.

The AD8138 has a 3dB small-signal bandwidth of 320MHz (G = +1) and is designed to give low harmonic distortion as an ADC driver (see Chapter 3). The circuit provides excellent output gain and phase matching, and the balanced structure suppresses even-order harmonics.

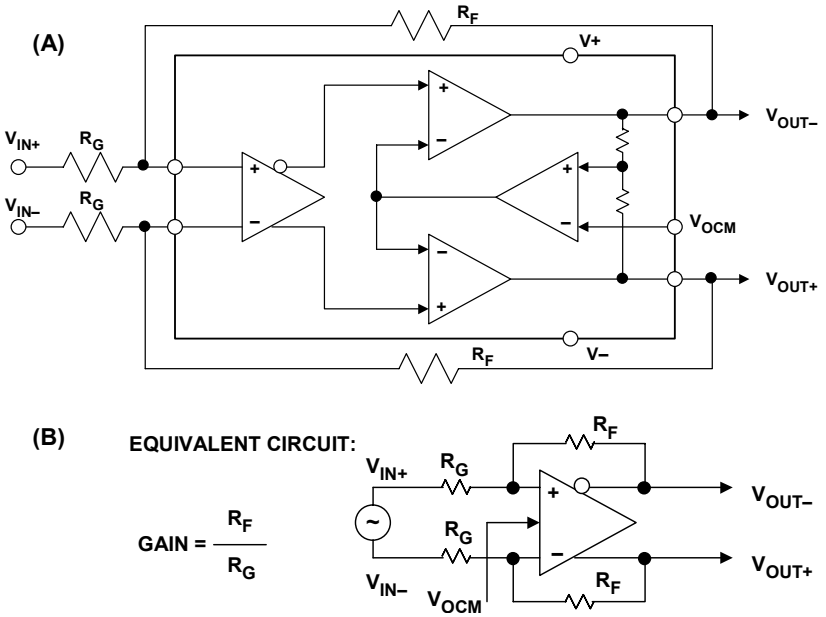


Figure 6-98: *AD8138 differential driver amplifier functional schematic (A) and equivalent circuit (B)*

It should be noted that the AD8131 differential driver is a sister device to the AD8138 in terms of the function illustrated in Fig. 6-98A, and includes internal gain-set resistors.

A 4-Resistor Differential Line Receiver

Figure 6-99 below shows a low cost, medium performance line receiver using a high speed op amp which is rated for video use. It is actually a standard 4 resistor difference amplifier optimized for high speed, with a differential to single-ended gain of R2/R1. Using low value, DC-accurate, AC-trimmed resistances for R1-R4 and a high speed, high CMR op amp provides the good performance.

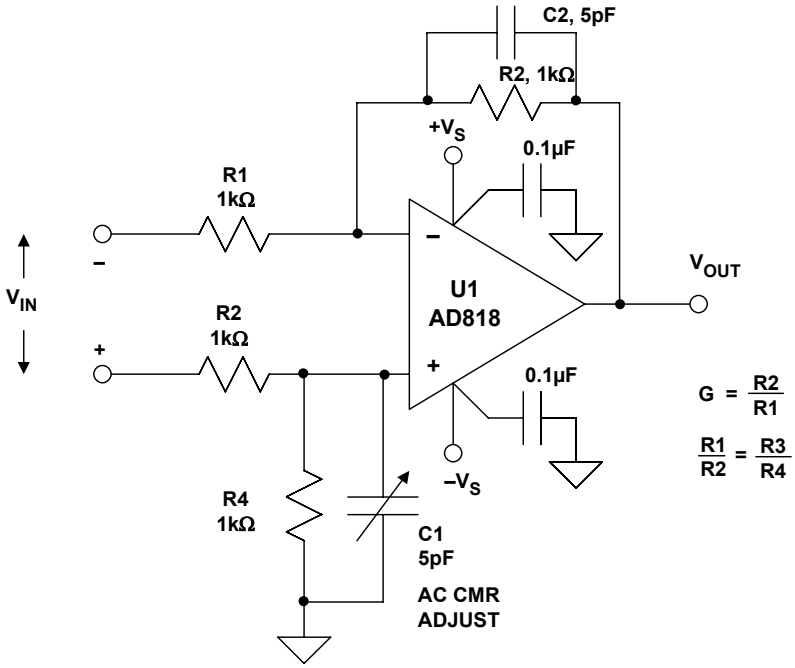


Figure 6-99: *Simple video line receiver using the AD818 op amp*

Practically speaking however, at low frequencies resistor matching can be more critical to overall CMR than the rated CMR of the op amp. For example, the worst case CMR (in dB) of this circuit due to resistor mismatch is:

$$\mathrm{CMR} = 20\log_{10}\left(\frac{1+\frac{\mathrm{R2}}{\mathrm{R1}}}{4\mathrm{Kr}}\right). \qquad \text{Eq. 6-27}$$

In this expression the term "Kr" is a single resistor tolerance in fractional form (1%=0.01, etc.), and it is assumed the amplifier has significantly higher CMR (≥100dB). Using discrete 1% metal films for R1/R2 and R3/R4 yields a worst case CMR of 34dB, 0.1% types 54dB, etc. Of course 4 random 1% resistors will on the average yield a CMR better than 34dB, but not dramatically so. A single substrate dual matched pair thin film network is preferred, for reasons of best noise rejection and simplicity. One type suitable is the Vishay VTF series part 1005, (see Reference 7) which has a ratio match of 0.1%, which will provide a worst case low frequency CMR of 66dB.

This circuit has an interesting and desirable side property. Because of the resistors it divides down the input voltage, and the amplifier is protected against overvoltage. This allows CM voltages to exceed ±5V supply rails in some cases without hazard. For operation with ±15V supplies, inputs should not exceed the supply rails.

At frequencies above 1MHz, the bridge balance is dominated by AC effects, and a C1-C2 capacitive balance trim should be used for best performance. The C1 adjustment is intended to allow this, providing for the cancellation of stray layout capacitance(s) by electrically matching the net C1-C2 values.

Within a given PC layout with low and stable parasitic capacitance, C1 is best adjusted once in 0.5pF increments, for best high frequency CMR. Using designated PC pads, production values then would use the trimmed value. Good AC matching is essential to achieving good high frequency CMR. C1-C2 should be types similar physically, such as NPO ceramic chip capacitors.

While the circuit as shown has unity gain, it can be gain-scaled in discrete steps, as long as the noted resistor ratios are maintained. In practice, this means using taps on a multi-ratio network for gain change, so as to raise both R2 and R4, in identical proportions. There is no other simple way to change gain in this receiver circuit.

Alternately, a scheme for continuous gain control without interaction with CMR is to simply follow this receiver with a scaling amplifier/driver, with adjustable gain. The use of an AD828 amplifier (AD818 dual) allows this, with the addition of only two resistors.

Video gain/phase performance of this stage is dependent upon the device used for U1 and the operating supply voltages. Suitable voltage feedback amplifiers work best at supplies of ±10 to ±15V, which maximizes op amp bandwidth. And, while many high speed amplifiers function in this circuit, those expressly designed with very low distortion video operation perform best.

The circuit just as shown can be used with supplies of ±5 to ±15V, but lowest NTSC video distortion occurs for supplies of ±10V or more using the AD818, where differential gain/differential phase errors are less than 0.01%/0.05°. With the AD818 operating at ±5V supplies, the distortion rises somewhat, but the lowest power drain of 70mW occurs. If low distortion and lowest power operation on ±5V is important, the use of an AD8055 (or AD8056 section) should be considered for the U1 function; they will dissipate 50mW.

A drawback to this circuit is that it does load a 75Ω video line to some extent, and so should be used with this loading taken into account. On the plus side, it has wide dynamic range for both signal and CM voltages, plus the inherent overvoltage protection.

Active Feedback Differential Line Receiver

The AD8129/AD8130 differential line receivers, along with their predecessor the AD830, utilize a novel amplifier topology called *active feedback* (see Reference 8). A simplified block diagram of these devices is shown below in Figure 6-100.

The AD830 and the AD8129/AD8130 have two sets of fully differential inputs, available at V_{X1}-V_{X2} and V_{Y1}-V_{Y2}, respectively. Internally, the outputs of the two GM stages are summed and drive a buffer output stage.

In this device the overall feedback loop forces the internal currents I_X and I_Y to be equal. This condition forces the differential voltages V_{X1}–V_{X2} and V_{Y1}–V_{Y2} to be equal and opposite in polarity. Feedback is taken from the output back to one input differential pair, while the other pair is driven directly by an input differential input signal.

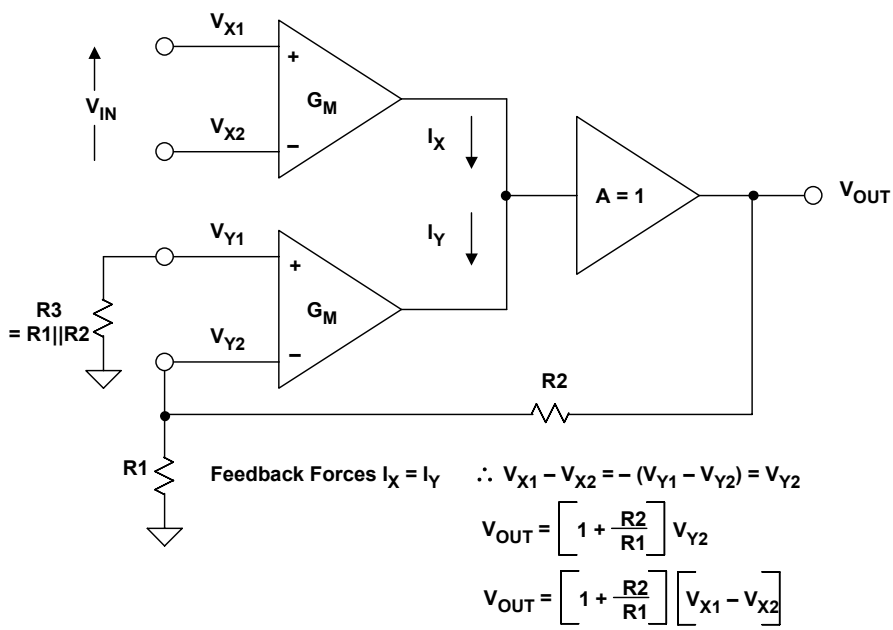


Figure 6-100: *The AD830/AD8129/AD8130 active feedback amplifier topology*

An important point of this architecture is that high CM rejection is provided by the two differential input pairs, so *CMR is not dependent on resistor bridges* and their associated matching problems. The inherently wideband balanced circuit and the quasi-floating operation of the driven input provide the high CMR, which is typically 100dB at DC.

The general expression for the stage's gain "G" is like a non-inverting op amp, or:

$$G = \frac{V_{OUT}}{V_{IN}} = 1 + \frac{R2}{R1} \ . \qquad \text{Eq. 6-28}$$

As should be noted, this expression is identical to the gain of a non-inverting op amp stage, with R2 and R1 in analogous positions.

The AD8129 is a low-noise high-gain (G = 10 or greater) version of this family, intended for applications with very long cables where signal attenuation is significant. The related AD8130 device is stable at a gain of one. It is used for those applications where lower gains are required, such as a gain-of-two, for driving source and load terminated cables.

The AD8129 and AD8130 have a wide power supply range, from single +5V to ±12V, allowing wide common-mode and differential-mode voltage ranges. The wide common-mode range enables the driver/receiver pair to operate without isolation transformers in many systems where the ground potential difference between driver and receiver locations is several volts. Both devices include a logic-controlled power-down function.

Both devices have high, balanced input impedances, and achieve 70dB CMR @ 10MHz, providing excellent rejection of high-frequency common-mode signals. Figure 6-101 below shows AD8130 CMR for various supplies. As can be noted, it can be as high as 95dB at 1MHz, an impressive figure considering that no trimming is required.

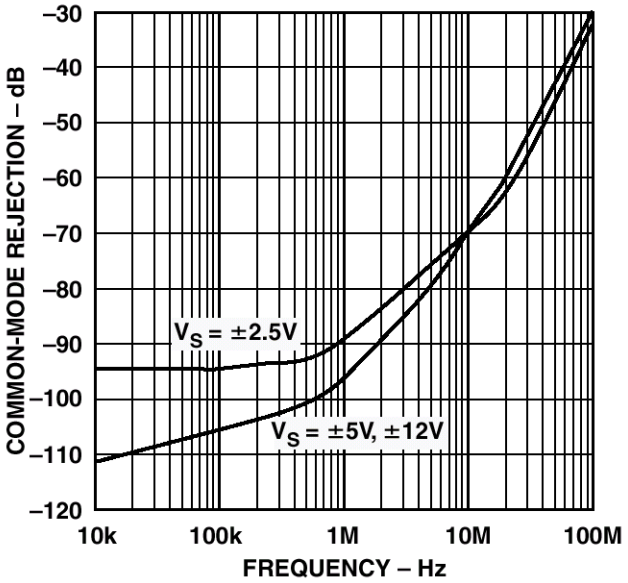


Figure 6-101: *AD8130 common-mode rejection versus frequency for ±2.5V, ±5V, and ±12V supplies*

The typical 3dB bandwidth for the AD8129 is 200MHz, while the 0.1dB bandwidth is 30MHz in the SOIC package, and 50MHz in the µSOIC package. The conditions for these specifications are for V_S = ±5V and G = 10.

The typical 3dB bandwidth for the AD8130 is 270MHz, and the 0.1dB bandwidth is 45MHz, in either package. The conditions for these specifications are for V_S = ±5V and G = 1. Typical differential gain and phase specifications for the AD8130 for G = 2, V_S = ±5V, and R_L = 150Ω are 0.13% and 0.15°, respectively.

A Cable-Tap or Loopthrough Amplifier

Figure 6-102 below shows an example of a video *cable-tap* amplifier (or *loopthrough*) connection where the input signal is tapped from a coax line and applied to one input stage of the AD8130, with the output signal tied to the second input stage. The net gain is unity. Functionally, the input and local grounds are isolated by the CMR of the AD8130, which is typically 70dB at 10MHz. Note that in order to provide a DC path for the input bias currents of the upper stage, there must be a common path between the source and local grounds (shown as Z_{CM}). This impedance is not critical, but must be low enough that 60Hz noise and other voltage components remain within the AD8130's CM range.

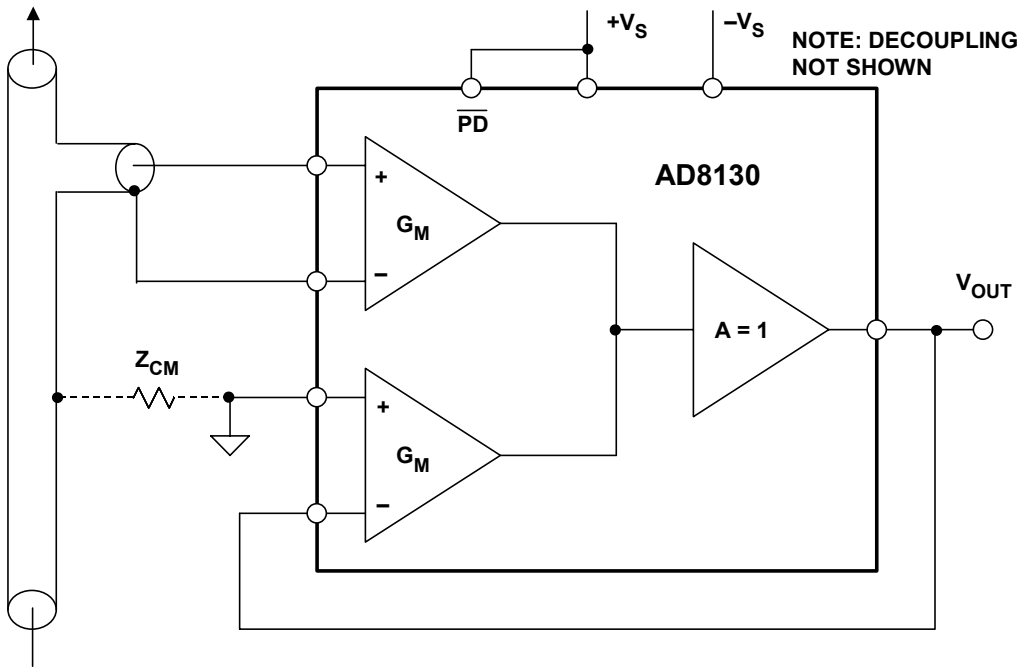


Figure 6-102: *Video "cable-tap" amplifier using the AD8130*

The circuit is efficient with the simplicity as shown, and requires no gain set resistors, etc. to implement. Normal bypass capacitors and supply decoupling must of course be used, as in any high-speed circuit. Other than the necessary DC path for the two inputs, it has little affect on the video cable it is monitoring, due to the high impedance AD8130 inputs. The circuit just as shown operates on supplies of ±5V to ±12V, but a ±15V version can also be implemented by using the AD830 (without the AD8130's power down function).

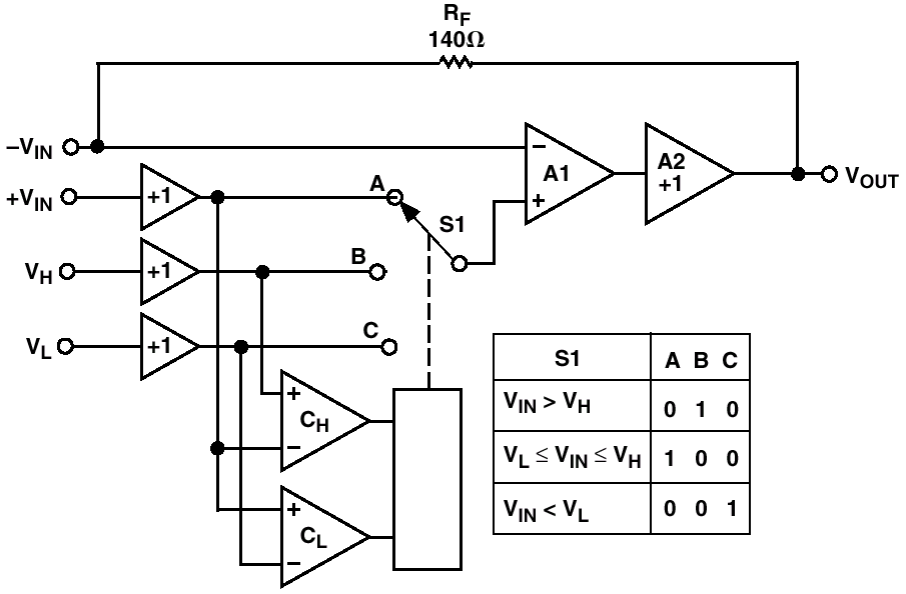
This circuit can also act as a video repeater, by connecting equal value feedforward and feedback resistors to implement a gain-of-two, for driving a source and load-terminated video cable (i.e., R2 and R1, as in Fig. 6-100, again).

Further application examples of this family of active feedback amplifiers are contained in the "Amplifier Ideas" section of this chapter, plus of course the device data sheets.

High Speed Clamping Amplifiers

There are many situations where it is desirable to *clamp* the output of an op amp, to prevent overdriving following circuitry. Specially designed high speed, fast recovery clamping amplifiers offer an attractive alternative to designing external clamping/protection circuits. The AD8036/AD8037 low distortion, wide bandwidth clamp amplifiers represent a significant breakthrough in this technology. These devices allow the designer to specify a high (V_H) and low (V_L) clamp voltage. The output of the device clamps when the input exceeds either of these two levels. The AD8036/AD8037 offer superior clamping performance compared to competing devices that use output-clamping. Recovery time from overdrive is less than 5ns, and small signal bandwidth is 240MHz (AD8036) and 270MHz (AD8037).

The key to the AD8036 and AD8037's fast, accurate clamp and amplifier performance is their proprietary input clamp architecture. This new design reduces clamp errors by more than 10x over previous output clamp based circuits, as well as substantially increasing the bandwidth, precision, and versatility of the clamp inputs.



S1	A	B	C
$V_{IN} > V_H$	0	1	0
$V_L \le V_{IN} \le V_H$	1	0	0
$V_{IN} < V_L$	0	0	1

Figure 6-103: *AD8036/AD8037 clamp amplifier equivalent circuit*

Figure 6-103 above is an idealized block diagram of the AD8036 clamp amplifier, connected as a unity gain voltage follower. The primary signal path comprises A1 (a 1200V/µs, 240MHz high voltage gain, differential to single-ended amplifier) and A2 (a G=+1 high current gain output buffer). The AD8037 differs from the AD8036 only in that A1 is optimized for closed-loop gains of two or greater.

The input clamp section is comprised of comparators C_H and C_L, which drive switch S1 through a decoder. The unity-gain buffers before the $+V_{IN}$, V_H, and V_L inputs isolate the input pins from the comparators and S1, without reducing bandwidth or precision. The two comparators have about the same bandwidth as A1 (240MHz), so they can keep up with signals within the useful bandwidth of the AD8036. To illustrate the operation of the

input clamp circuit, consider the case where V_H is referenced to +1V, V_L is open, and the AD8036 is set for a gain of +1 by connecting its output back to its inverting input through the recommended 140Ω feedback resistor. Note that the main signal path always operates closed loop, since the clamping circuit only affects A1's non-inverting input.

If a 0V to +2V voltage ramp is applied to the AD8036's $+V_{IN}$ for the connection, V_{OUT} should track $+V_{IN}$ perfectly up to +1V, then limit at exactly +1V as $+V_{IN}$ continues to +2V. In practice, the AD8036 comes close to this ideal behavior. As the $+V_{IN}$ input voltage ramps from zero to 1V, the output of the high limit comparator C_H starts in the off state, as does the output of C_L. When $+V_{IN}$ just exceeds V_H (practically, by about 18mV), C_H changes state, switching S1 from "A" to "B" reference level. Since the + input of A1 is now connected to V_H, further increases in $+V_{IN}$ have no effect on the AD8036's output. The AD8036 is now operating as a unity-gain buffer for the V_H input, as any variation in V_H, for $V_H > 1V$, will be faithfully produced at V_{OUT}.

AD8036 operation for negative inputs and negative V_L clamp levels is similar, with comparator C_L controlling S1. Since the comparators see the voltage on the $+V_{IN}$ pin as their common reference level, the voltage V_H and V_L are defined as "High" or "Low" with respect to $+V_{IN}$. For example, if V_{IN} is zero volts, V_H is open, and V_L is +1V, comparator C_L will switch S1 to "C", and the AD8036 will buffer the V_L voltage and ignore $+V_{IN}$.

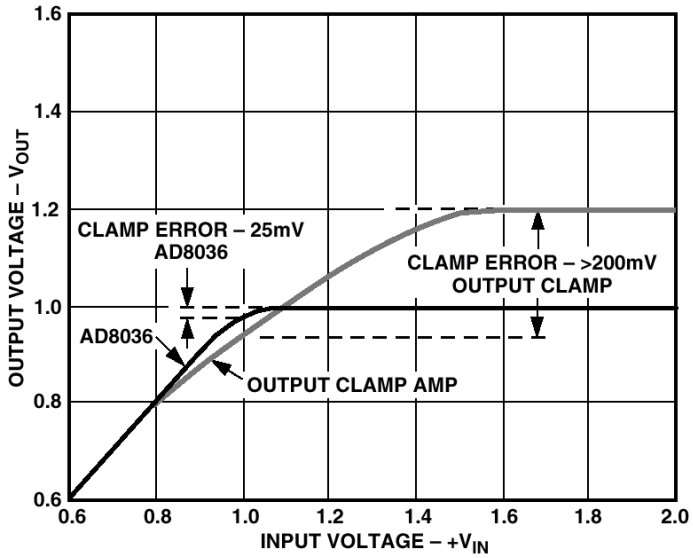


Figure 6-104: *Comparison between input and output clamping*

The AD8036/AD8037 performance closely matches the described ideal. The comparator's threshold extends from 60mV inside the clamp window defined by the voltages on V_L and V_H to 60mV beyond the window's edge. Switch S1 is implemented with current steering, so that A1's + input makes a continuous transition from say, V_{IN} to V_H as the input voltage traverses the comparator's input threshold from 0.9V to 1.0V for V_H = 1.0V.

The practical effect of the non-ideal operation softens the transition from amplification to clamping modes, without compromising the absolute clamp limit set by the input clamping circuit. Figure 6-104 above is a graph of V_{OUT} versus V_{IN} for the AD8036 and a typical *output* clamp amplifier. Both amplifiers are set for G=+1 and V_H = +1V. The

worst case error between V_{OUT} (ideally clamped) and V_{OUT} (actual) is typically 18mV times the amplifier closed-loop gain. This occurs when V_{IN} equals V_H (or V_L). As V_{IN} goes above and/or below this limit, V_{OUT} will stay within 5mV of the ideal value.

In contrast, the output clamp amplifier's transfer curve typically will show some compression starting at an input of 0.8V, and can have an output voltage as far as 200mV over the clamp limit. In addition, since the output clamp causes the amplifier to operate open-loop in the clamp mode, the amplifier's output impedance will increase, potentially causing additional errors, and the recovery time is significantly longer.

Flash Converter with Clamp Amp Input Protection

Figure 6-105 below shows the AD9002 8-bit, 125MSPS flash converter driven by the AD8037 (240MHz bandwidth) clamping amplifier. The clamp voltages on the AD8037 are set to +0.55 and –0.55V, referenced to the ±0.5V input signal, with the twin 806Ω/100Ω external resistive dividers. The AD8037 also supplies a gain of two, and an offset of –1V (using the AD780 voltage reference), to match the 0 to –2V input range of the AD9002 flash converter. The output signal is clamped at +0.1V and –2.1V.

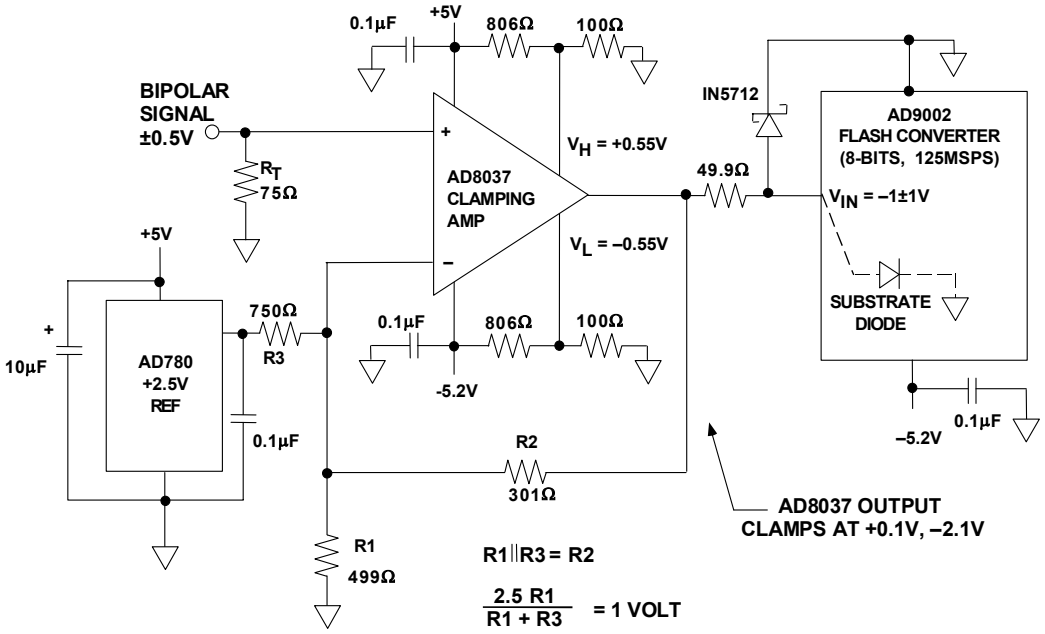


Figure 6-105: *AD9002 8-bit, 125MSPS flash converter driven by AD8037 clamp amplifier*

This multi-function clamping circuit therefore performs several important functions as well as preventing damage to the flash converter (which would otherwise occur should the input exceed +0.5V, thereby forward biasing the substrate diode). The 1N5712 Schottky diode is a safety-valve device, adding further protection for the flash converter during power-up.

There are multiple criteria that must be met in designing the feedback network around the AD8037. These are a specified gain, and a fixed offset which will enable the output swing of the clamped amplifier to match the target input range of the converter.

The feedback resistor, R2 = 301Ω, is selected for optimum bandwidth per the data sheet recommendation. For a gain of two, the parallel combination of R1 and R3 must also equal R2:

$$\frac{R1 \cdot R3}{R1 + R3} = R2 = 301\Omega \ , \qquad \text{Eq. 6-29}$$

(nearest 1% standard resistor value).

In addition, the Thevenin equivalent output voltage from the AD780 +2.5V reference and the R3/R1 divider must be +1V, to provide the required –1V offset at the output of the AD8037. This will cause the output swing of the AD8037 to be biased at –1V when V_{IN} is zero, and to range from 0 to –2V as V_{IN} ranges from –0.5 to 0.5V.

$$\frac{2.5 \cdot R1}{R1 + R3} = 1\text{volt} \ . \qquad \text{Eq. 6-30}$$

Solving these equations yields resistance values of R1 = 499Ω, R3 = 750Ω, using the nearest 1% standard values.

Other input and output voltages ranges can also be accommodated, by appropriate changes in the external resistors.

Further fast clamping op amp application examples are given in Reference 9, and the "Amplifier Ideas" section of this chapter (plus of course the device data sheets).

High Speed Video Multiplexing with Op Amps Utilizing Disable Function

A common video circuit function is the multiplexer, a stage which selects one of "n" video inputs and transmits a buffered version of the selected signal to the output. A number of video op amps (AD810, AD813, AD8013, AD8074/AD8075) have a *disable* mode which, when activated by applying the appropriate control level to a pin on the package, disables the op amp output stage and drops the power to a lower value.

In the case of the AD8013 (triple current-feedback op amp), asserting any one of the disable pins about 1.6V from the negative supply will put the corresponding amplifier into a disabled, powered-down state. In this condition, the amplifier's quiescent current drops to about 0.3mA, its output becomes a high impedance, and there is a high level of isolation from the input to the output. In the case of the gain-of-two line driver, for example, the impedance at the output node will be about equal to the sum of the feedback and feedforward resistors (1.6kΩ) in parallel with about 12pF capacitance. Input-to-output isolation is about 66dB at 5MHz.

Leaving the disable pin disconnected (floating) will leave the corresponding amplifier operational (i.e., enabled). The input impedance of the disable pin is about 40kΩ in parallel with 5pF. When driven to 0V, with the negative supply at –5V, about 100µA flows into the disable pin.

When the disable pins are driven by CMOS logic, on a single +5V supply, the disable and enable times are about 50ns. When operated on dual supplies, level shifting will be required from standard logic outputs to the disable pins.

The AD8013's input stages include protection from the large differential voltages that may be applied when disabled. Internal clamps limit this voltage to about ±3V. The high input-to-output isolation will be maintained for voltages below this limit.

Wiring the amplifier outputs together as shown in Figure 6-106 (opposite) forms a 3:1 multiplexer with about 50ns switching time between channels. The 0.1dB bandwidth of the circuit is 35MHz, and the OFF channel isolation is 60dB at 10MHz. The simple logic level-shifting circuit shown on the diagram does not significantly affect switching time.

Setting up this amplifier is not entirely straightforward, and some explanation will help with subtleness. The feedback resistor R2 of 845Ω was chosen first, to allow optimum bandwidth of the AD8013 current feedback op amp. The analogous resistors of the other channels use an identical value, for similar reasons.

Note that when any given channel is ON, it must drive both the termination resistor R_L, and the net dummy resistance, $R_X/2$, where R_X is an equivalent series resistance equal to R1 + R2 + R3. To provide a net overall gain of unity, as well as an effective source resistance of 75Ω, the other resistor values must be as shown. In essence, the Thevenin

equivalent value of $R_X/2$ and R3 should equal the desired source termination impedance of 75Ω (which it does).

It is also desirable that the ON channels have a net gain of 2x, as seen behind the 75Ω output impedance. The lower value of R1 vis-à-vis R2, along with the above relationship, allows these mutual criteria to be met.

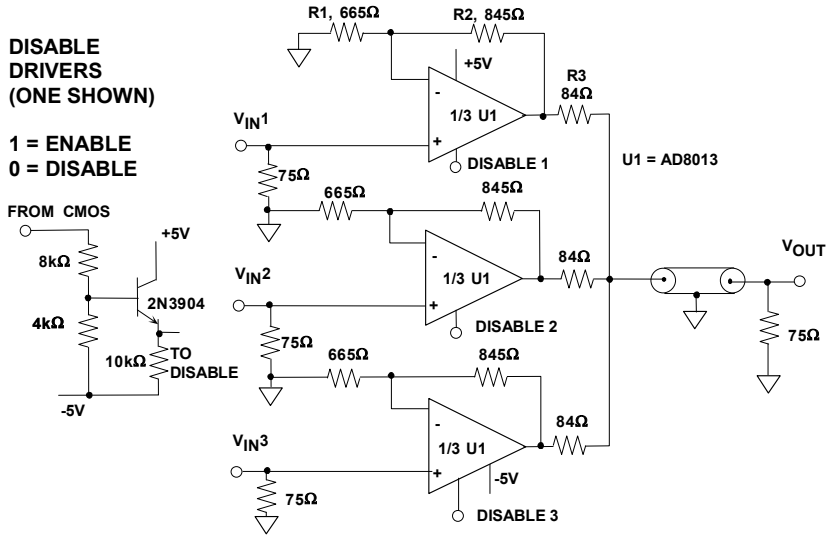


Figure 6-106: AD8013 3:1 video multiplexer switches in 50ns

Configuring two amplifiers of an AD8013 as unity gain followers with the third to set the gain results in a high performance 2:1 multiplexer, as shown in Figure 6-107 below.

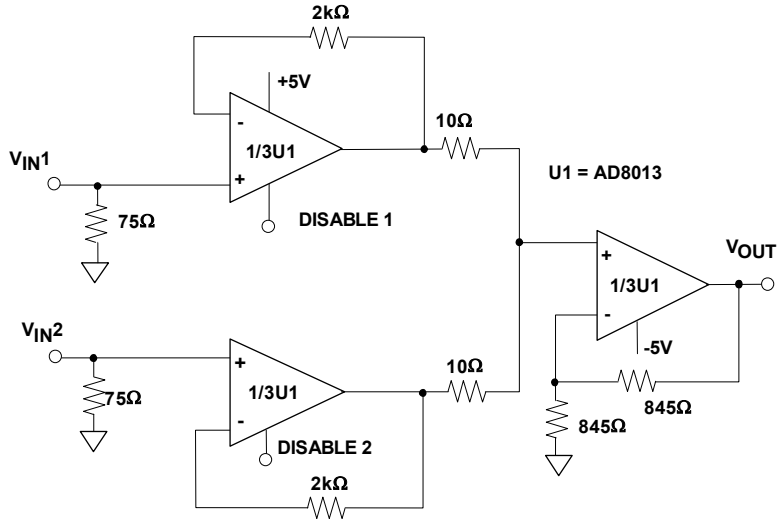


Figure 6-107: *2:1 video multiplexer based on the AD8013*

This circuit takes advantage of the low crosstalk between the amplifiers, and achieves an OFF channel isolation of 50dB at 10MHz. The differential gain and phase performance of the circuit is 0.03% and 0.07°, respectively. The output stage operates at again of 2x, and can drive a 75Ω source terminated line if desired.

Programmable Gain Amplifier using the AD813 Current Feedback Video Op Amp

Closely related to the multiplexers described above is a programmable gain video amplifier, or PGA, as shown in Figure 6-108 below. In the case of the AD813, the individual channels are disabled by pulling the disable pin about 2.5V below the positive supply. This puts the corresponding amplifier in its powered down state. In this condition, the amplifier's quiescent supply current drops to about 0.5mA, its output becomes a high impedance, and there is a high level of isolation between the input and the output. Leaving the disable pin disconnected (floating) will leave the amplifier operational, in the enabled state. When grounded, about 50µA flows out of a disable pin when operating on ±5V supplies. The switching threshold is such that the disable pins can be driven directly from +5V CMOS logic as shown, with no level shifting (as in the previous example).

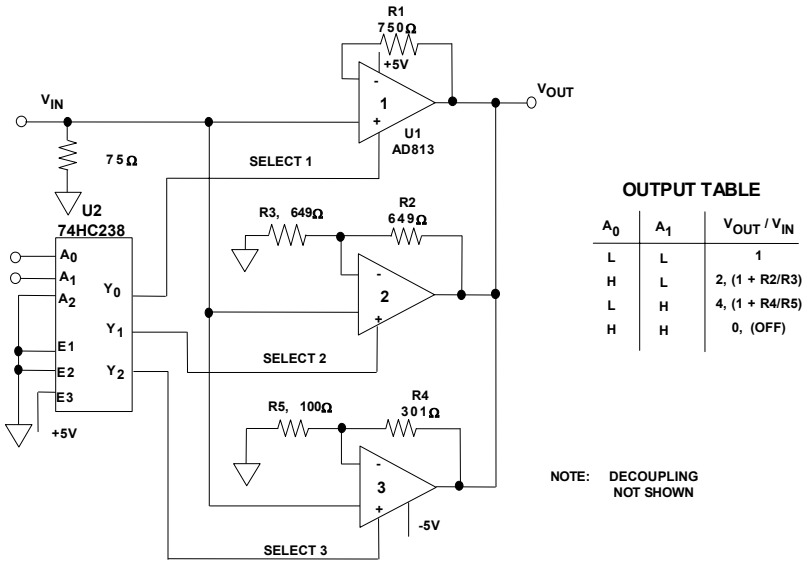


Figure 6-108: *Programmable gain video amplifier using the AD813 triple current feedback amplifier*

With a two-line digital control input, this circuit can be set up to provide 3 different gain settings. This makes it a useful circuit in various systems which can employ signal normalization or gain ranging prior to A/D conversion, such as CCD systems, ultrasound, etc. The gains can be binary related as here, or they can be arbitrary. An extremely useful feature of the AD813 CFB current feedback amplifier is the fact that the bandwidth does not reduce as gain is increased. Instead, it stays relatively constant as gain is raised. Thus, more useful bandwidth is available at the higher programmed gains than would be true for a fixed gain-bandwidth product VFB amplifier type.

In the circuit, channel 1 of the AD813 is a unity gain channel, channel 2 has a gain of 2, and channel 3 a gain of 4, while the fourth control state is OFF. As is indicated by the table, these gains can easily be varied by adjustment of the R2/R3 or R4/R5 ratios. For the gain range and values shown, the PGA will be able to maintain a 3dB bandwidth of about 50MHz or more for loading as shown (a high impedance load of 1kΩ or more is assumed). Fine tuning the bandwidth for a given gain setting can be accomplished by lowering the resistor values at the higher gains, as shown in the circuit, where for G=1, R1=750Ω, for G=2, R2=649Ω, and for G=4, R4=301Ω.

Integrated Video Multiplexers and Crosspoint Switches

Traditional CMOS switches and multiplexers suffer from several disadvantages at video frequencies. Their switching time (typically 100ns or so) is not fast enough for today's applications, and they require external buffering in order to drive typical video loads. In addition, the small variation of the CMOS switch "on" resistance with signal level (R_{on} *modulation*) introduces unwanted distortion in differential gain and phase. Multiplexers based on complementary bipolar technology offer a better solution at video frequencies.

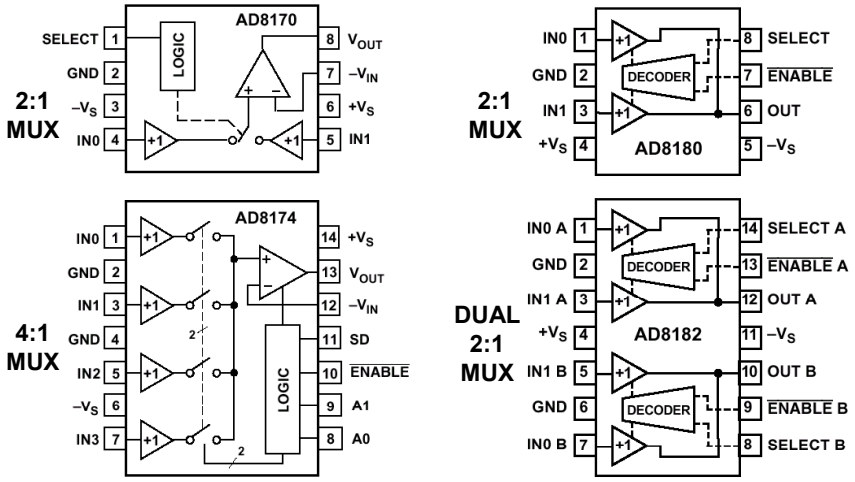


Figure 6-109: *AD8170/8174/8180/8182 bipolar video multiplexers*

Functional block diagrams of the AD8170/8174/8180/8182 bipolar video multiplexer are shown in Figure 6-109 above. The AD8183/AD8185 video multiplexer is shown in Figure 6-110, below. These devices offer a high degree of flexibility and are ideally suited to video applications, with excellent differential gain and phase specifications. Switching time for all devices in the family is 10ns to 0.1%.

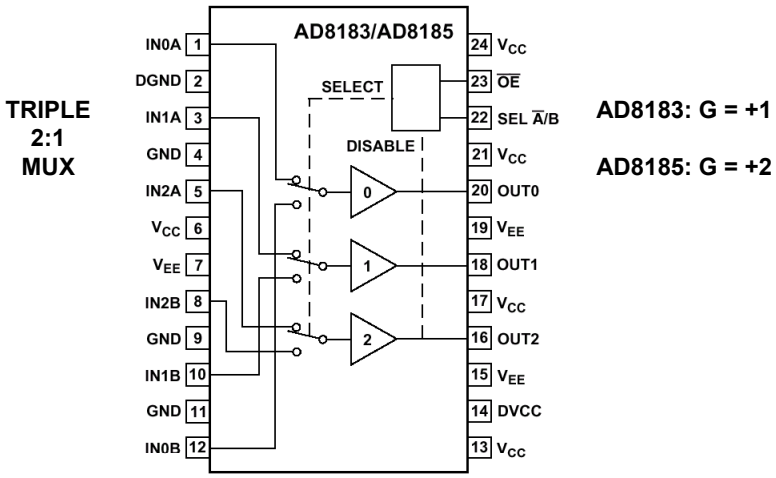


Figure 6-110: *AD8183/AD8185 triple 2:1 video multiplexers*

The AD8170/8174 series of muxes include an on-chip current feedback op amp output buffer whose gain can be set externally. Off channel isolation and crosstalk are typically greater than 80dB for the entire family.

Dual RGB Source Video Multiplexer

Figure 6-111 below shows an application circuit for three AD8170 2:1 muxes, where a single RGB monitor is switched between two RGB computer video sources.

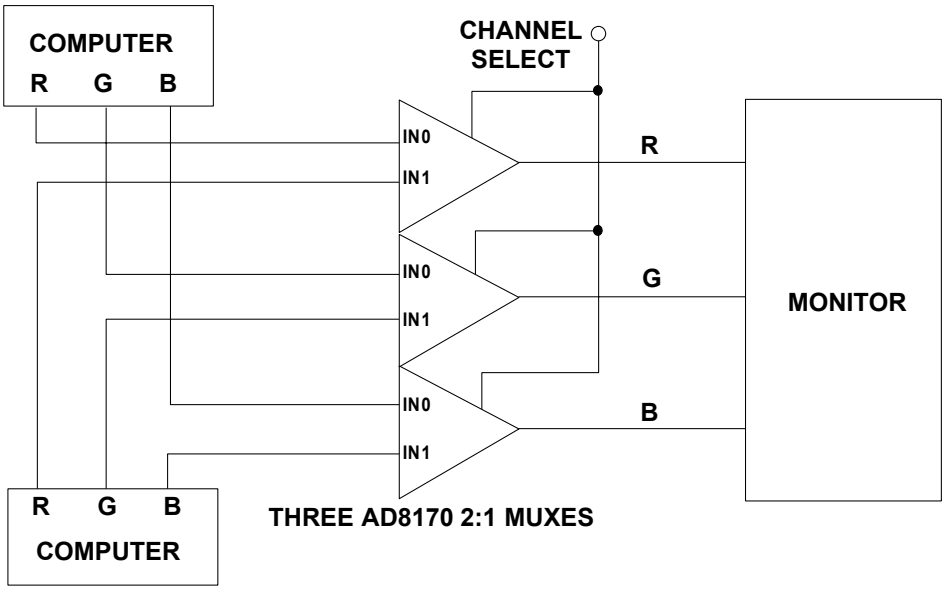


Figure 6-111: *Dual source RGB multiplexer using three 2:1 muxes*

In this setup, the overall effect is that of a three-pole, double-throw switch. The three video sources constitute the three poles, and either the upper or lower of the video sources constitute the two switch states.

Digitizing RGB Signals With One ADC

The AD8174 4:1 mux is used in Figure 6-112 below, to allow a single high speed ADC to digitize the RGB outputs of a scanner.

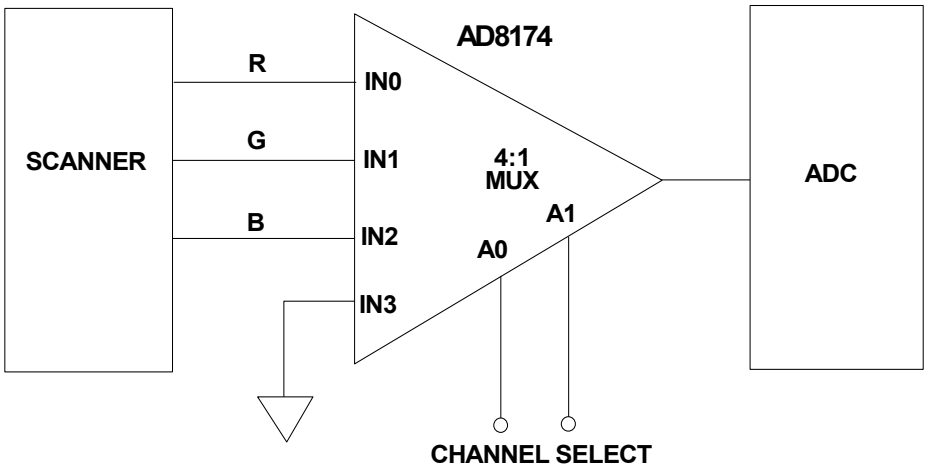


Figure 6-112: *Digitizing RGB signals with one ADC and a 4:1 mux*

The RGB video signals from the scanner are fed in sequence to the ADC, and digitized in sequence, making efficient use of the scanner data with one ADC.

Figure 6-113 below shows two AD8174 4:1 muxes functionally expanded into an 8:1 multiplexer. The A0 and A1 inputs are conventional, with complemented Enable inputs.

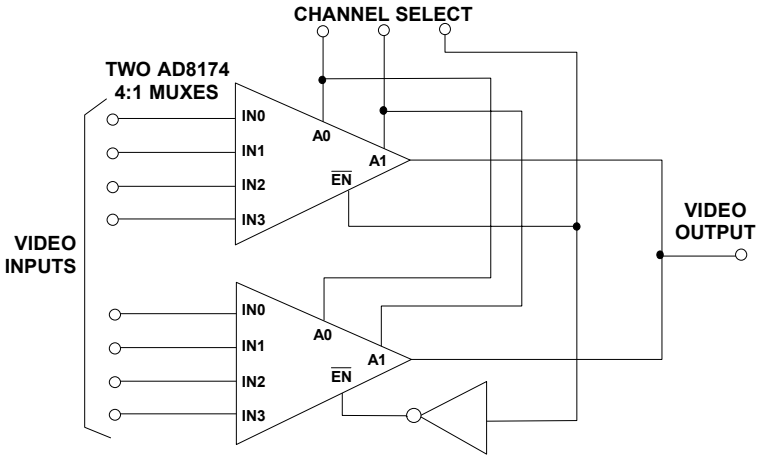


Figure 6-113: *Expanding two 4:1 muxes into an 8:1 mux*

The AD8116 extends the mux concepts to a fully integrated, 16×16 buffered video crosspoint switch matrix (Figure 6-114). The 3dB bandwidth is greater than 200MHz, and the 0.1dB gain flatness extends to 60MHz. Channel switching time is less than 30ns to 0.1%. Channel-to-channel crosstalk is −70dB measured at 5MHz. Differential gain and phase is 0.01% and 0.01° for a 150Ω load. Total power dissipation is 900mW on ±5V.

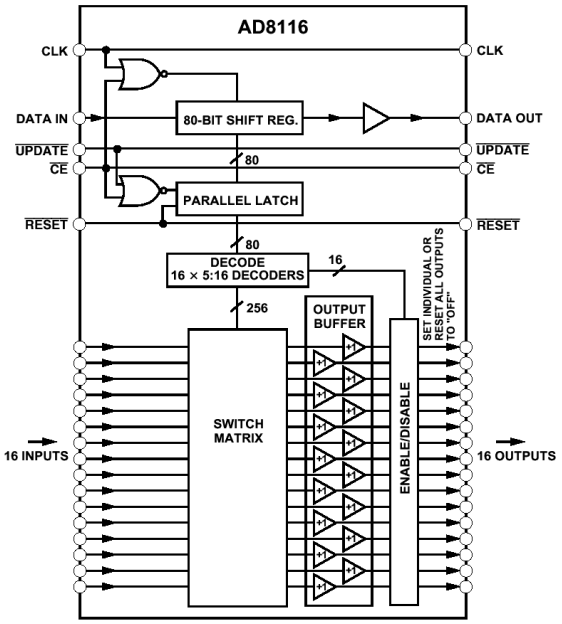


Figure 6-114: *AD8116 16×16 200MHz buffered video crosspoint switch*

The AD8116 includes output buffers that can be put into a high impedance state for paralleling crosspoint stages so that the off channels do not load the output bus. The channel switching is performed via a serial digital control that can accommodate "daisy chaining" of several devices. The AD8116 package is a 128-pin 14mm×14mm LQFP. Other members of the crosspoint switch family include the AD8110/AD8111 260MHz 16×8 buffered crosspoint switch, the AD8113 audio/video 60MHz 16×16 crosspoint switch, and the AD8114/AD8115 low cost 225MHz 16×16 crosspoint switch.

Single Supply Video Applications

Optimum video performance in terms of differential gain and phase, bandwidth flatness, etc., is generally achieved using dual supplies of ±5V or ±12V. In many applications, however, stringent broadcast standards are not required, and single-supply operation may be desirable from a cost and power standpoint. This section illustrates a few op amp single-supply applications. All of the op amps are fully specified for both ±5V and +5V (and +3V where the design supports it). Both rail-to-rail and non-rail-to-rail applications are shown (details of rail-to-rail op amp topologies are discussed in Chapter 1).

Single-Supply RGB Buffer

Op amps such as the AD8041/AD8042/ and AD8044 can provide buffering of RGB signals that include ground, while operating from a single +3V or +5V supply. The signals that drive an RGB monitor are usually supplied by current output DACs that operate from a single +5V supply. Examples are triple video DACs such as the ADV7120/21/22 from Analog Devices.

During the horizontal blanking interval, the current output of the DACs goes to zero, and the RGB signals are pulled to ground by the termination resistors. If more than one RGB monitor is desired, it cannot simply be connected in parallel because this would be a mis-termination. Therefore, buffering must be provided before connecting a second monitor.

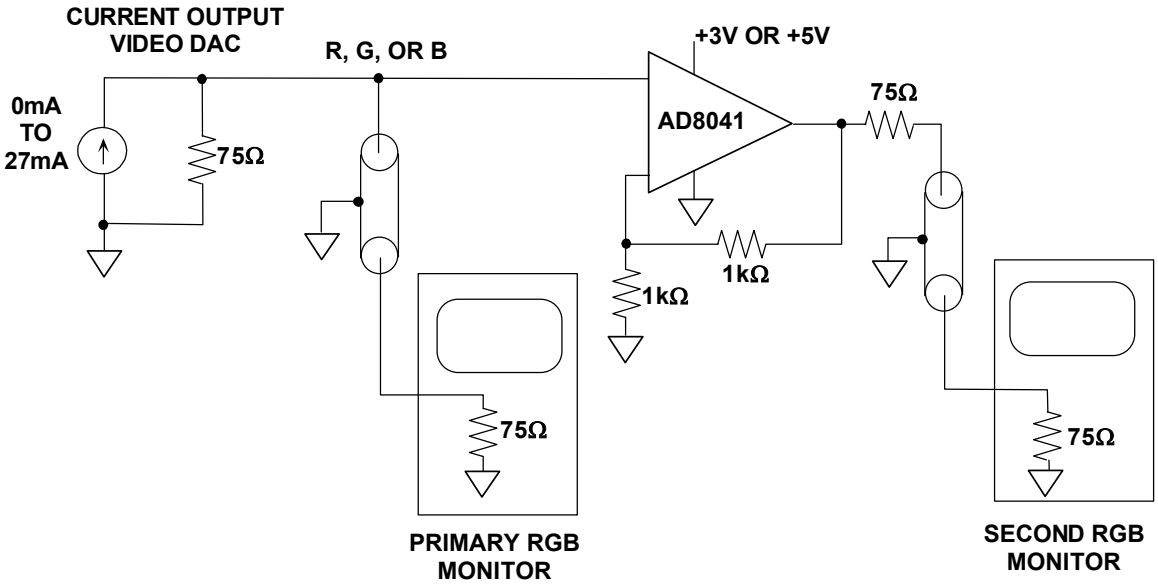


Figure 6-115: *Single-supply RGB buffer operates on +3V or +5V*

RGB signals include ground as part of their dynamic output range. Previously a dual supply op amp has been required for this buffering, with sometimes this being the only component requiring a negative supply. This makes it quite inconvenient to incorporate a multiple monitor feature. Figure 6-115 shows a diagram of one channel of a single supply op amp gain-of-two buffer, for driving a second RGB monitor. No current is required when the amplifier output is at ground. The termination resistor at the monitor helps pull the output down at low voltage levels.

Note that the input and output are at ground during the horizontal blanking interval. The RGB signals are specified to output a maximum of 700mV peak. The peak output of the AD8041 is +1.4V, with the termination resistors providing a divide-by-two. All three channels (RGB) signals can be buffered in a like manner with duplication of this circuit. Another possibility is to use three sections of the (similar) quad AD8044 op amp.

Single-Supply Sync Stripper

Some RGB monitors use only three cables total and carry the synchronizing signals and the Green (G) signal on the same cable (Green-with-sync). The sync signals are pulses that go in the negative direction from the blanking level of the G signal.

In some applications, for example prior to digitizing component video signals with ADCs, it is desirable to remove or strip the sync portion from the G signal. Figure 6-116 is a circuit using the AD8041 running on a single +5V supply to perform this function. The signal at V_{IN} is the Green-with-sync signal from an ADV7120, a single supply triple video DAC.

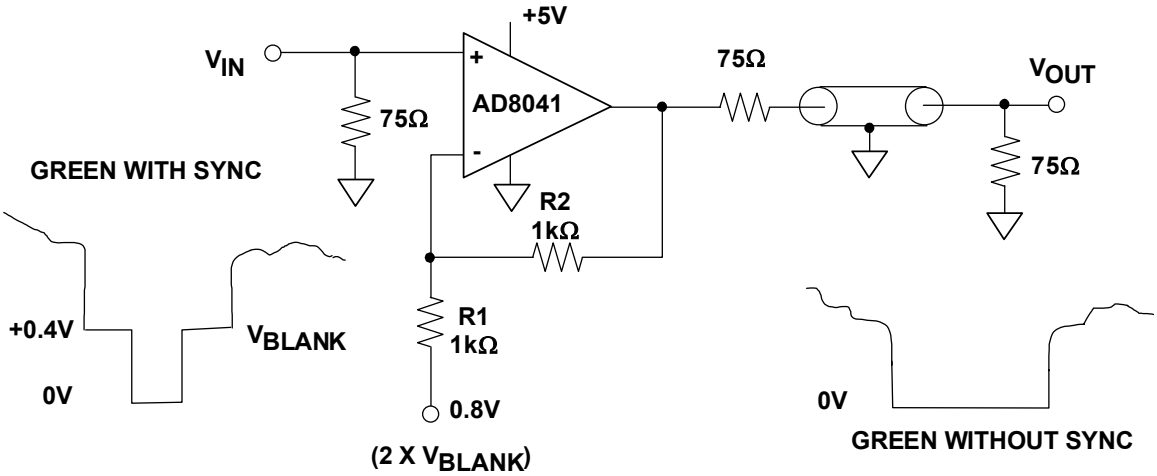


Figure 6-116: *Single-supply video sync stripper*

Because of the fact that the DAC used is single supply, the lowest level of the sync tip is at ground or slightly above. The AD8041 is set for a gain of two to compensate for the divide-by-two of the output terminations.

In this setup, the op amp used must have a CM capability that includes zero (as is true for the AD8041 family). For voltages *above* ½ the 0.8V reference level applied to R1, the op amp operates as a linear amplifier, going positive from ground level at the output. For inputs *below* the reference level, the op amp saturates, with the output going to ground as used here. The result is that the negative sync tips are removed.

The reference voltage for R1 is twice the DC blanking level of the G signal; normally, this is 2×0.4V = 0.8V. Alternately, if the blanking level is at ground and the sync tip is negative (as in some dual supply systems), then R1 is tied to ground. The resulting V_{OUT} will have the sync removed, and the blanking level at ground, as noted.

A Low Distortion, Single-Supply Video Line Driver with Zero-Volt Output

When operated with a single supply, the AD8031 80MHz rail-to-rail voltage feedback op amp has optimum distortion performance when the signal has a common mode level of $V_S/2$, and when there is also about 500mV of headroom to each rail. If this rule is violated, distortion performance suffers. But, if low distortion is required for signals close to ground, a level-shifting emitter follower can be used at the op amp output.

Figure 6-117 below shows an AD8031 op amp, configured as a single supply gain-of-two line driver. With the output driving a back terminated 50Ω line, the overall gain is unity from V_{IN} to V_{OUT}. In addition to minimizing reflections, the 50Ω back termination resistor protects the transistor from damage if the cable is short circuited.

The 2N3904 emitter follower inside the feedback loop ensures that the output voltage from the AD8031 always stays about 700mV (or more) above ground, which minimizes distortion. Using this circuit excellent distortion is obtained, even when the output signal swings to within 50mV of ground.

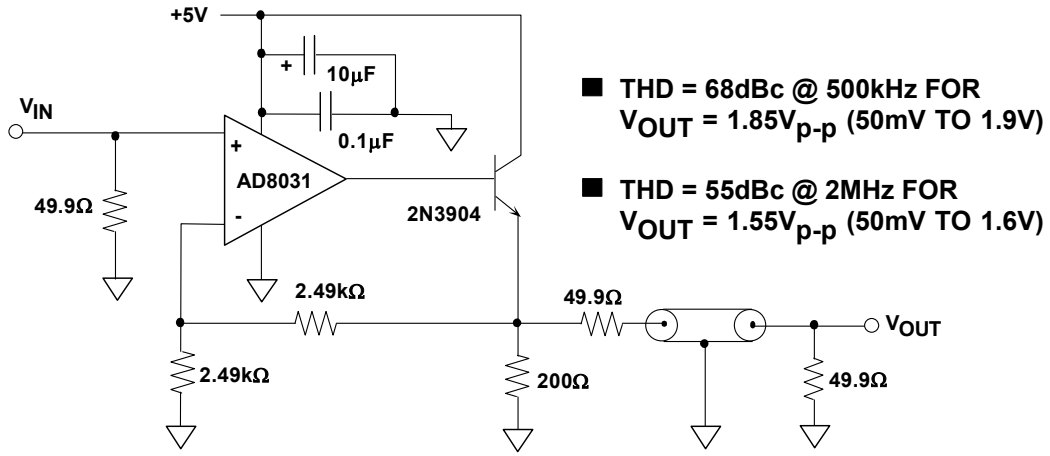


Figure 6-117: *Low distortion zero-volt output single-supply line driver using the AD8031*

The circuit was tested at 500kHz and 2MHz using a single +5V supply. For the 500kHz signal, THD was 68dBc with a peak-to-peak swing at a V_{OUT} of 1.85V (50mV to +1.9V). This corresponds to a signal at the emitter follower output of 3.7Vp-p (100mV to 3.8V). Data was taken with an output signal of 2MHz, and a THD of 55dBc was measured with a V_{OUT} of 1.55Vp-p (50mV to 1.6V).

This circuit can also be used to drive the analog input of a single supply high speed ADC whose input voltage range is ground-referenced. In this case, the emitter of the external transistor is connected to the ADC input, and the termination resistor is deleted. In this case, peak positive voltage swings of approximately 3.8V are possible before significant distortion begins to occur.

Headroom Considerations in AC-Coupled Single-Supply Video Circuits

The AC coupling of arbitrary waveforms can actually introduce problems that don't exist at all in DC coupled or DC restored systems. These problems have to do with the waveform duty cycle, and are particularly acute with signals that approach the rails, as they can in AC coupled, low supply voltage systems.

In Figure 6-118(A), an example of a 50% duty cycle square wave of about 2Vp-p level is shown, with the signal swing biased symmetrically between the upper and lower clip points of a 5V supply amplifier. Assume that the amplifier has a complementary emitter follower output and can only swing to the limited DC levels as marked, about 1V from either rail. In cases (B) and (C), the duty cycle of the input waveform is adjusted to both low and high duty cycle extremes *while maintaining the same peak-to-peak input level*. At the amplifier output, the waveform is seen to clip either negative or positive, in (B) and (C), respectively.

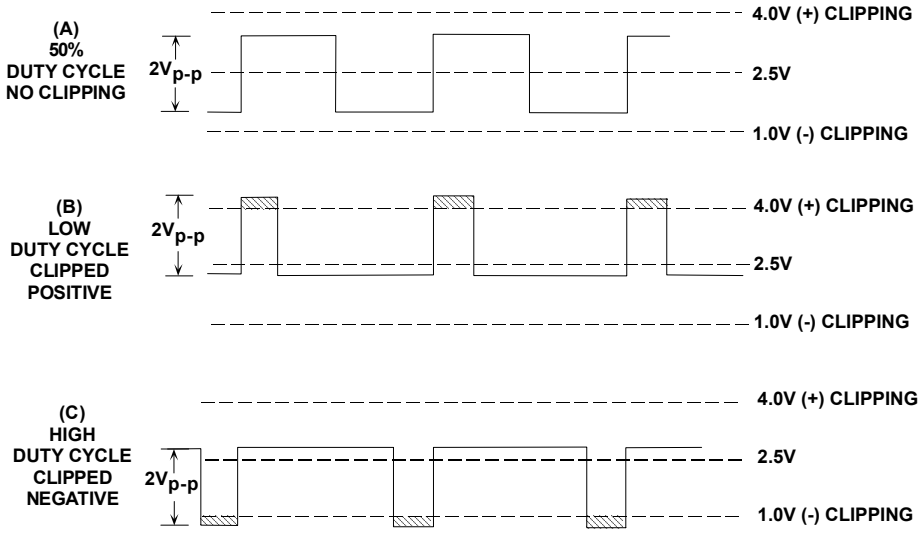


Figure 6-118: *Waveform duty cycle taxes headroom in AC coupled single-supply op amps*

Since standard video waveforms *do* vary in duty cycle as the scene changes, the point is made that low distortion operation on AC coupled single supply stages must take the duty cycle headroom degradation effect into account. If a stage has a 3Vp-p output swing available before clipping, and it must cleanly reproduce an *arbitrary* waveform, then the maximum allowable amplitude is less than ½ this 3Vp-p swing, that is <1.5Vp-p.

An example of violating this criteria are the 2Vp-p waveforms of Figure 6-118(B) and (C), which clip for both the low and high duty cycles. Note that the criteria set down above is based on avoiding hard clipping, while subtle distortion increases may in fact take place at lower levels. This suggests an even more conservative criterion for lowest distortion operation, such as in composite NTSC video amplifiers.

Single-supply AC coupled composite video line driver

Figure 6-119 shows a single supply gain-of-two composite video line driver using the AD8041. Since the sync tips of a composite video signal extend below ground, the input must be AC coupled and shifted positively to prevent clipping during negative excursions. The input is terminated in 75Ω and AC coupled via the 47µF to a voltage divider that provides the DC bias point to the input. Setting the optimal common-mode bias voltage requires some understanding of the nature of composite video signals and the video performance of the AD8041.

As discussed above, signals of bounded peak-to-peak amplitude that vary in duty cycle require larger dynamic swing capability than their peak-to-peak amplitude after AC coupling. As a worst case, the dynamic signal swing required will approach twice the peak-to-peak value. The two bounding cases are for a duty cycle that is mostly low, but occasionally goes high at a fraction of a percent duty cycle, and vice versa.

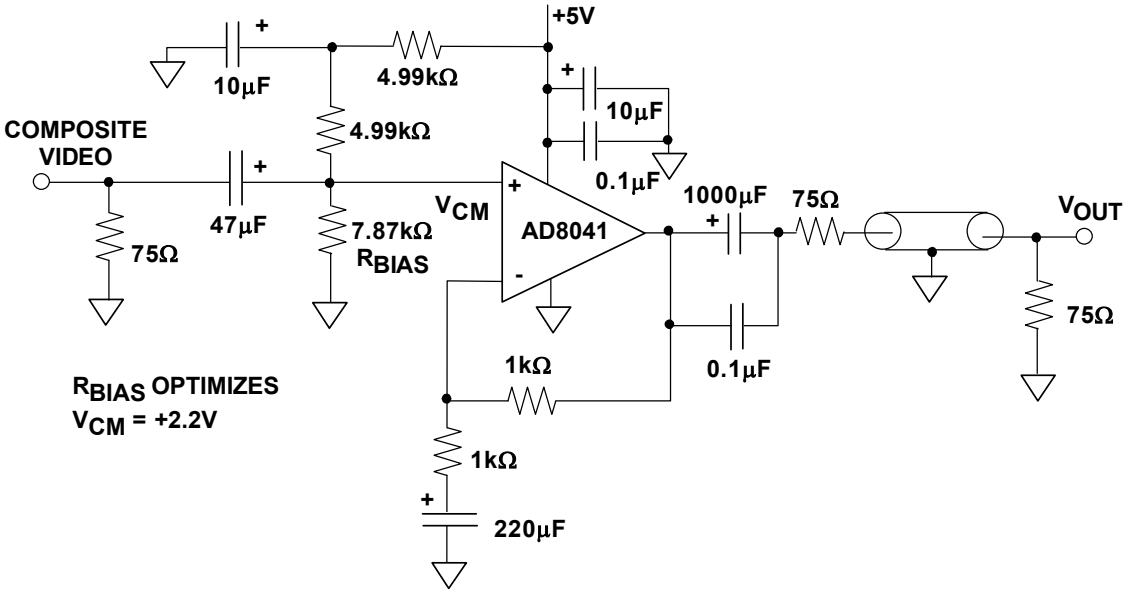


Figure 6-119: *Single-supply AC coupled composite video line driver has ΔG = 0.06% and $\Delta\phi$ = 0.06°*

Composite video is not quite this demanding. One bounding extreme is for a signal that is mostly black for an entire frame, but occasionally has a white (full intensity), minimum width spike at least once per frame.

The other extreme is for a video signal that is full white everywhere. The blanking intervals and sync tips of such a signal will have negative going excursions in compliance with composite video specifications. The combination of horizontal and vertical blanking intervals limit such a signal to being at its highest level (white) for about 75% of the time.

As a result of the duty cycle variations between the extremes presented above, a 1Vp-p composite video signal that is multiplied by a gain-of-two requires about 3.2Vp-p of dynamic voltage swing at the output for the op amp, to pass a composite video signal of arbitrary duty cycle without distortion.

The AD8041 device family not only has ample signal swing capability to handle the dynamic range required, but also has excellent differential gain and phase when buffering these signals in an AC coupled configuration.

To test this, the differential gain and phase were measured for the AD8041 while the supplies were varied. As the lower supply is raised to approach the video signal, the first effect is that the sync tips become compressed before the differential gain and phase are adversely affected. Thus, there must be adequate swing in the negative direction to pass the sync tips without compression.

As the upper supply is lowered to approach the video, the differential gain and phase were not significantly adversely affected until the difference between the peak video output and the supply reached 0.6V. Thus, the highest video level should be kept at least 0.6V below the positive supply rail.

Taking the above into account, it was found that the optimal point to bias the non-inverting input was at +2.2V DC. Operating at this point, the worst case differential gain was 0.06% and the differential phase 0.06°.

The AC coupling capacitors used in the circuit may at first glance appear quite large. There is a reason for this. Note that a composite video signal has a lower frequency band edge of 30Hz. The resistances at the various AC coupling points— especially at the output— are quite small. In order to minimize phase shifts and baseline tilt, the large value capacitors shown are required for best waveform reproduction.

For video system performance that is not to be of the highest quality, the value of these capacitors can be reduced by a factor of up to five with only a slight observable change in the picture quality.

Single-Supply AC Coupled Single-Ended-to-Differential Driver

The circuit shown below in Figure 6-120 provides a flexible solution to differential line driving in a single-supply application and utilizes the dual AD8042. The basic operation of the cross-coupled configuration has been described earlier in this section. The input, V_{IN}, is a single-ended signal that is capacitively coupled into the feedforward resistor, R1. The non-inverting inputs of each half of the AD8042 are biased at +2.5V.

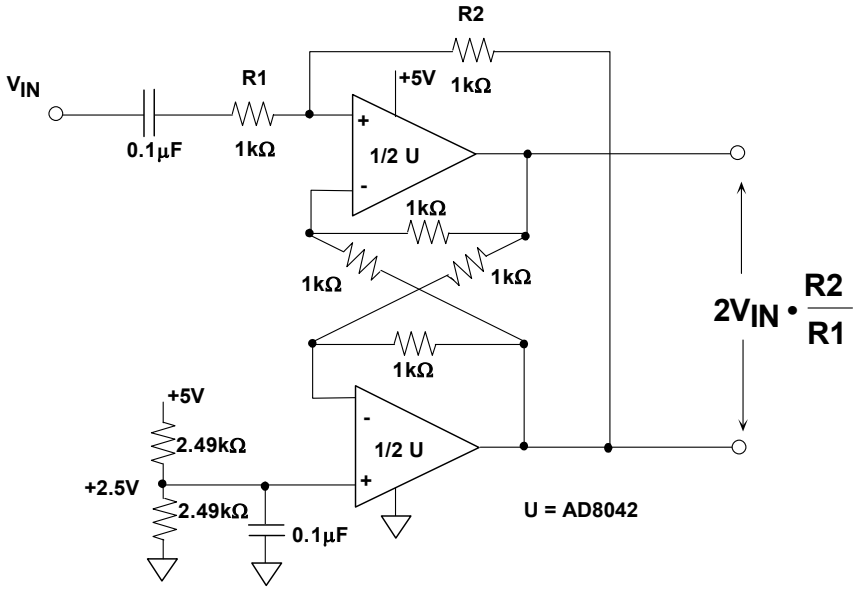


Figure 6-120: *Single-supply AC coupled differential driver*

The gain from single-ended input to the differential output is equal to 2R2/R1, as noted in the figure. If desired, this gain can be varied by simply changing one resistor (either R1 or R2). The input capacitor may need increase, for the processing of low frequency information with low phase shift.

It should also be noted that there is no output coupling capacitor, as none is required for differentially connected loads. The output terminals will be biased at approximately 2.5V.

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5. Dave Whitney, Walt Jung, "Applying a High-Performance Video Operational Amplifier," **Analog Dialogue**, 26-1, 1992.

6. Walt Jung, Scott Wurcer, "Design Video Circuits Using High-Speed Op-Amp Systems," **Electronic Design Analog Applications Issue**, November 7, 1994.

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8. Walt Kester, "Video Line Receiver Applications Using the AD830 Active Feedback Amplifier Topology," within Chapter 11 of Walt Kester, Editor, **System Application Guide**, Analog Devices, Inc., 1993, ISBN 0-916550-13-3.

9. Peter Checkovich, "Understanding and Using High-Speed Clamping Amplifiers," **Analog Dialogue**, Vol. 29-1, 1995.

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NOTES:

SECTION 6-4: COMMUNICATIONS AMPLIFIERS

Walt Kester

Components used in the signal path in communications systems must have wide dynamic range at high frequencies. Dynamic range is primarily limited by distortion and noise introduced by the active elements in amplifiers, mixers, etc. In the past, amplifiers for communications applications consisted primarily of "gain blocks" with appropriate specifications. Typically such amplifiers are specified for gain, bandwidth, distortion, etc., as a system is designed, and purchased as a self-contained package. This package itself is actually a communications amplifier sub-system.

Today, however, op amps with bandwidths of hundreds of megahertz, low noise, high dynamic range and flexible supply voltages also make popular building blocks in communications systems. They are easily configured for a given gain, and can deliver good performance.

Communications-Specific Specifications

As a necessity, this means that high frequency op amps must be fully specified not only in terms of traditional op amp AC specifications (bandwidth, slew rate, settling time), but also in terms of *communications-specific specifications*. These latter specifications would include performance for harmonic distortion, spurious free dynamic range (SFDR), intermodulation distortion, intercept points (IP2, IP3), noise, and noise figure (NF). Figure 6-121 illustrates these specifications, below.

- **Noise**
  - **Noise referred to input (RTI)**
  - **Noise referred to output (RTO)**
- **Distortion**
  - **Second and third order intercept points (IP2, IP3)**
  - **Spurious free dynamic range (SFDR)**
  - **Harmonic distortion**
    - **Single-tone**
    - **Multi-tone**
    - **Out-of-band**
  - **Multitone Power Ratio (MTPR)**
  - **Noise Factor (NF), Noise Figure (NF)**

Figure 6-121: *Dynamic range specifications in communications systems*

Within this portion of the chapter we will examine these specifications, and how they apply to the amplifiers used in wireless and wired communications systems. In addition, several application specific amplifiers such as variable gain amplifiers (VGAs), CATV drivers, and xDSL drivers will also be discussed.

Distortion Specifications

When a spectrally pure sinewave passes through an amplifier (or other active device), various harmonic distortion products are produced depending upon the nature and the severity of the non-linearity. However, simply measuring harmonic distortion produced by single tone sinewaves of various frequencies does not give all the information required to evaluate the amplifier's potential performance in a communications application. In most communications systems there are a number of channels which are "stacked" in frequency. It is often required that an amplifier be rated in terms of the intermodulation distortion (IMD) produced with two or more specified tones applied.

Intermodulation distortion products are of special interest in the IF and RF area, and a major concern in the design of radio receivers. Rather than simply examining the harmonic distortion or total harmonic distortion (THD) produced by a single tone sinewave input, it is often useful to look at the distortion products produced by two tones.

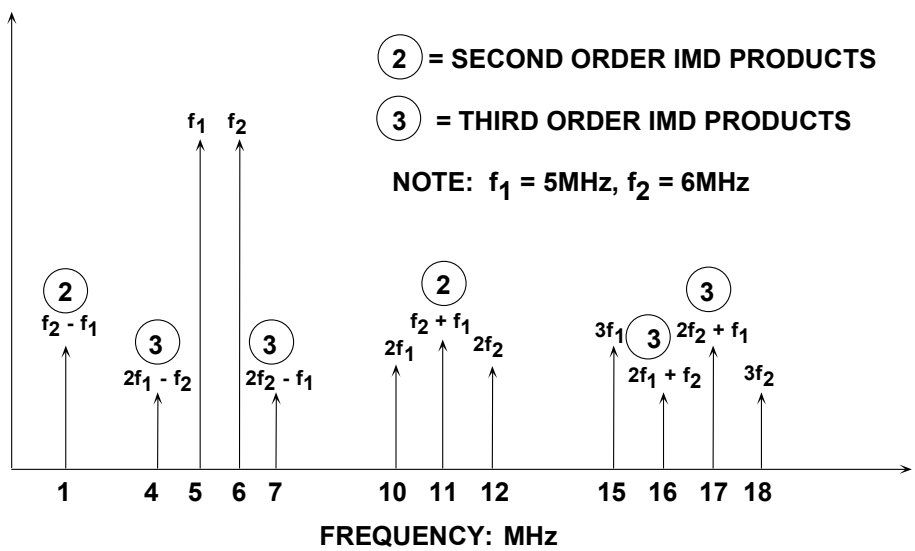


Figure 6-122: *Second and third order intermodulation distortion products*

As shown in Figure 6-122 above, two tones will produce second and third order intermodulation products. The example shows the second and third order products produced by applying two frequencies, f_1 and f_2, to a nonlinear device. The second order products located at f_2+f_1 and $f_2–f_1$ are located far away from the two tones, and may be removed by filtering. The third order products located at $2f_1+f_2$ and $2f_2+f_1$ may likewise be filtered. The third order products located at $2f_1–f_2$ and $2f_2–f_1$, however, are close to the original tones, and filtering them is difficult.

Third order IMD products are especially troublesome in multi-channel communications systems where the channel separation is constant across the frequency band. Third-order IMD products can mask out small signals in the presence of larger ones.

Third order IMD is often specified in terms of the *third order intercept* point, as is shown by Figure 6-123, below. Two spectrally pure tones are applied to the system. The output signal power in a single tone (in dBm) as well as the relative amplitude of the third-order products (referenced to a single tone) is plotted as a function of input signal power. The fundamental is shown by the *slope = 1* curve in the diagram. If the system non-linearity is approximated by a power series expansion, it can be shown that second-order IMD amplitudes increase 2dB for every 1dB of signal increase, as represented by *slope = 2* curve in the diagram.

Similarly, the third-order IMD amplitudes increase 3dB for every 1dB of signal increase, as indicated by the *slope = 3* plotted line. With a low level two-tone input signal, and two data points, one can draw the second and third order IMD lines as they are shown in Figure 6-123 (using the principle that a point and a slope define a straight line).

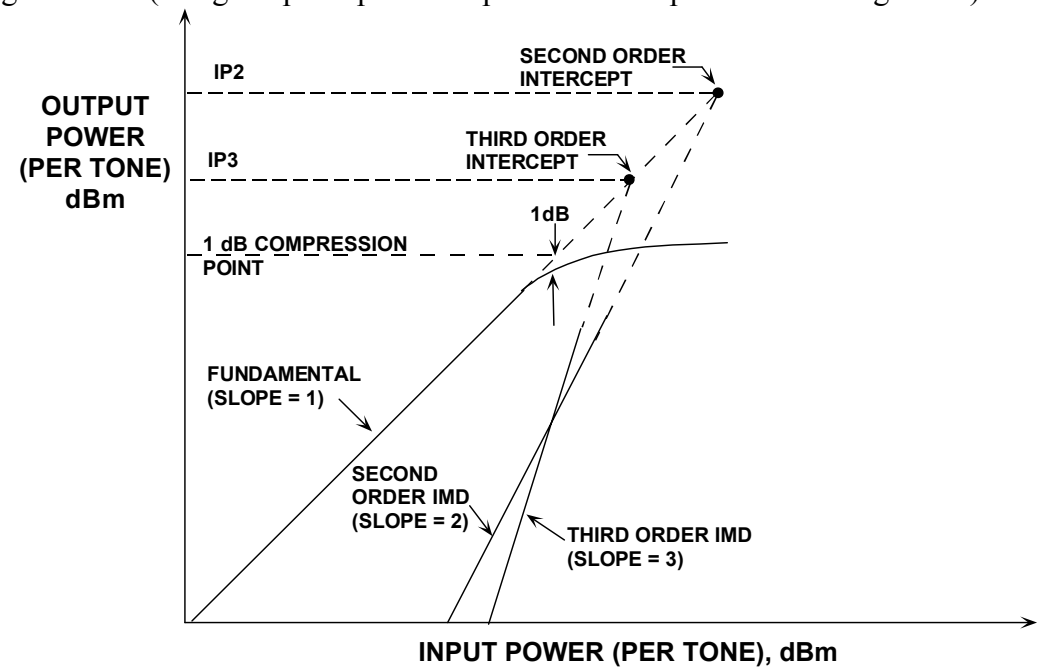


Figure 6-123: *Intercept points and 1dB compression point*

Once the input reaches a certain level however, the output signal begins to soft-limit, or compress. A parameter of interest here is the *1dB compression point*. This is the point where the output signal is compressed 1dB from an ideal input/output transfer function. This is shown in Figure 6-123 within the region where the ideal slope = 1 line becomes dotted, and the actual response exhibits compression (solid).

Nevertheless, both the second and third-order intercept lines may be extended, to intersect the (dotted) extension of the ideal output signal line. These intersections are called the *second* and *third order intercept points*, respectively, or IP2 and IP3. These power level values are usually referenced to the output power of the device delivered to a matched load (usually, but not necessarily 50Ω) expressed in dBm.

It should be noted that IP2, IP3, and the 1dB compression point are all a function of frequency, and as one would expect, the distortion is worse at higher frequencies.

For a given frequency, knowing the third order intercept point allows calculation of the approximate level of the third-order IMD products as a function of output signal level. Figure 6-124 below shows the third order intercept value as a function of frequency for a typical wideband low-distortion amplifier.

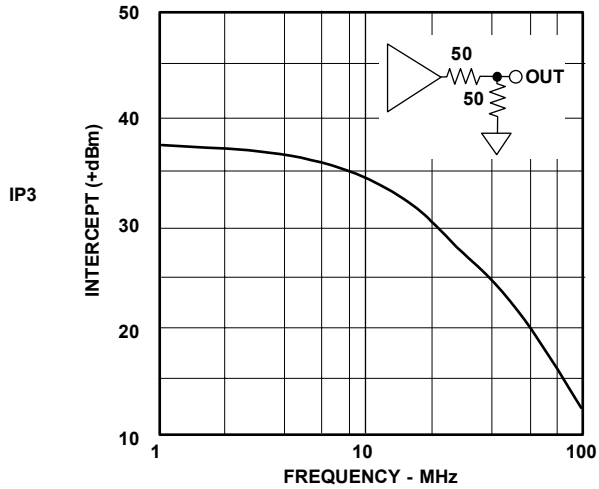


Figure 6-124: *Third order intercept point (IP3) versus frequency for a low distortion amplifier*

Assume the op amp output signal is 5MHz and 2V peak-to-peak into a 100Ω load (50Ω source and load termination). The voltage into the 50Ω load is therefore 1V peak-to-peak, corresponding to +4dBm. From Fig. 6-124, the value of the third order intercept at 5MHz is 36dBm. The difference between +36dBm and +4dBm is 32dB. This value is then multiplied by 2 to yield 64dB (the value of the third-order intermodulation products referenced to the power in a single tone). Therefore, the intermodulation products should be –64dBc (dB below carrier frequency), or at an output power level of –60dBm.

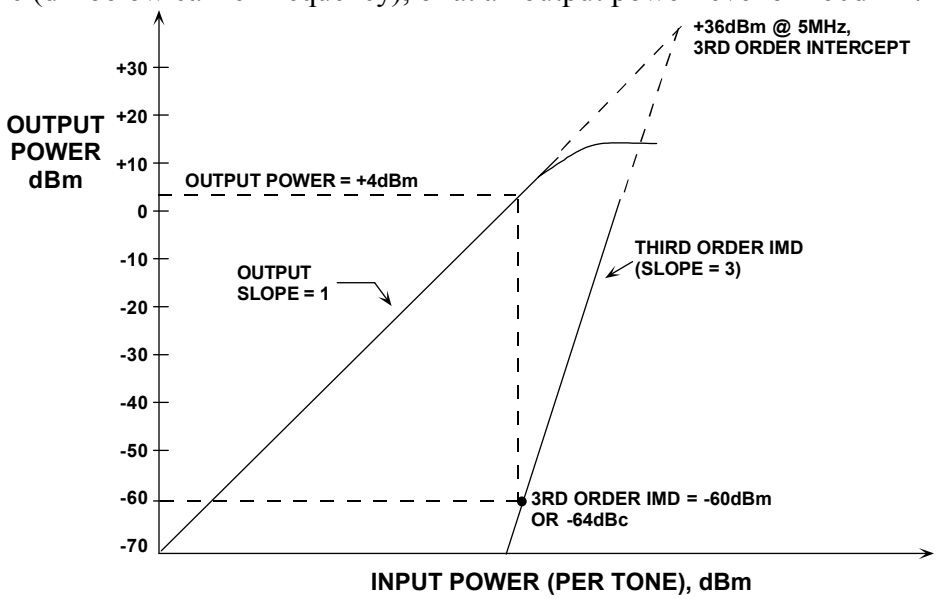


Figure 6-125: *Using IP3 to calculate the third-order IMD product amplitude*

Figure 6-125 shows the graphical analysis for this example. A similar analysis can be performed for the second-order intermodulation products, using data for IP2.

Another popular specification in communications systems is *spurious free dynamic range*, or SFDR. Figure 6-126 below shows two variations of this specification. Single-tone SFDR (left) is the ratio of the signal (or carrier) to the *worst* spur in the bandwidth of interest. This spur may or may not be harmonically related to the signal. SFDR can be referenced to the signal or carrier level (dBc), or to full scale (dBFS).

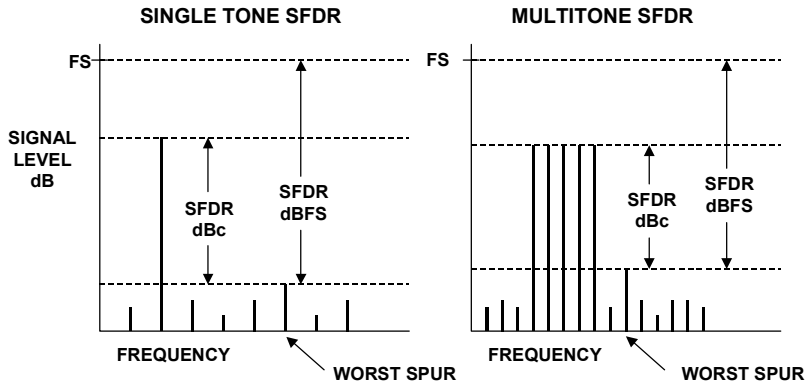


Figure 6-126: *Spurious free dynamic range (SFDR) in communications systems*

Because most amplifiers are soft limiters, the dBc unit is more often used. However, in systems that have a hard-limiter that precisely defines full scale (such as with ADCs), both dBc and dBFS may be used. It is important to understand that they both describe the worst spur amplitude. SFDR can also be specified for two tones or multitones (right), thereby simulating complex signals that contain multiple carriers and channels.

Multitone power ratio is another way of describing distortion in a multichannel communication system. Figure 6-127 below shows the frequency partitioning in an xDSL system. The QAM signals in the upstream data path are represented by a number of equal amplitude tones, separated equally in frequency. One channel is completely eliminated from the input signal (shown as an empty bin), but intermodulation distortion caused by the system nonlinearity will cause a small signal to appear in that bin.

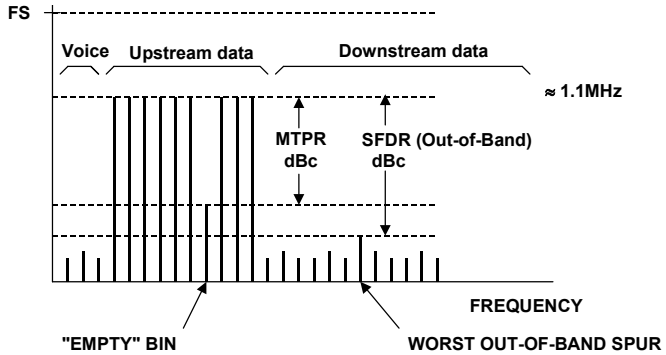


Figure 6-127: *Multitone power ratio (MTPR) and out-of-band SFDR in xDSL applications*

The ratio of the tone amplitude to the amplitude of the unwanted signal in the empty bin is defined as the multitone power ratio, or MTPR. It is equally important that the amplitude of the intermodulation products caused by the multitone signal (simulating multiple channels) not interfere with signals in either the voice band or the downstream data band. The amplitude of the worst spur produced in these bands to the amplitude of the multitone signal is therefore defined as the *out-of-band SFDR*.

Noise Specifications

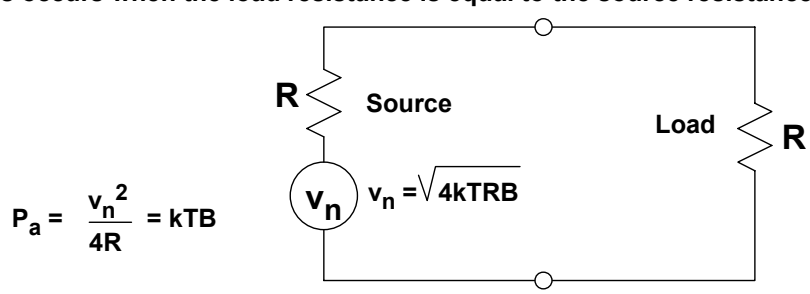
Op amp noise is generally specified in terms of input current and voltage noise, as previously discussed in Chapter 1 of this book. In communications systems, however, noise is often specified in terms of *noise figure* (NF)— see Figure 6-128. This can lead to confusion, especially when op amps are used as gain blocks and the noise figure of the op amp is not specified for the specific circuit conditions. In order to understand how to apply noise figure to op amps, we will first review the basic theory behind noise figure.

- **NF is usually specified for matched input/output conditions, but this is not always a system requirement**
- **Noise Figure is a popular figure of merit in RF applications: LNAs, Mixers, etc.**
- **Difficulties arise when applying NF to op amps. NF is dependent on**
  - **Impedance levels**
  - **Feedback network**
  - **Closed loop gain**
- **Other difficulties arise due to different definitions of NF as found in various textbooks**
- **We will start with the basics and work up to the op amp issues**

Figure 6-128: *Noise figure in communications applications*

The first concept is that of *available power* from a source. The available power of a source is the maximum power that can be drawn from the source. Figure 6-129 below shows a resistor of value R as the noise source. The thermal noise of this source is √(4kTBR). The maximum noise that can be transferred to an ideal noiseless load occurs when the load resistance is also equal to R.

The *available power*, P_a, of a source is the maximum power that can be drawn from the source. This occurs when the load resistance is equal to the source resistance.



$$P_a = \frac{v_n^2}{4R} = kTB$$

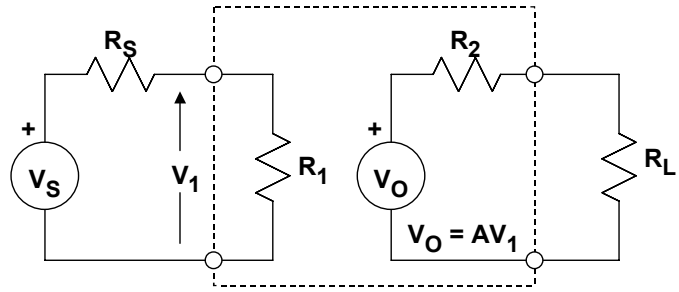
k = 1.38 × 10^{-23} Joules / K (Boltzman's Constant)
T = Temperature (assume 300K, room temperature)
B = Noise bandwidth (Hz)

$$P_{a\,(dBm)} = -174dBm + 10 \log B$$

Figure 6-129: *Available noise power from a source*

Under these conditions, the maximum available noise power from the source reduces to kTB, where k is Boltzmann's constant, T is the absolute temperature, and B is the noise bandwidth. Note that this power is independent of the value of the source resistance, R.

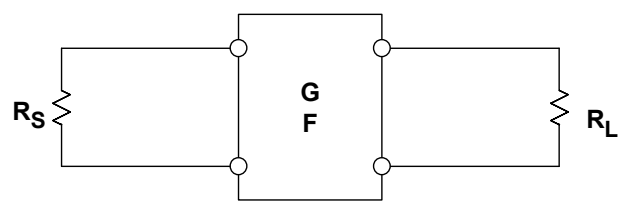
The next important concept is that of *available power gain* of a two-port network, as shown in Figure 6-130 below. The two-port network is driven from a signal source having an impedance. The equations show the available signal power from the source and the available signal power from the output of the network. The available power gain is simply the ratio of the available output power to the available power from the source.



- Available signal power from source $= P_{as} = \dfrac{V_S^2}{4R_S}$
- Available signal power at output $= P_{ao} = \dfrac{V_o^2}{4R_2}$
- Available power gain $= G_a = \dfrac{P_{ao}}{P_{as}} = \dfrac{V_O^2 R_S}{V_S^2 R_2}$

Figure 6-130: *Available power gain of a two-port network*

The gain and the noise of a two-port network can now be defined in terms of the available power gain, G, and the noise factor, F, as shown below in Figure 6-131. The noise factor, F, is defined as the ratio of the total available output noise power to the available output noise power due to the source only. For a resistive source, the available noise power from the source is simply kTB, and the output noise power due to the source only is G·kTB.



G = Available Power Gain of Network

$$F = \text{Noise Factor} = \frac{\text{Total Available Output Noise Power}}{\text{Available Output Noise Power Due to Source Only}}$$

$$= \frac{\text{Total Available Output Noise Power}}{G \cdot kTB}$$

$$NF = \text{Noise Figure} = 10 \log_{10} F$$

Figure 6-131: *Definition of noise factor and noise figure for a two-port noisy network.*

Note that the noise factor, F, is expressed as a ratio, and the noise figure, NF, is simply the ratio F expressed in dB. An ideal noiseless two-port network therefore has noise factor F = 1, and a noise figure NF = 0dB.

We can use these same definitions to calculate the NF of an op amp circuit, however it is much easier to work in terms of the square of voltage noise spectral density and current noise spectral density, rather than power or power spectral density (see Figure 6-132 below). Also, unmatched conditions are easier to deal with using this approach. *The noise factor F for an op amp is simply the ratio of the square of the total output noise spectral density to the square of the output noise spectral density due to the source only.* The noise figure NF = 10•logF.

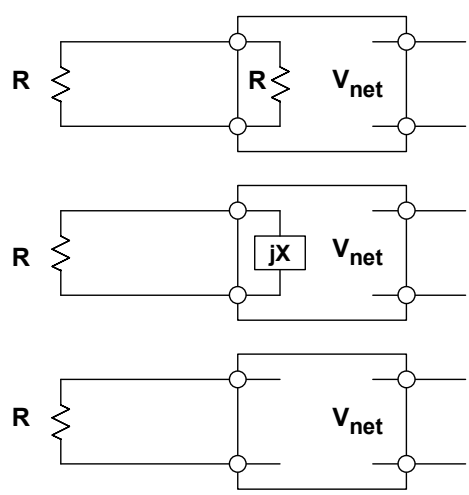
- **With op amps, it is easier to work with voltage and current noise spectral density, rather than power or power spectral density.**
- **Unmatched conditions are more easily dealt with using voltage noise spectral density analysis.**
- **Voltage noise spectral densities add using root-sum-squares (RSS).**
- **A 1000Ω resistor has a voltage noise spectral density of 4nV/√Hz @ 25°C (300K). (This is good to remember!)**
- **The basic definition of Noise Factor and Noise Figure in terms of voltage noise spectral density becomes:**

$$\text{Noise Factor} = F = \frac{(\text{Total Output Voltage Noise Spectral Density})^2}{(\text{Output Voltage Noise Spectral Density Due to Source Only})^2}$$

$$\text{Noise Figure} = NF = 10 \log_{10} F$$

Figure 6-132: *Noise figure for op amps*

In RF or IF gain blocks, the input impedance is defined. However, when using an op amp in the non-inverting mode as a gain block, the input impedance is high (relative to transmission line impedances), and there are several options regarding the input termination which affect the noise figure. These options have been generalized to cover any two-port network with optional input terminations in Figure 6-133 below.



$$F = 2 + \frac{V_{net}^2}{A^2kTR}$$ **Matched Resistive Termination**

$$F = 1 + \frac{V_{net}^2}{A^2kTR}$$ **Matched Reactive Termination R = |X|**

$$F = 1 + \frac{V_{net}^2}{A^2 4kTR}$$ **Unterminated**

V_{net} = Voltage noise density of network excluding source and load terminations
A = Open circuit voltage gain of network

Figure 6-133: *Noise factor for resistive, reactive, and unterminated conditions*

Assume that the open circuit voltage gain of the network is A and that the total output noise spectral density (excluding that due to the source resistance and the input termination) is equal to V_{net}.

The top diagram of Figure 6-133 (opposite) shows the traditional matched case where the input is resistively terminated to match the source impedance. In this case, the input termination resistor not only attenuates the voltage noise of the source by a factor of 2 but also contributes noise due to its own thermal resistance.

The middle diagram of this figure shows the case of a reactive matched termination. Reactive terminations are often used where the bandwidth is limited but centered on a high frequency carrier. In this case, the source voltage noise is attenuated by a factor of 2, but the reactive termination adds no additional noise of its own to the total output noise.

The bottom diagram in Figure 6-133 shows the case of an unmatched, unterminated input. In this case, the voltage noise of the source is not attenuated, and there is obviously no additional noise due to the input termination because there is no input termination! Although this situation is not likely in a system using RF/IF gain blocks which generally require impedance matching at all interfaces, it is a possibility when using an op amp as the gain block, since the non-inverting configuration input impedance is relatively high.

- **For a low noise network, adding the matching input termination resistor makes the noise figure 3dB worse. The voltage gain is also reduced by a factor of 2.**
- **For a high noise network, adding the matching termination resistor makes the noise figure 6dB worse.**
- **Reactive matched terminations are often used at fixed IF/RF frequencies in LNAs, mixers, etc.**
- **Using large source and termination resistors decreases noise figure but increases overall circuit noise.**
- **Noise figures should only be compared at the same impedance level.**

Figure 6-134: *Effects of input termination on noise figure*

If we assume that the noise of the network, V_{net}, is very small relative to the source noise, then it is obvious that the input termination resistor adds 3dB to the overall noise figure as well as reduces the overall voltage gain by a factor of 2. This is compared to the lowest noise case where there is no input termination. In fact, the lowest possible noise figure for a noiseless network with only an input resistive matched termination is 3dB. Lower noise figures can be obtained only by using matched reactive terminations.

On the other hand, if the noise of the network, V_{net}, is very large with respect to the source noise, then adding the resistive termination increases the overall noise figure by 6dB compared to the unmatched unterminated case.

Summarizing, it is interesting to note that using large source resistances will decrease the noise figure but increase overall circuit noise. This illustrates the important fact that *noise figures can be compared only if they are specified at the same impedance level*. In Figure 6-134 above these effects of amplifier input terminations on overall circuit noise and noise figure are summarized.

Op amp noise has two components: low frequency noise whose spectral density is inversely proportional to the square root of the frequency, and white noise at medium and high frequencies. The low-frequency noise is known as 1/f noise (the noise *power* obeys a 1/f law— the noise voltage or noise current is proportional to $1/\sqrt{f}$). The frequency at which the 1/f noise spectral density equals the white noise is known as the "1/f Corner Frequency". This is an important figure of merit for op amps, with low values indicating better performance. Values of the 1/f corner frequency vary from a few Hz for the most modern low noise low frequency amplifiers, to several hundreds, or even thousands of Hz for some high-speed op amps.

In most applications of high speed op amps, it is the total output RMS noise that is generally of interest. Because of the high bandwidths, the chief contributor to the output RMS noise is the white noise, and that of the 1/f noise is negligible.

In order to better understand the effects of noise in high speed op amps, we use the classical noise model shown in Figure 6-135 below. This diagram identifies all possible white noise sources, including the external noise in the source and the feedback resistors.

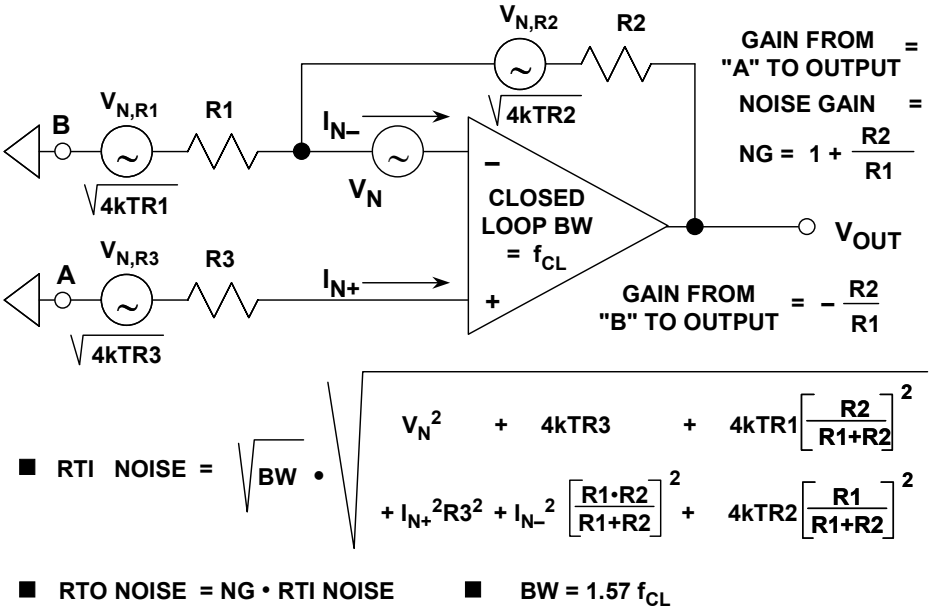


Figure 6-135: *Calculating total op amp circuit noise*

The equation in the figure allows you to calculate the total output RMS noise over the closed-loop bandwidth of the amplifier. This formula works quite well when the frequency response of the op amp is relatively flat. If there is more than a few dB of high frequency peaking, however, the actual noise will be greater than the predicted because the contribution over the last octave before the 3dB cutoff frequency will dominate.

In most applications, the op amp feedback network is designed so that the bandwidth is relatively flat, and the formula provides a good estimate. Note that BW in the equation is the equivalent *noise bandwidth,* which, for a single-pole system, is obtained by multiplying the closed-loop 3dB bandwidth by 1.57.

Figure 6-136 below is a table which indicates how the individual noise contributors of Fig. 6-135 are referred to the output. After calculating the individual noise spectral densities in this table, they can be squared, added, and then the square root of the sum of the squares yields the RSS value of the output noise spectral density, since all the sources are uncorrelated. This value is multiplied by the square root of the noise bandwidth (noise bandwidth = closed-loop 3dB bandwidth multiplied by a correction factor of 1.57) to obtain the final value for the output RMS noise.

Typical high speed op amps have bandwidths greater than 150MHz or so, and bipolar input stages have input voltage noises ranging from about 2 to 20nV/√Hz. To put voltage noise in perspective, let's look at the Johnson noise spectral density of a resistor: $v_n = \sqrt{4kTR \cdot BW}$, where k is Boltzmann's constant, T is the absolute temperature, R is the resistor value, and BW is the equivalent noise bandwidth of interest. (The equivalent noise bandwidth of a single-pole system is 1.57 times the 3dB frequency). Using the formula, a 100Ω resistor has a noise density of 1.3nV/√Hz, and a 1000Ω resistor about 4nV/√Hz (values are at room temperature: 27°C, or 300K).

NOISE SOURCE EXPRESSED AS A VOLTAGE	MULTIPLY BY THIS FACTOR TO REFER TO THE OP AMP OUTPUT
Johnson Noise in R3: √(4kTR3)	Noise Gain = 1 + R2/R1
Non-inverting Input Current Noise Flowing in R3: $I_{n+}R3$	Noise Gain = 1 + R2/R1
Input Voltage Noise: V_n	Noise Gain = 1 + R2/R1
Johnson Noise in R1: √(4kTR1)	–R2/R1 (Gain from input of R1, "B", to Output)
Johnson Noise in R2: √(4kTR2)	1
Inverting Input Current Noise Flowing in R2: $I_{n-}R2$	1

Figure 6-136: *Referring all noise sources to the output*

The base-emitter in a bipolar transistor has an equivalent noise voltage source which is due to the "shot noise" of the collector current flowing in the transistor's (noiseless) incremental emitter resistance, r_e. The current noise is proportional to the square root of the collector current, Ic. The emitter resistance, on the other hand, is inversely proportional to the collector current, so *the shot-noise voltage is inversely proportional to the square root of the collector current*.

Voltage noise in FET-input op amps tends to be larger than for bipolar ones, but current noise is extremely low (generally only a few tens of fA/√Hz) because of the low input bias currents. However, FET-inputs are not generally required for op amp applications requiring bandwidths greater than 100MHz.

Op amps also have input current noise on each input. For high-speed FET-input op amps, the gate currents are so low that input current noise is almost always negligible (measured in fA/√Hz).

For a voltage feedback (VFB) op amp, the inverting and non-inverting input current noise are typically equal, and almost always uncorrelated. Typical values for wideband VFB op amps range from 0.5pA/√Hz to 5pA/√Hz. The input current noise of a bipolar input stage is increased when input bias-current cancellation generators are added, because their current noise is not correlated, and therefore adds (in an RSS manner) to the intrinsic current noise of the bipolar stage.

The input voltage noise in current feedback (CFB) op amps tends to be lower than for VFB op amps having the same approximate bandwidth. This is because the input stage in a CFB op amp is usually operated at a higher current, thereby reducing the emitter resistance and hence the voltage noise. Typical values for CFB op amps range from about 1 to 5nV/√Hz.

The input current noise of CFB op amps tends to be larger than for VFB op amps because of the generally higher bias current levels. The inverting and non-inverting current noise of a CFB is usually different because of the unique input architecture, and are specified separately. In most cases, the inverting input current noise is the larger of the two. Typical input current noise for CFB op amps ranges from 5 to 40pA/√Hz.

The general principle of noise calculation is that uncorrelated noise sources add in a root-sum-squares manner, which means that if a noise source has a contribution to the output noise of a system which is less than 20% of the amplitude of the noise from other noise source in the system, then its contribution to the total system noise will be less than 2% of the total, and that noise source can almost invariably be ignored— in many cases, noise sources smaller than 33% of the largest can be ignored. This can simplify the calculations using the formula, assuming the correct decisions are made regarding the sources to be included and those to be neglected.

The sources which dominate the output noise are highly dependent on the closed-loop gain of the op amp. Notice that for high values of closed loop gain, the op amp voltage noise will tend be the chief contributor to the output noise. At low gains, the effects of the input current noise must also be considered, and may dominate, especially in the case of a CFB op amp.

Feedforward/feedback resistors in high speed op amp circuits may range from less than 100Ω to more than 1kΩ, so it is difficult to generalize about their contribution to the total output noise without knowing the specific values and the closed loop gain. The best way to make the calculations is to write a simple computer program that performs the calculations automatically and includes all noise sources (see Reference 1 for one example). In most high speed applications, the source impedance noise can be neglected for source impedances of 100Ω or less.

Figure 6-137 below shows an example calculation of total output noise for the AD8011 (300MHz, 1mA) CFB op amp. All six possible sources are included in the calculation. The appropriate multiplying factors which reflect the sources to the output are also shown on the diagram. For G=2, the close-loop bandwidth of the AD8011 is 180MHz. The correction factor of 1.57 in the final calculation converts this single-pole bandwidth into the circuit's equivalent noise bandwidth.

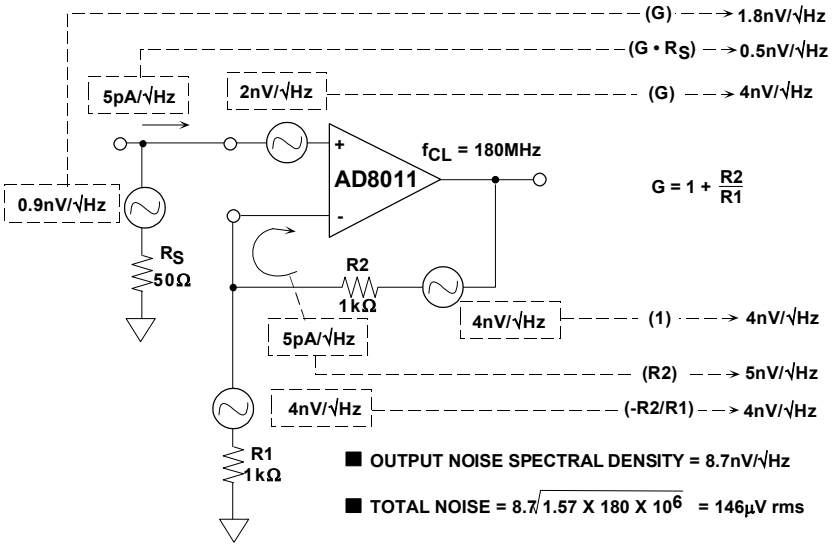


Figure 6-137: *AD8011 output noise analysis*

Now that the total output noise has been calculated, we can address the issue of noise figure. Figure 6-138 below shows two cases for the AD8011 circuit: the top diagram corresponds to an unterminated input condition, and the bottom diagram corresponds to a terminated input condition.

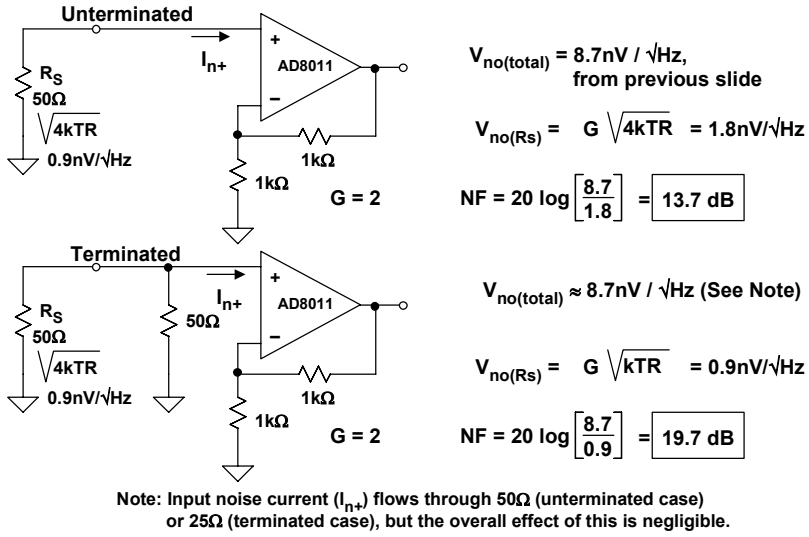


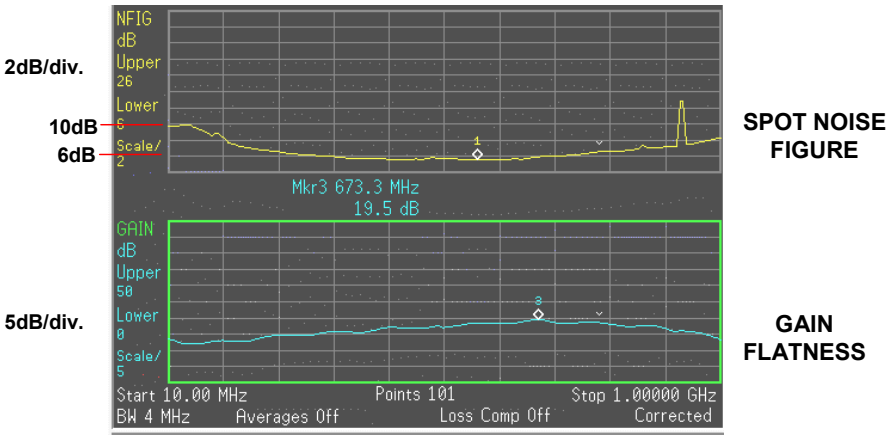
Figure 6-138: *AD8011 noise figure for unterminated and terminated input conditions*

For the unterminated case (top), the total output noise from the previous diagram (i.e., Fig. 6-137) was 8.7nV/√Hz. Note this includes the noise of the 50Ω source. The output

noise due only to the source is simply the noise gain multiplied by the noise of the source, or $G\sqrt{(4kTR_S)} = 1.8nV/\sqrt{Hz}$. The noise figure is simply NF = 20log(8.7/1.8) = 13.7dB.

For the terminated case (bottom), the total output noise is still approximately $8.7nV/\sqrt{Hz}$. Note that the input noise current (I_{n+}) now actually flows through 25Ω rather than 50Ω for the unterminated case, but the overall effect of this difference on the total output noise calculation is negligible.

The noise of the source, however, is now $\sqrt{(kTR)}$ due to the 50Ω divider network, and reflected output, it becomes $G\sqrt{(kTR)} = 0.9nV/\sqrt{Hz}$. The noise figure is calculated as NF = 20log(8.7/0.9) = 19.7dB. Notice that the terminated case yields a noise figure which is approximately 6dB worse than the unterminated case.



- **Spot Noise Figure shows variations over frequency: 10MHz to 1GHz**
- **Measurement bandwidth set to 4MHz for above data**
- **Integration required to get average noise power**

Figure 6-139: *AD8350 spot noise figure and gain vs. frequency from 10MHz to 1GHz*

Finally, it should be noted that noise figure is actually a function of frequency. In Figure 6-139 above is shown the noise figure of the AD8350 measured with a spot noise meter, as a function of frequency over the bandwidth 10MHz to 1GHz. The top curve is the noise figure, and the bottom curve is the closed-loop gain flatness.

In most cases, the approximations such as those used in the example of Figs. 6-135 through 6-137 will give sufficient accuracy, provided the closed-loop bandwidth is relatively flat. However, using the actual spot noise figure may be desirable in high frequency narrowband applications involving specific carrier frequencies.

Variable Gain Amplifiers (VGAs) in Automatic Gain Control (AGC)

Wideband, low distortion variable gain amplifiers find wide applications in communications systems. One example is automatic gain control (AGC) in radio receivers. Typically, the received energy exhibits a large dynamic range due to the variability of the propagation path, requiring dynamic-range compression in the receiver. In this case, the wanted information is in the modulation envelope (whatever the modulation mode), not in the absolute magnitude of the carrier. For example, a 1MHz carrier modulated at 1kHz to a 30% modulation depth would convey the same information, whether the received carrier level is at 0dBm or –120dBm. Some type of automatic gain control (AGC) in the receiver is generally utilized to restore the carrier amplitude to some normalized reference level, in the presence of large input fluctuations. AGC circuits are dynamic-range compressors which respond to some signal metric (often mean amplitude) acquired over an interval corresponding to many periods of the carrier.

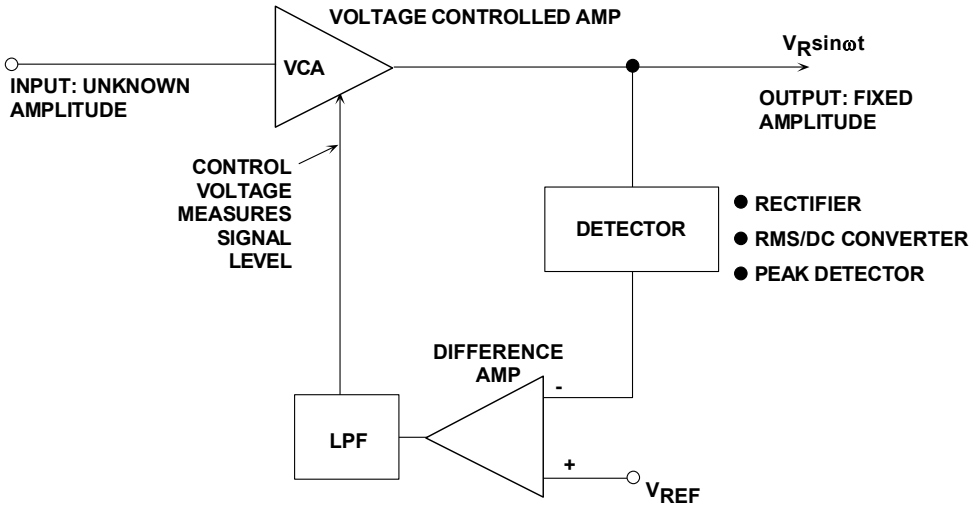


Figure 6-140: *A typical automatic gain control (AGC) system*

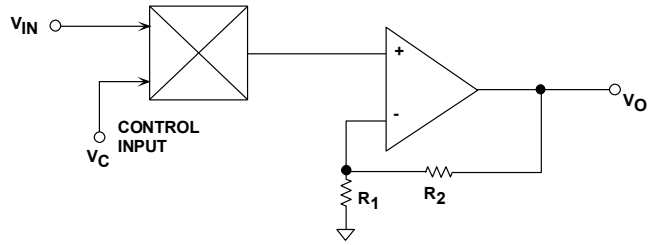
Consequently, they require time to adjust to variations in received signal level. The time required to respond to a sudden increase in signal level can be reduced by using peak detection methods, but with some loss of robustness, since transient noise peaks can now activate the AGC detection circuits. Nonlinear filtering and the concept of "delayed AGC" can be useful in optimizing an AGC system. Many tradeoffs are found in practice; Figure 6-140 above shows a basic AGC system.

It is interesting to note that an AGC loop actually has *two* outputs. The more obvious output is of course the amplitude-stabilized signal. The less obvious output is the control voltage to the VCA. In reality, this voltage is a measure of the average amplitude of the input signal. If the system is precisely scaled, the control voltage may be used as a measure of the input signal, which is sometimes also known as a *received signal strength indicator* (RSSI).

This latter point, given a suitably precise VCA gain control law, allows implementation of a receiving system which is calibrated for incoming signal level.

Voltage Controlled Amplifiers (VCAs)

An analog multiplier can be used as a variable-gain amplifier, as shown in Figure 6-141 below. The control voltage is applied to one input, and the signal to the other. In this configuration, the gain is directly proportional to the control voltage.



$$V_O = \frac{V_{IN}}{K} \cdot \left(1 + \frac{R_2}{R_1}\right) V_C$$

Figure 6-141: *Using a multiplier as a voltage-controlled amplifier (VCA)*

Most VCAs made with analog multipliers have gain which is *linear in volts* with respect to the control voltage, and they tend to be noisy. There is a demand, however, for a VCA which combines a wide gain range with constant bandwidth and phase, low noise with large signal-handling capabilities, and low distortion with low power consumption, while providing accurate, stable, *linear-in-dB* gain. The AD600, AD602, AD603, AD604, and AD605, and AD8367 achieve these demanding and conflicting objectives with a unique and elegant solution— the X-AMP® (for *exponential amplifier* see Reference 2).

The concept is simple: a fixed-gain amplifier follows a passive, broadband attenuator, with special means to alter voltage-controlled attenuation, as in Figure 6-142 below.

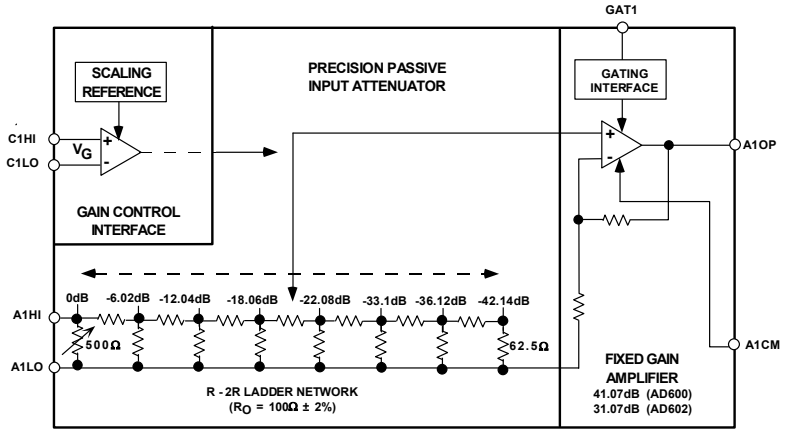


Figure 6-142: *Single channel of the dual 30MHz AD600/AD602 X-AMP®*

The AD600/AD602 amplifier stage is optimized for low input noise, and negative feedback is used to accurately define its moderately high gain (30-40dB) and minimize distortion. Since amplifier gain is fixed, so also are its AC and transient response characteristics, including distortion and group delay. As its gain is high, the input is never driven beyond a few millivolts, always operating within a small signal response range.

The attenuator network is a 7-section (8-tap) R-2R ladder. The ratio between adjacent taps is exactly 2, or 6.02dB, providing the basis for precise linear-in-dB behavior, while overall attenuation is 42.14dB. As will be shown, the amplifier's input can be connected to any one of these taps, or even *interpolated* between them, with only a small deviation error of about ±0.2dB. Overall gain can be varied from the fixed (maximum) gain, to a value 42.14dB less. In the AD600, the fixed gain is 41.07dB (voltage gain of 113); using this choice, the full gain range is –1.07dB to +41.07dB. The gain is related to control voltage by the relationship $G_{dB} = 32V_G + 20$ where V_G is in volts. For the AD602, the fixed gain is 31.07dB (voltage gain of 35.8), and the gain is given by $G_{dB} = 32V_G + 10$.

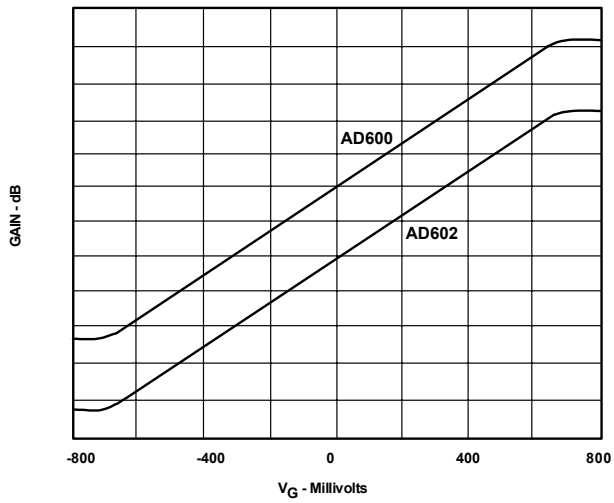


Figure 6-143: *Gain of the AD600/AD602 as a function of control voltage*

The gain at $V_G = 0$ is laser trimmed to an absolute accuracy of ±0.2dB. The gain scaling is determined by an on-chip bandgap reference (shared by both channels), laser trimmed for high accuracy and low temperature coefficient. Figure 6-143 above shows the gain versus the differential control voltage for both the AD600 and the AD602. Deviation from an ideal control law is only a fraction of a dB over a large part of the dynamic range.

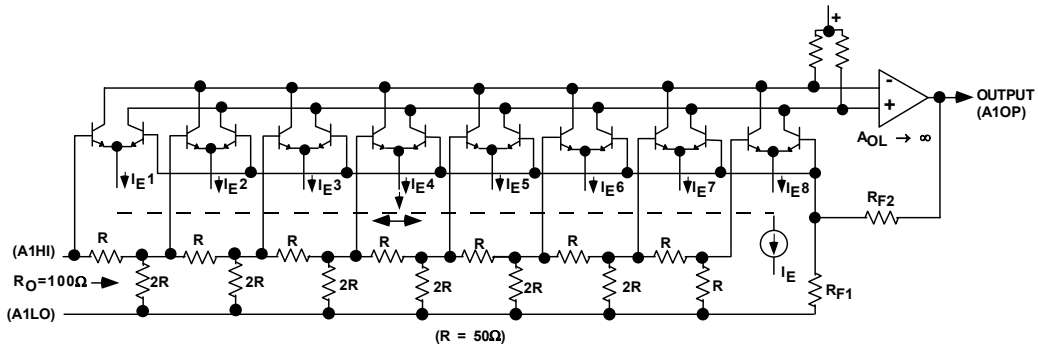


Figure 6-144: *Continuous interpolation between taps using current-controlled g_m stages in the X-AMP®*

In order to understand the operation of the X-AMP®, consider the simplified diagram shown in Figure 6-144 above. Note that each of the eight taps is connected to an input of one of eight bipolar differential pairs, used as current-controlled transconductance (g_m) stages; the other input of all these g_m stages is connected to the amplifier's gain-

determining feedback network, R_{F1}/R_{F2}. When emitter bias current I_E is directed to one of the 8 transistor pairs (not shown here), it becomes the complete amplifier input stage.

When I_E is connected to the left-most pair, the signal input is connected directly to the amplifier, giving maximum gain. The distortion is very low, even at high frequencies, due to the careful open-loop design, aided by the negative feedback. If I_E were now to be abruptly switched to the second pair, the overall gain would drop by exactly 6.02dB, and the distortion would remain low, because only one g_m stage remains active.

In reality, the bias current is *gradually* transferred from the first pair to the second. When I_E is equally divided between two g_m stages, both are active, and the situation arises where we have an op amp with two input stages fighting for control of the loop, one getting the full signal, and the other getting a signal exactly half as large.

Analysis shows that the effective gain is reduced, not by 3dB, as one might first expect, but rather by 20log1.5, or 3.52dB. This error, when divided equally over the whole range, would amount to a gain ripple of ±0.25dB; however, the interpolation circuit actually generates a Gaussian distribution of bias currents, and a significant fraction of I_E always flows in adjacent stages. This smoothes the gain function and actually lowers the ripple. As I_E moves further to the right, the overall gain progressively drops.

	BANDWIDTH	DISTORTION	NOISE	INPUT Z	SUPPLY
AD600/602	35MHz	–60dBc @ 10MHz	1.4nV/√Hz	100Ω	±5V
AD603	90MHz	–60dBc @ 10MHz	1.3nV/√Hz	100Ω	±5V
AD604	40MHz	–43dBc @ 10MHz	0.8nV/√Hz	300kΩ	±5V
AD605	40MHz	–51dBc @ 10MHz	1.8nV/√Hz	200Ω	+5V
AD8367	500MHz	IP3 = +31.5dBm @140MHz	NF = 7.8dB @140MHz	200Ω	+2.7 to +5V

Figure 6-145: *X-AMP® family key specifications*

The key features of the X-AMP product family are summarized in Figure 6-145 above. Note the other members of the family beyond the described AD600/AD602.

The total input-referred noise of the AD600/AD602 X-AMP® is 1.4nV/√Hz; only slightly more than the thermal noise of a 100Ω resistor (1.29nV/√Hz at 25°C). The input-referred noise is constant regardless of the attenuator setting, therefore the output noise is always constant and independent of gain.

For the AD600, the amplifier gain is 113 and the output noise spectral density is therefore 1.4nV/√Hz×113, or 158nV/√Hz. Referred to its maximum output of 2Vrms, the signal-to-noise ratio would be 82dB in a 1MHz bandwidth. The corresponding signal-to-noise ratio of the AD602 is 10dB greater, or 92dB.

Digitally Controlled Variable Gain Amplifiers for CATV Upstream Data Line Drivers

Cable modems offer much higher data rates than standard dial-up connections and have become very popular. In addition to receiving data (*downstream*), the cable modem also transmits data (*upstream*). This requires a low distortion digitally controlled variable gain amplifier capable of driving the 75Ω coaxial cable at a nominal level of 1V RMS (+11.2dBm, or 60dBmV). The AD8323 is a member of a family of CATV upstream line drivers suitable for this application. The AD8323 gain is controlled by an 8-bit serial word that determines the desired gain over a 53.5dB range, resulting in gain changes of 0.7526dB/LSB. The AD8323 block diagram is shown Figure 6-146 below.

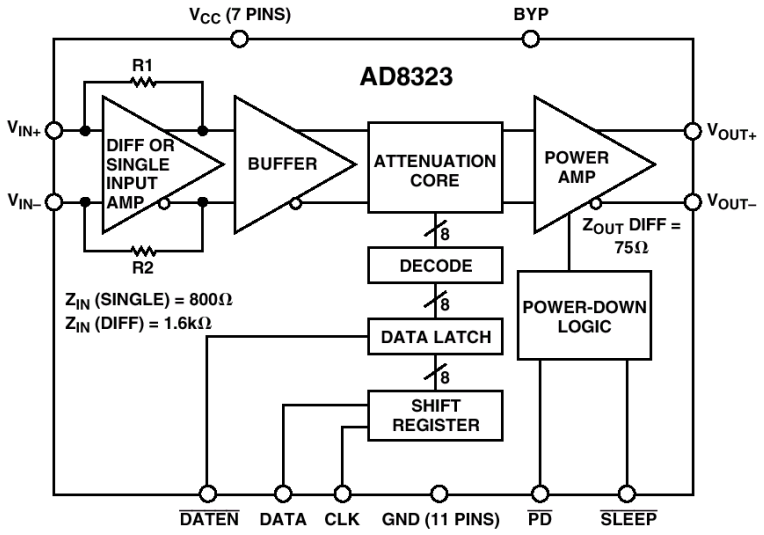


Figure 6-146: *AD8323 CATV digitally controlled variable gain amplifier*

The AD8323 has a variable attenuator core where the attenuation is digitally controlled from 0dB to –53.5dB. The input buffer has a gain of approximately + 27.5dB, therefore the resulting overall gain range is from –26dB to +27.5dB. The AD8323 is composed of four analog functions in the power-up mode. The input amplifier (preamp) can be used either single-ended or differentially. The preamp stage drives a vernier stage that provides the fine tune gain adjustment. The 0.7526dB/LSB resolution is implemented in this stage and provides a total of approximately 5.25dB of attenuation. After the vernier stage, a DAC provides the bulk of the AD8323's attenuation (8-bits, or 48dB).

The signals in the preamp and vernier gain blocks are differential to improve the PSRR and linearity. A differential current is fed from the DAC to the output stage, which amplifies these currents to the appropriate levels necessary to drive the 75Ω load.

A key performance and cost advantage of the AD8323 results from the ability to maintain a constant dynamic output impedance of 75Ω during power-up/ power-down conditions. The output stage utilizes negative feedback to implement a differential 75Ω dynamic output impedance. This eliminates the need for an external 75Ω termination, resulting in twice the effective output voltage when compared to a standard op amp.

These features allow the AD8323 to operate on a single +5V supply and still deliver the required output power. Distortion performance of –56dBc is achieved with an output level up to 1V RMS (+11.2dBm, or 60dBmV) at a 21MHz bandwidth.

- **Supports cable modem DOCSIS (Data Over Cable Service) standard for upstream path transmission**
- **Gain/attenuation programmable in 0.7526dB steps over a 53.5dB range:**
  –26dB to +27.5dB
- **3-wire SPI digital interface**
- **Bandwidth: > 100MHz (all gains)**
- **Low distortion @ 1V RMS (+11.2dBm, +60dBmV) output into 75Ω**
  - **–56dBc SFDR @ 21MHz**
  - **–55dBc SFDR @ 42MHz**
- **Single +5V supply (133mA)**
- **Power-down mode (35mA), sleep mode (4mA)**
- **75Ω dynamic output impedance in power-up or power-down modes**

Figure 6-147: *AD8323 CATV line driver key specifications*

The key specifications for the AD8323 are shown in Figure 6-147 above.

xDSL Upstream Data Line Drivers

Various versions of DSL are now used to provide fast internet connections. The upstream data path requires the transmission of +13dBm discrete multitone (DMT) signals occupying a bandwidth between approximately 144kHz and 500kHz. The DMT signal can have a crest factor as high as 5.3, requiring the line driver to provide peak power of +27.5dBm, which translates into 7.5V peak voltage on the 100Ω telephone line.

DMT modulation appears in the frequency domain as power contained in several individual frequency subbands, sometimes referred to as tones or bins, each of which is uniformly separated in frequency. A quadrature amplitude modulated (QAM) signal occurs at the center of each subband or tone. Difficulties will exist when decoding these subbands if a signal from one subband is corrupted by the signal from other subbands, regardless of whether the corruption comes from an adjacent subband or harmonics of other subbands.

Conventional methods of expressing the output signal integrity of line drivers, such as single-tone harmonic distortion or THD, two-tone intermodulation distortion (IMD), and third order intercept (IP3), become significantly less meaningful when amplifiers are required to process DMT and other heavily modulated waveforms.

A typical ADSL upstream DMT signal can contain as many as 27 carriers (subbands or tones) of QAM signals (as shown in Figure 6-148, opposite). Multitone power ratio (MTTR) is the relative difference between the measured power in a typical subband (at one tone or carrier) versus the power at another subband specifically selected to contain no QAM data. In other words, a selected subband (or tone) remains open and void of intentional power (without a QAM signal), yielding an empty frequency bin. MTPR,

sometimes referred to as the "empty bin test," is typically expressed in dBc and is a key specification for all types of DSL systems.

Another important specification for an xDSL line driver is *out-of-band* SFDR. Spurs produced by distortion of the DMT upstream data can fall in the downstream frequency regions and distort voiceband and downstream data.

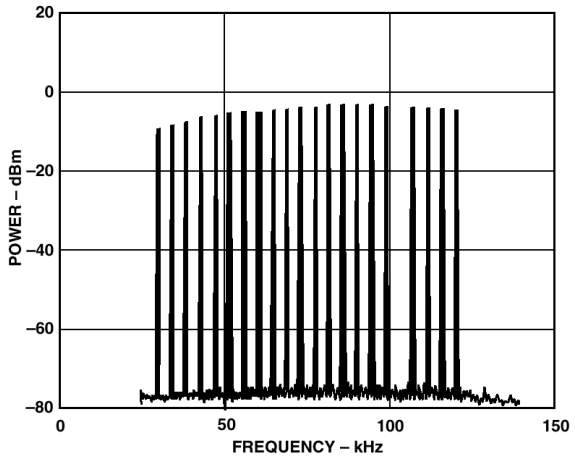


Figure 6-148: *Discrete multitone (DMT) signal in the frequency domain*

Figure 6-149 below shows an xDSL line driver application circuit based on the AD8018 line driver (one member of a family of Analog Devices' DSL line drivers). The peak DMT signal can be 7.5V on the 100Ω telephone line.

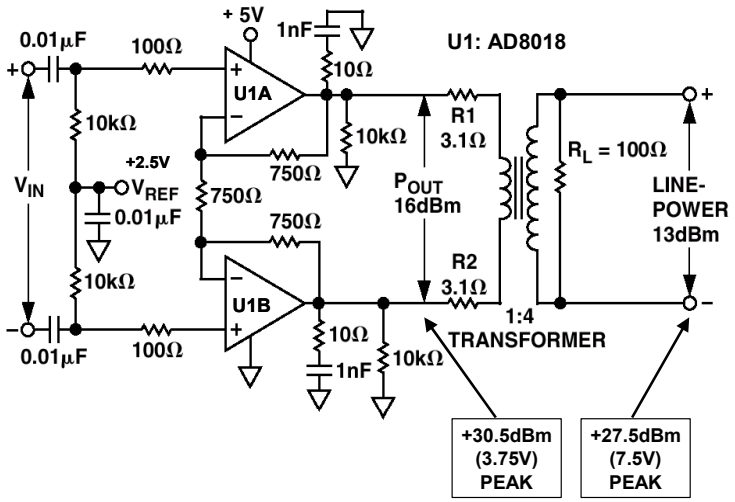


Figure 6-149: *AD8018 xDSL upstream data line driver application*

Assuming maximum low-distortion output swing available from the AD8018 line driver on a single +5V supply is 4V, taking into account the power lost due to the two 3.1Ω back-termination resistors, a transformer with a 1:4 or greater step-up is needed.

The AD8018 is therefore coupled to the phone line through a step-up transformer with a 1:4 turns ratio. R1 and R2 are back-termination or line-matching resistors, each 3.1Ω. The total differential load presented to the AD8018 output is 12.5Ω, including the

termination resistors. Even under these conditions, the AD8018 provides low distortion signals to within 0.5V or the power rails.

The transformer circuit presents a complex impedance to the AD8018 output, and therefore for stability, a series R-C network should be connected between each amplifier's output and ground. The recommended values are 10Ω for the resistor and 1nF for the capacitor to create a low impedance path to ground at frequencies above 16MHz. The 10kΩ output resistors connected to ground are added to improve common-mode stability.

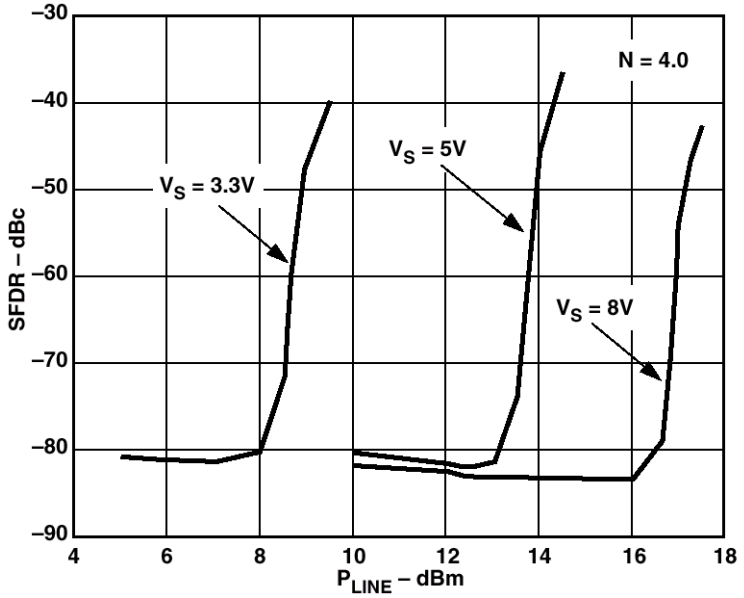


Figure 6-150: *Out-of-band SFDR vs. upstream line power, 144kHz to 500kHz*

For the AD8018 circuit of Fig. 6-149, the out-of-band SFDR versus upstream line power is shown in Figure 6-150 above for various supply voltages

- **Dual current feedback amplifiers**
- **Bandwidth: 130MHz (–3dB)**
- **Slew rate: 300V/µs**
- **Rail-to-rail output stage (swings within 0.5V of rails for R_L = 5Ω)**
  - **+16dBm into 12.5Ω load**
  - **+30.5dBm peak power (3.75V) with +5V supply**
- **MTPR: –70dBc (25kHz to 138kHz)**
- **Maintains –82dBc out-of-band SFDR, 144kHz to 500kHz, for output power = +16dBm, R_L = 12.5Ω**
- **Input voltage noise: 4.5nV/√Hz @100kHz**
- **Low supply current: 9mA/amplifier (full power mode)**
- **Standby mode (4.5mA/amplifier)**
- **Shutdown mode (0.3mA/amplifier)**

Figure 6-151: *AD8018 xDSL line driver key specifications*

Some key AD8018 features and specifications are summarized in Figure 6-151, above.

REFERENCES: COMMUNICATIONS AMPLIFIERS

1. Bob Clarke, "Find Op Amp Noise with Spreadsheet", **Electronic Design**, December 13, 1990, or Analog Devices AN253.

2. Barrie Gilbert, "A Low Noise Wideband Variable-Gain Amplifier Using an Interpolated Ladder Attenuator," **IEEE ISSCC Technical Digest**, 1991, pp. 280, 281, 330.

NOTES:

SECTION 6-5: AMPLIFIER IDEAS

Walt Jung, Walt Kester

This section of the chapter features miscellaneous op amp applications, within a format of *amplifier ideas*. They range broadly across the spectrum, illustrating many innovative op amp uses that don't otherwise fit categories. Some of the concepts have been inspired by publication elsewhere. In such cases, an appropriate original reference is given.

High Efficiency Line Driver

Conventional video line drivers use a series or *back-termination* resistor, selected to match the transmission line characteristic impedance. Although simple, this scheme is inherently inefficient, as both load and series termination resistors drop the same voltage. This isn't usually a problem with 1Vp-p video signals operating on high voltage supplies, such as ±12V or ±15V. However, with lower voltage supplies, particularly 5V or less, driver headroom is definitely an issue. For such conditions, a conventional driver may simply not be able to accommodate a signal of twice V_{OUT} without distortion.

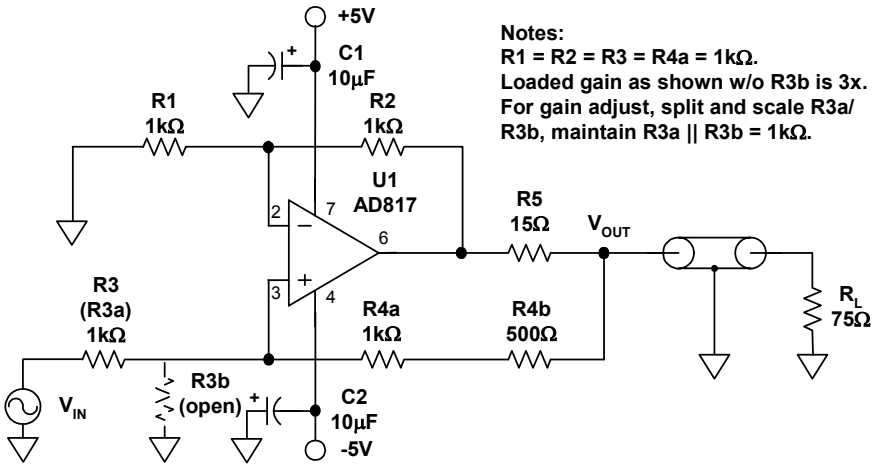


Figure 6-152: *A high efficiency video line driver*

Figure 6-152 illustrates a solution to this driver efficiency problem. In this line driver (adapted from a circuit by Victor Koren, see Reference 1), a Howland type of feedback configuration is used. This allows the series termination resistor R5 to be appreciably smaller, thus dropping less voltage and improving stage efficiency. Both positive and negative loop feedback paths are used around the op amp, R3 and R4, plus R1 and R2. An AD817 is chosen for its video characteristics, and line driving capability. The circuit also works with many other op amps, provided they have sufficient output drive.

In this example, a 75Ω line is being driven, and R5 is set to 15Ω. With the scaling chosen, this produces 1/5 the voltage drop of a more conventional 75Ω resistor. For every volt of V_{OUT}, the amplifier needs only to produce 20% more, i.e., 1.2V per V of V_{OUT}. This allows the design to operate easily on 5V or even lower supplies, and still provide undistorted 1Vp-p video signals at V_{OUT}. The ± feedback paths produce the proper synthesized source impedance when the R1-R5 resistors are properly selected.

Given the desired output impedance R_O, R5 is related by a scaling factor, so that R5 < R_O. A direct design approach is to simply set R5 at some fraction of R_O, which then leads to a R1 through R4 resistor set that will provide the proper R_O. In this example design, R5 is set at 1/5 R_O as noted earlier, or 15 ohms.

As per the notes of the figure, a major simplifying design step is to make four of the feedback resistors equal, namely R1 through R3 and R4a. It also helps further to make these a common, readily available value. This should be a value moderately higher than the target load impedance. In this case, a 1kΩ base value is chosen.

This defines the R4 value (R4a + R4b) as:

$$R4 = (R5 \bullet R1 + R_O \bullet R2)/(R_O - R5) \qquad \text{Eq. 6-31}$$

R4b is then simply R4-R4a. The design is further simplified with all of the noted resistors part of a single common array, *including* R4b (which is made from two parallel 1kΩ resistors in this case). Note that R4b won't necessarily be so easily achieved in other design examples. Nevertheless, it is desirable for as many of the R1 through R4 resistors as possible be part of a common array, matched to 1% or better.

Gain of the stage just as shown is about 3× with the output loaded. If gain must be adjusted, there is a specific procedure to be followed. This is a necessary condition for proper stage function (for any gain), and is needed to maintain the synthesized R_O. For example, if a unity (1×) overall gain is desired, R3 can be changed to two resistors, i.e., R3a = 3kΩ, R3b = 1.5kΩ. Note that this reduces the drive to the op amp, but it also maintains the same 1kΩ Thevenin impedance for R3 (where R3 is the resistance looking back to the input from R4a). Similarly, equal value 2kΩ resistors could be used, which provides a net loaded stage gain of 1.5×. Of course, for arbitrary gains, a common array may not be possible, and ordinary 1% metal film types can also be used.

Also related to the above, the driving source at V_{IN} must be a very low impedance with respect to 1kΩ, again so as to maintain the synthesized impedance relations. This is best achieved by use of an R3 driving source direct from an op amp output. Alternately, if the V_{IN} driving impedance is both fixed and known, it can be subtracted from R3.

A more general caveat (which applies to all Howland circuits) is that the design environment must maintain this source driving impedance *for all conditions*, as the circuit itself is *not* open source stable. For example, if R3 is opened, the positive feedback can override the negative feedback via R1 and R2, and the circuit could latch up.

Finally, although this design illustrates a driver oriented to a video standard of 75Ω with 1Vp-p signals, there is no reason why the same design principles cannot be applied to other impedances and/or signal levels.

A Simple Wide Bandwidth Noise Generator

While most electronic designs seek noise minimization, there are occasions where a known quantity and/or quality of spectrally flat (white) noise is desirable. One such example is a dither source for enhanced dynamic resolution A/D conversion. For such applications, it is useful to be able to predict the output of a noise generator. It turns out that a carefully chosen decompensated op amp set up to amplify its own input noise is very useful as a wideband noise generator (see Reference 2).

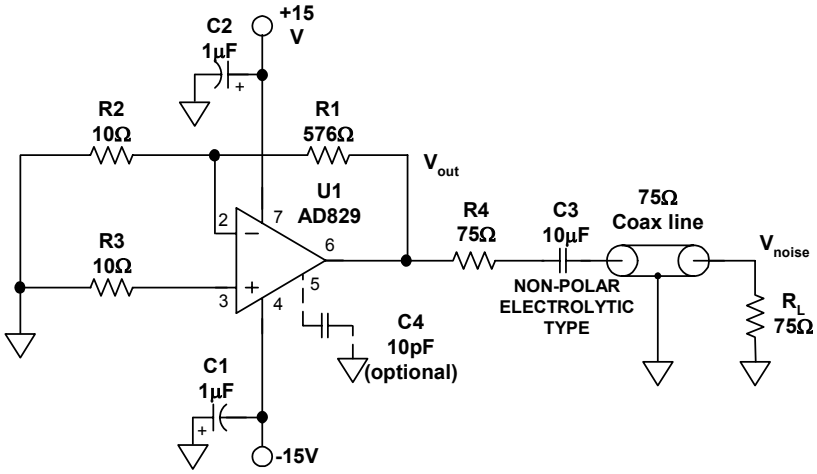


Figure 6-153: *A simple wideband noise generator*

Figure 6-153 above illustrates this technique, which simply employs the op amp U1 as a fixed gain stage, amplifying its input noise by the stage factor G, where G = 1 + (R1/R2). This process is made easier by some simplifying assumptions, as described below.

By purposely selecting R2 and R3 values of 10Ω or less, their Johnson noise contribution is forced to be less than the voltage noise of the amplifier. Similarly, the amplifier's current noise components in R2-R3, when converted to voltage noise, are also negligible. Thus the dominant circuit noise is reduced to the input voltage noise of U1.

To scale the amplifier noise to a given level of V_{noise} across R_L, select a stage gain which produces a noise density at V_{OUT} which is 2G times the typical U1 noise of 1.7nV/√Hz. This will produce a V_{OUT} twice V_{noise}. For example, for a V_{noise} of 50nV/√Hz, using a fixed R2 value of 10Ω, the required R_1 is:

$$R1 = 10 \bullet (((2 \bullet V_{noise})/1.7) - 1) \qquad \text{Eq. 6-32}$$

Where V_{noise} is in nV/√Hz, and the 1.7 is the U1 voltage noise (nV/√Hz). This computes to 576Ω (nearest standard value) for a wideband 50nV/√Hz. Alternately, an audio range noise source of 1000nV/√Hz with several hundred kHz of bandwidth is achieved with R1 = 11.8kΩ, and C3 = 100µF. By choosing a bipolar-input, voltage feedback U1 device, with a single effective gain stage, a major performance point is achieved. Such an amplifier has a flat, frequency independent input voltage noise response (i.e., a white noise characteristic). Many of the ADI high-speed amplifiers use this topology within a folded cascode architecture.

In contrast to this, multiple stage, pole-zero compensated amplifiers such as the OP27 (and other similar architectures) can have peaks in the output noise response. This is due to the frequency compensation method used, and the associated gain distributions in the signal path. When picking U1, look for a noise characterization plot which shows flat input referred voltage noise over several decades.

For the AD829 device used, input voltage noise is flat from below 100Hz to more than 10MHz, as is noted below in Figure 6-154. Within the actual circuit, the upper bandwidth limit will be gain/compensation dependent, which can be controlled as described below.

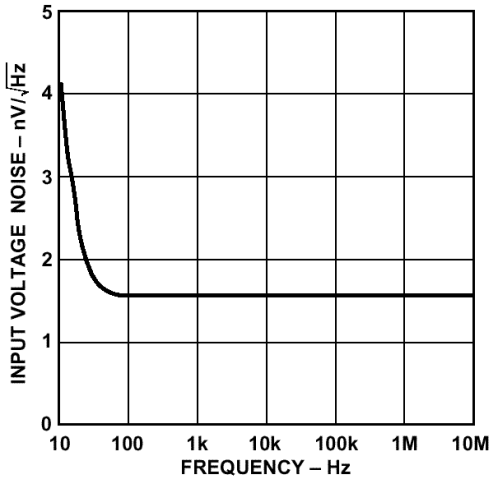


Figure 6-154: *AD829 input voltage noise spectral density*

The output is coupled through a non-polar capacitor, C3, which removes any amplified DC offset at V_{out}. The C3 value should be large enough to pass the lowest noise frequencies of interest. As shown the response of this network is –3 dB at about 100Hz, but C3 can be changed for other low frequency limits. Source termination resistance R4 allows standard 75Ω cables to be driven, providing distribution to a remote 75Ω load, R_L.

In general, this noise generator's utility is greatest with a decompensated (or externally compensated) op amp, to take advantage of the maximum bandwidth possible. For the AD829, bandwidth is highest with lowest pin 5 capacitance (i.e., no PCB pin 5 pad, or pin 5 cut off). Conversely, C4 can be used to reduce bandwidth, if desired. With minimum pin 5 capacitance, the AD829 gain-bandwidth can be above 500MHz, allowing extended response. In any case, the stage's effective -3 dB bandwidth varies inversely proportional to stage gain G. Some noise variations can be expected from IC sample-sample, so an R1 trim method can be used to set a output calibration level. Alternately, if ultra-wide bandwidth noise isn't required, another op amp to consider is the AD817.

A final note— bipolar input amplifiers such as the AD829 typically use PTAT biasing for the input's differential stage tail current. Since equivalent input noise varies as the square root of this tail current, this can make noise output vary somewhat with temperature. The net effect causes noise to change less than 1dB for a 50°C temperature change.

Single-Supply Half and Full-Wave Rectifier

There are a number of ways to construct half and full-wave rectifiers using combinations of op amps and diodes, but the circuit shown in Figure 6-155 below requires only a dual op amp, two resistors, and operates on a single supply (see Reference 3).

The circuit will work with any single-supply op amp whose inputs can withstand being pulled below ground. The AD820 (single) or AD822 (dual) op amps have N-channel JFET inputs, which allow the input voltage to go to 20V below the negative supply.

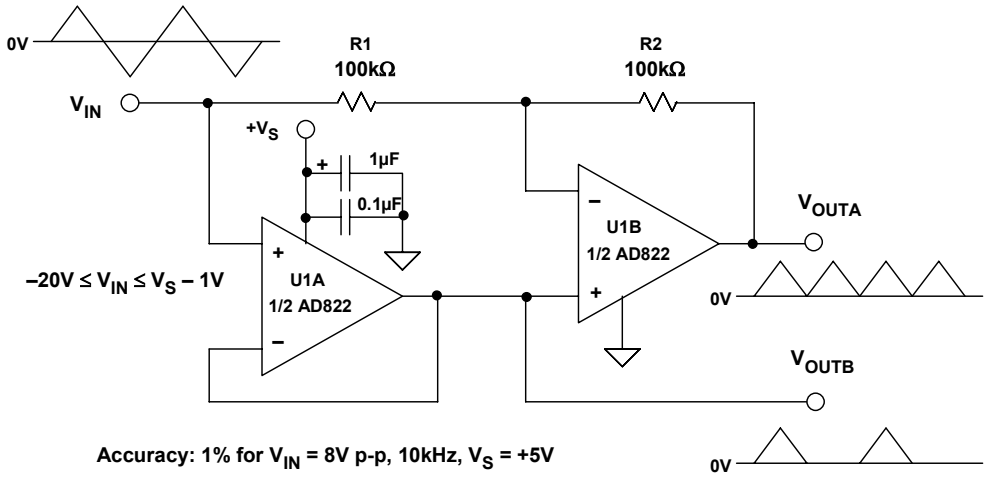


Figure 6-155: *Single-supply half and full-wave rectifier uses no diodes*

The output stage of these op amps is a complementary bipolar common emitter rail-to-rail stage with an output resistance of approximately 40Ω when sourcing current and 20Ω when sinking current. As a result of this stage, the outputs can go within a few millivolts of the supply rails under light loading.

When the input signal is above ground, unity-gain follower U1A and the loop of the amplifier U1B bootstrap R1. This bootstrapping forces the inputs of U1B to be equal. Thus, no current flows in R1 or R2, and the output V_{OUTA} tracks the input. Conversely, when the input is negative, the output of U1A is forced to zero (saturated). The non-inverting input of U1B sees the ground-level output of U1A, and during this phase operates as a unity-gain inverter, rectifying the negative portion of the input V_{IN}.

The net output at V_{OUTA} is therefore a full-wave rectified version of V_{IN}. In addition, a half-wave rectified version is obtained at the output of U1A (V_{OUTB}) if desired.

The circuit operates with a single power supply of +3 to +20V. The circuit will maintain an accuracy of better than 1% over a 10kHz bandwidth for inputs of 8Vp-p on a +5V supply. The input should not go more than 20V below the negative supply, or closer than 1V to the positive supply. Inputs of ±18V can be rectified using a single +20V supply.

Paralleled Amplifiers Drive Loads Quietly

Paralleling op amps is a method to increase load drive while keeping output impedance low, and also to reduce noise voltage. Figure 6-156A below shows a classic stacked-amplifier circuit. This configuration halves the input voltage noise of a single op amp, and quadruples load drive. However, it does have several weaknesses.

First, you need to set the correct gain for each amplifier *individually*. Second, series resistors must be added to each output, to ensure equal load current distribution among the op amps. Third, the input range can become limited at high gains because of the inherent offset of any of the amplifiers.

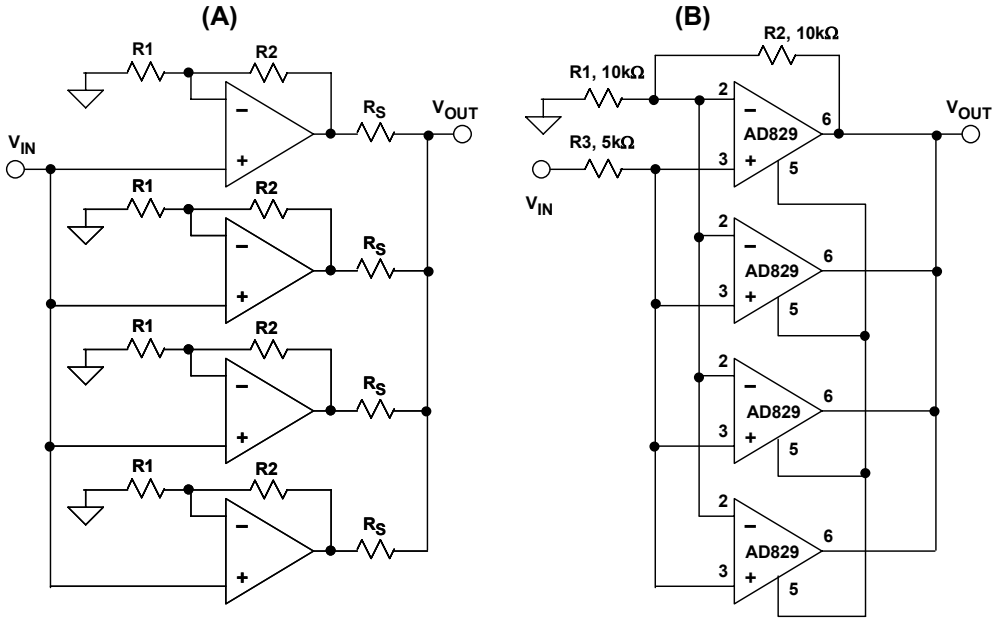


Figure 6-156: *Paralleled amplifiers drive loads quietly*

The circuit shown in Figure 6-156B also has half the noise voltage of an individual amplifier, and it also quadruples the load drive. But in so doing, it reduces the component count from twelve resistors to three (see Reference 4). In addition, the circuit has a gain-bandwidth product of about 750MHz. Although the topology of Figure 6-156B is generally applicable to all externally compensated amplifiers (i.e., those with a pinned-out high impedance node before the output driver stage— such as the AD844 and AD846), the AD829 op amp is particularly well suited to video and other broadband applications.

Note that in the B circuit, external R_S load sharing resistors aren't required, because the only voltage difference between the individual outputs is due to the slight offset mismatch between the AD829 complementary emitter follower output driver stages, and internal 15Ω emitter resistors ensure equal output current distribution. The closed-loop gain has no effect on this small offset voltage.

The end result of the 4 paralleled output stages in Fig. 6-156B is a composite amplifier with both greater load drive and lower noise, but using only the conventional feedback

components. The circuit in B increases the drive current by a factor of four, similar to A, but with a vast difference in the parts count.

In order to understand how the circuit reduces noise, let the RTI voltage noise of the individual op amps be V_{N1}, V_{N2}, V_{N3}, and V_{N4}, and let the total noise voltage be V_N.

Because all the inputs are connected in parallel, as well as the high impedance nodes, then:

$$(V_N - V_{N1})gm + (V_N - V_{N2})gm + (V_N - V_{N3})gm + (V_N - V_{N4})gm = 0 \quad \text{Eq. 6-33}$$

$$V_N = \tfrac{1}{4}\,(V_{N1} + V_{N2} + V_{N3} + V_{N4}). \quad \text{Eq. 6-34}$$

But because the voltage noise of the amplifiers is uncorrelated, and the noise spectral density for each amplifier is the same:

$$V_N = \tfrac{1}{4}\,\sqrt{[4(V_{N1})^2]} \quad \text{Eq. 6-35}$$

$$V_N = V_{N1} / 2 \quad \text{Eq. 6-36}$$

This result also implies that all uncorrelated parameters such as input offset voltage, input offset voltage drift, CMRR, PSRR, etc., will also approach their true mean values, thus reducing effects arising from the variability of the devices.

The AD829 is flexible and can operate on supply voltages from ±5V to ±15V. It's uncompensated gain-bandwidth product is 750MHz. Nominal output current for rated performance is 20mA, so in the circuit shown, 80mA is available to drive the load.

The input voltage noise of a single AD829 is 1.7nV/√Hz, so the parallel circuit has an input voltage noise of approximately 0.85nV/√Hz. In order to take advantage of this low voltage noise, however, the circuit must be driven from a relatively low source impedance, because the input current noise of a single AD829 is 1.5pA/√Hz. In the parallel circuit, the input current noise is therefore 3pA/√Hz.

Notice that in the AD829 circuit, R3 = R1||R2 for bias current cancellation. This works because the input bias currents of the AD829 are not internally compensated: they are approximately equal, and of the same sign. If amplifiers with internal bias current compensation or current feedback op amps are used, the input bias currents may not be equal or of the same sign, and R3 should be made equal to zero.

Power-Down Sequencing Circuit for Multiple Supply Applications

The operating time of battery operated portable equipment can be extended by using power-down techniques. Many new components offer a power-down feature to implement this function. However, there may be times when this feature is not offered and other means must be devised. The solution may also require proper power supply sequencing in multiple supply systems.

Figure 6-157 shows a single-supply op amp powered from +15V driving an single-supply ADC powered from +5V. In many cases, the same +5V can supply the op amp and the ADC, and in that case, there is no sequencing problem. However, in some cases better system performance is obtained by driving the op amp with a higher supply voltage.

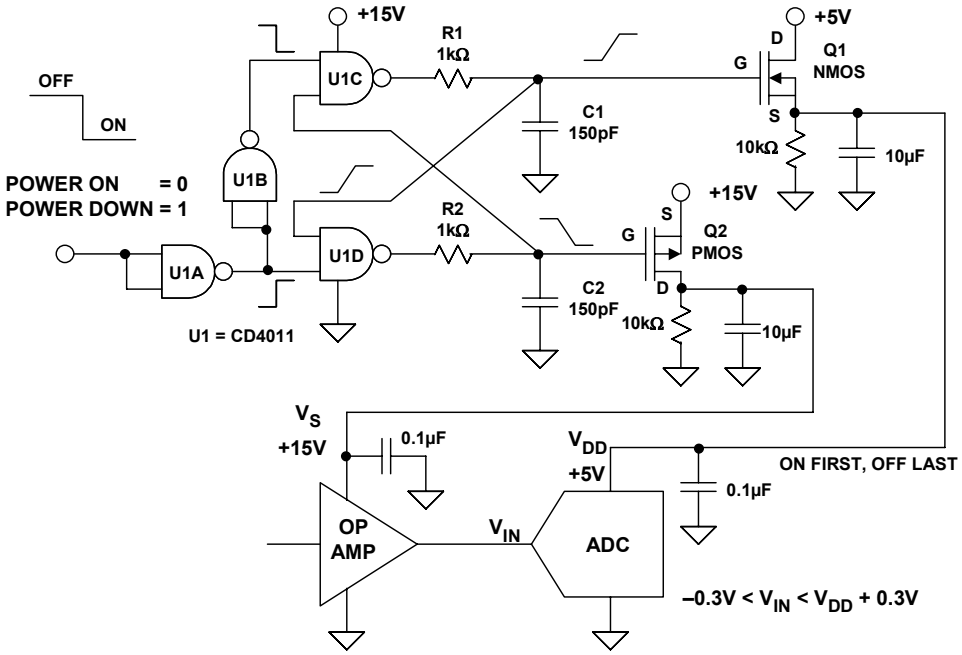


Figure 6-157: *Power-down sequencing circuit for multiple supply applications*

In the circuit, MOSFETs Q1 and Q2 switch the +5V and the +15V to the devices in the proper sequence. On power-up, the voltage to the ADC must be supplied first; and on power-down, the voltage to the ADC must be removed last. This is to ensure that the V_{IN} input to the ADC is never more than 0.3V above the V_{DD} positive supply or more than 0.3V below the negative supply, thereby preventing damage and possible latch-up.

The MOSFETs, Q1 and Q2 switch the +5V and the +15V to the ADC and the op amp, respectively, in a sequence controlled by two cross-coupled CD4011 CMOS NAND gates (U1C and U1D). The gates are powered from the +15V supply so that sufficient gate drive voltage is available to turn Q1 and Q2 on and off.

To initiate the power-on mode, a logic 0 is applied to the input of U1A, forcing it's output high. This forces the output of U1B low, which causes U1C's output to go high. The R1-C1 time constant delays the application of the +15V to the gate of Q1 which ultimately

turns Q1 on with 5V at its source. The delayed output of U1C is also applied to an input of U1D which forces it's output low. U1D's output is delayed by the R2-C2 time constant, and ultimately forces the gate of Q2 to zero, which applies +15V to the drain of Q2, and to the op amp V_S supply.

To initiate the power-down mode, a logic 1 is applied to the input of U1A which forces it's output to zero, and the output of U1D is forced high, ultimately turning off Q2, the +15V supply. The delayed output of U1D is applied to an input of U1C, the output of U1C goes low, and ultimately the gate of Q1 is forced to zero, turning off the +5V to the V_{DD} input of the ADC.

It is important to note that when system power is applied to the overall circuit, the +5V should come up either before, or simultaneously with the +15V. Similarly, when system power is removed, the +15V should be removed first or simultaneously with the +5V.

This circuit is based on a modification of the one described in Reference 5, where the desired sequencing is the reverse of the one described here. The reverse sequence (+15V turned on before +5V, and +5V turned off before +15V) can be easily achieved by replacing the CD4011 NAND gates with CD4001 NOR gates, reversing the "sense" of the power-on/power-down control input, and swapping the gate drive signals to Q1 and Q2.

Programmable Pulse Generator Using the AD8037 Clamping Amplifier

The AD8036 (G ≥ 1 stable) and AD8037 (G ≥ 2 stable) clamp amplifier outputs can be set accurately to a well controlled flat levels determined by the clamping voltages. This, along with wide bandwidth and high slew rate suits them well for numerous applications.

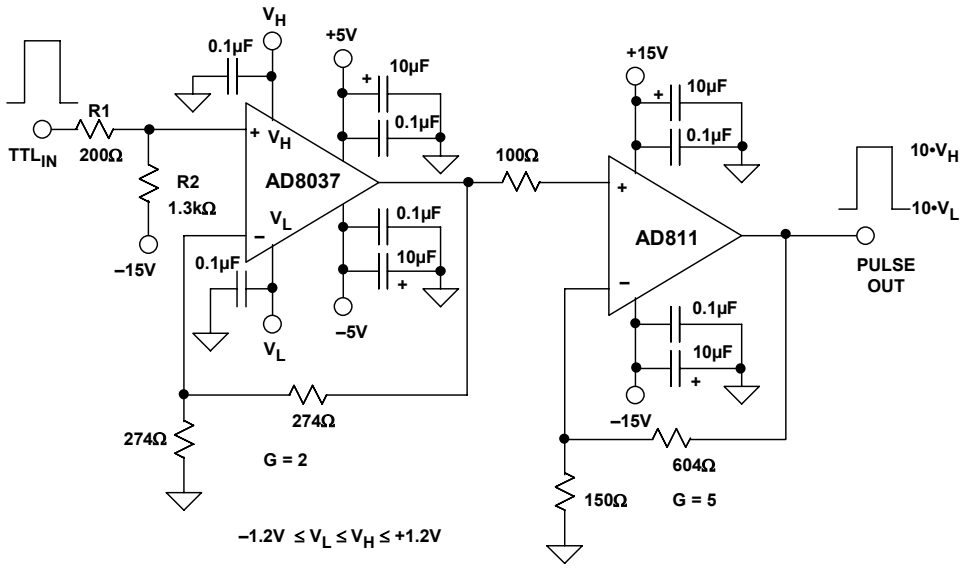


Figure 6-158: *Programmable pulse generator using AD8037 clamping amplifier*

A basic description of the AD8036/AD8037 operation can be found in the Video Applications section of this chapter. Figure 6-158 above is a diagram of a programmable level pulse generator (see Reference 6).

The circuit accepts a TTL timing signal for its input and generates pulses at the output up to 24Vp-p with 2500V/µs slew rate. The output levels can be programmed to anywhere in the range between –12V to +12V.

The circuit uses an AD8037 operating at a gain of two with an AD811 to boost the output to the ±12V range. The AD811 was chosen for its ability to operate with ±15V supplies and its high slew rate. R1 and R2 level shift the TTL input signal level approximately 2V negative, making it symmetrical above and below ground. This ensures that both the high and low logic levels will be clamped by the AD8037. For well controlled signal levels in the output pulse, the high and low output levels result from the clamping action of the AD8037 and aren't controlled by either the high/ low logic levels passing through a linear amplifier. For good output rise/fall times, logic with high edge speed should be used.

The high logic levels are clamped at 2 times the voltage at V_H, while the low logic levels are clamped at two times the voltage at V_L. The output of the AD8037 is amplified by the AD811 operating at a gain of 5. The overall gain of 10 will cause the high output level to be 10 times the voltage at V_H, and the low output level 10 times the voltage at V_L. For this gain, the clamping levels for a ±12V output pulse are V_H = +1.2V and V_L = –1.2V.

Full-Wave Rectifier Using the AD8037 Clamping Amplifier

The clamping inputs can be used as additional inputs to the AD8036/AD8037. As such, they have an input bandwidth comparable to the amplifier inputs and lend themselves to some unique functions when they are driven dynamically.

Figure 6-159 (opposite) is a schematic for a full wave rectifier, also called an absolute value generator (Reference 6 again). It works well up to 20MHz and can operate at significantly higher frequencies with some performance degradation. The distortion performance is significantly better than diode-based full-wave rectifiers, especially at high frequencies.

The AD8037 is configured as an inverting amplifier with a gain of unity. The V_{IN} input drives the inverting amplifier and also directly drives V_L, the lower level clamping input. The high level clamping input, V_H, is left floating and plays no role in the circuit.

When the input is negative, the amplifier acts as a unity-gain inverter and outputs a positive signal at the same amplitude as the input, with opposite polarity. V_L is driven negative by V_{IN}, so it performs no clamping action, because the positive output signal is always higher than the negative level driving V_L.

When the input is positive, the output result is the sum of two separate effects. First, the inverting amplifier multiplies the V_{IN} input by –1, because of the unity-gain inverting configuration. This effectively produces an offset at the output, but with a dynamic level that is equal to –1 times the input. Second, although the positive input is grounded (through 100Ω), the output is clamped at two times the voltage applied to V_L (a positive, dynamic voltage in this case). The factor of two is because the 2× amplifier noise gain.

The sum of these two actions results in an output that is equal to unity times the input signal for positive input signals, as shown in Figure 6-159. Thus, for either positive or negative input signals, the output is unity times the absolute value of the input signal. The circuit can be easily configured to produce the negative absolute value of the input by applying the input to V_H rather than V_L.

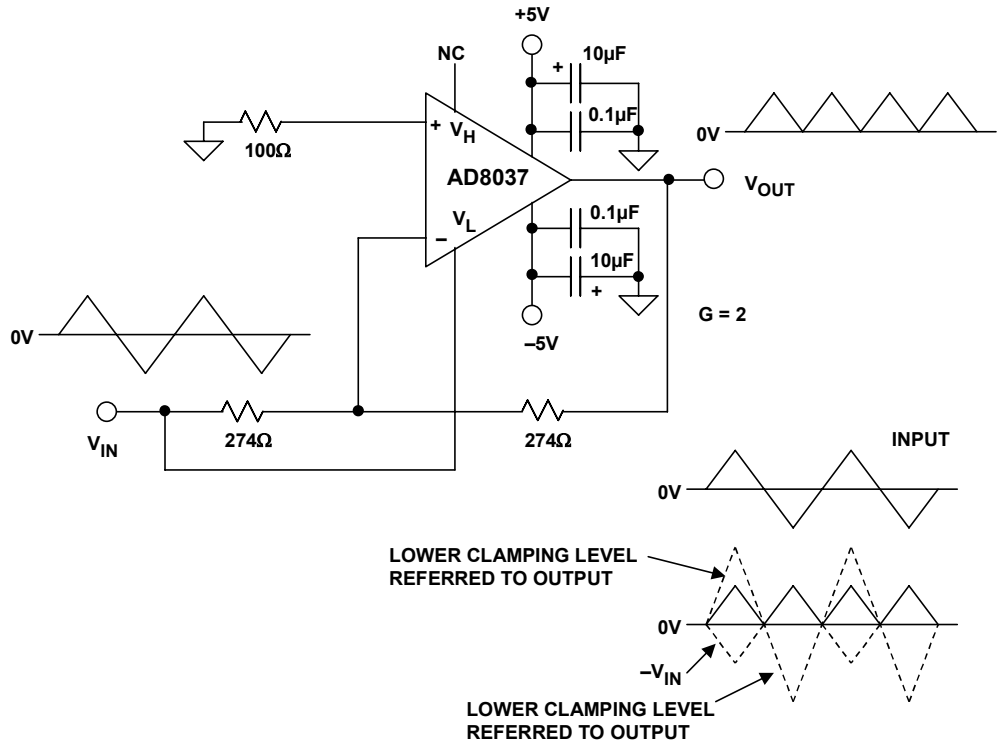


Figure 6-159: *Full-wave rectifier using the AD8037 clamping amplifier*

The circuit can get to within about 40mV of ground during the time when the input crosses zero. This voltage is fixed over a wide frequency range, and is a result of the switching between the conventional op amp input and the clamp input. However, because there are no diodes to rapidly switch from forward to reverse bias, the performance far exceeds diode-based full wave rectifiers. Signals up to 20MHz can be rectified with minimal distortion.

If desired, the 40mV offset can be removed by adding an offset to the circuit, with little additional complexity. A 27.4kΩ input resistor to the inverting input will have a gain of 0.01, while changing the gain of the circuit by only 1%. A plus or minus 4V DC level (depending on the polarity of the rectifier) fed into this resistor will then compensate for the offset.

Full wave rectifiers are useful in many applications including AM signal detection, high frequency AC voltmeters, and various arithmetic operations.

AD8037 Clamping Amplifier Amplitude Modulator

The AD8037 can also be configured as an amplitude modulator as shown in Figure 6-160 (Reference 6 again). The positive input of the AD8037 is driven with a square wave of sufficient amplitude to produce clamping action at both the high and low levels set by V_H and V_L. This is the higher frequency carrier signal.

The modulation signal is applied to both the input of a unity gain inverting amplifier and to V_L, the lower clamping input. V_H is biased at +0.5V for the example to be discussed but can assume other values.

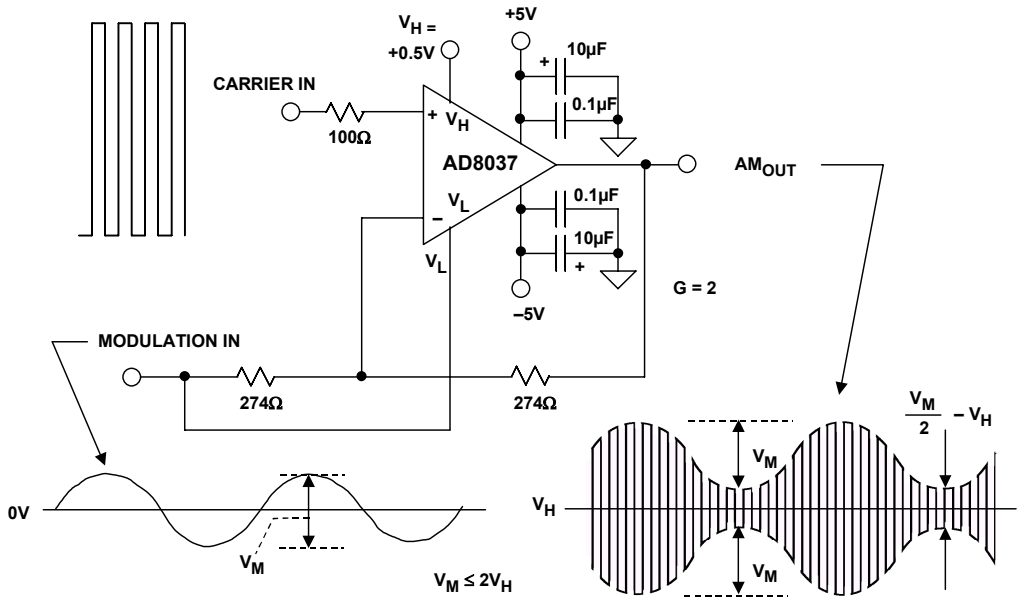


Figure 6-160: *AD8037 clamping amplifier amplitude modulator*

To understand the circuit operation, it is helpful to first consider a simpler circuit. If both V_H and V_L are DC biased at +0.5V and –0.5V, respectively, and the carrier and modulation inputs driven as above, the output would be a 2Vp-p square wave at the carrier frequency riding on a waveform at the modulating frequency.

The inverting input (modulation signal) is creating a varying offset to the 2Vp-p square wave at the output. Both the high and low levels clamp at twice the input levels on the clamps because the noise gain of the circuit is two.

When V_L is driven by the modulation signal instead of being held at a DC level, a more complicated situation results. The resulting waveform is composed of an upper envelope and a lower envelope with the carrier square wave in between. The upper and lower envelopes are 180° out of phase as in a typical AM waveform.

The upper envelope is produced by the upper clamp level being offset by the waveform applied to the inverting input. This offset is the opposite polarity of the input waveform because of the inverting configuration.

The lower envelope is produced by the sum of two effects. First, it is offset by the waveform applied to the inverting input as in the case of the simpler circuit above. The polarity of this offset is in the same direction as the upper envelope.

Second, the output is driven in the opposite direction of the offset at twice the offset voltage by the modulation signal being applied to V_L. This results from the noise gain being equal to two, and since there is no inversion in this connection, it is opposite in polarity from the offset.

The result at the output for the lower envelope is the sum of these two effects, which produces the lower envelope of an AM waveform. The depth of modulation can be modified by changing the amplitude of the modulation signal. This changes the amplitude of the upper and lower envelope waveforms.

The modulation depth can also be changed by changing the DC bias applied to V_H. In this case, the amplitudes of the upper and lower envelope waveforms stay constant, but the spacing between them changes. This alters the ratio of the envelope amplitude to the amplitude of the overall waveform.

For $V_H = +0.5V$, 100% modulation occurs when the peak-to-peak amplitude of the modulation input $V_M = 1V$. The AM output is always offset by V_H for a bipolar modulation input. In general, for a peak-to-peak modulation amplitude of V_M, the two output modulated envelopes are separated by an amount equal to $V_M/2 - V_H$.

Sync Inserter Using the AD8037 Clamping Amplifier

Video signals typically combine an active video region with both horizontal and vertical blanking intervals during their respective retrace times. A sync signal is required during the blanking intervals in some systems. In RGB systems, the sync is usually inserted on the Green signal. In composite video systems, it is inserted during blanking on the single-channel composite signal, or on the luminance (or Y) signal in an S-video system. Further details on video signals can be found in the Video Applications section of this chapter.

The AD8037 input clamping amplifier can be used to make a video sync inserter that does not require accuracy in the amplitude or shape of the sync pulse (see Reference 7). The circuit shown below in Figure 6-161 uses the AD8037 to create the proper amplitude sync insertion, and the DC levels of the sync pulse do not affect the active video level. The circuit is also non-inverting with a gain-of-two, which allows for driving a back-terminated cable with no loss of amplitude.

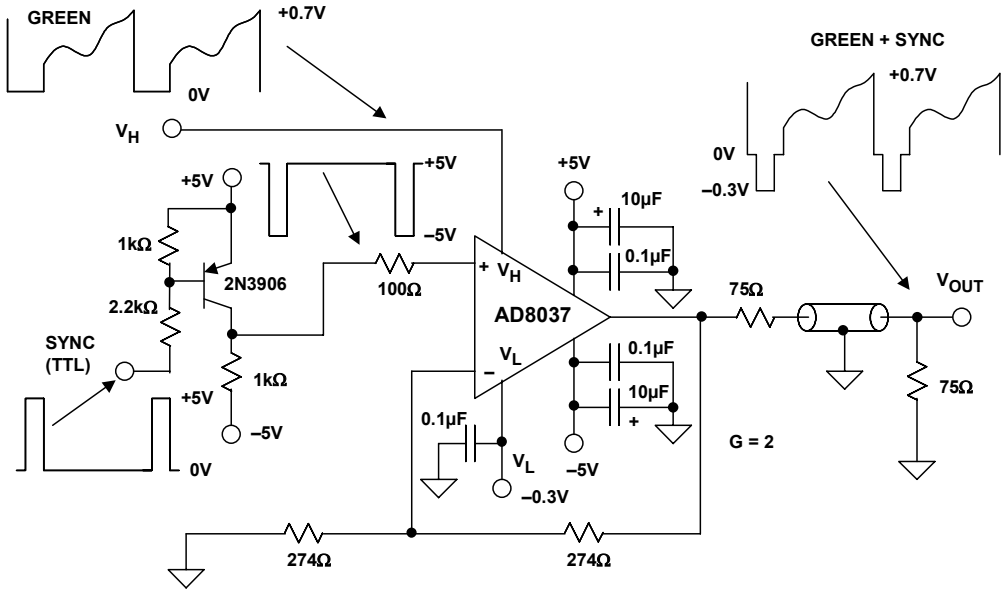


Figure 6-161: *Sync inserter using the AD8037 clamping amplifier*

The Green video signal is applied to the V_H input of the AD8037. This signal has a blanking level of 0V and an approximate full-scale value of +0.7V. The TTL-level sync pulse is applied to the base of the 2N3906 transistor. The signal at the collector of the 2N3906 are inverted sync pulses with an amplitude of 10Vp-p which are applied to the non-inverting input of the AD8037.

The amplitude of the signal into the non-inverting input of the AD8037 is +5V during the active video portion, and since this is greater than the maximum positive Green signal excursion of +0.7V on the V_H input, the Green signal is passed through to the output of the AD8037 with a gain of +2.

During the blanking interval, the sync signal into the non-inverting input of the AD8037 goes to –5V, and the output of the AD8037 is clamped to a value which is 2 times the DC

level on the V_L input. Nominally, the sync should be –0.3V referenced to a 0V blanking level, and this level is applied to V_L from a voltage reference, or a simple divider.

The high and low levels of the sync pulse generated by the 2N3906 can be relatively loosely defined. The value of the high-level sync input to the non-inverting input of the AD8037 must be higher than the active video signal; the value of the low-level sync input must be lower than the DC voltage on the V_L input. The rising and falling edges of the sync pulse input determine the timing of the inserted sync, but the DC level at the V_L input of the AD8037 will always determine the sync amplitude.

The 2N3906 PNP transistor serves as a level translator and simply provides an appropriate drive signal from a TTL source of positive-going sync. The sync input to the non-inverting input of the AD8037 neither influences the DC level of the output video nor determines the amplitude of the inserted sync.

AD8037 Clamped Amplifier As Piecewise Linear Amplifier

Piecewise linear amplifiers are often implemented using diodes in the feedback loop of an op amp. When the diodes become forward biased, they switch in resistors that alter the closed-loop gain of the amplifier.

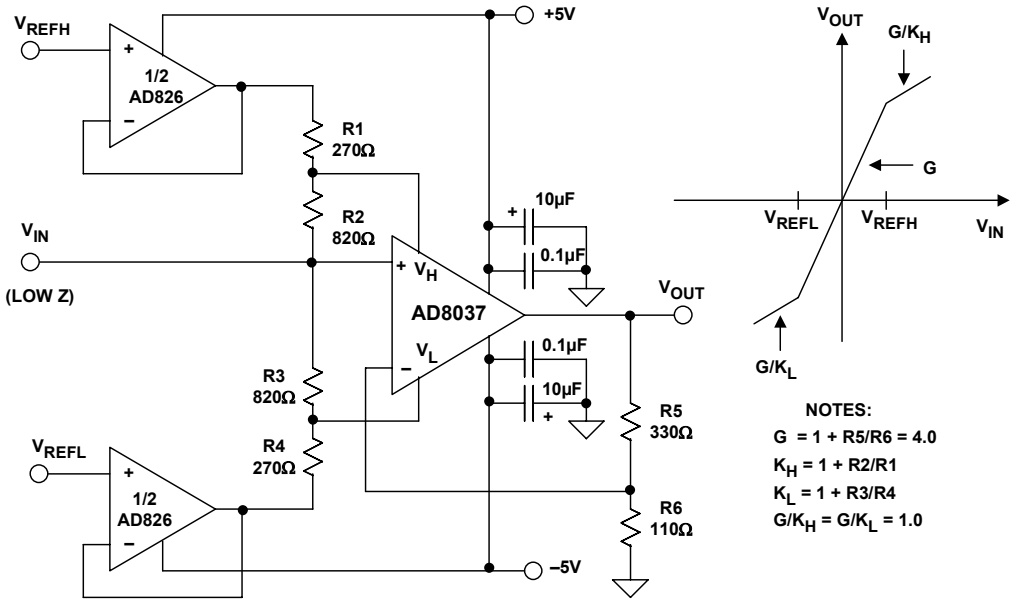


Figure 6-162: *Piecewise linear amplifier uses AD8037 clamping amplifier rather than diodes*

This approach has three disadvantages. First, the diode's forward voltage drop (even with Schottky diodes) reduces accuracy and speed during the switching region. Second, diode stray capacitance can limit bandwidth. Third, the 2mV/ºC drift of the diode's forward bias voltage introduces errors in the transfer function. The circuit shown in Figure 6-162 avoids these problems by using the fast and accurate clamping function of the AD8037 to set the breakpoints (see Reference 8).

If the V_{IN} signal applied to the noninverting input of the AD8037 lies between the clamp voltages (set by V_{REFH} and V_{REFL}), the AD8037 works as a standard op amp with a gain = G = 1 + R5/R6. If the input signal is greater than the upper clamp voltage, V_H, the amplifier disconnects the input signal, and V_H becomes the noninverting signal input. Likewise, if the signal at the noninverting input of the AD8037 is below the lower clamp voltage, V_L, then the amplifier also disconnects the signal input, and V_L becomes the noninverting signal input.

Figure 6-162 also graphically illustrates the operation of the circuit. When V_{IN} is between V_{REFH} and V_{REFL}, the circuit is a standard noninverting op amp with a gain G = 1 + R5/R6. When V_{IN} is greater than V_{REFH}, V_H becomes the noninverting input to the amplifier.

The transfer function from V_{IN} to V_{OUT} comprises two parts under this condition. From V_{IN} to V_H, the signal is attenuated by a factor K_H = 1 + R2/R1. From V_H to V_{OUT}, the gain remains G = 1 + R5/R6. This leads to an overall gain of G/K_H in this region. The circuit behaves similarly when V_{IN} is below V_{REFL}. The gain in this condition is G/K_L, where K_L = 1 + R3/R4.

Careful layout ensures adherence to the desired nonlinear transfer function over a 5MHz bandwidth. The stability of the breakpoints is determined by the tracking of the resistor temperature coefficients, the 10µV/ºC offset voltage drift of the AD8037, and the temperature stability of the reference voltages.

The reference voltages can be generated using precision voltage references or DACs. To maintain accuracy, the reference voltages should be buffered with a fast op amp, such as the dual AD826, to provide a low source impedance throughout the input signal bandwidth.

The analog input voltage, V_{IN}, should also be driven from a low impedance source, such as an op amp, to prevent errors due to the loading effect of the R1-R2-R3-R4 network.

Using the AD830 Active Feedback Amplifier as an Integrator

The active feedback amplifier topology used in the AD830/AD8130 can be used to produce a precision voltage-to-current converter, which in turn, makes possible the creation of grounded-capacitor integrators (see Reference 9).

The design discussed here uses the AD830 to deliver a bipolar output current at high impedance (see Figure 6-163 below). Using R = 1kΩ, the output current is simply equal to V_{IN}/R, or 1mA per volt of input. The maximum output current is limited to ±30mA by the output drive capability of the AD830.

The output resistance is determined by the CMR performance of the AD830. A CMR of 60dB yields an effective output resistance of 1000 × R. The output impedance at any frequency can be determined by consulting the CMR data provided in the data sheet. The compliance range on the output is ± (V_S – 2V) reduced or increased by V_{IN}.

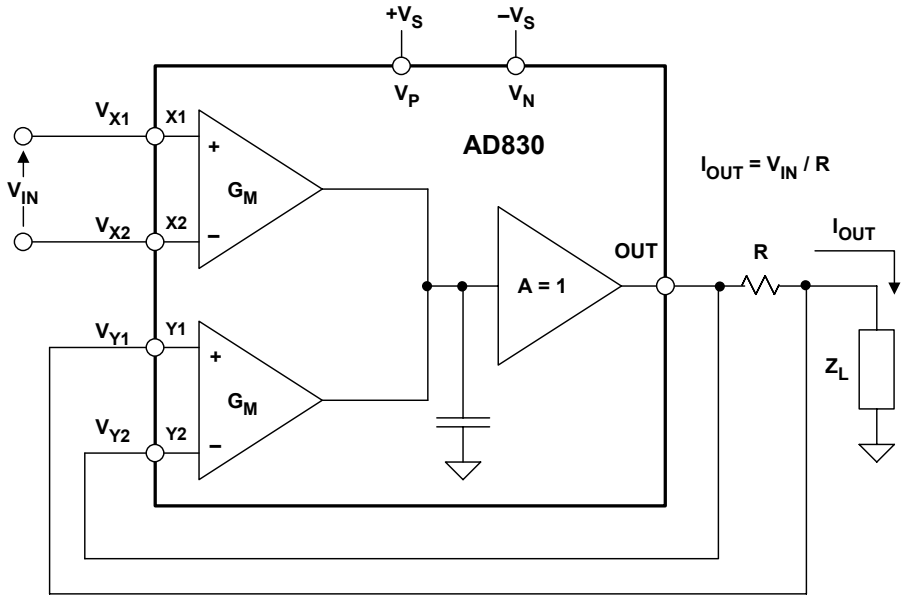


Figure 6-163: *Constant current source using the AD830 active feedback amplifier*

Figure 6-164A (next page) shows a standard op-amp integrator circuit using the AD825, and Figure 6-164B shows the improved AD830 grounded-capacitor circuit. The DC operating point for testing purposes is determined by R1 in the AD825 op amp circuit, and by R1 and C1 in the AD830 circuit. R2 and C2 determine the integrator time constant in both circuits.

If the op amp in Figure 6-164A is assumed to be ideal, i.e., zero output impedance, and infinite input impedance, then the only difference between the two circuit topologies is the finite input resistance of the op amp based integrator as set by R2.

However, in a real op amp, the output resistance is finite and increases with signal frequency as the open-loop gain decreases. This causes the "ground" at the output of the op amp to degrade at high frequencies. The result is a relatively large spike on the output voltage waveform whenever the input switches.

This can be explained as follows. Assume the input V_{IN} switches between $-V_A$ and $+V_A$. When the input is at $-V_A$ long enough for the op amp to settle, then the current in resistor R2 is $-V_A/R2$, and the output increases due to C2 being charged by the op amp. As V_{IN} suddenly switches to $+V_A$, the voltage across C2 cannot change instantaneously, and neither can the op amp's output because it behaves itself as an integrator. This implies that the change in input voltage will be impressed upon the voltage divider formed by the R_O of the op amp and R2. This change in voltage at V_{OUT} will also be coupled by C2 to the summing node at the inverting input of the op amp.

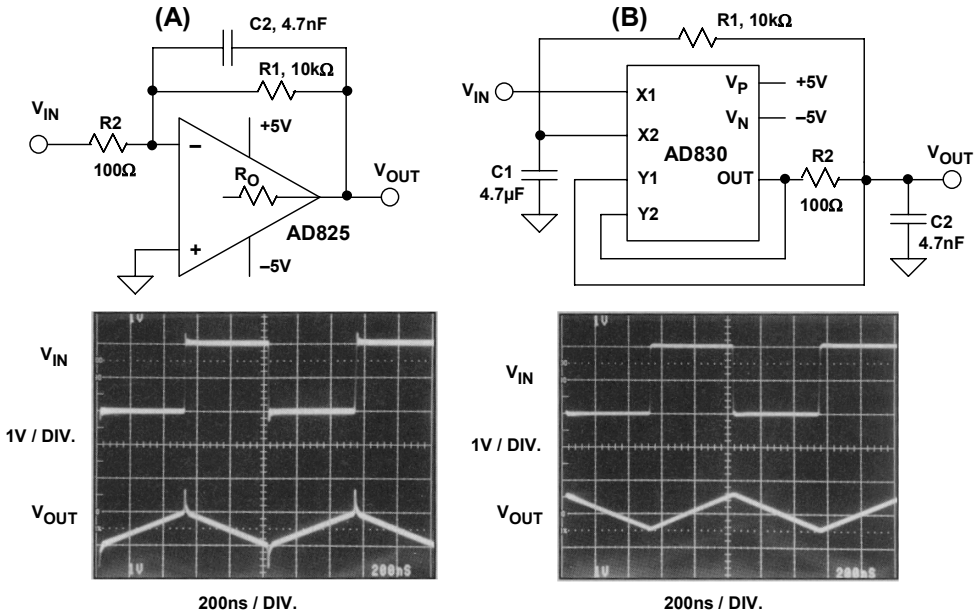


Figure 6-164: *Traditional op amp integrator vs. grounded capacitor integrator*

If V_{IN} is generated by a source with finite source resistance, this voltage spike will also appear at the input. Only after the amplifier settles will the external components again define the integrator time constant and the circuit function as desired.

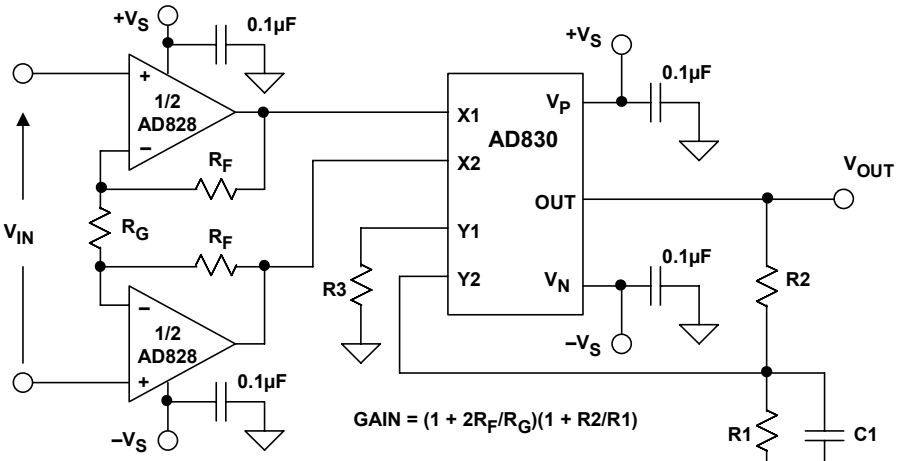
It can be seen by comparing the waveforms of (A) and (B) that no spike develops in the output waveform produced by the grounded capacitor integrator using the AD830. This is because the integrating capacitor is connected to a true ground. In addition, the input is completely isolated from the output. Therefore, if an aberration did occur, it would not be coupled back to the driving source.

Various active filter topologies can be realized from this fundamental integrator building block. For example, two such sections can implement a biquad. An example of a simple all-pass filter using the AD830 is described in Reference 10.

Instrumentation Amplifier with 290MHz Gain-Bandwidth

The circuit shown in Figure 6-165 below combines a dual AD828 op amp with the AD830 active feedback difference amplifier to form a high frequency instrumentation amplifier (see Reference 11). The circuit's performance for ±5V supplies for gains of 10 and 50 are shown in the figure, along with appropriate component values.

The circuit can be configured for different gains, and will operate on supplies ranging from ±4V to ±16.5V.



NOTE: V_S = ±5V

GAIN	R_F	R_G	R1	R2	R3	C1
10	1050Ω	1050Ω	348Ω	348Ω	169Ω	60pF
50	1150Ω	255Ω	127Ω	510Ω	100Ω	300pF

GAIN	3dB BW	SLEW RATE	0.1% SETTLING TIME	CMR@1MHz	V_N@10kHz	I_N@10kHz	V_{OS}	I_S
10	14.2MHz	200V/µs	80ns	64dB	15nV/√Hz	1.5pA/√Hz	0.6mV	27.5mA
50	5.8MHz	60V/µs	200ns	64dB	15nV/√Hz	1.5pA/√Hz	0.6mV	27.5mA

Figure 6-165: *Instrumentation amplifier with 290MHz gain-bandwidth*

The gain is proportioned between the AD828 stage and the AD830 stage, such that the closed-loop bandwidths of both stages are approximately equal. Under these conditions, a gain-bandwidth of 290MHz is obtained.

The input AD828 stage dominates the effective referred-to-input (RTI) input voltage noise and offset voltage. Capacitor C1 causes gain peaking in the AD830 which compensates for the AD828 input stage rolloff. The optimum value for C1 must be determined experimentally in a prototype or by a careful SPICE evaluation.

Note that R3 is made equal to the parallel combination of R1 and R2 to provide first-order input bias current cancellation at the Y1-Y2 input of the AD830.

Programmable Gain Amplifier with Arbitrary Attenuation Step Size

The R/2R ladder is a popular resistor topology often used to implement a current or voltage 6dB step attenuator. However, if the resistors are appropriately scaled, the network can be modified to provide any desired attenuation step.

A programmable gain amplifier (PGA) can be made with a attenuating ladder network followed by CMOS multiplexer and a fixed gain amplifier, as in Figure 6-166 below. This circuit has several advantages (see Reference 12).

First, as stated above, the attenuation step size doesn't have to be 6dB. Manipulating the resistor ratios, as described below, can easily change it. Second, the bandwidth of the circuit is always the same, regardless of the attenuation, due to the fact that the op amp buffer operates at a fixed gain. Third, the circuit is flexible, because practically any CMOS multiplexer and op amp can be used. The bandwidth of the circuit is determined primarily by the output op amp. Switching time between gain settings is determined by the multiplexer switching time and the op amp settling time.

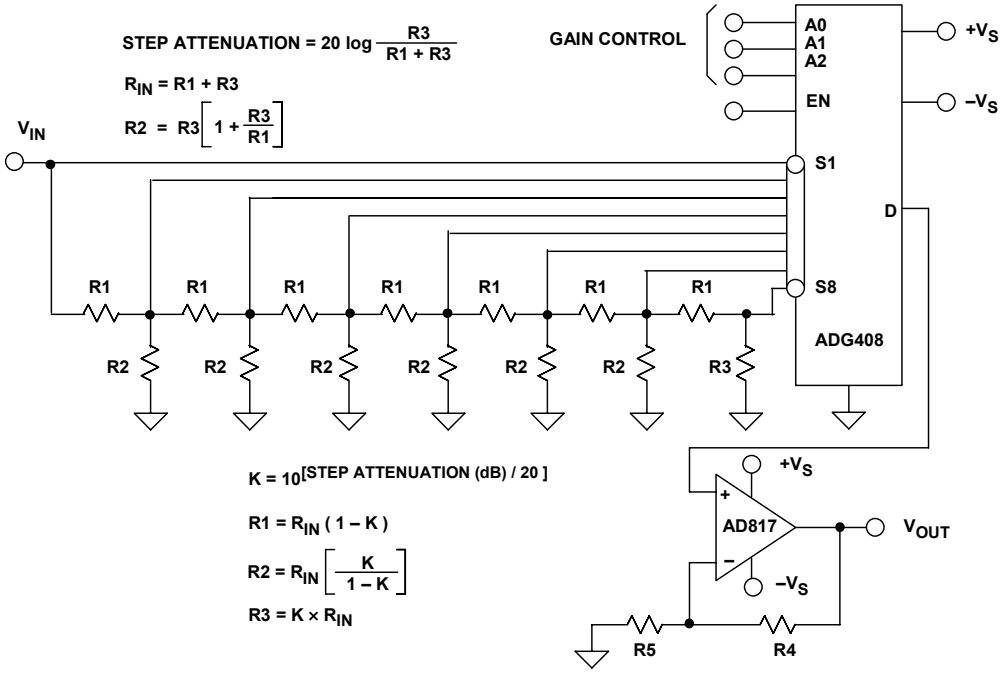


Figure 6-166: *Programmable gain amplifier with arbitrary attenuation step size*

The resistor ladder as shown uses three different resistor values: R1, R2, and R3. The step attenuation in dB is given by

$$\text{Step Attenuation (dB)} = 20\log\,[R3/(R1 + R3)] \qquad \text{Eq. 6-37}$$

Also, the following relationships apply:

$$R_{IN} = R1 + R3 \qquad \text{Eq. 6-38}$$

$$R2 = R3\ [1 + R3/R1] \qquad \text{Eq. 6-39}$$

If R1 = R3, then R2 = 2 × R1. In this case, the R-2R network provides 6dB step attenuation.

To determine the resistor values for a specific step attenuation and input resistance, use the formulas as follows:

$$K = 10^{[\text{Step Attenuation (dB)} / 20]} \qquad \text{Eq. 6-40}$$

where the step attenuation is entered as a negative number.

Then, the following equations complete the design:

$$R1 = R_{IN}\ (1 - K) \qquad \text{Eq. 6-41}$$

$$R2 = R_{IN} \times K / (1 - K) \qquad \text{Eq. 6-42}$$

$$R3 = K \times R_{IN} \qquad \text{Eq. 6-43}$$

For example, to implement a resistor ladder with a −1.5dB step attenuation and a 500Ω input impedance: K = 0.8414, R1 = 79.3Ω, R2 = 2653Ω, and R3 = 420.7Ω using the above equations.

The gain of the op amp is equal to 1 + R4/R5. The overall gain of the PGA is equal to the op amp gain minus the attenuation setting.

Finally, it is interesting to note that the AD60x-series of X-Amps® discussed in the previous "Communications Amplifiers" section of this chapter uses the same basic approach described above. In the AD60x X-Amp® series however, attenuation is continuously variable, because an interpolation circuit rather than a multiplexer is used to connect the individual taps of the network to the op amp input.

A Wideband In-Amp

Some op amps with provisions for external offset trim can be used in unusually creative ways. In fact, if the two offset null inputs are considered as an additional differential signal input pair, this point becomes more clear. Although designed principally for adjustment of device V_{OS}, the null inputs can often be used for additional signals. An example is the wideband in-amp of Gerstenhaber and Gianino (see Reference 13). In the circuit of Figure 6-167 below, the op amp used is the AD817. Designed for low distortion video circuits, it has a relatively high resistance between the input differential pair emitters, R_E, approximately 1kΩ. It also has internal, large-value 8kΩ resistors in series with the V_{OS} nulling terminals at pins 1 and 8, labeled here as R_1.

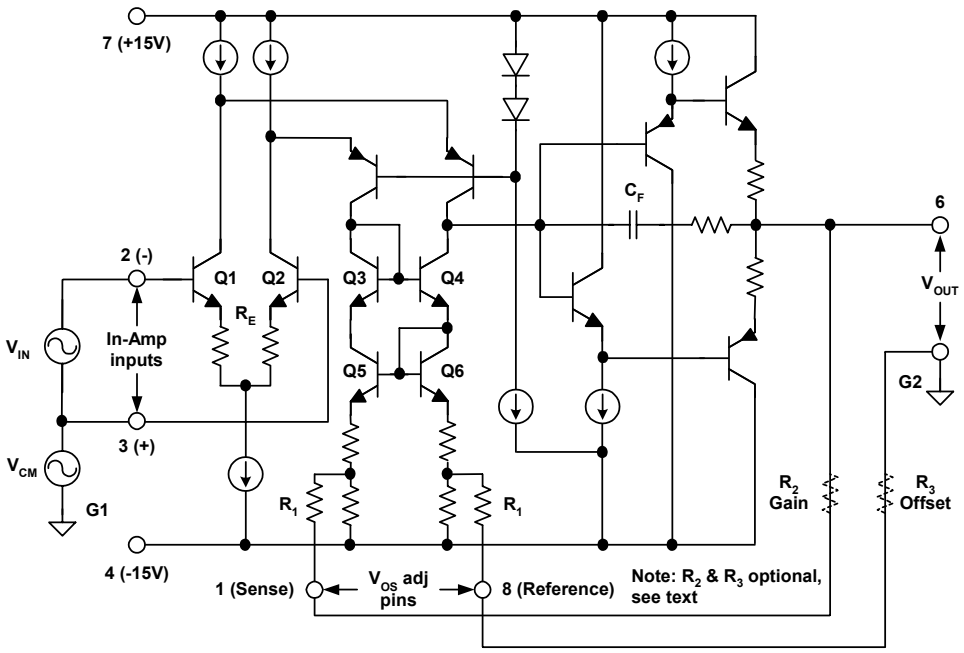


Figure 6-167: *An AD817 wideband in-amp configuration*

Functioning here as an in-amp, the AD817 is operated unconventionally. No feedback is used to inverting input pin 2. Instead, the V_{IN} differential signal is applied between pins 2 and 3, as noted. Typically there is also an associated CM noise, V_{CM}. Note that there must be a return path between the input ground G1 and output ground G2, to allow bias current flow (as with standard in-amps). The input differential pair stage Q1 and Q2 produces an output signal current, driving quad-connected current mirror stage Q3, Q4, Q5, Q6. At the bottom of the current mirror is the balancing resistor network, functioning here as a signal current input. The connection from pin 1 to the amplifier output closes a negative feedback loop, to the output at pin 6. A balancing reference input is applied to pin 8, either ground (as shown) or a variable offset voltage. Differential gain of the circuit, G, is:

$$G = V_{OUT}/V_{IN} = R_1/R_E \qquad \text{Eq. 6-44}$$

For the values noted, gain is about 8×, and bandwidth is 5MHz. CMR is excellent, measuring more than 80dB at 1MHz. Optional trim resistors R_2 and R_3 are used to adjust gain via R_2, or, alternately, offset via R_3. The values should be the same, for best CMR.

Negative Resistance Buffer

There is often a requirement for driving a lower load impedance than a given op amp may be capable of meeting. This can be particularly true for precision op amps in general, and, more specifically, with rail-rail output types. The latter class of op amps typically can have an output impedance on the order of several kΩ, which can limit load drive and lower open loop gain when driving low impedances. A straightforward way of addressing this problem is a unity gain buffer, which will work in almost all cases. But ordinary op amps can also be used for the buffer function. An interesting method is to use a second op amp as a negative resistance generator, to synthesize a negative resistance whose value is set equal to the load resistance. When this is carefully done the load disappears, as a parallel connection of R_L and $-R_L$ is infinite. Figure 6-168 below illustrates this technique, in both basic and practical forms.

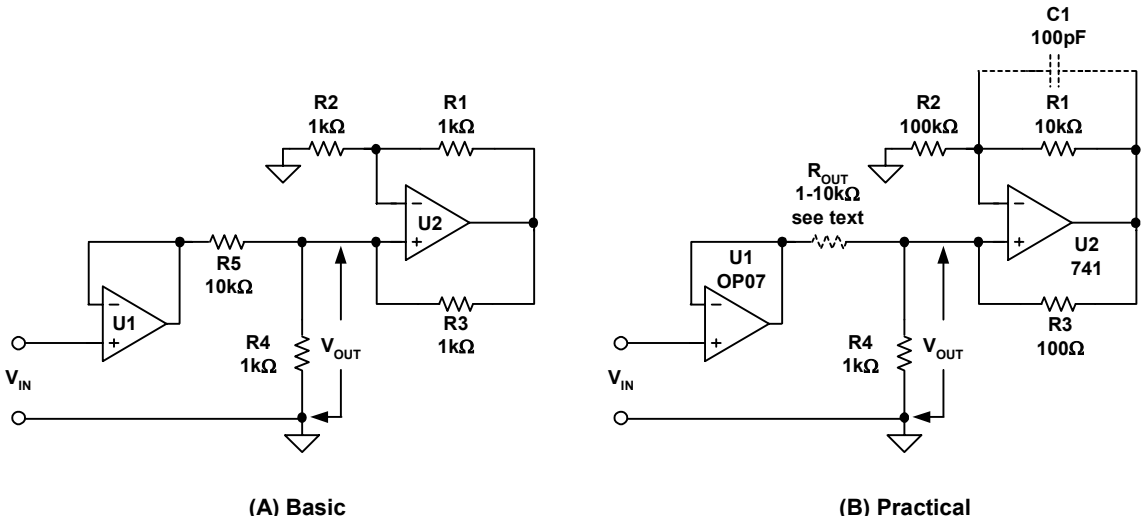


Figure 6-168: *Negative resistance buffer circuits*

In Fig. 6-168A, a basic form of the circuit is shown, to illustrate the concept. Here op amp U1 is intended to drive load resistor R4, but would normally be prevented from doing so with high precision by the output resistance represented by R5. But, due to the connection of the U2 stage the voltage V_{OUT} is amplified by a factor of 1 + R1/R2. This amplified voltage is fed back to the V_{OUT} node by R3. With the R1–R4 values scaled as shown, this produces a negative resistance of –R4 at the V_{OUT} node. Thus the driving amplifier U1 does not see the real resistance R4 loading, which can be confirmed by examining the (small) current in R5. If operation is not apparent, the circuit can be analyzed by viewing it as a balanced bridge, with ratios of R1/R2 matching R3/R4.

But the Fig. 6-168A circuit isn't very efficient, as twice the load voltage must be developed for operation, and double the load current flows in U2. The same principles are employed in the more practical Figure 6-168B version, with the R1–R4 values rescaled to reduce power and to gain headroom in U2, *while maintaining the same ratios*. In a real circuit there is likely no need for R5, and U1 can drive the load directly. It does so taking full advantage of the precision characteristics of the U1 type. U2 can be almost any ordinary op amp capable of the load current required.

Cross-Coupled In-Amps Provide Increased CMR

A primary in-amp benefit is the ability to reject CM signals in the process of amplifying a low-level differential signal. While most in-amps perform well below about 100Hz, their CM rejection degrades rapidly with frequency. The circuit below in Figure 6-169 is a composite in-amp with much increased CMR vis-à-vis more conventional hookups (see Reference 15). It consists of three in-amps, with unity-gain connected U1 and U2 cross-coupled at their inputs. In-amp U3 amplifies the difference between V_{O1} and V_{O2}, while rejecting CM signals. The in-amps are AD623s, but the scheme works with other devices.

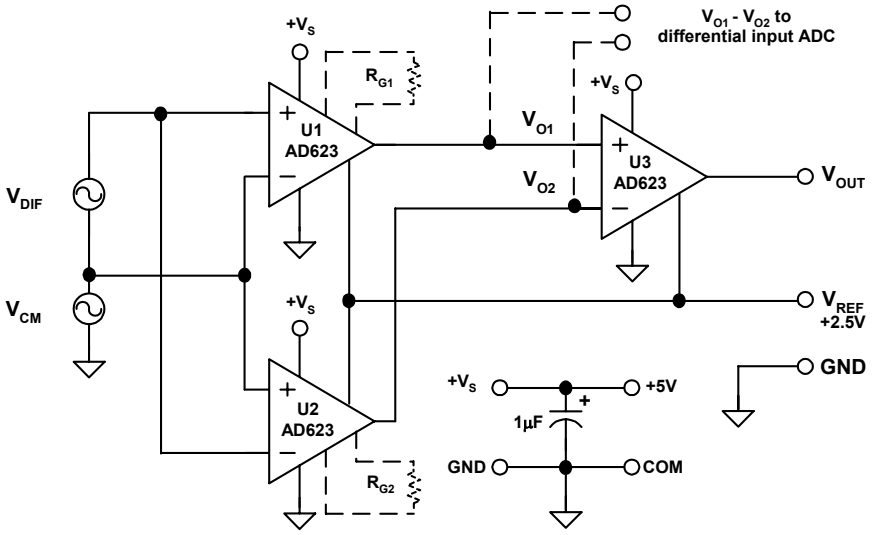


Figure 6-169: *Two cross-coupled and similar in-amp devices followed by a third provides much increased CMR with frequency*

Because of the fact that U1 and U2 have CM responses that are correlated (by the nature of their design), their output CM errors due to V_{CM} will be similar. For U3, this CM error appears as a CM signal, and is rejected further. Meanwhile, the desired differential signal, equal to $2V_{DIF}$ appears as $V_{O1} - V_{O2}$, and is amplified by U3 at unity gain. Overall gain is 2× as shown, but can be raised by a gain factor programmable by R_{G1} and R_{G2}. Note that due to the fact that the U1 and U2 CM errors correlate, their matching isn't necessary.

A big advantage of this scheme is the extended frequency range over which the composite in-amp has good CMR. For example, at the gain of 2 as shown, CMR as measured at either V_{O1} or V_{O2} will be on the order of 60dB or more at 10kHz. At V_{OUT} however (the output of U3), the CMR is increased to about 85dB, or more than 20dB. The low frequency CMR corner of the composite in-amp is about 6kHz, as opposed to about 500Hz as measured at either V_{O1} or V_{O2}. At higher gains, for example a gain of 100 (as set by R_{G1} and R_{G2} = 2.05kΩ), CMR increases to more than 110dB at low frequencies, and a corner frequency of about 2kHz is noted, while 10kHz CMR is more than 100dB. For these measurements $+V_S$ was 5V, and the V_{REF} applied to all devices was 2.5V.

Although the example shown is single-supply, it is also useful with dual supply in-amps. Another possible mode is to use V_{O1} and V_{O2} to drive a differential input ADC, which eliminates a need for in-amp U3. ADC scaling can be matched via R_G, and the V_{REF} used.

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Helpful comments on this section were received from Victor Koren and Moshe Gerstenhaber, and were much appreciated.

NOTES:

SECTION 6-6: COMPOSITE AMPLIFIERS

Walt Jung

The term "composite op amp" can mean a variety of things. In the most general sense of the word, any additional circuitry at either the input or the output of an op amp could make the combination what is termed a composite amplifier. This can be a valuable thing, as often such enhancements allow new performance levels to be realized from the resultant amplifier.

Some straightforward op amp performance enhancements of this type of have already been treated elsewhere in this book. For example, within the "Buffer Amplifiers" section of this chapter, as well as some of the specialized buffers in the "Audio" section of this chapter are found what could be termed composite op amps. In these examples, a standard output stage buffering design step is to utilize a unity-gain buffer, running on the same supplies as the op amp being buffered. So long as this buffer has sufficient bandwidth, this is an easy and straightforward step— insert the buffer between the op amp and the load, connect the feedback around the op amp plus buffer, and that's it.

A very useful means of increasing op amp performance can be obtained by blending the performance advantages of two ICs, or a standard op amp IC and discrete transistors. Such a combination is known as a *composite amplifier.* In special situations, a well-designed composite amp can often outperform standard op amps. The reason this is true is that the composite amplifier can be optimized for a unique and specialized performance, a combination that may not be available (or practical) in a standard op amp.

However, whenever an input (or output) circuit is added to an op amp that provides additional voltage gain, then the open-loop gain/phase characteristics of the composite op amp may need to be examined for possible stability problems. Note that this applies even when a unity-gain stable op amp is used within the composite, because the additional voltage gain raises the net open-loop gain of the combination. This will be made clearer by some circuit examples that follow.

In this section composite op amp circuits are described which fall into these categories:

- Multiple Op Amp Composite Amplifiers
- Voltage-Boosted Output Composite Amplifiers
- Gain-Boosted Input Composite Amplifiers
- A Nostalgia Composite Op Amp

These sections follow, with one or more circuit examples of each type.

Multiple Op Amp Composite Amplifiers

The simplest composite amplifier form utilizes two (or more) op amps, merged into a single equivalent composite. This is usually done for reasons of offset control, although in some instances it may be for increased gain capability, more output swing, etc.

Two Op Amp Composite Amplifier

The most flexible composite amplifier version combines two op amps in such a way that both signal inputs are still accessible to an application. A good example of this is the circuit shown below in Figure 6-170 (see Reference 1).

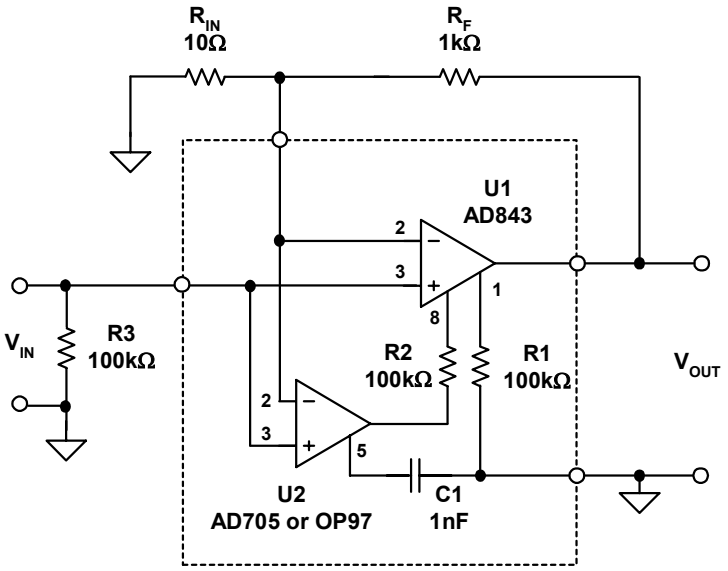

Figure 6-170: *Low noise, low drift two op amp composite amplifier*

In this circuit, U1 is a high-speed FET input op amp, the AD843. While FET input devices are typically excellent for fast data acquisition applications, their offset and drift is often higher than the best bipolar op amps. By combining the fast AD843 with a low offset and low drift, super-β input device for U2, the best of both worlds is achieved. Offset and drift are reduced essentially to the maximum U2 specification levels— an offset of 60µV, a drift of 0.6µV/°C, and 100pA of bias current (for the OP97E). The composite op amp formed is the dotted box outline, and is applied as a four-pin op amp.

Both the U1 and U2 op amps have inputs connected in parallel, and both amplify the signal. Device U1 drives the load and feedback loop directly. U2 however drives the offset null input of U1, via a 100kΩ resistor connected to pin 8, R2. R1 provides a complementary resistance at the opposite offset input, pin 1. C1 is used to over-compensate U2, at pin5. Note that the three just described pins are unique to the AD843, and either the AD705 or the OP97 devices. The U1/U2 signal inputs, output, and power supply pins are all standard, and the circuit operates on conventional ±15V supplies.

The circuit as shown has a non-inverting gain of 101×, as determined by R_F and R_{IN}. However, other application are also possible, both inverting and non-inverting in style. A detailed technical analysis of this circuit was presented in Reference 2.

Low Voltage Single-Supply to High Output Voltage Interface

There are numerous cases when an op amp designed for low (or single) supply voltage operation might need to be interfaced into a system operating on higher voltage and/or dual power supplies. An example would be the numerous low voltage chopper-stabilized op amps, which, without some means of easy interfacing, would simply not be available for use on high voltage supplies.

The circuit of Figure 6-171 below shows how a low voltage, single-supply chopper-stabilized amplifier, the AD8551, can be used on a ±15V supply system.

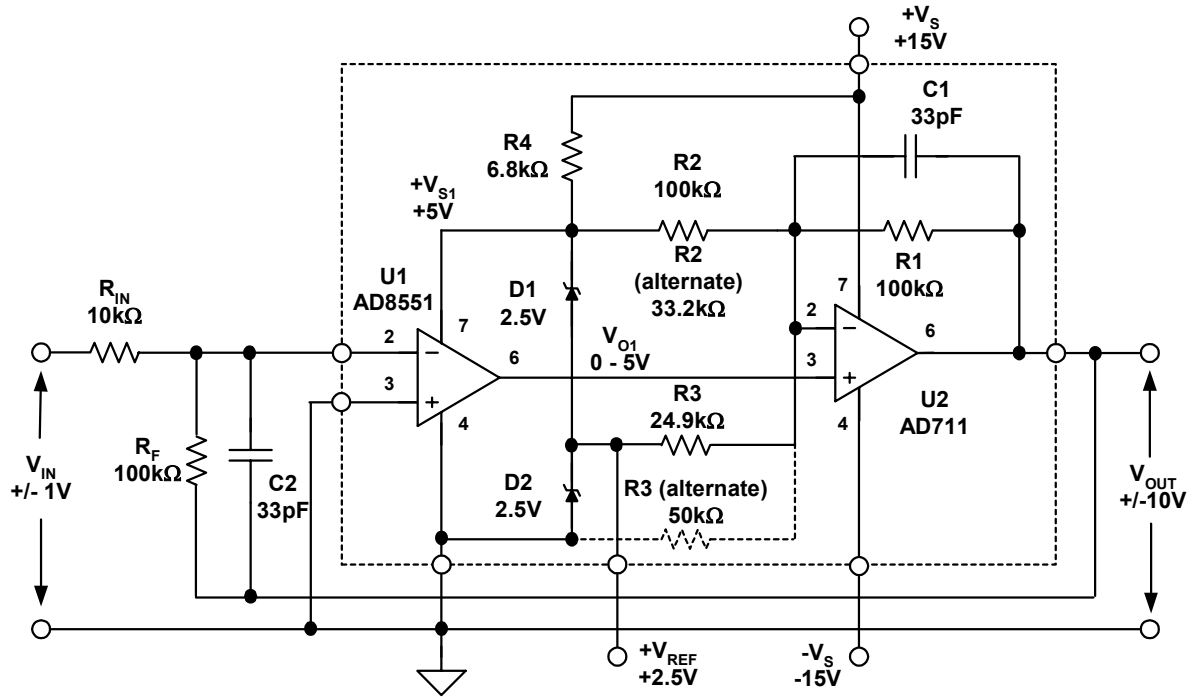

Figure 6-171: *Chopper-stabilized 160dB gain, low voltage single-supply to high output voltage composite amplifier*

In this circuit, the U1 AD8551 operates as a precision input stage of the composite amplifier, working from a local +5V supply generated from the main +15V rail by reference diodes D1, D2. This satisfies the supply requirements for the U1 stage, with the R4 value selected to supply the required current.

To interface the 0 to 5V output swing of U1 to a ±10V range, the U2 output stage operates as both a level shifter and a gain stage. A nominal gain of 6× is provided, with a DC offset providing the required level shifting. With the R1-R3 resistors and the 5V supply used as a reference, the gain and level-shifting is accomplished. The gain of 6× translates back to a 0.833 to 4.167V positive output swing from U1, a range which even non rail-rail output op amps can most likely accommodate.

A virtue of this circuit is that the output of U1 is not loaded, and thus it operates at its full characteristic gain. For the AD8551, this is typically 145dB. When the additional 15.6dB of the U2 stage is added, the net open-loop gain of the composite amplifier formed is

more than 160dB. Further, this high gain will be maintained for relatively lower impedance loads, by virtue of the fact that a standard emitter-follower type output stage is used within U2. So, the DC accuracy of this composite amplifier will be very high, and will also be well-maintained over a wide range of loads due to the buffering of stage U2.

The voltage-offsetting network as shown uses two 2.5V reference diodes, which provides a 2.5V V_{REF} output from D2. This is usually a handy asset to have in any +5V supply device system. Alternately, a single 5V reference diode can be used, with the alternate values and connections for R2 and R3 substituted.

To compensate the system for the additional voltage gain of U2, two feedback capacitors are used, C1 and C2. *Note that for anything other than this exact circuit, one or both of these capacitors may require adjustment.* This is best done by applying a low-level square wave to the input such that the final output is on the order of 100mVp-p or less, and verifying that the output step response is well-damped, with minimal overshoot.

C1 ensures stability for stage U2, and C2 provides overall bandwidth control for the main feedback loop. In general, the U2 amplifier should have more bandwidth than the U1 stage. However, the relative DC accuracy of U2 is not at all critical. The AD711 is shown as one possible choice, but many other types can also be used. While not shown for simplicity, conventional supply bypassing of the composite amplifier should be used.

System-wise, this composite amplifier behaves as a ±15V powered op amp with an input CM range equal to the specification of the U1 device in use. Overall loop feedback is provided as with any conventional feedback stage, i.e., by R_F, R_{IN} and C2. The circuit is applied by treating the parts within the dotted box as a single op amp, with the external components adjusted to suit a given application. An application caveat is that saturation of U1–U2 should be avoided, due to the longer overload recovery. This can be addressed with a 11-12V back-back clamping network across the feedback impedance.

Although the example hookup shown is a gain-of-10 inverter, other inverting configurations such as integrators and also non-inverting stages are possible. The caveat here is that the CM range of U1 must be observed. However this is likely no handicap; as such an amplifier is most likely to be used with very high gain and low CM input voltages. It could for example be used as a 5V-powered bridge amplifier with a ±10V output range.

There are of course any number of other op amp input and output devices that will work within this general setup. A more general-purpose low voltage part for U1 would be the AD8541. Offset voltage will be higher, and gain less, vis-à-vis the AD8551. For optimum dynamic range and linearity, the biasing of the U1 stage output is centered within the total U1 supply voltage V_{S1}, which can be different than 5V if needed. This feature is provided by R1-R3. The absolute values of these resistors aren't critical, but they should be maintained as to their ratio. They can be part of a common 100kΩ array for simplicity.

Voltage-Boosted Output Composite Amplifiers

A number of schemes are useful towards boosting the output swing of standard op amps. This can be either to achieve greater swing (i.e., closer to the rails), or, to develop swings greater than normally possible with standard ICs, i.e., ≈40V swings. In both cases it may also be desirable to increase load drive to 100mA or more.

Voltage Boosted, Rail-Rail Output Driver

A common requirement in modern system is the rail-rail capable op amp. But all op amps aren't designed with rail-rail outputs, so this may not be possible in all instances. Of course, it makes good sense to utilize standard off-the-shelf rail-rail IC op amps, whenever they meet the application requirements. Nevertheless, it is possible to add an output stage to a standard op amp device that may itself not be rail-rail in function. By using common-emitter (or common-source) discrete transistors external to the op amp, a rail-rail capability is realized. An example designed in this fashion is Figure 6-172 below.

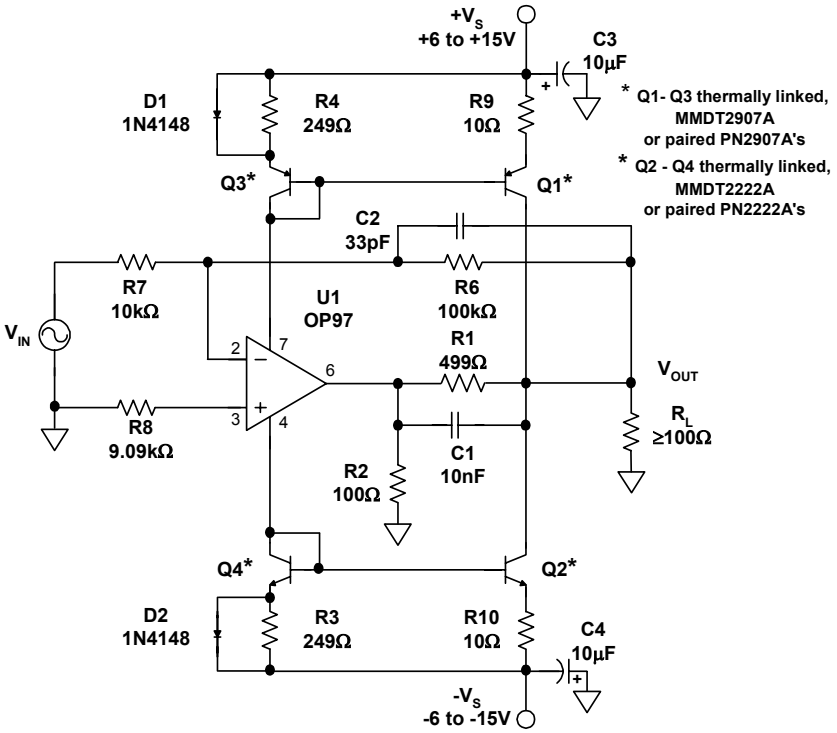

Figure 6-172: *Voltage boosted rail-rail output composite op amp*

Within this circuit Q1 and Q2 are the complementary buffer transistors that provide the rail-rail output swing. The circuit works as follows: Q1 is driven by the voltage drop across R4, and diode-connected Q3. This voltage is developed from the positive rail supply terminal of U1, so the quiescent bias current of Q1 will be related to the quiescent current of U1. Similarly, Q2 is driven from R3 and Q4, via the negative rail terminal of U1. The Q1-Q3 and Q2-Q4 pairs make up current mirrors, developing a quiescent bias current that flows in Q1-Q2. The U1 quiescent current is about 400µA, and with the resistance values shown, the Q1-Q2 bias current is about 10mA.

The output stage added to the U1 op amp adds additional voltage gain, and a current gain boost of 25 times, essentially the ratio of R4/R9 and R3/R10. Thus for a 100mA output from Q1-Q2, U1 only supplies 4mA. The swing across R2 is relatively low, allowing operation on low voltage supplies of ±6V, or up to ±15V.

The simulation data of Figure 6-173 illustrates some salient characteristics of the composite op amp while driving a load of 85Ω. The open loop gain of the circuit is shown by the topmost, or composite gain curve, which indicates a low frequency gain of over 130dB, crossing unity gain at about 630kHz. The intermediate curve is the OP97 op amp gain characteristics. The difference between this and the upper curve is the added gain, which is about 13dB. The lowest curve indicates the closed-loop gain versus frequency characteristics of the composite op amp, which is 20dB in this case, as set by R6 and R7 (as in a standard inverter).

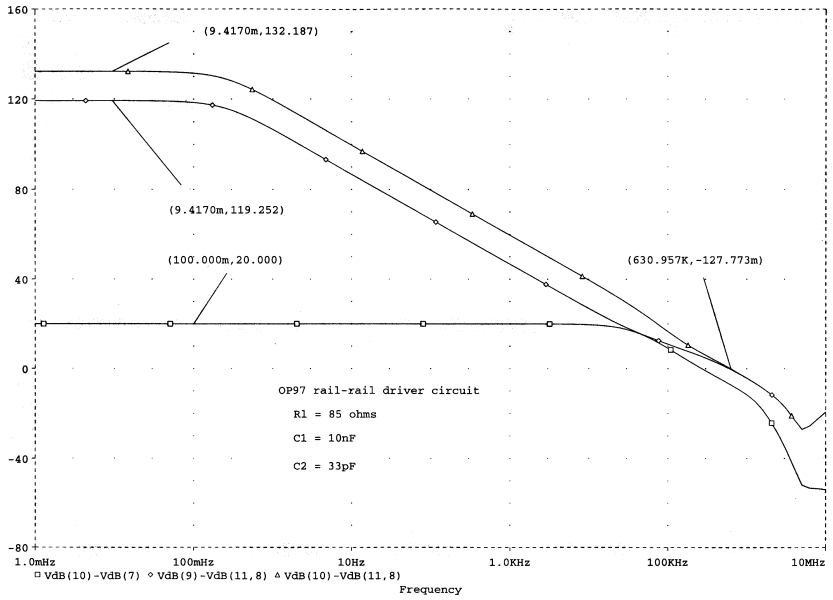

Figure 6-173: *Gain (dB) versus frequency characteristics of Fig. 6-172 composite op amp*

There are a couple of critical points in setting up this circuit. Bandwidth can be controlled by C1 and C2. C1 reduces the added gain at high frequencies, which can be noticed from the composite gain curve, starting below 100kHz. C2 reduces the closed-loop gain, starting about 50kHz. For greater closed-loop gains, C2 may not be needed at all.

Bias control is achieved by the use of thermal coupling between the dual current mirror transistors. The easiest way to accomplish this is to use packaged dual types, either SOT-363 or SM-8 devices (see References 3 and 4). Alternately, TO92 equivalent PN2222A and PN2907A types can be used, with the two flat sides facing and clipped together.

The circuit as shown drives a 100Ω load to within 2V of the rails, limited by the drop across R9 and R10. Current limiting is provided by a shunt silicon diode across R4 and R3, either with 1N4148 diodes, or diode connected transistors. This limits peak output current to about ±60mA. More output current is possible, by adding additional like devices in parallel to Q1 and Q2, with additional 10Ω emitter resistors for each.

A point that should be noted about the booster circuit of Fig. 6-172 is that *the biasing is dependent upon the quiescent current of the op amp*. Thus, this current must be stable within certain bounds, otherwise the idle current in Q1-Q2 could deviate— either too low (causing excess distortion), or too high, causing overheating. So, changing the U1 op amp isn't recommended, unless the biasing loop is re-analyzed for the new device.

Another point is that this type of circuit, which uses the power pins of the op amp for a signal path, *may not model at all in SPICE!* This is due to the fact that many op amp SPICE models do *not* model power supply currents so as to reflect output current— so be forewarned. However, the ADI OP97 model does happen to model these currents correctly, so the reader can easily replicate this circuit with the OP97 (as well as many other ADI models). Discussion of these models can be found in Chapter 7 of this book.

High Voltage Boosted Output Driver

With some subtle but key changes to the basic voltage-boosted composite amplifier of Fig. 6-172, output swing can be extended even higher, more than double the standard ±10V swing for ±15V rails. A basic circuit that does this is shown below in Figure 6-174.

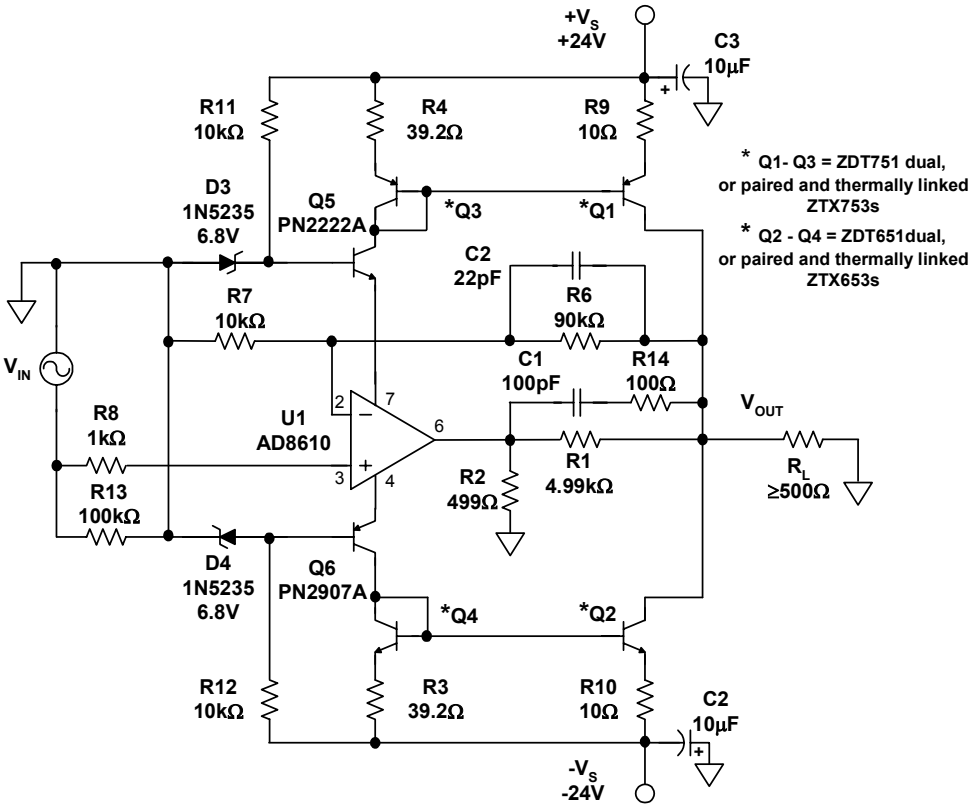

Figure 6-174: *High voltage boosted rail-rail output composite op amp*

This circuit can readily be recognized as being similar to the lower voltage counterpart of Fig. 6-172. To achieve higher voltage capability, the U1 op amp is operated from a pair of combination level-shift/regulator transistors, Q5 and Q6. These are biased in turn from the D3 and D4 zener diodes at their bases, to ±6.8V, respectively. The op amp rails are

then simply ±6.2V, while the main rails $+V_S$ and $-V_S$ can be virtually any potential, as will be ultimately limited by the Q1 and Q2 voltage/power ratings.

The op amp supply current passes through Q5 and Q6, driving the bases of Q1 –Q2 as previously. To accommodate the higher ±24V supplies, the standard 2222A and 2907A parts used in Fig. 6-172 are replaced by higher voltage parts, the dual ZDT751 and ZDT651 (see Reference 4). Thermal matching is best maintained by using these dual types, but comparable TO92 pairs can also be used, for Q1-Q3, ZTX753s, and for Q2-Q4, ZTX653s (see References 5 and 6). In any case, a large area PCB land (i.e., 1-2 square inches) should be used to for the Q1 –Q2 collectors for heat sinking purposes.

In this new circuit, an AD8610 op amp is used for U1, offering very low offset voltage, and higher speed. The quiescent current of the AD8610 is typically 2.5mA. A 4/1 gain is used in this circuit, as established by R4/R9 and R3/R10. The idle current in Q1-Q2 is therefore about 10mA, leading to a ≈240mW dissipation each, on ±24V supplies. This is low enough to not require a heat sink. However, the copper land area described above should be provided on the PCB around Q1-Q2 for heat sink purposes, tied electrically to their collectors. These measures, plus the active current limiting, help protect the output devices against shorts.

This circuit has a novel method of current limiting. As operated on ±6.2V, the AD8610 will swing just over ±5V. In driving R2 to this limit, ±10mA of current will be delivered to the current mirrors, resulting in a maximum output current four times this, or ±40mA. This is just about the DC safe-area limit of the Q1 and Q2 devices as used on ±24V. For low impedance loads below 500Ω, the maximum output voltage is a product of the 40mA limit and the load (for example 40mA into 100Ω yields 4V peak). The maximum voltage swing into a 500Ω load is then about ±20V, again, as determined by the current limiting. Into higher impedance loads, the swing is proportionally greater, up until the point Q1-Q2 reach their saturation limits.

Although the circuit is quite versatile as shown, there are many other options also possible. Other op amps can be used, but as noted before, the idle current should be taken into account. This is even more critical on higher voltage supplies, as it directly affects the power dissipated in Q1 and Q2.

For higher output currents from Q1-Q2, additional similar transistors can be paralleled, each with individual emitter resistors like R9 and R10. This will be practical for scaling up current by a factor of 2-3 times (assuming one additional package of the ZDT751 and ZDT651 types).

For ampere level current outputs, an additional current gain stage in the form of a complementary emitter follower can be added, driven from the Q1-Q2 collectors, with a 1:1 gain in the current mirror, and appropriate emitter follower biasing. With this step, the circuit will have been converted into a complete power amplifier. Details of this are left as an exercise-for-the-reader. However, a good starting point towards this might be the Alexander power amplifier topology (see Reference 7).

Gain-Boosted Input Composite Amplifiers

One of the most popular configurations used to enhance op amp performance is the gain-boosted input composite op amp. Here, a preamp gain stage is added ahead of a standard IC op amp, allowing greater open-loop gain, lower noise, and other performance enhancements. Another worthy improvement is the thermal isolation between the critical input stage, and the IC output stage that delivers the load current. The preamp can be a matched pair of bipolar transistors (NPN or PNP), or JFETs of either N or P types.

Prototype bipolar transistor gain-boosted input composite amplifier

For illustration of the basics, a prototype example composite amplifier is the two-stage op amp of Fig. 6-175. This circuit uses a matched NPN differential pair as a preamp stage ahead of U1, a standard AD711 type op amp. The preamp stage adds voltage gain to that of U1, making the overall gain higher, thus lowering gain-related errors.

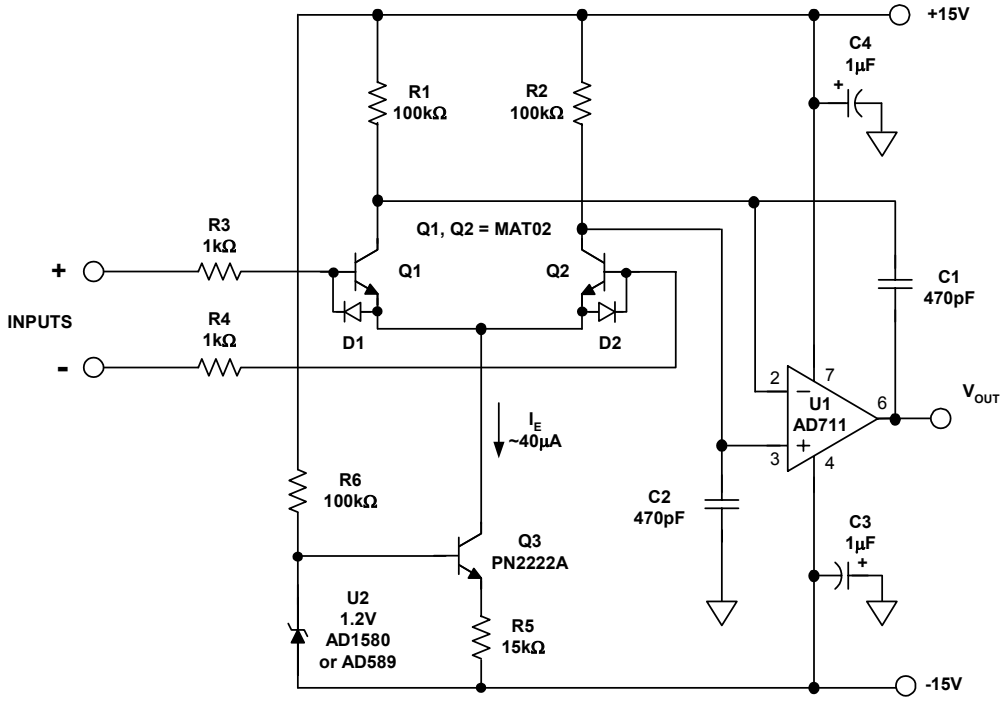

Figure 6-175: *Bipolar transistor gain-boosted input composite op amp*

Because of the added gain, the relative precision of the output op amp isn't very critical. It can be selected for sufficient output drive, slew rate and bandwidth. Within a given application the composite amplifier has overall feedback around both stages. Note— for this and following circuit examples, the op amp is *uncommitted* (i.e., external feedback).

In this example, a bipolar transistor differential pair, Q1-Q2 is loaded by a stable, matched load resistor pair, R1 and R2 (where R1 = R2 = R_L). The exact value of these resistors isn't overly critical, but they should match and track well. R1 and R2 are selected to drop 2-3V at ½ I_E. For a 2V drop, a suitable R_L is then:

$$R_L = \frac{4}{I_E} \qquad \text{Eq. 6-45}$$

Here, Q1 and Q2 operate at ≈20µA each, so 100kΩ values work for R1-R2. Note that in operation, *the second stage op amp must be capable of operating with input CM voltages of 2V below the $+V_S$ rail*. This criterion is fine for many PFET input amplifiers such as the AD711, but others should be checked for CM input voltage compatibility. Note that similar preamp stages can also be built with PNP bipolars, or with JFETs, and some of these will be described later.

The DC or low frequency gain of the preamp stage, G1, can be quite high with bipolar transistors, since their g_m is high. G1 can be expressed as:

$$G1 = \frac{R_L I_E}{2V_T} \qquad \text{Eq. 6-46}$$

Where $V_T = KT/q$ (≈0.026V at 27°C).

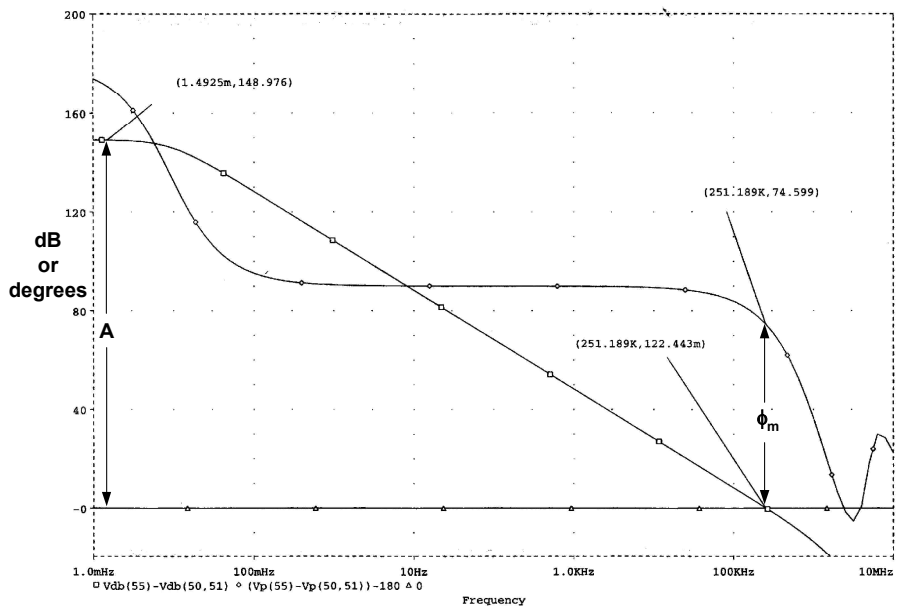

Figure 6-176: *Gain/phase versus frequency for Fig. 6-175 composite op amp*

In this example, at 27°C, G1 is about 77 times (37.7dB). Overall numeric gain is of course the product of the preamp gain and the U1 op amp gain. The minimum AD711 DC gain is 150,000, so the gain of the composite is more than 11.5 million (≥141dB).

As the preamp stage provides additional gain, this extra gain must be phase controlled at high frequencies for unity-gain stability of the composite amplifier with applied feedback. In this circuit, compensation caps C1 and C2 provide this function with U1 connected as a differential integrator.

The unity gain frequency, Fu, can be expressed approximately as:

$$F_u \approx \frac{I_E}{4\pi C_C V_T} \qquad \text{Eq. 6-47}$$

where π is 3.14, C1 = C2 = C_C.

In the gain and phase versus frequency simulation plot of Figure 6-176 (opposite), the performance of this composite op amp is illustrated. The additional gain of the preamp raises the net DC gain to ≈149dB, and the unity gain crossover frequency is shown to be ≈252kHz, both of which generally agree with the estimated figures. The phase margin ϕ_m at 252kHz is about 75 degrees, which is conservative. This op amp should be stable for all closed-loop gains down to unity (in fact, C1 and C2 could possibly be lowered).

Slew rate of the composite op amp can be no higher than the specified SR of output stage U1. For cases where the effective SR is to be lower, it can be estimated as:

$$SR \approx \frac{I_E}{C_C} \qquad \text{Eq. 6-48}$$

Using Eq. 6-47 and 6-48, the chosen values calculate a bandwidth of 260kHz, and an SR of just under 0.1V/µs. Actual bandwidths of 236-238kHz were measured on 4 op amps for U1 (AD711, AD820, LM301A and LF356), while SR was +0.085 and –0.087V/µs. As would be expected, the least bandwidth was measured with the lowest bandwidth U1 device, an LM301A. This demonstrates the relative insensitivity to U1 bandwidth.

With high gain input transistors, the bias current can be low. Generally, this will be:

$$I_B = \frac{I_E}{2H_{FE}} \qquad \text{Eq. 6-49}$$

Where I_B is the bias current of either Q1 or Q2, and H_{FE} is their DC gain. The MAT02 diodes protect against E-B reverse voltage, while the 1kΩ resistors limit diode current.

Bias currents of 30nA were measured with a MAT02 for Q1-Q2. Similar results can be obtained with high gain discrete transistors, such as 2N5210s. Offset voltage however, is a different story. Monolithic duals such as the MAT02 will be far superior for offset voltage, with a V_{OS} specification of 50µV. Non-monolithic packaged duals will also function in this circuit, but with degradation of DC parameters versus a monolithic device such as the MAT02. As can be noted from the numbers quoted above, speed isn't major asset of this amplifier. However, the DC performance is excellent, as noted, placing it in an OP177 class for gain.

The Q1 - Q2 emitter current, I_E, can be established by a variety of means. The most general form is the U2, Q3, and R5 arrangement. This works for a wide range of inputs, and also offers relatively flat gain for a bipolar Q1-Q2 gain stage, since the PTAT current from Q3 compensates the temperature–related gain (Eq. 6-46). For those applications where the input of the amplifier is operating in an inverting mode, a more simple solution would be a resistor of 332kΩ from the Q1-Q2 emitters to $-V_S$.

Of course, as a practical matter one wouldn't use the complex Fig. 6-175 circuit, if an OP177 (or another standard device) could do the job more simply or inexpensively. Nevertheless, what the above discussion does do is illustrate how one can *tailor* a composite op amp's characteristics, to get exactly what is needed. The composite op amp circuit of Fig. 6-175 could be used with a rail-rail output stage device for U1 (AD820), or with a very high current output stage (AD817, AD825), or any other performance niche not available from standard devices. Examples of these performance options follow.

Low noise, gain-boosted input composite amplifier

One of the more sound reasons for adding a preamp stage before a standard op amp is to lower the effective input noise, to a level lower than that of readily available IC devices. Figure 6-177 below shows how this can be achieved within the same basic topology as described above for the Fig. 6-175 prototype composite. As will be noticed, this circuit is similar to the prototype, with the exception of the added offset trim network, a higher bias level for I_E, and a faster output op amp, U1. Rtrim nulls the offset for best DC accuracy in critical applications. If this isn't necessary, connect R1-R2 as in Fig. 6-175.

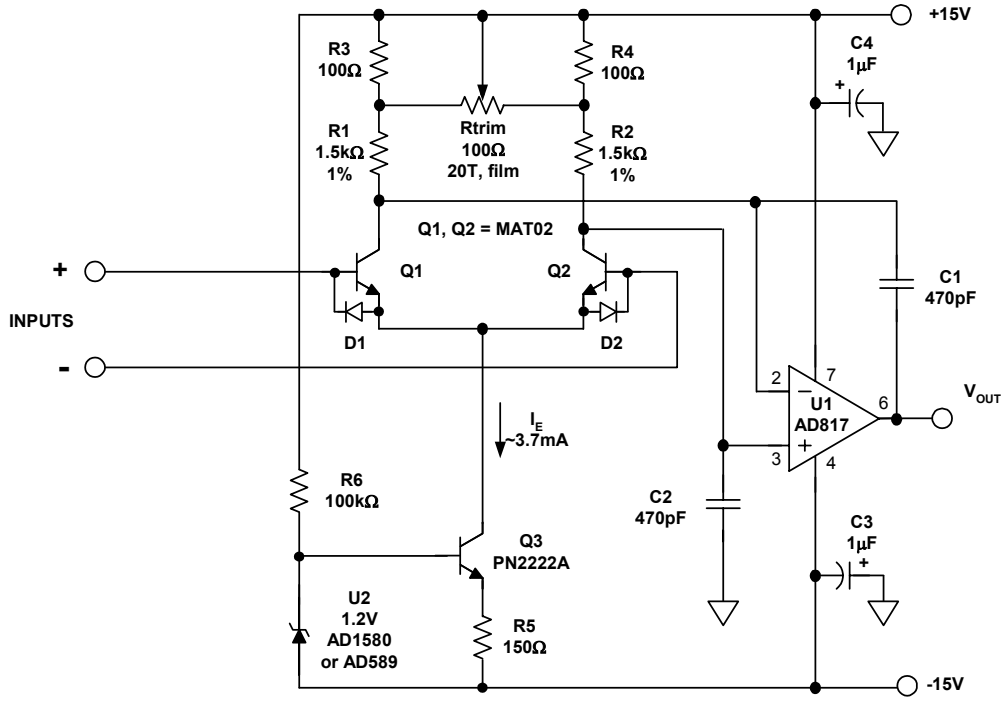

Figure 6-177: *Low noise gain-boosted input composite op amp*

By raising the current level of Q1-Q2 by roughly a factor of 100× compared to the prototype, the effective input noise of Q1-Q2 is lowered dramatically. At the operating current level of 3.7mA, the MAT02 achieves an input voltage noise density <1nV/√Hz (see Reference 10). To eliminate their added noise, the series base resistors are dropped.

Both bandwidth and SR are also improved in this circuit, since they are both proportional to I_E. The estimated bandwidth and SR for this circuit are 24MHz and 7.9V/µs, respectively. Measurements show about 21.2MHz for bandwidth, and a SR close 7.6V/µs. Both the actual bandwidth and SR are less than the AD817 specifications of 50MHz and 350V/µs. The circuit as shown is close to unity-gain stable, with 44° of phase margin at the unity gain frequency. Of course, very low noise amplifiers such as this will often be applied at some appreciably higher gain, for example 10, 100 or more. When this is the case, then C1 and C2 can be reduced, allowing greater bandwidth and SR.

An even lower noise op amp can be achieved simply by adding one or more low noise pairs parallel to Q1-Q2, and operating the combination at 6mA of current. See References 11 and 12 for examples to achieve 0.5nV/√Hz or less noise.

JFET transistor gain-boosted input composite amplifier

The circuit of 6-178 below illustrates an alternative compensation method for composite op amps. This technique has the advantage of simplicity, but also the disadvantage of being conditionally stable. This technique goes back to the very earliest days of IC op amps, when discrete or monolithic matched FET pairs were used ahead of a standard IC op amp such as the 741, 709, etc. Further details are contained within References 13 and 14. The example here isn't offered as a practical example, inasmuch as so many superior IC FET op amps are available today. However, it does give insight into this type of compensation, which is applicable either to FET or bipolar input stages.

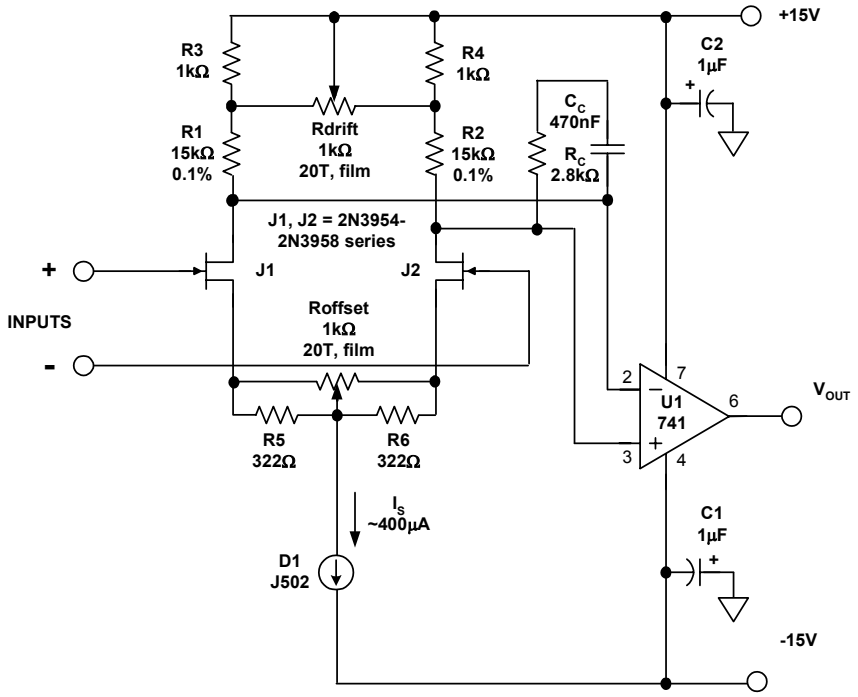

Figure 6-178: *JFET transistor gain-boosted input composite amplifier*

There are practical reasons why this type of FET input composite amplifier isn't used today. One is that to do it correctly involves many involved trims, another is that it requires a considerable number of parts. Dual FET devices don't come with sub-mV offsets, as do bipolars, so there is the need to trim out offset. Roffset does this, for J1-J2 V_{OS} up to 50mV. For lowest drift, the drain currents should also be trimmed, via Rdrift.

N-channel JFET duals such as the 2N3954 and J401 series are specified for operation at a total I_S of 400µA, or 200µA/side. Their transconductance is much lower than a bipolar; for these conditions; it is typically ≈1400µS. Therefore the gain of this preamp will typically be much lower than would a bipolar stage. With matched load resistors, gain is:

$$G1 = \frac{R_L \bullet g_{fs}}{2} \qquad \text{Eq. 6-50}$$

where g_{fs} is the specified JFET transconductance at $I_S/2$.

For the conditions shown, G1 works out to be 10.5 (20.4dB). Note— if used, the Roffset network reduces gain somewhat, and Eq. 6-50 *doesn't* take this into account.

Compensation for this composite amplifier is via the RC network, R_C-C_C. This network reduces the gain of the preamp to unity above the zero frequency, which allows the aggregate open-loop response to then assume that of the U1 amplifier before the unity-gain crossover. It is chosen by setting R_C as:

$$R_C = \frac{4}{g_{fs}} \qquad \text{Eq. 6-51}$$

where g_{fs} is again the specified JFET transconductance at $I_S/2$.

In this case, R_C works out to be 2.8kΩ. C_C is then chosen to provide a zero at some frequency that should be a very small fraction of the U1 op amp's unity gain frequency. The importance of this point will be made clearer by various open-loop response shapes.

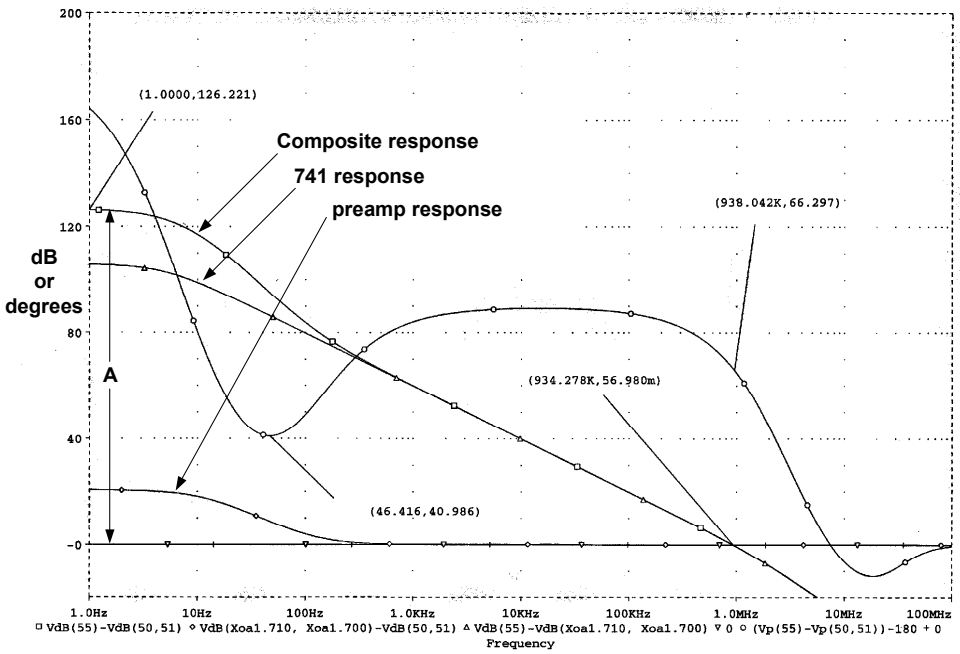

Figure 6-179: *Gain/phase versus frequency for Fig. 6-178 composite amplifier*

It should be recalled that the classic open-loop response of an unconditionally stable op amp is a constant –6dB/octave for gain, with an associated 90° phase shift. For such a device, any 1/β closed-loop response that intersects this open-loop response will be stable. For example, the 741 response (Δ), as so marked in Figure 6-179 above, is such a characteristic. But, as can also be noted from Fig. 6-179, the gain/phase response of a composite op amp compensated as in Fig. 6-178 just isn't a simple matter.

In the case of the added preamp stage and the R_C-C_C network compensation, the composite gain response (□) assumes *a multiple-slope response.* Associated with this gain response, note also that *the phase characteristic (o) varies radically with frequency*. In particular, the phase dip around 46Hz signifies a frequency where a loop closure could be problematic, as the phase margin is only 40° at this point.

Faced with this type of open-loop gain/phase response, a designer needs to careful in crafting the closed-loop gain configuration. The first step is to decide what level of

closed-loop gain is required by the application. Given that, an ideal 1/β curve can be drawn on a Bode diagram, to determine the rate-of-closure at the intersection. For optimum stability, it is desirable that this intersection occurs with a relative –6dB/octave between the open-loop gain curve and an ideal 1/β curve. Note that if such a 1/β curve were drawn on Fig. 6-179 at a 100dB gain, it would intersect in a –12dB/octave region. This is because C_C is 470nF in this example, which places the phase dip at 46Hz, with a composite gain curve which, as noted, is dropping at a rate greater than 6dB/octave. So, with the proposed gain curve intersecting in this region, stability could be marginal.

On the other hand however, with the R_C-C_C "phase funnies" forced down to a low frequency that corresponds to very high closed-loop gains (i.e., ≈100dB), the practical potential for instability is minimized. Note also that it doesn't make good sense to build a 100dB gain feedback amplifier based on limited open-loop gain such as Fig. 6-179.

On the other hand, if C_C were smaller, this wouldn't necessarily be the case, because the associated phase dip would then move upward in frequency. This could wreak havoc with loop closures at more practical closed-loop gains. In contrast to this, with C_C sized as shown at 470nF, the phase anomalies are confined to very low frequencies, yet the added DC gain of the preamp is still available. Loop closures at frequencies above ≈200Hz (at closed-loop gains of 80dB or less) see a high frequency composite response closely resembling the 741 (□ and Δ, respectively), and should thus be stable.

Watch out for the time domain response!

It should also be noted that there is a more subtle side effect related to the R_C-C_C method of compensation, as illustrated in Fig. 6-178. Simply put, this is the fact that *the time domain response of the resulting composite amplifier will be marred, compared to that of a classic 6dB/octave roll off* (see Reference 15).

So, wherever time domain response is critical, then the more conservative, unconditionally stable compensation method of Fig. 6-175 should be used. A case in point using this method with a FET preamp is the next composite amplifier.

In summary, for the AC performance characteristics as a composite amplifier, the circuit of Fig. 6-178 offers a gain raised higher that that of U1, or by about 20dB (126dB total) using the 741. At high frequencies, the overall gain bandwidth properties of this composite mimics the U1 amplifier, when the R_C-C_C time constant is relatively large.

DC performance limitations

The DC input characteristics of this circuit will be those specified for the J1-J2 pair, with typical room temperature bias currents of 50pA or less. Common-mode rejection will be limited by the J1-J2 specifications, and typically no more than about 80dB, over a limited CM range. This could be improved by cascoding the J1-J2 pair, but again, given the availability of such FET-input IC amplifiers as the AD8610, this would be a questionable design for a precision FET amplifier. In Fig. 6-178, the current source used for I_S is a simple FET current limiter diode (see Reference 16). This offers simple, two-terminal operation, at a current level optimum for the J1-J2 pair.

Low noise JFET gain-boosted input composite amplifier

An alternative method of executing a JFET input gain-boosted composite is to operate the input differential pair into an output op amp stage that acts as a differential integrator (i.e., similar to the Fig. 6-175 prototype, insofar as the compensation). The circuit of Figure 6-180 below is such an example, one that is also optimized for low noise operation, medium speed, and higher output current.

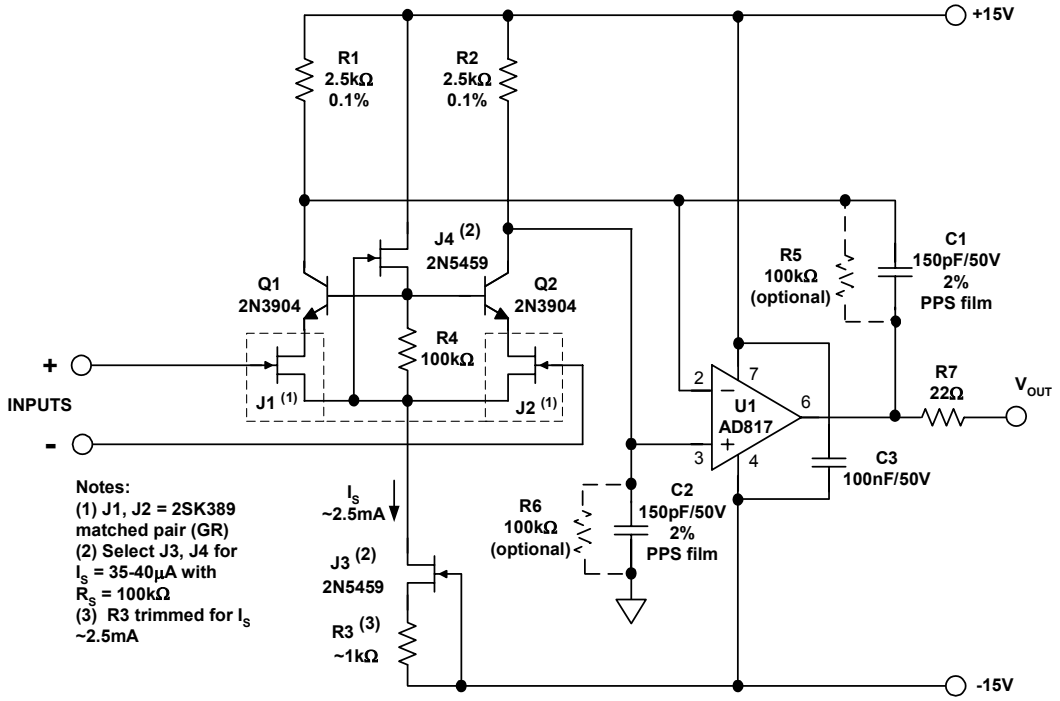

Figure 6-180: *Low noise JFET gain-boosted input composite amplifier*

The design uses a low noise JFET pair as the gain stage, the 2SK389 device (see Reference 17). Biased for drain currents of more than 2mA, this device pair is capable of achieving an input voltage noise density of less than 1.5nV/√Hz. The basic device is available in three I_{DSS} grades, GR (2.6-6.5mA), BL (6-12mA), and V (12-20mA). The lowest noise will be found with use of the highest I_{DSS} parts, at the expense of course, of supply current. This design example can use any grade, by biasing J1-J2 for the GR parts (at an I_{DSS} of 2.5mA). This still gives good noise performance for an FET-input amplifier (about 1.8nV/√Hz), but at a still reasonable power supply drain.

A byproduct of the large geometry devices of this devices series is a relatively high capacitance. If this factor is not addressed, this large and non-linear capacitance could cause distortion, for applications operating the circuit as a follower. To counteract this, the input stage of J1-J2 is cascoded, by the Q1-Q2 and J4 arrangement. This removes the major degradation of operation due to the J1-J2 capacitance, and it also stabilizes the DC operating points of J1-J2. From the output collectors of Q1-Q2 onward, the amplifier operates generally as the Fig. 6-177 circuit previously described. An AD817 is used for U1, so as to take advantage of its wide bandwidth and high output current.

The unity-gain bandwidth of this circuit is about 15MHz, but the open-loop gain is user selectable, by virtue of optional resistors R5 and R6. With these resistors connected, the composite amplifier open-loop bandwidth is ≈10kHz, and open-loop gain is about 63dB. These attributes make it well suited for audio applications, for example. Without R5 and R6, the open-loop gain is more like that of a conventional op amp, with a gain of more than 100dB at low frequencies.

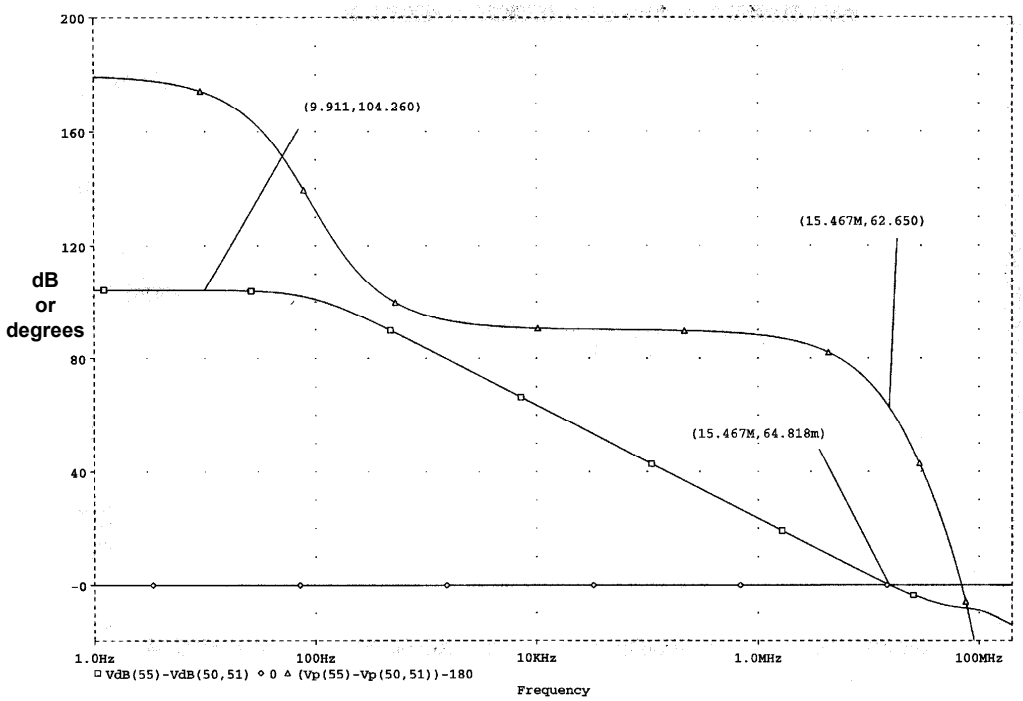

Figure 6-181: *Gain/phase versus frequency for Fig. 6-180 composite amplifier*

The open-loop response for R5 and R6 open is shown in Figure 6-181 above. In this simulation the load resistance was 600Ω. As can be noted, the response is clean, without phase aberrations. Phase margin at the unity-gain crossover frequency is about 63°, and the low frequency gain is about 104dB.

Although this circuit does have some excellent AC characteristics, it should be noted that it is *not* a general purpose op amp circuit. One reason for this is that the cascode input stage is a two-edged sword. While it reduces capacitance and improves distortion, it also limits the allowable CM input range. The positive swing headroom is limited by roughly the DC drop across R1 and R2, plus that of the cascode, or 3 + 4.5V. This means the most positive CM input should be less than about 5Vpeak, or 3.5Vrms. This of course won't be a practical limitation for non-inverting amplifiers with noise gains of 5× or more, or for low-level preamps with high gains of 100 or 1000×.

As compensated in Fig. 6-180, the composite op amp should be unity-gain stable. At closed-loop gains appreciably higher than about 5×, a reduction of C1-C2 can be considered, which will allow greater bandwidth and SR to be realized. Offset of the J1-J2 pair can be as high as 20mV, so offset trim may be in order for DC-coupled applications. For lower noise, a high I_{DSS} grade for J1-J2 should be used, with I_S raised to 5mA or more. R1-R2 will need to be lowered, and C1-C2 raised, in proportion.

"Nostalgia" vacuum tube input/output composite op amp

In keeping with the theme of this book's History chapter, the final composite amplifier design for this section uses venerable vacuum tube devices, which formed the basis of the first ever op amps. Today however, designing a vacuum tube op amp has some advantages, vis-à-vis the early days— transistors didn't exist! Thus the nostalgia op amp shown in Figure 6-182 below incorporates techniques of both today as well as yesteryear.

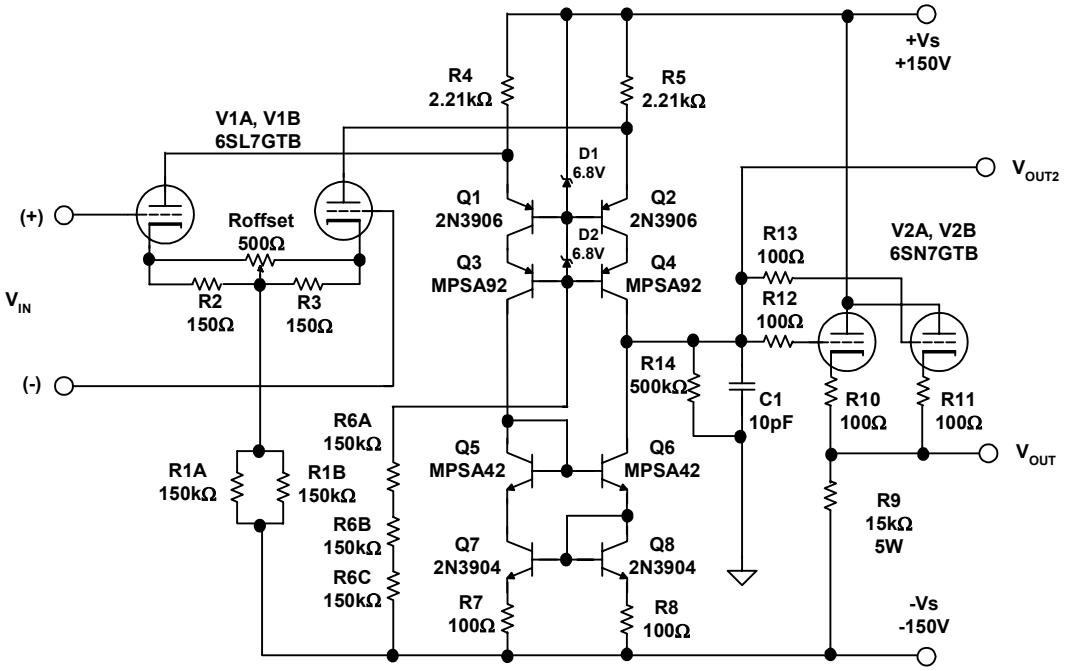

Figure 6-182: *"Nostalgia" vacuum tube input/output composite op amp*

Note that this particular circuit should be taken as a design exercise rather than a practical example. Yet, it was still a lot of fun to design using available SPICE models (see Reference 18). As such, it offers some insights not available to early op amp designers.

Here V1 is a dual triode input stage, using the high gain 6SL7 (or alternately, the close-cousin 12AX7 miniature). It is operated here as a linear transconductance, long-tailed differential pair. Rather than using conventional plate loading, the output signal current from V1A-V1B is passed to a folded cascode stage Q1-Q4, which is loaded by a linear, high voltage current mirror, Q5-Q8. The transistors of the current mirror are also cascaded, both for higher output impedance as well as for required high voltage capability. A regulated 6.3V heater supply for V1 is suggested, for highest stability.

Voltage gain of this one stage op amp is approximately equal to the V1A-V1B transconductance times the nodal impedance seen at V_{OUT2}. With R14 open this impedance is very high, so gain can also be quite high (≈77dB simulated). With R14 500k, gain is about 53dB. Open-loop bandwidth is established by the shunt capacitance at the high-Z node and R14, and measures about 7MHz gain bandwidth in simulation. A 6SN7 dual cathode follower output stage for V2 allows up to 10mA of load drive.

Laboratory test results for this design are left as an exercise for the interested reader, and feedback is welcome.

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NOTES: